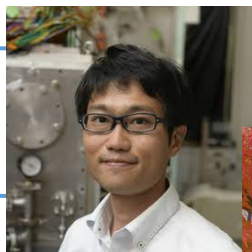


RCNP, the University of Osaka: People



Shinsuke OTA
Prof.

DAQ framework development (NestDAQ), SPADI-Alliance founder, online-offline processing framework (Artemis), UI



Ken OYAMA
Prof.

Detector FEE and integration (ALICE TRD&TPC), FPGA Acceleration, Trigger electronics, DAQ development, **ePIC DAQ**



Tomoaki HOTTA
Assoc. Prof.

HPC, Network, **ePIC Echelon 2**



Nobuyuki KOBAYASHI
Assoc. Prof.

DAQ framework development (NestDAQ), Large Deployment (Container)



Sun-Young RYU
Assoc. Prof.

DAQ framework development (NestDAQ), GPU Acceleration



Lakmin WICKREMASINGHE
Assis. Prof.

Detector FEE, FPGA firmware, Hardware Design, Silicon Pixel/Strip Detector (ATLAS), **interest in UI and Slow-CTRL in ePIC**



Tomonori TAKAHASHI
Assis.

DAQ framework development (NestDAQ), Streaming readout technology, **ePIC Streaming DAQ**



Koki TANAKA
Master Student

FPGA firmware, NestDAQ, **Interest in SVT Readout**

RCNP: capabilities & technical infrastructure

Readout electronics and data acquisition system technologies developed through RCNP, J-PARC (**SPADI Alliance**), and **LHC experiments**

- FEE development
- Si detector QA bench development
- FPGA firmware, acceleration, GPU processing
- DAQ construction/deployment (**NestDAQ**)

In addition

- RCNP recently invited the Japanese NP community to join the EIC Consortium
- Receiving responses from over 60 interested individuals
- This framework supports participation on an individual basis rather than as an institute
- Wide spectrum of people: theorists, general physics, detector, electronics, computing
- Anticipate active involvement from those interested in MAPS detector

SPADI Alliance

Signal processing and data acquisition infrastructure alliance

> 200 researchers (32 institute)



RCNP: institutional interest in SVT

- **Readout of MOSAIX**

- Adaptation of NestDAQ for MOSAIX readout [Tomonori & Koki]
- FPGA firmware development for detector readout (FELIX, RDO?)
- Streaming filtering, online analysis

- **Future: MAPS+ASIC integration technology (upgrade?)**

- MAPS on MAPS or ASIC on MAPS 3D integration
- Large scale, low cost silicon tracking

detail will be discussed tomorrow

