https://pixelphilab.mit.edu

Wafer probing status & plans

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Gian Michele Innocenti (MIT)

SVT Working Meeting
(October 8-9th, 2026)

The work of the MIT HI group and MIT PixElφ Lab
was supported by US DOE-NP and by the SVT-EIC project

Overview of the talk

Wafer-probing setup and performance

Testing results and schedule

System upgrades and software development

Next steps towards production-scale LAS testing

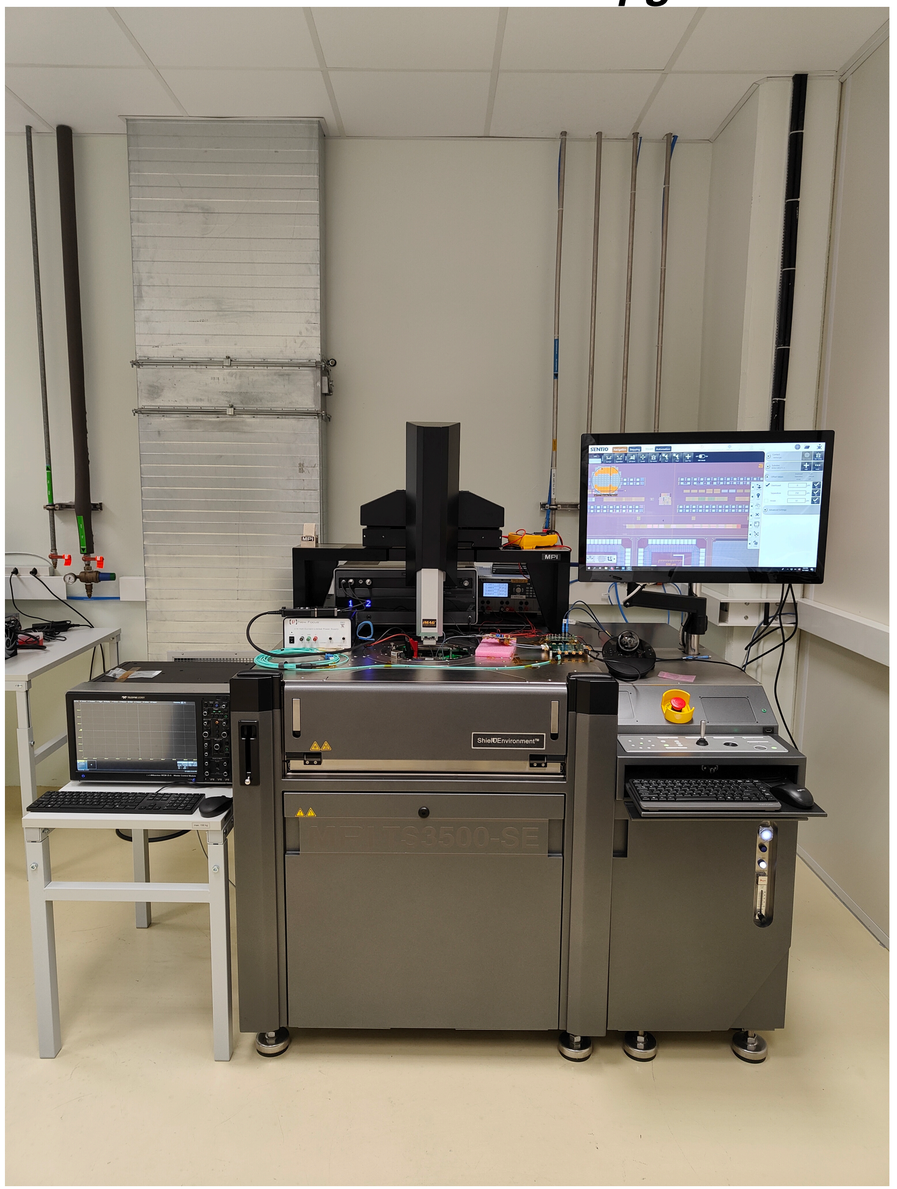
MIT Wafer Prober at CERN

MPI TS-3500 SE Automated test system
Installed in CERN Departmental Silicon Facility (DSF)

Cutting edge industry system for 300 mm (12”) wafers:

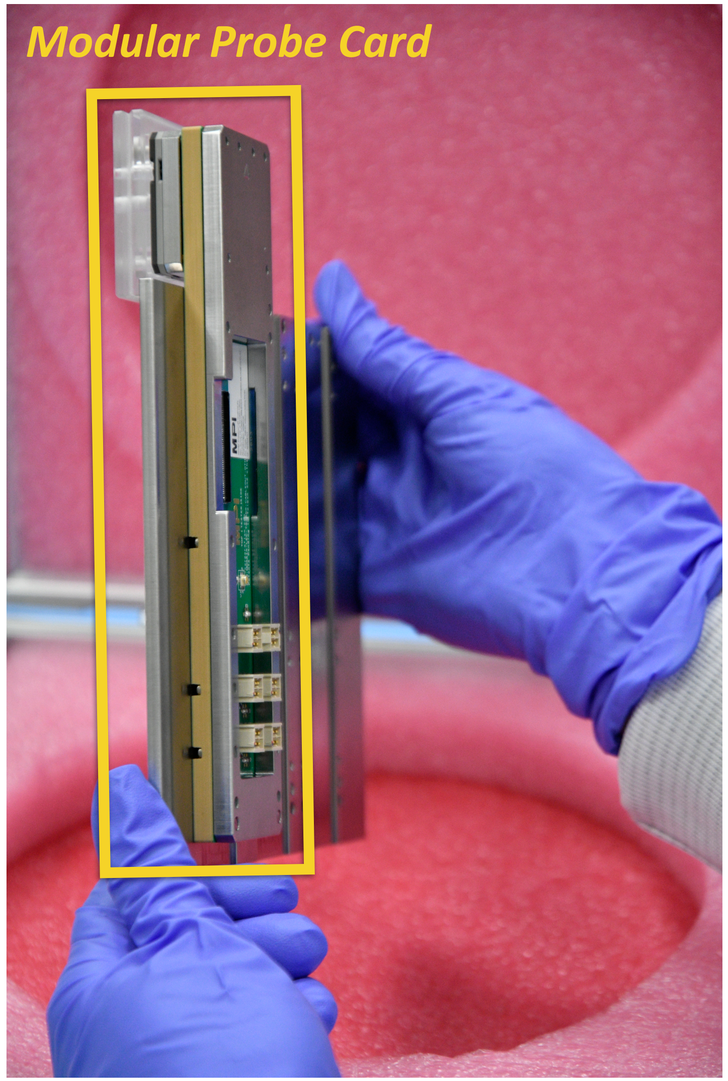
- Designed for **full compatibility with vertical probing**
  (wide*, chuck (vertical probing), off-axis (vertical probing), VCE*
- **Enabling multi-Gbps signals probing**
  additional cameras: *wide, chuck (vertical probing), off-axis (vertical probing), VCE*
- **Automated software** including probe to pad alignment
- **Automatic wafer loader** *(up to 25 wafers)*
  could be added for higher automatization

Before the recent upgrade



MOSAIX / LAS Modular Vertical Probe Card

Side View

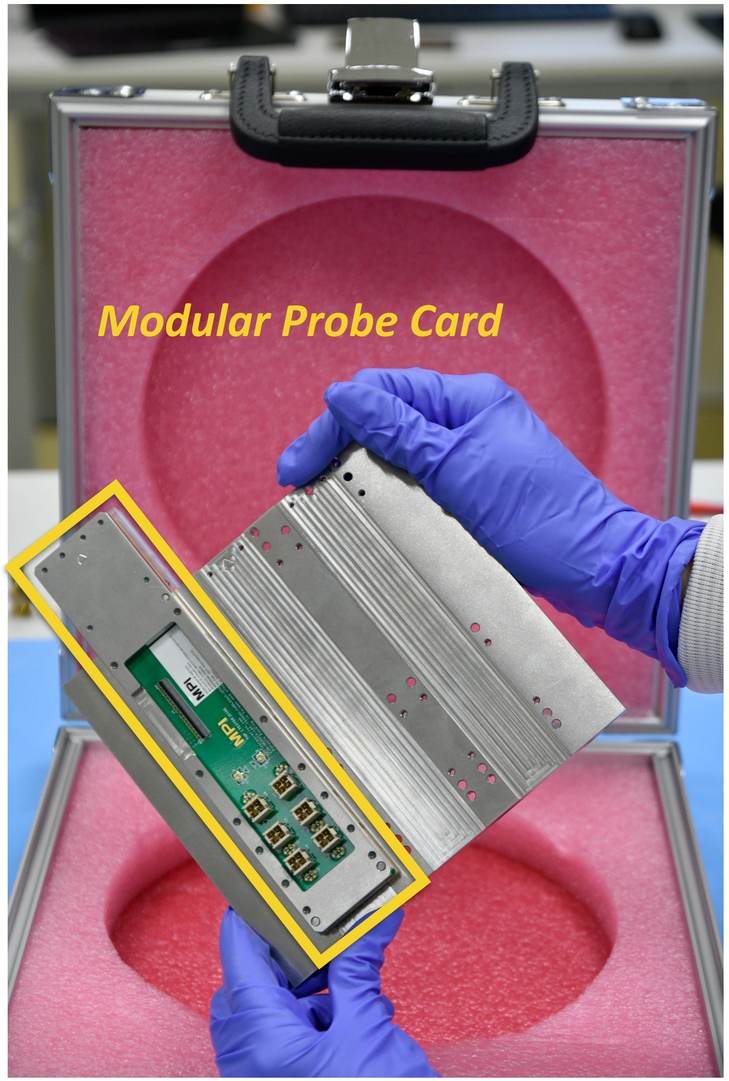


Concept by PixElφ Lab

Custom Vertical Probe Card:

- Compact and Modular design

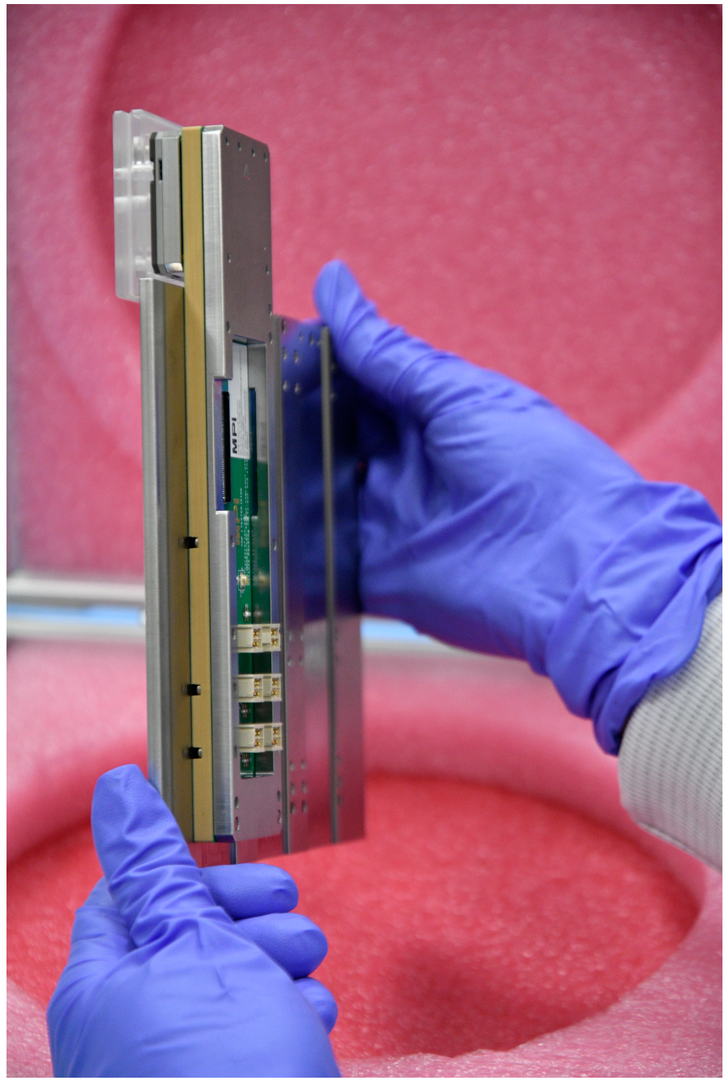
Front View



See TWEPP 2025 concept introduction (link)

MOSAIX / LAS Modular Vertical Probe Card

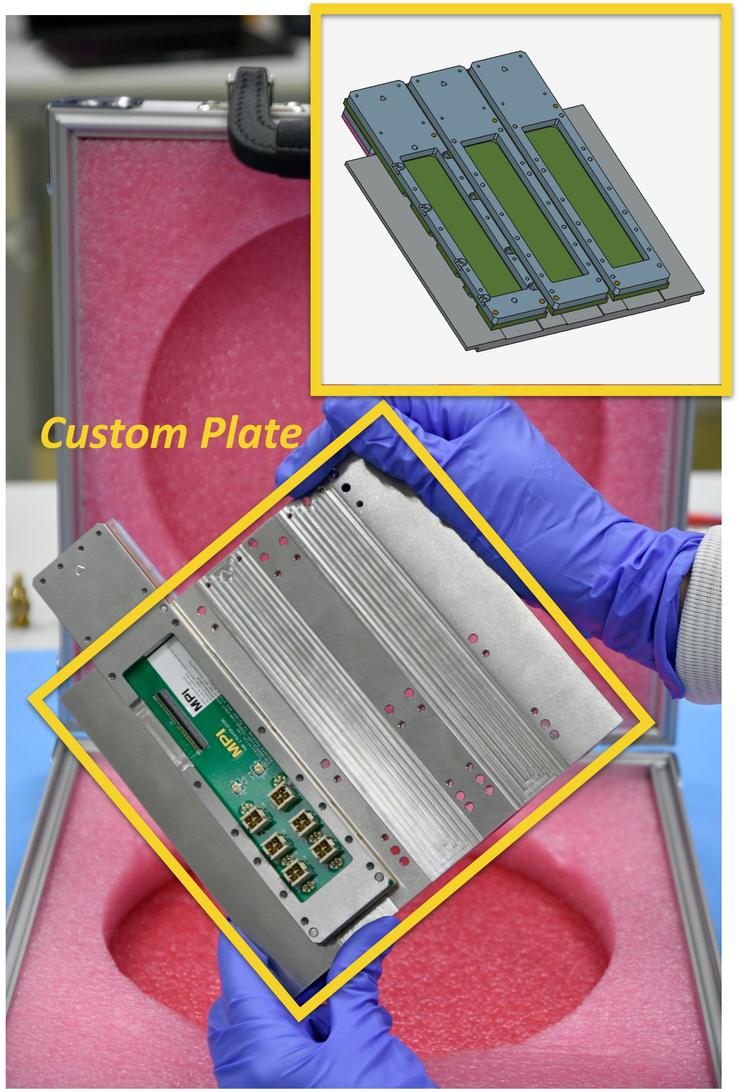
Side View



Custom Vertical Probe Card:

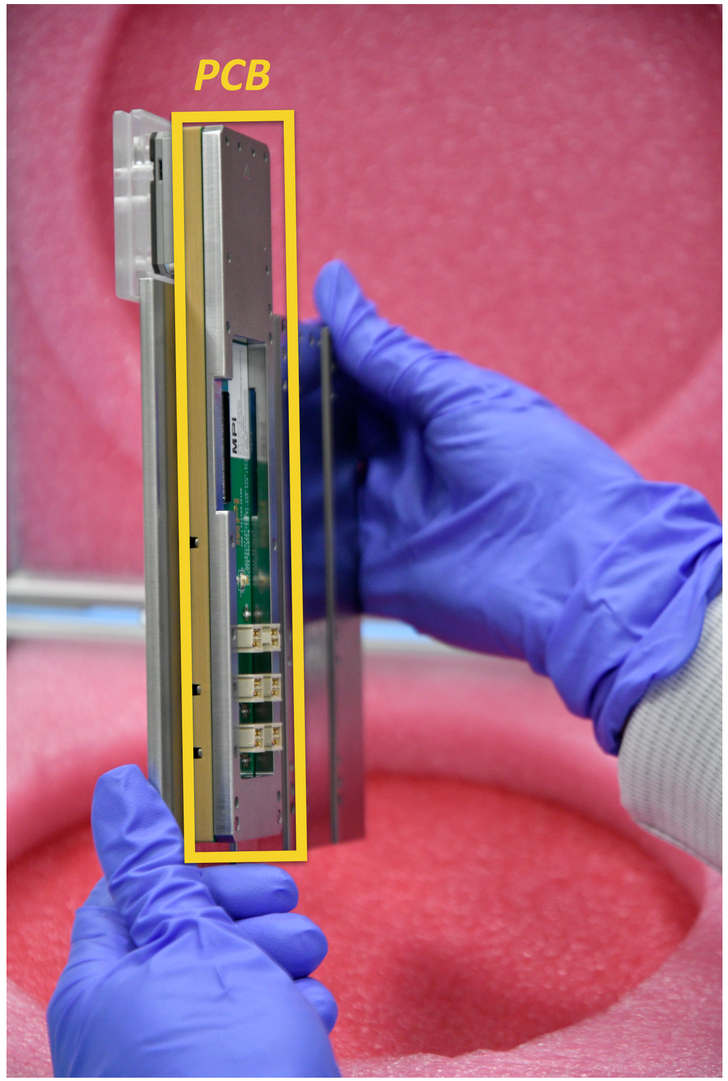
- Compact and Modular design
- Custom plate for mounting multiple probe cards, enabling parallel wafer testing
- Enable testing of different wafer layouts by redesigning only the mounting plate.

Front View



MOSAIX / LAS Modular Vertical Probe Card

Side View



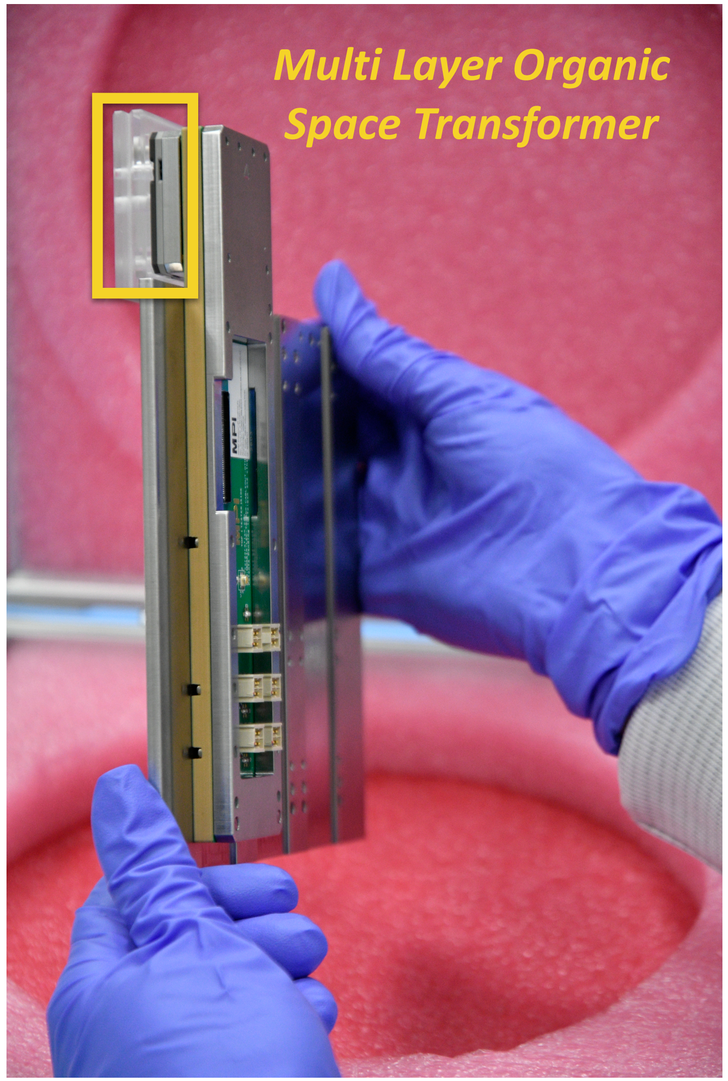
- High Speed MPI Technology:
  18 Layers High Speed MLO
- 34 Layers High Speed PCB (Megtron6)

The MLO fans out the fine-pitch probe connections to the main PCB. Its multilayer structure accommodates dense routing and allows signal paths and ground references to be designed for high-speed operation.

Front View

MOSAIX / LAS Modular Vertical Probe Card

Side View

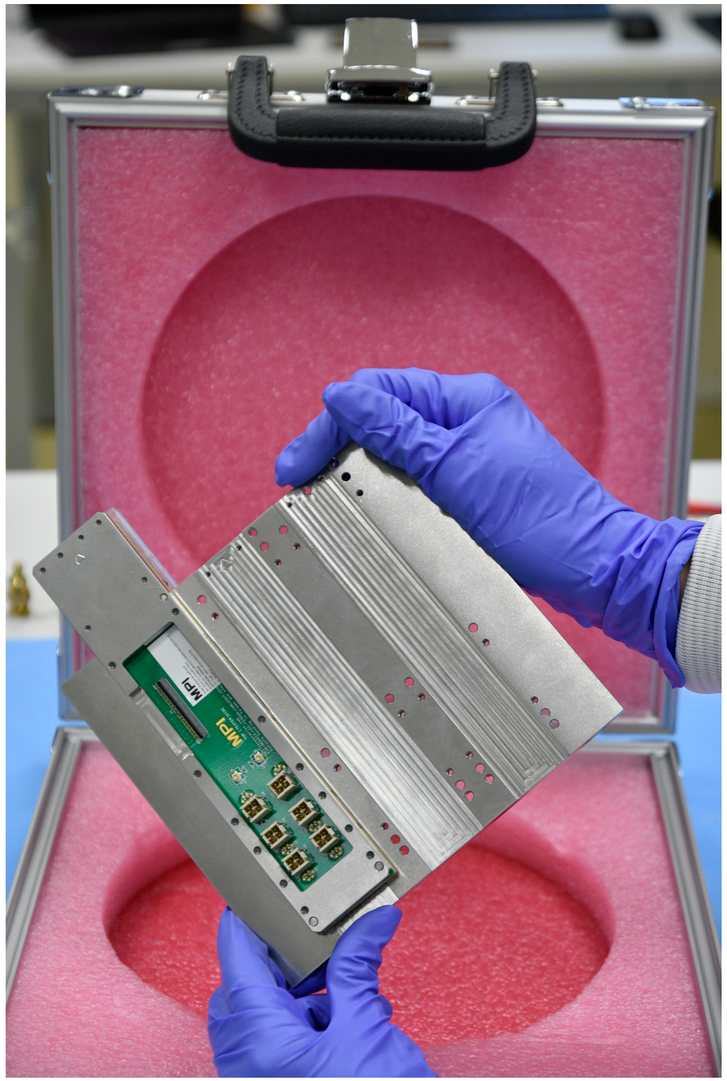


- High Speed MPI Technology:
  18 Layers High Speed MLO

The main PCB routes signals and power between the space transformer and the test electronics.

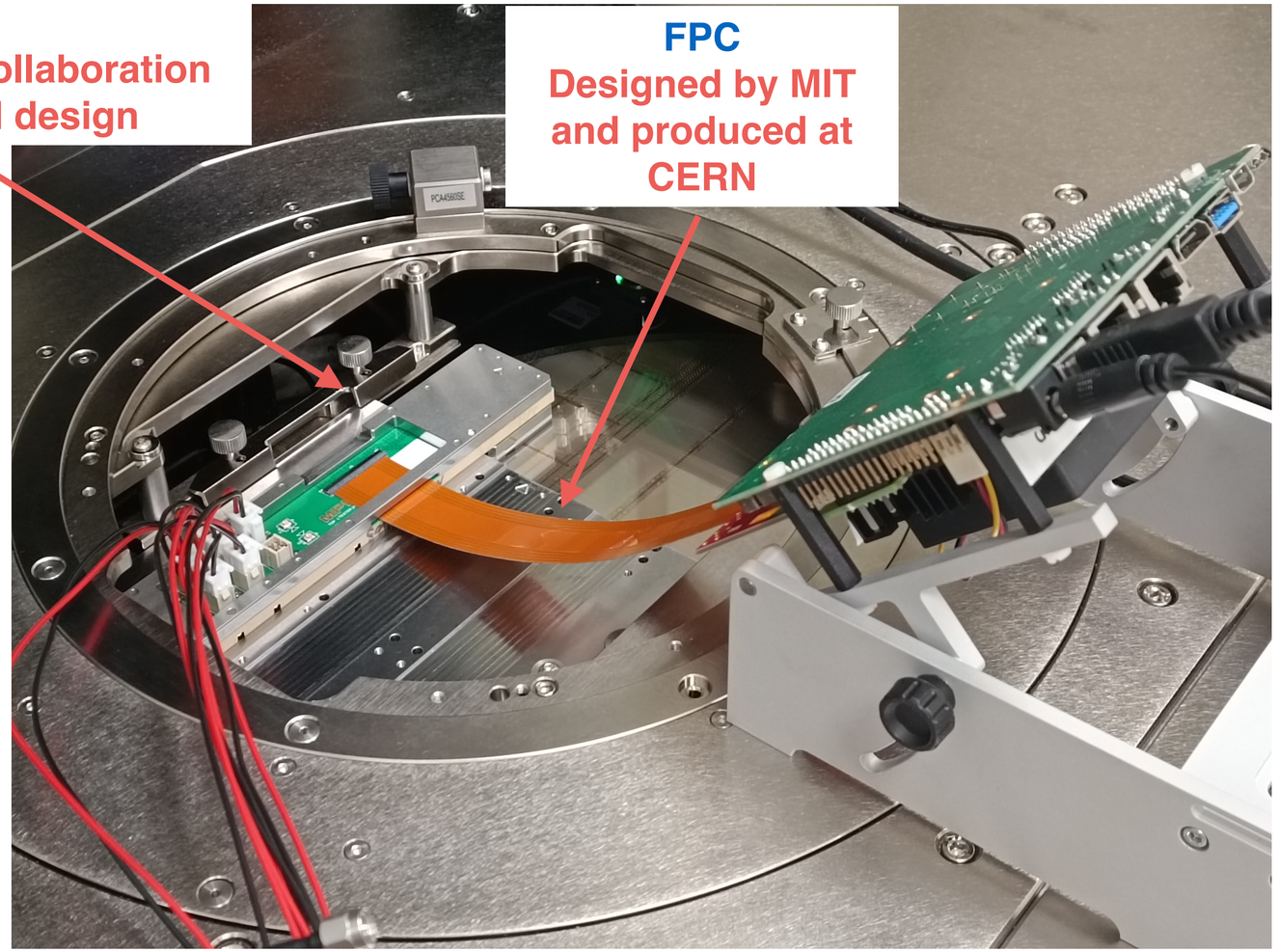
MEGTRON6 is a low-loss laminate that helps limit dielectric losses at high frequencies.

Front View



The Wafer Prober test and characterization system

Probe Card
Developed by MIT/MPI collaboration
Custom concept and design

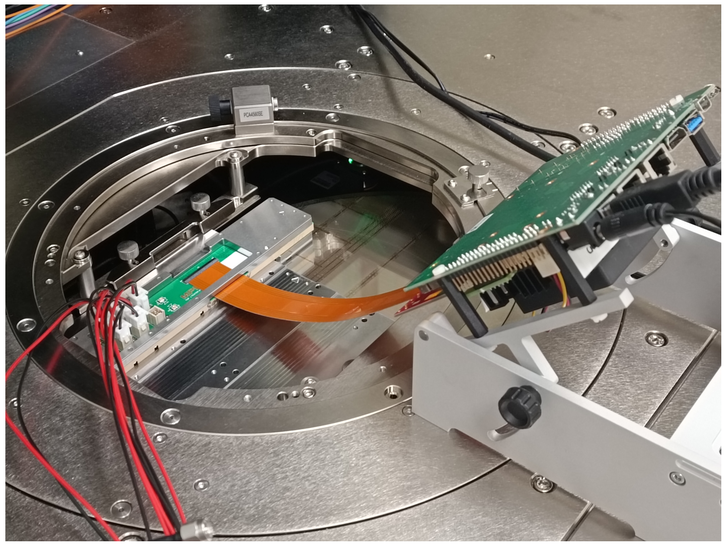


Enclustra FPGA based readout
Commercial HW
FW developed through an ITS3/ SVT collaboration

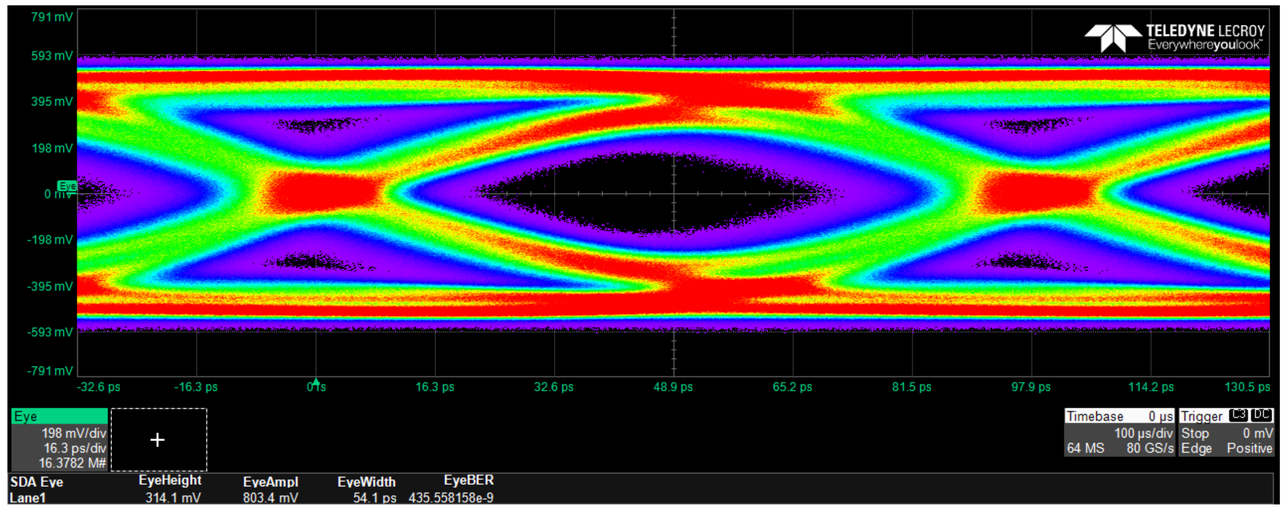
The system is designed for the readout of 3 MOSAIX/LAS in parallel
(Only 1 MOSAIX probe card is displayed in the picture)

Measurements: eye diagrams

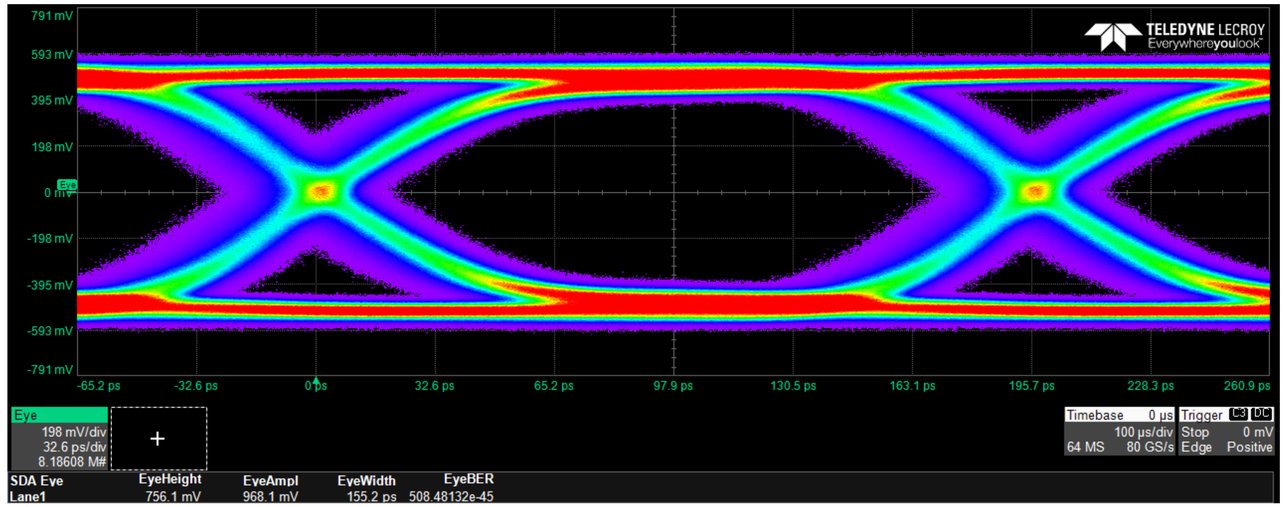
Vertical Probing System:
open Eye Diagrams both at 5.12 and 10.24 Gbps



Eyes measured after the interconnects (Probe Card, FPC (19cm), Interposer PCB, 1m high speed cables, oscilloscope)



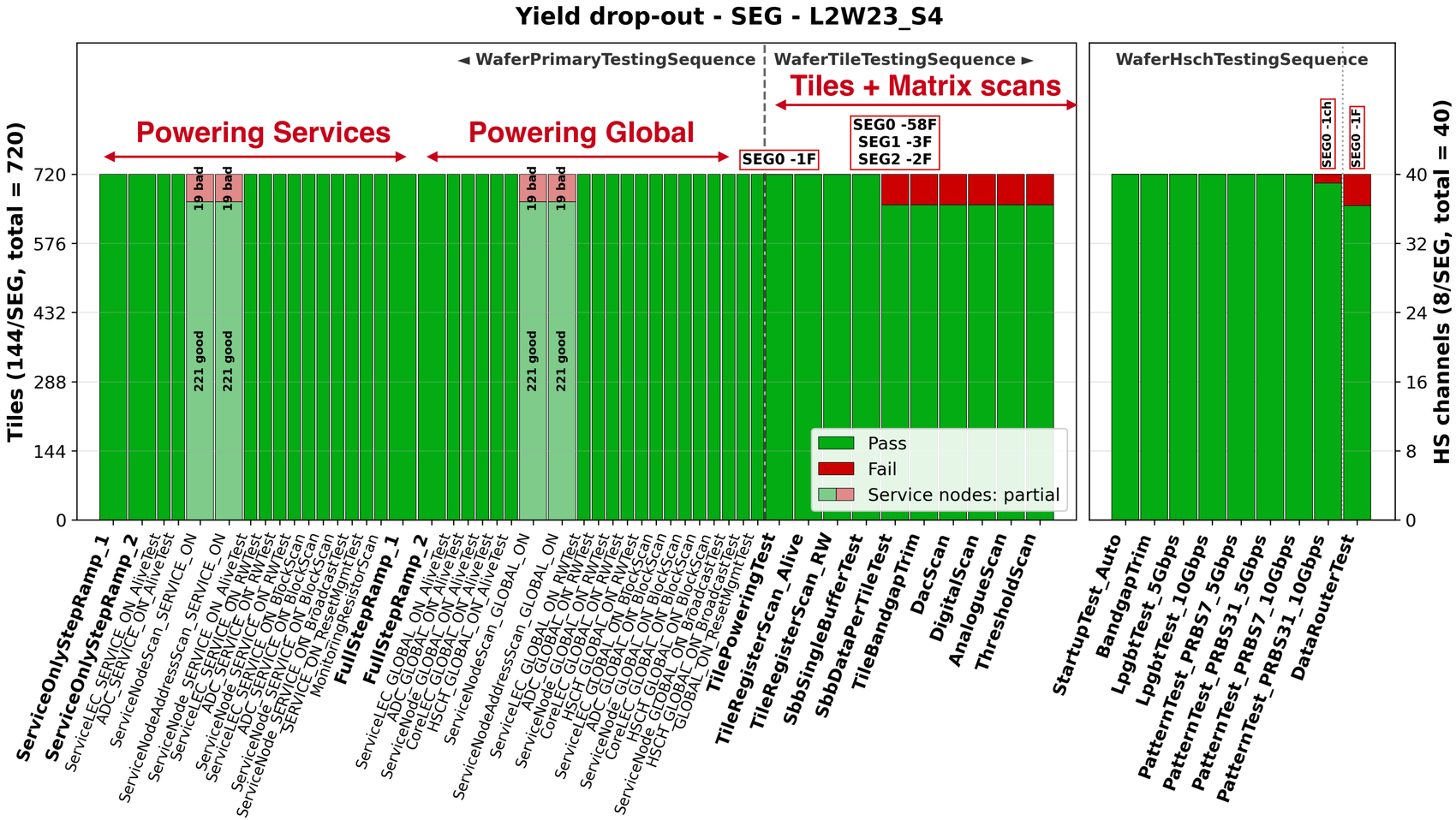
10.24 Gbps



5.12 Gbps

The more open and rectangular the eye diagram, the better the signal integrity and transmission quality.
Amplitude (vertical opening): indicates the noise margin for signal discrimination.
Timing (horizontal opening): indicates the timing margin for reliable sampling.
Jitter appears as horizontal spreading (blurring) of the signal transitions, reducing the eye opening.

Test sequence for each MOSAIX / HS channel



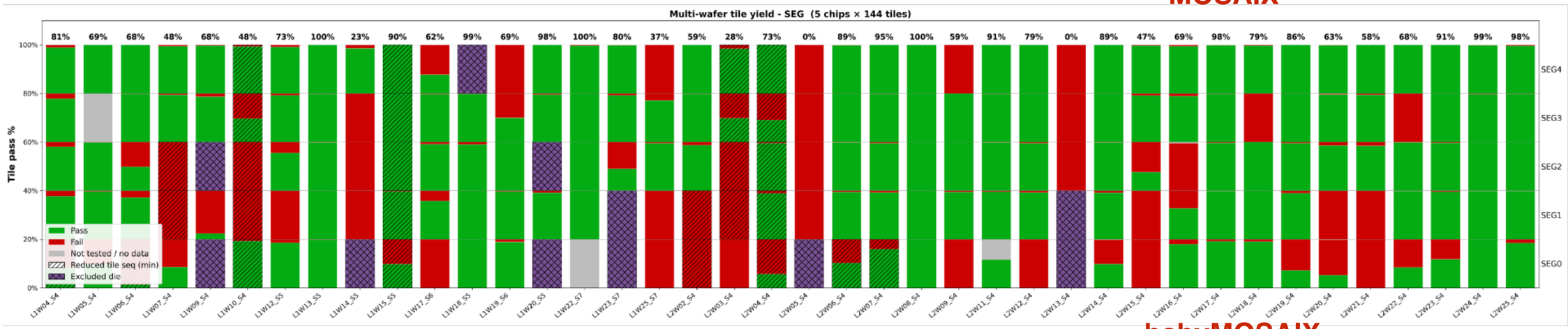
The system can automatically perform full ER2 MOSAIX characterization performing the tests listed above

(the plot summarizes pass/fail results for 720 MOSAIX tiles and 40 high-speed channels across the automated test sequence)

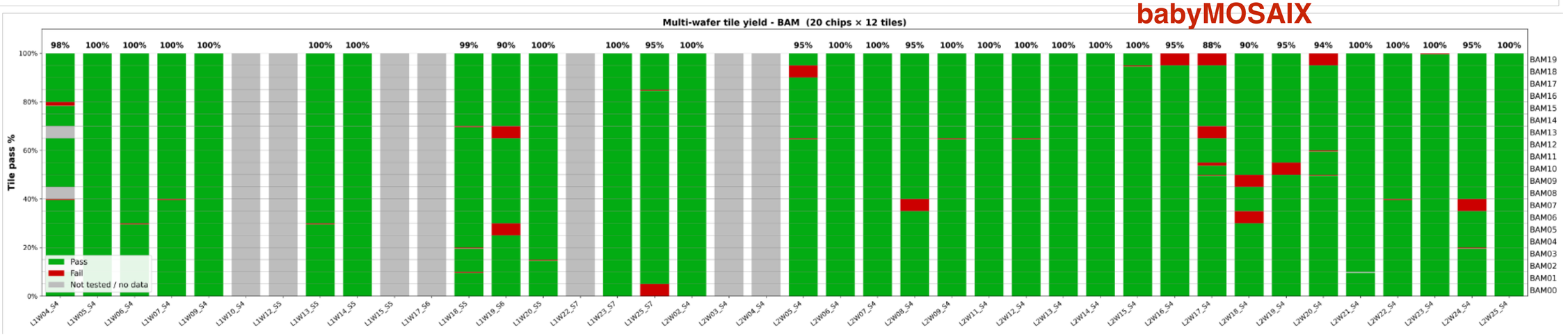
Global analysis framework under construction

ER2 tiles yield (SVT batch)

MOSAIX



babyMOSAIX

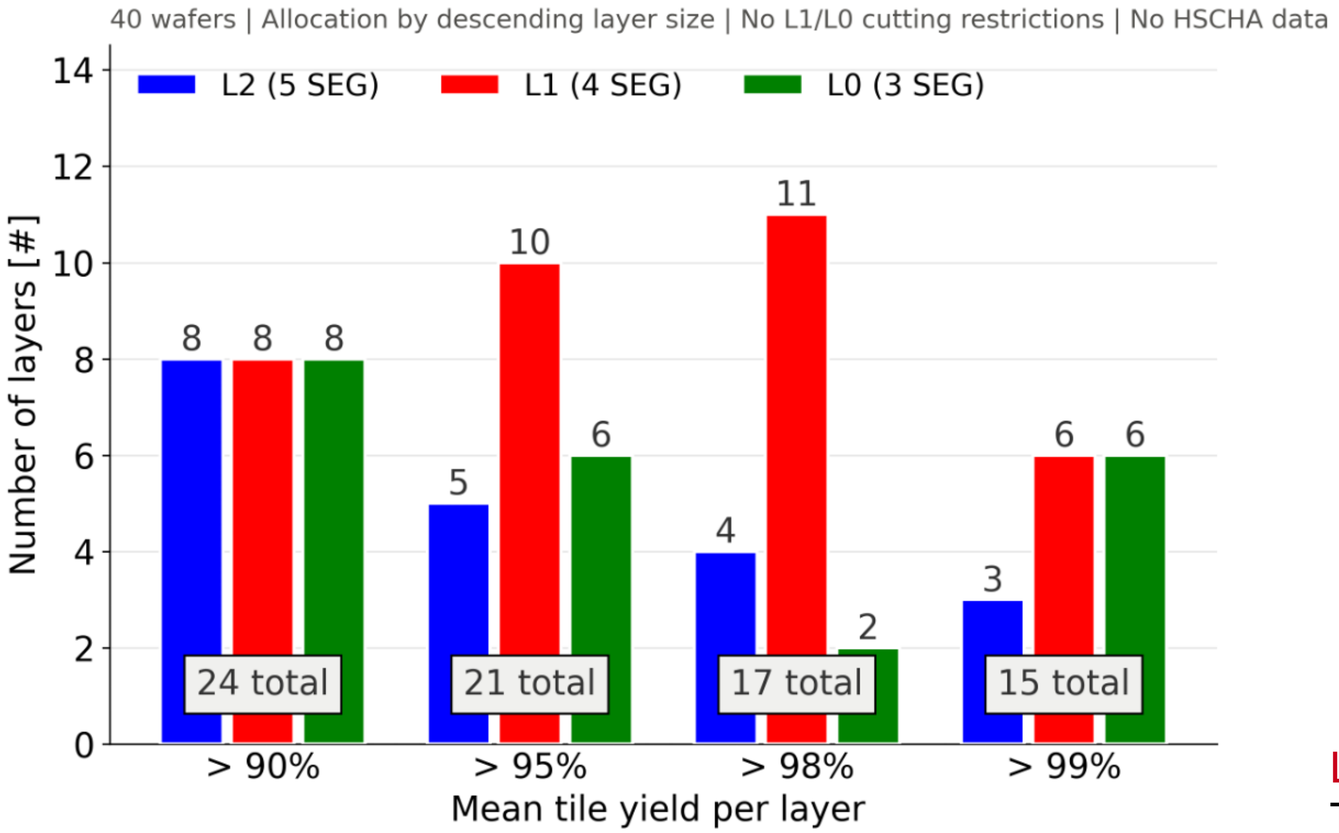


X-axis: individual wafer identifiers, with one vertical bar per wafer.

Left Y-axis: percentage of the wafer's tile population, from 0–100%. Each bar stacks the results for individual chips.

Right-hand labels: chip positions: **SEG0–SEG4** for MOSAIX (upper panel) and **BAM00–BAM19** for babyMOSAIX (lower panel).

ER2 tiles yield (SVT batch)



Estimation of the number of detector layers obtainable from 40 ER2 wafers at different mean tile yield thresholds:

24 layers with mean tile yield >90%
15 layers with mean tile yield >99%

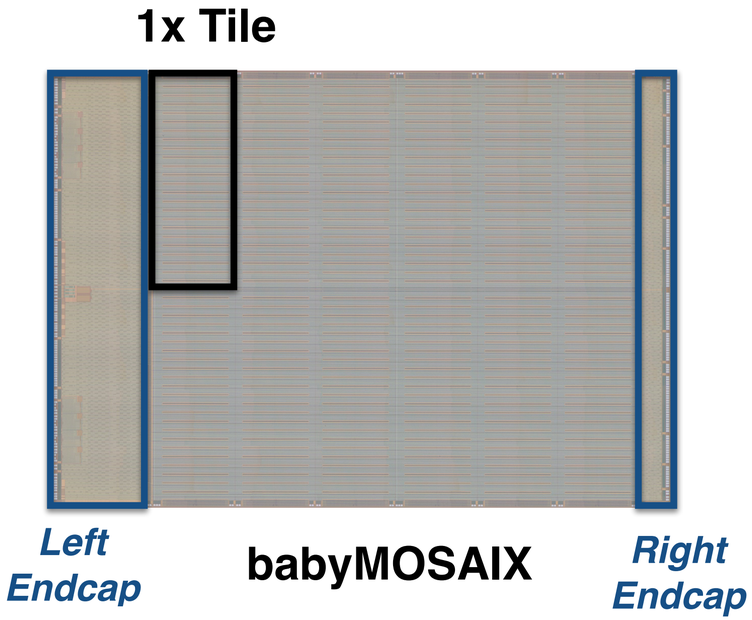
Low yield observed due to manufacturing issue
TowerJazz will update the production process

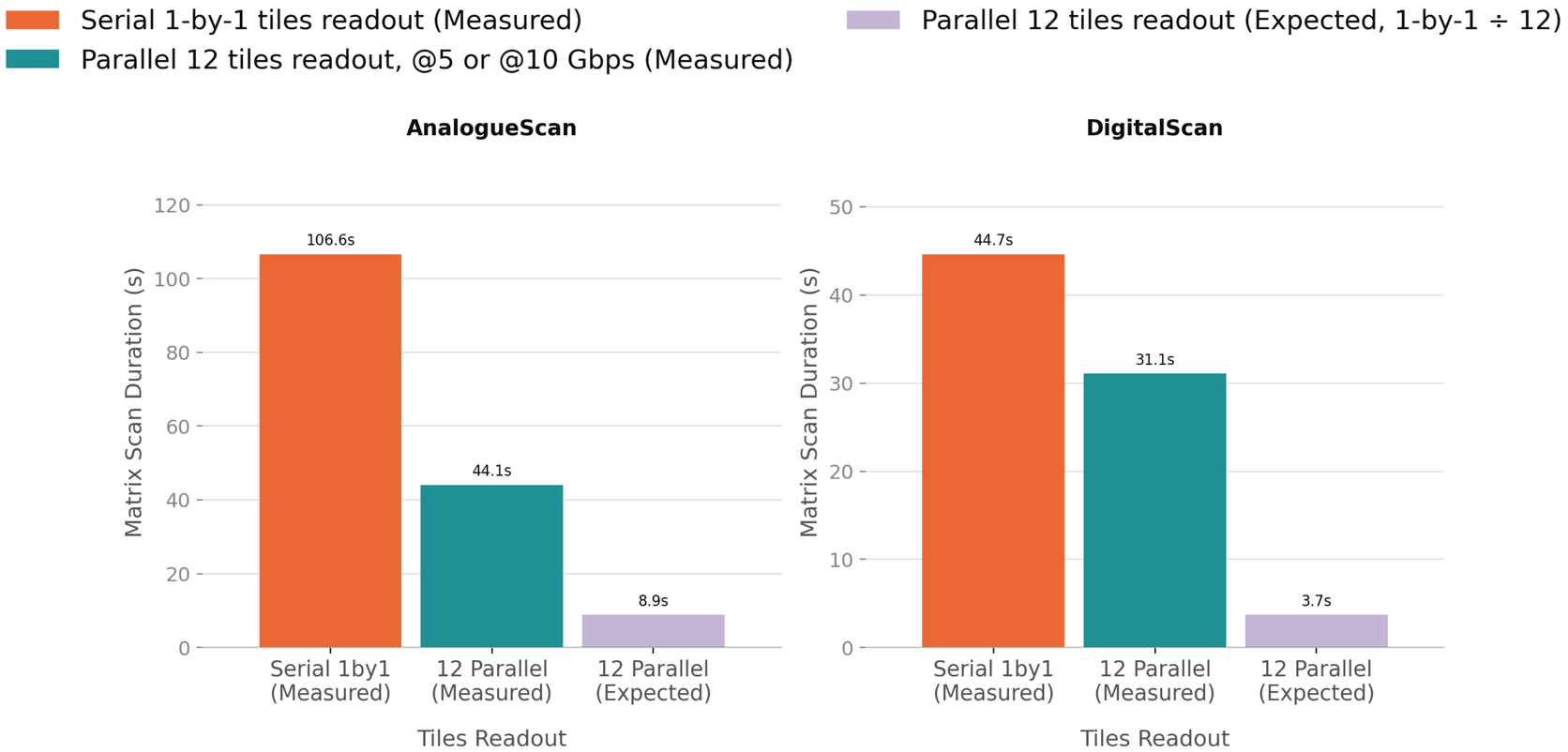
Impact of SBB crosstalk (unwanted electrical coupling involving those connections) not considered here
Mitigation has been put in place for ER3

High speed readout

Parallelized high-speed scan the matrix of tiles, **drastically reducing testing times**

BabyMOSAIX: all 12 tiles can be read out in parallel through a single transmitter operating at 5.12 or 10.24 Gb/s,

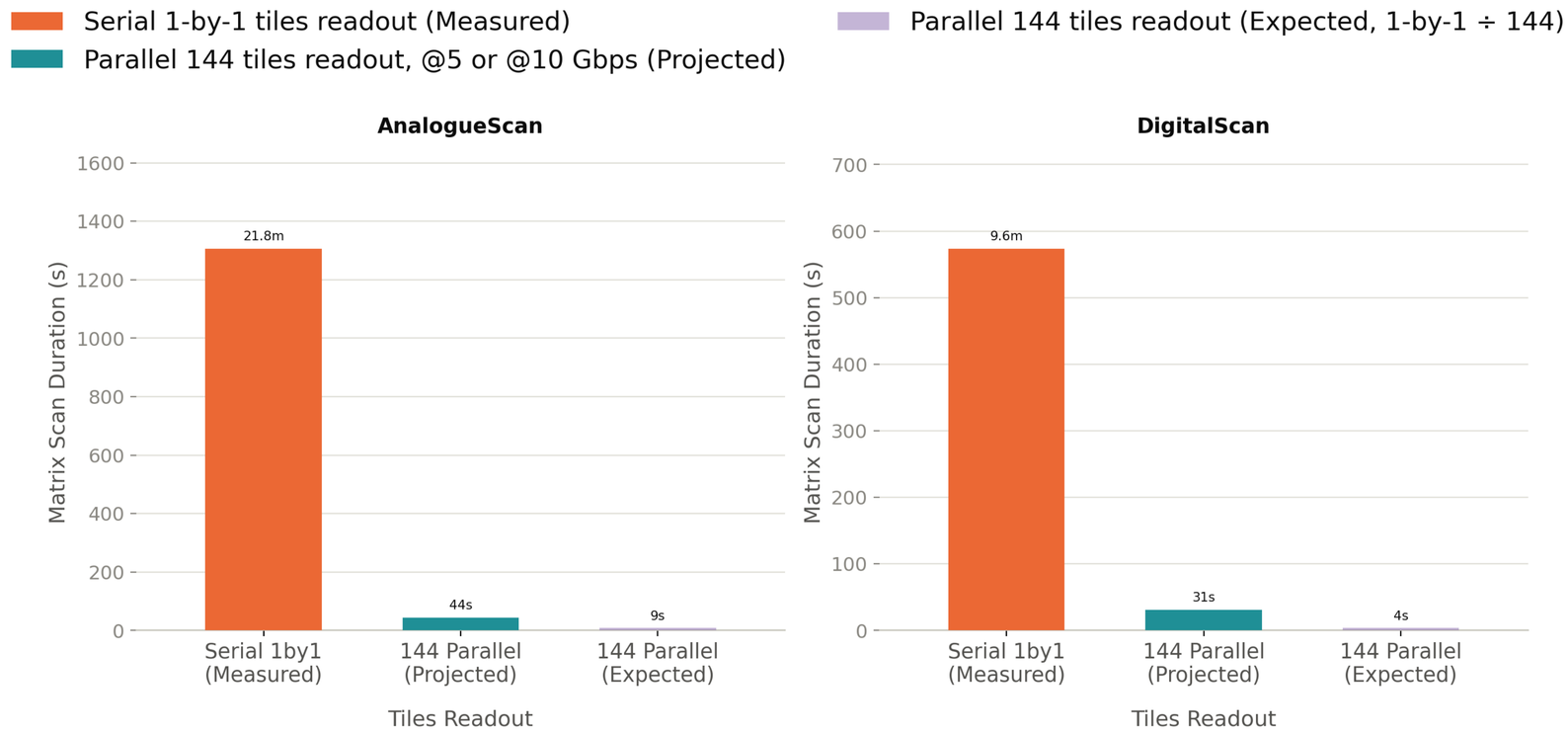




Parallel readout reduces the **analogue scan time from 106.6 s to 44.1s**.

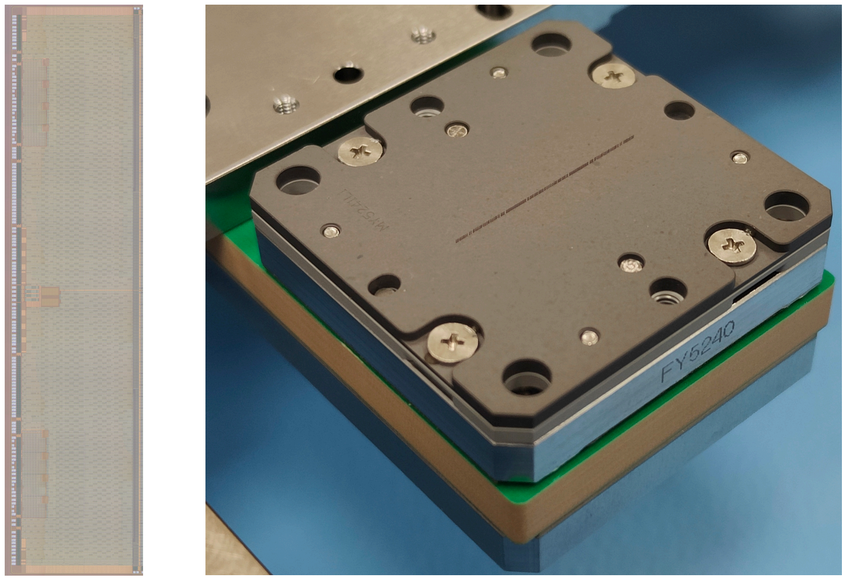
High speed readout: MOSAIX

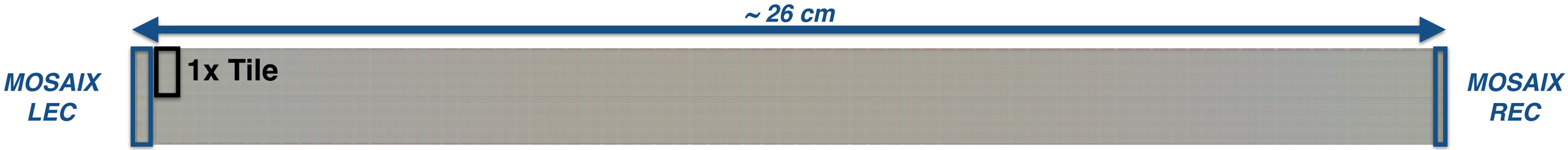
All **144 tiles** can be read out in parallel using **3 transmitters at 10.24 Gb/s** or **6 at 5.12 Gb/s**



Analogue: **~ 44 s**, compared with **21.8 min** for sequential readout
Digital: **~31 s**, compared with **9.6 min** for sequential readout

Requirement for “all-tiles” parallel operation with MOSAIX

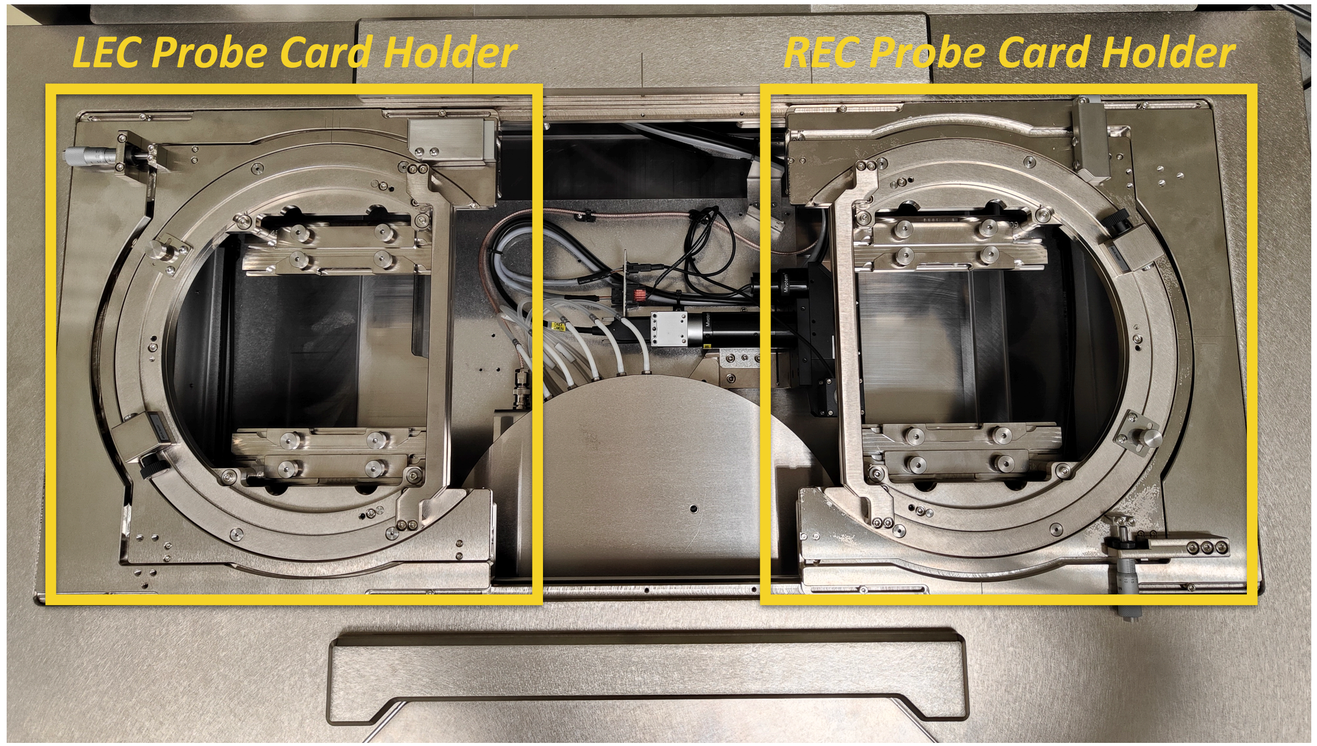


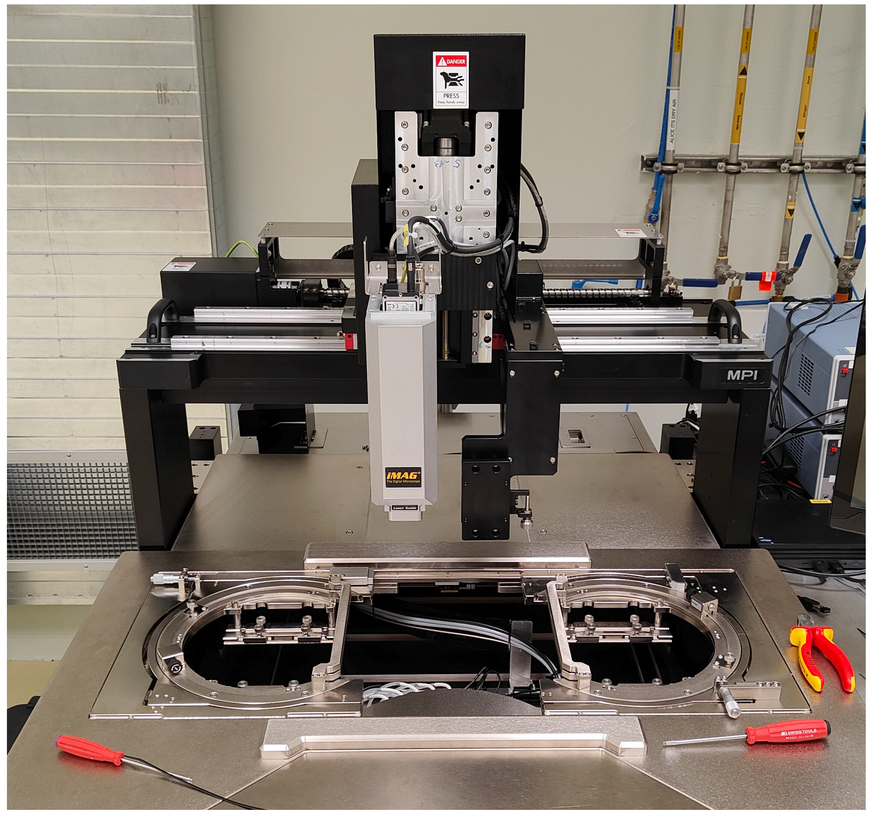


Full parallel operation requires **power from both endcaps (LEC and REC)**

Wafer Prober: custom upgrades

- Custom platen allows to **host multiple Probe Card Holders**
- **Double side probing allows full chip powering and operation**

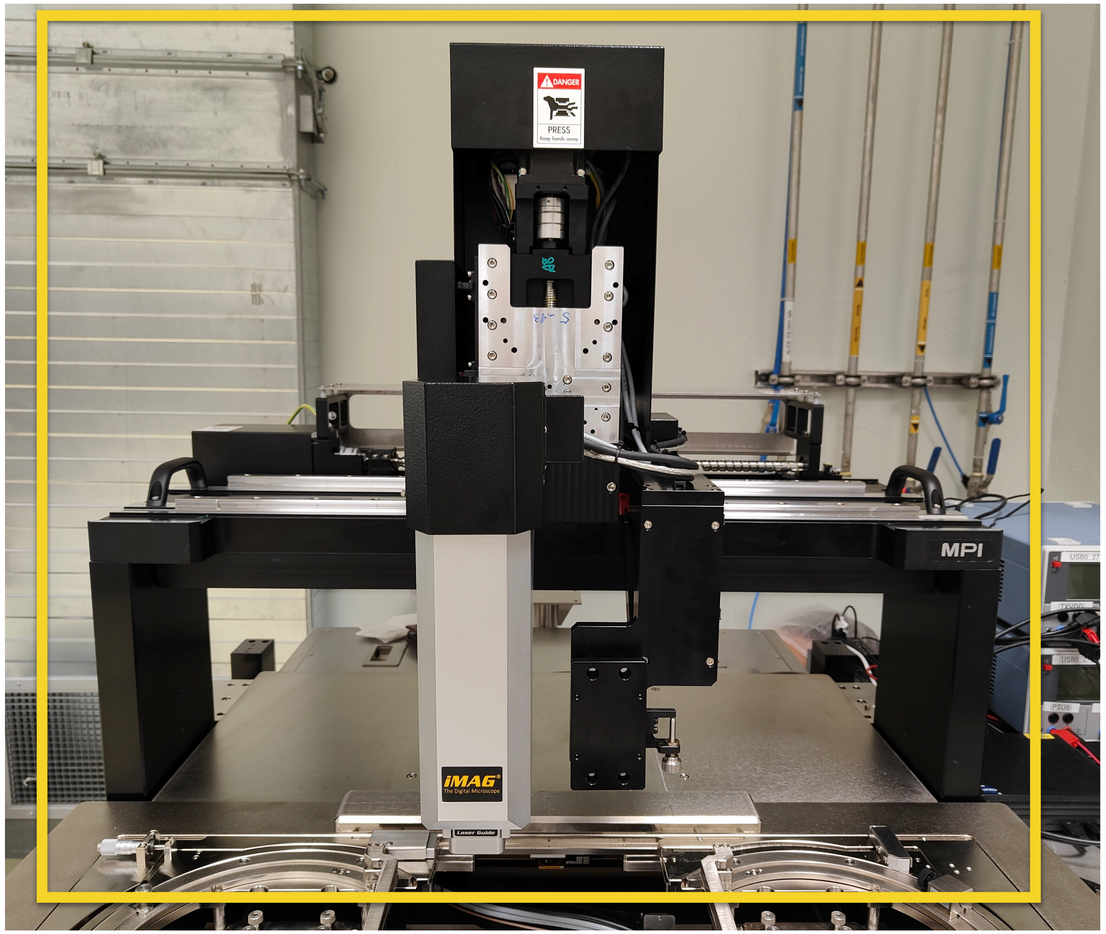




Designed by PixElϕ Lab, realised by MPI Taiwan

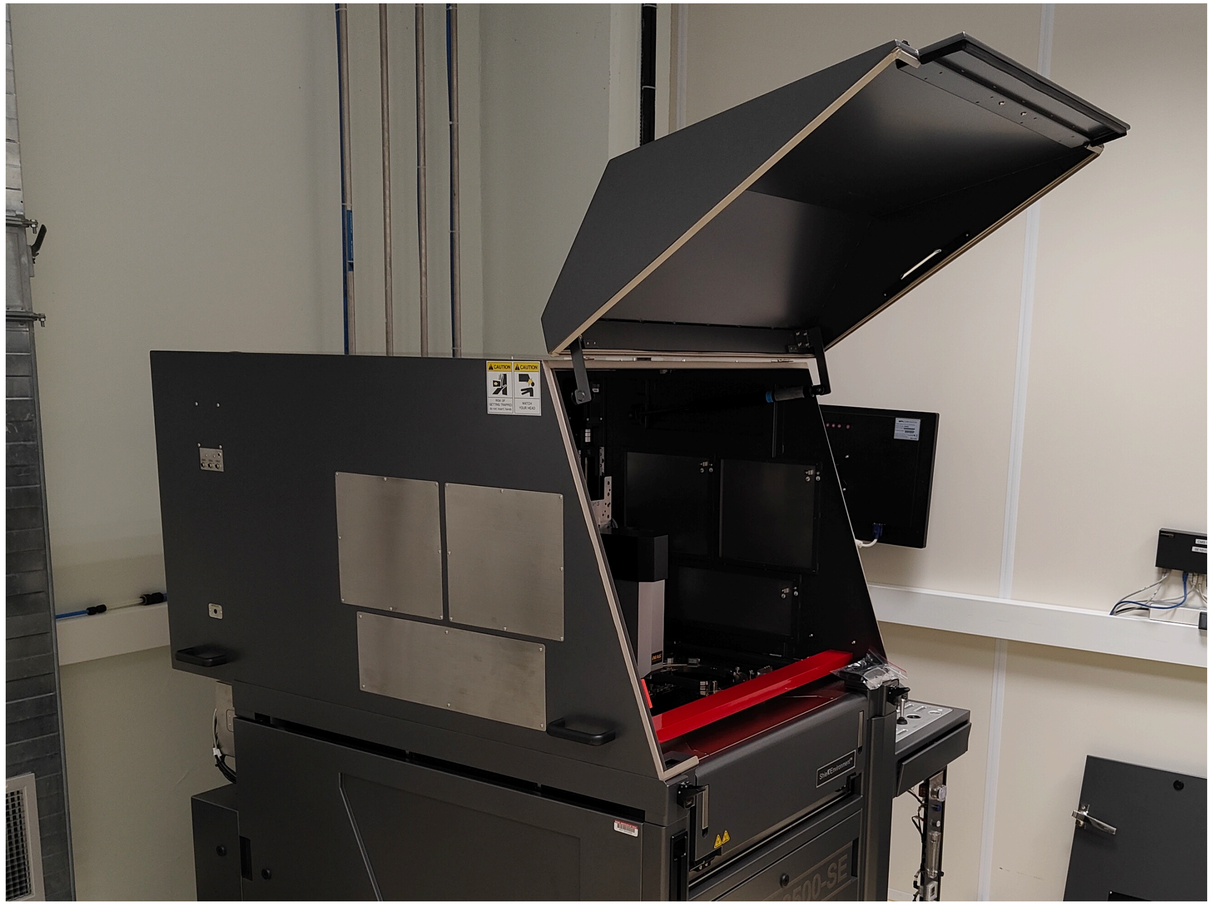
Wafer Prober: custom upgrades

Custom movement on pixel matrix



Custom movement allows **fully automated scan of pixel matrix with custom instrumentation**: laser, radiation source, IR camera

Wafer Prober: custom upgrades



See S. Caregari's talk at TWEPP
https://indico.cern.ch/event/1502285/contributions/6554595

Dark box extends shielded environment volume allowing **possible installation of instruments for sensor characterization**

These custom upgrades **add sensor characterization capabilities to the wafer prober's** fully automated high-speed ASIC testing setup

→ Essential for large-scale SVT production.

Throughput Scenarios for functional Tests

Testing target: 400 wafers, approximately **5,300 sensors to test**

Multipoint probing: Up to **3 sensors probed in parallel on the same wafer**
→ Enabled by the recent upgrades

Automated operation: Automatic wafer loading and unattended operation for **up to 25 wafers**
→ The prober is designed to support this option, but it is not yet available

Throughput Scenarios for functional Tests

Too Slow

Optimistic

MOSAIX Wafers	LAS Wafers	Technology	Test Coverage	MOSAIX/LAS Test Time (h)	Prober-busy (h)	Prober utilisation	Calendar days
100	300	**Vertical (LEC Only)**	Only few RSU/Tiles can be powered & readout	1.5 *	8350	59%	**559**
100	300	**Vertical (LEC + REC)**	Full Powering & Readout or 1 MOSAIX	0.75 *	4375	34%	**488**
100	300	**Vertical (LEC + REC) Multipoint (3 DUT)**	Full Powering & Readout of 3-MOSAIX	0.75 *	1900	24%	**256**
100	300	**Vertical (LEC + REC) Multipoint (3 DUT) Automatic**	Full Powering & Readout of 3-MOSAIX	0.75 *	1624	70% (25 w slots is 92%)	**89**

Multi-site Vertical, Multi-point Vertical, Automatic Vertical guarantee the fastest QC throughput

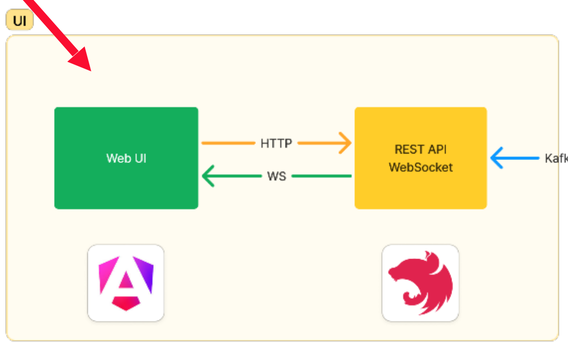
SVT SW Framework

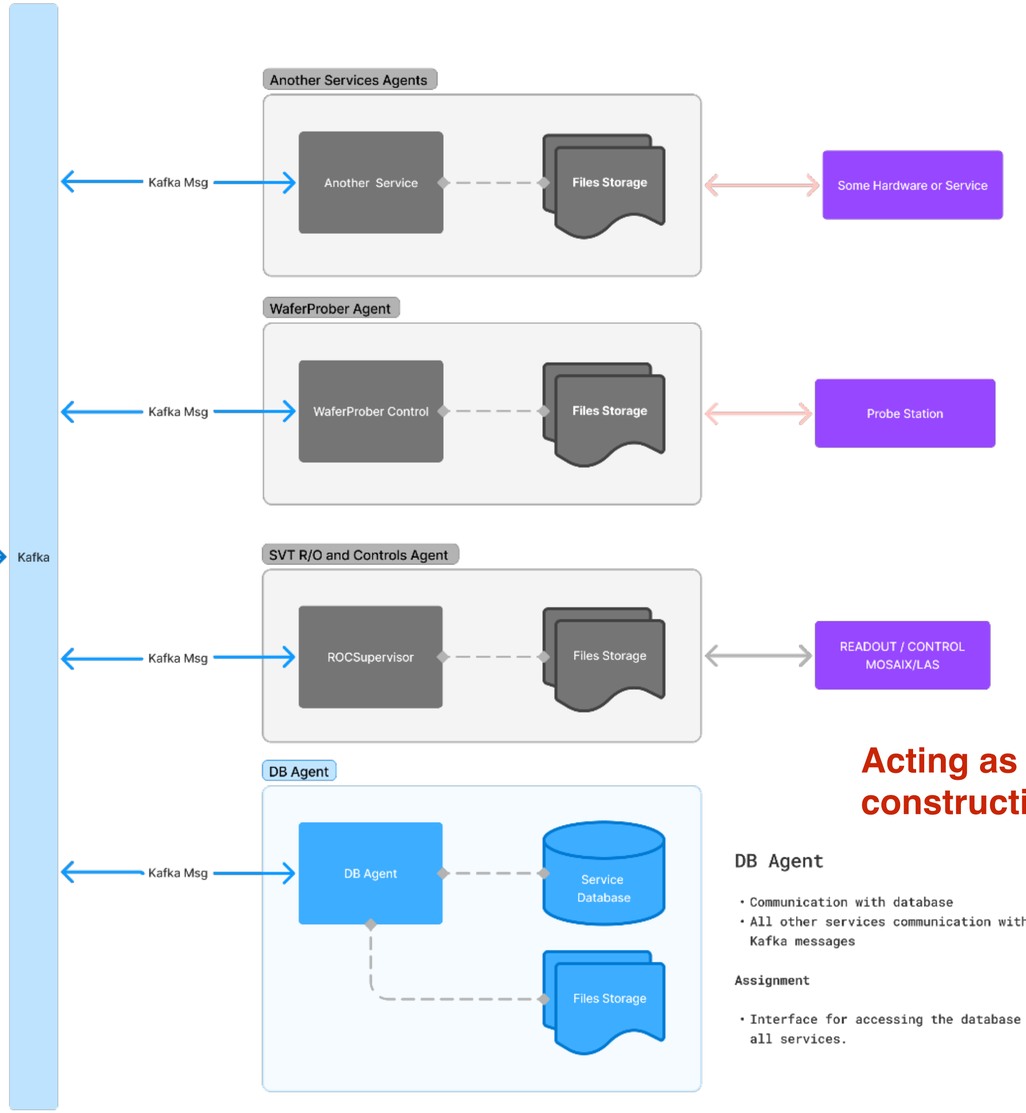
Agents layer, **distributed**

Kafka backbone, **distributed**

UI produces commands and receives data to visualize. **Web Based**

SVTSupervisor acts as global brain of the system. **On a dedicated server**





Acting as preliminary construction DB

DB Agent

- Communication with database
- All other services communication with Kafka messages

Assignment

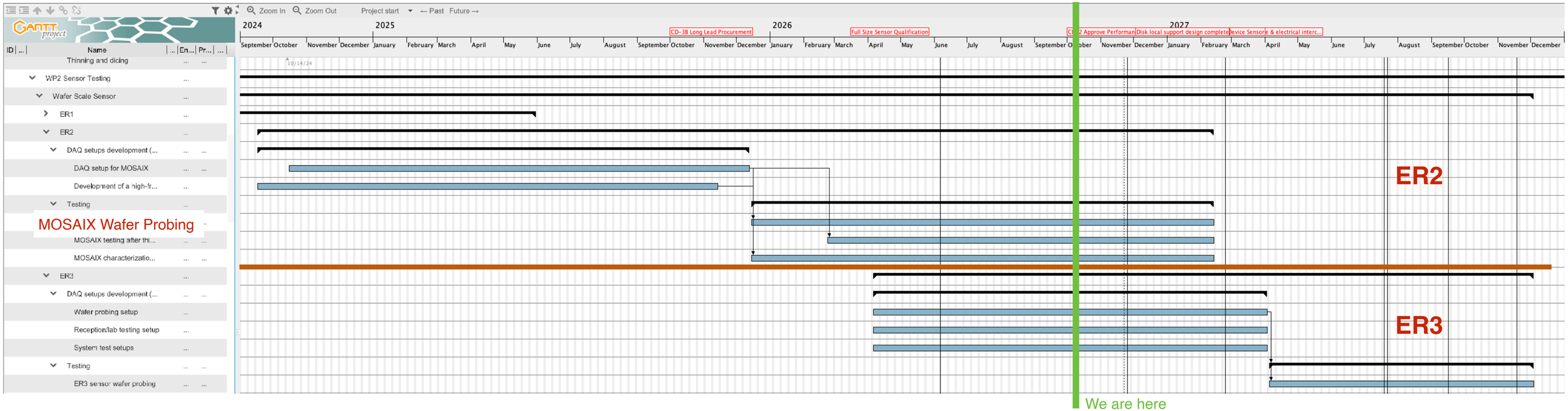
- Interface for accessing the database for all services.

A version of the system including UI, DB, WaferProber controller, R/O controller software is already in production!

→ **Already deployed for ongoing testing and characterization activities**

→ **This framework represents the baseline for the future detector control and calibration systems**

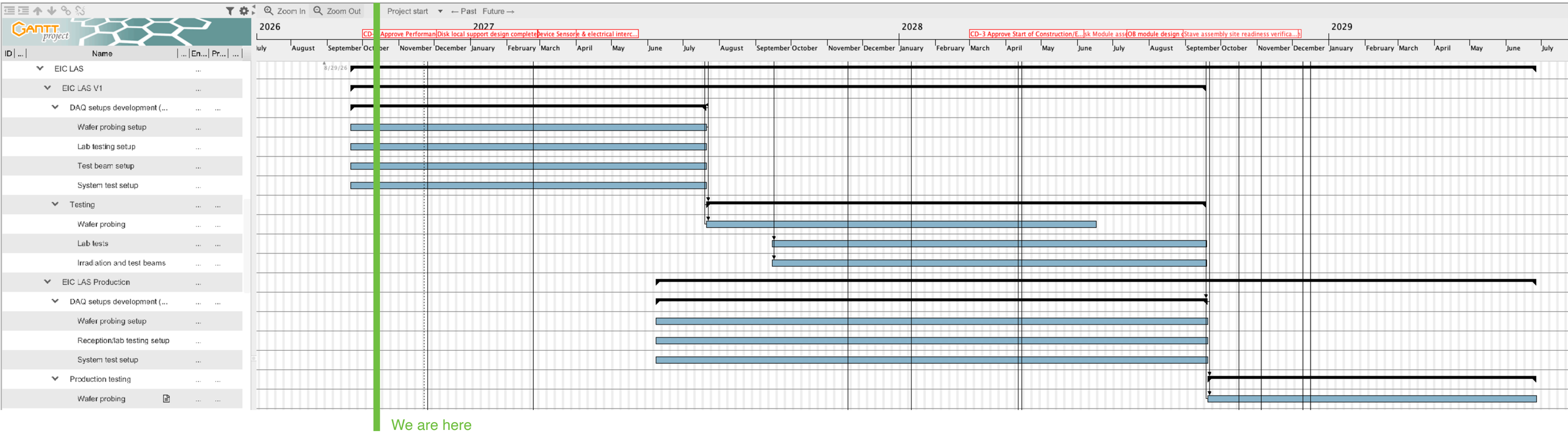
Schedule ER2/ER3



The high-speed vertical probing strategy has proven to be successful

→The milestone for wafer probing testing/characterization of ER2
was completed several months ahead of schedule

Schedule LAS



The next challenge (work is in progress) is to deliver a fully-automatic testing system ready for large scale LAS testing

Toward a full LAS production system: work needed

Hardware optimization:

- LEC probe card V2 design (agreed with MPI a revision of V1 with ~no cost)
- REC probe card design with multipoint architecture
- Data transfer from probe card to readout electronics improvement (Flex, HS cables, etc)
- Redesign of Enclustra baseboard to optimize high-speed communication (verified improvement already with ITS3 DME)
- Readout firmware optimization to speed up calibration procedures

SVT Software Framework:

- Wafer-Prober automatic control V1 in production but work ongoing for further automatic operation
- MOSAIX readout and control software V1 in production. Optimization and functionality extension ongoing
- Ancillary chip control and test agent V1 under deployment.
- DB in production with minimal information parameters. Ongoing development to cover the full spectrum of test required
- UI in production as demonstrator with core functionalities. Ongoing development
- Framework for data analysis to be produced

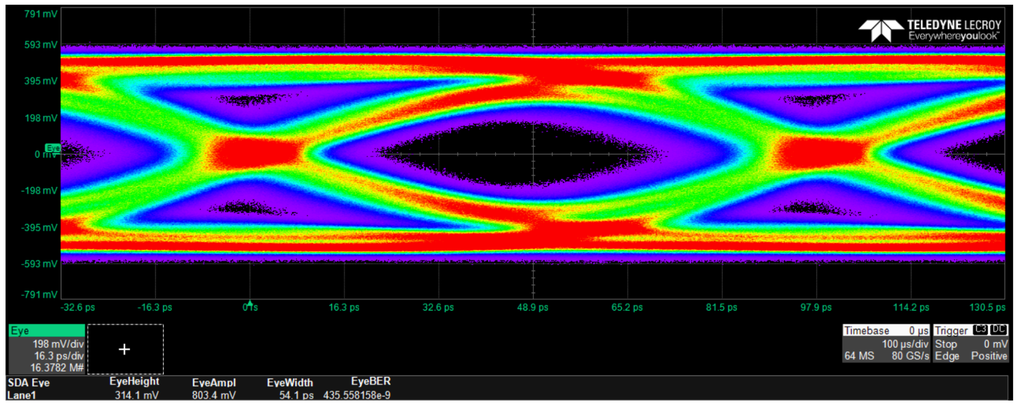
General operation:

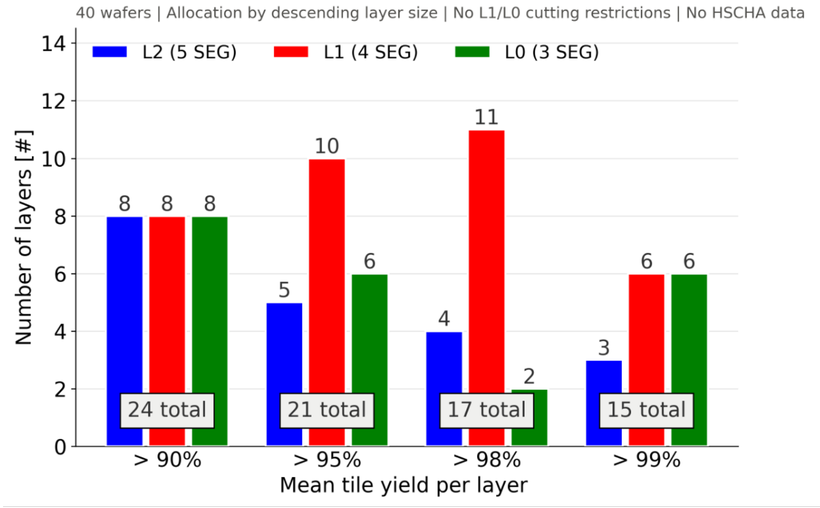
- Exercise multisite operation
- Characterization with laser and radioactive source
- Further automation

Summary: a major milestone completed!

High-speed vertical probing has proven successful
on-wafer testing at 5.12 and 10.24 Gbps

→ parallel tile readout and shorter test times for SVT sensor qualification
→ essential to support ER2 characterization and yield assessment.



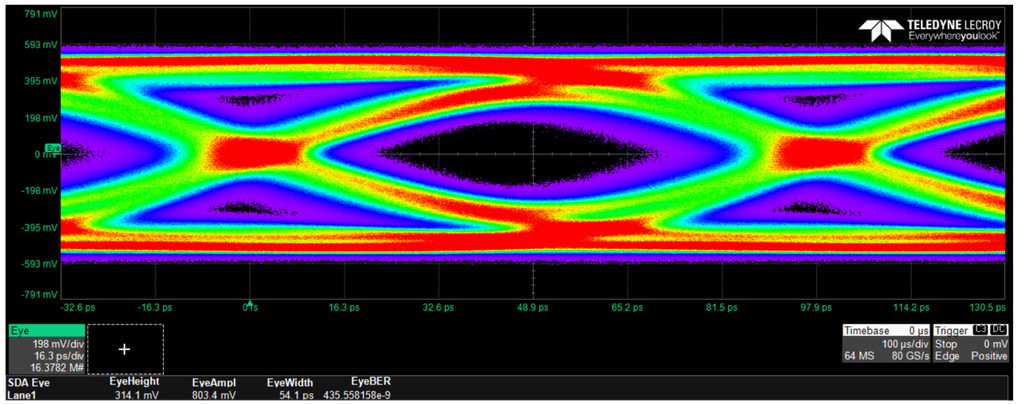


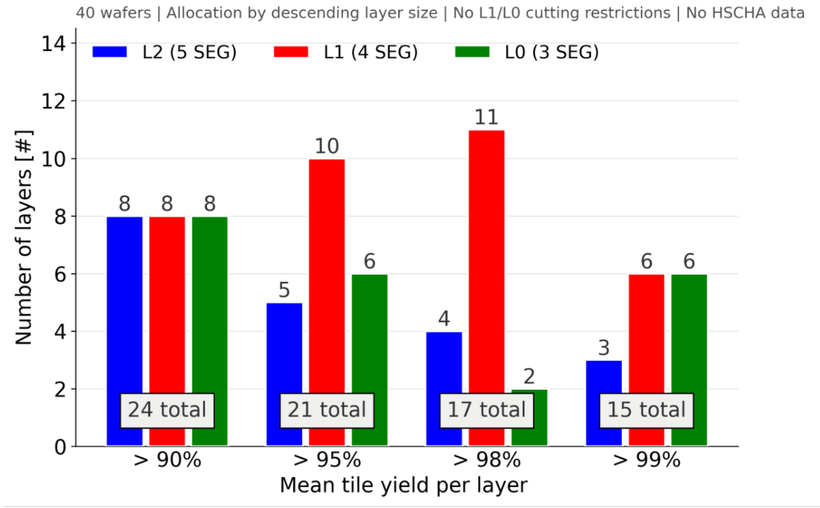
→ **The ER2 wafer-probing and characterization milestone was completed several months ahead of schedule**
→ **The next challenge is readiness for SVT production tests**

Summary: a major milestone completed!

High-speed vertical probing has proven successful
on-wafer testing at 5.12 and 10.24 Gbps

→ parallel tile readout and shorter test times for SVT sensor qualification
→ essential to support ER2 characterization and yield assessment.





→ **The ER2 wafer-probing and characterization milestone was completed several months ahead of schedule**
→ **The next challenge is readiness for SVT production tests**

thank you for your attention!

BACKUP

(Few) Throughput Scenarios – Impedance & Functional Tests

Number of Wafers: 400, Number of Sensors (MOSAIX / LAS) per Wafer: 5 / 16, ~ 5300 Sensors to test

Multipoint: multiple sensors probed in parallel on the wafer (up to 3)

Automatic: Fully automatic wafer loading and continuous operation without operator (for 25 wafers)

** Current Test Time estimates, subject to further optimization*

Too Slow

Optimistic

MOSAIX Wafers	LAS Wafers	Technology	Test Coverage	MOSAIX/LAS Test Time (h)	Prober-busy (h)	Prober utilisation	Calendar days
100	300	**Vertical (LEC only)**	Almost Complete (Missing Full Powering & Readout)	1.5 + 5m *	9200	48%	**733**
100	300	**Vertical (LEC + REC)**	**Complete**	0.75 + 5m *	5225	28%	**652**
100	300	**Vertical (LEC + REC) Multipoint**	**Complete**	0.75 + 5m *	2750	19%	**425**
100	300	**Vertical (LEC + REC) Multipoint Automatic**	**Complete**	0.75 + 5m *	2174	43% (25 w slots is 89%)	**187**

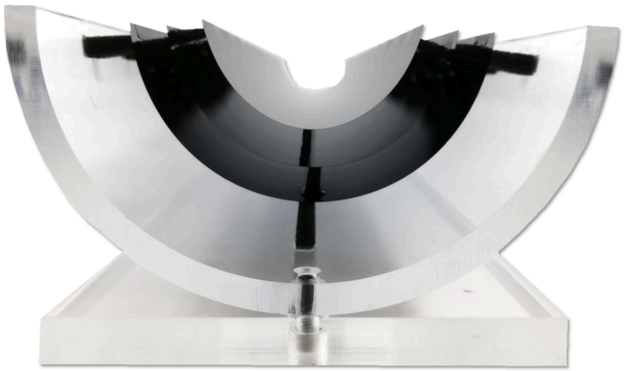
Multi-site Vertical, Multi-point Vertical, Automatic Vertical guarantee the fastest QC throughput

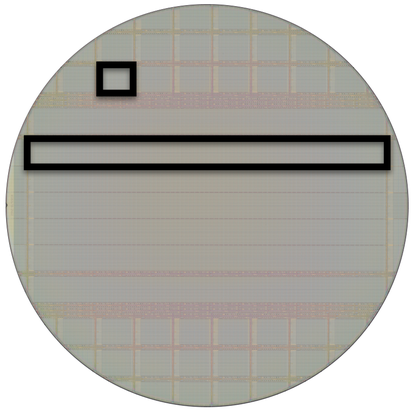
ALICE ITS3 and ePIC SVT

ALICE ITS3
ALICE Future Tracker Detector - CERN
Based on MOSAIX - MAPS
Readout @ 5.12, 10.24 Gbps
~ 0.6m^2 of active silicon -

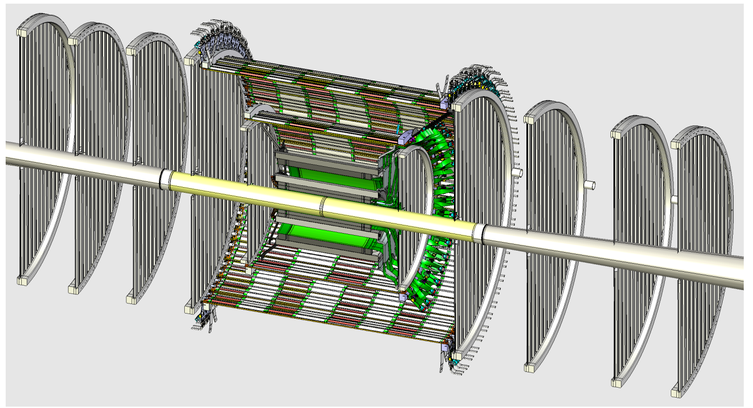
ePIC SVT
ePIC Future Tracker Detector - BNL
Based on MOSAIX and LAS - MAPS
Readout @ 5.12, 10.24 Gbps
~ 8.5m^2 of active silicon

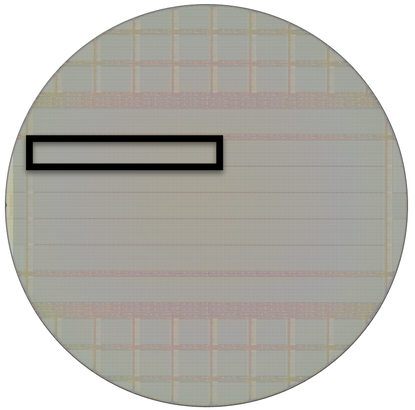
ITS3 MOSAIX Wafer





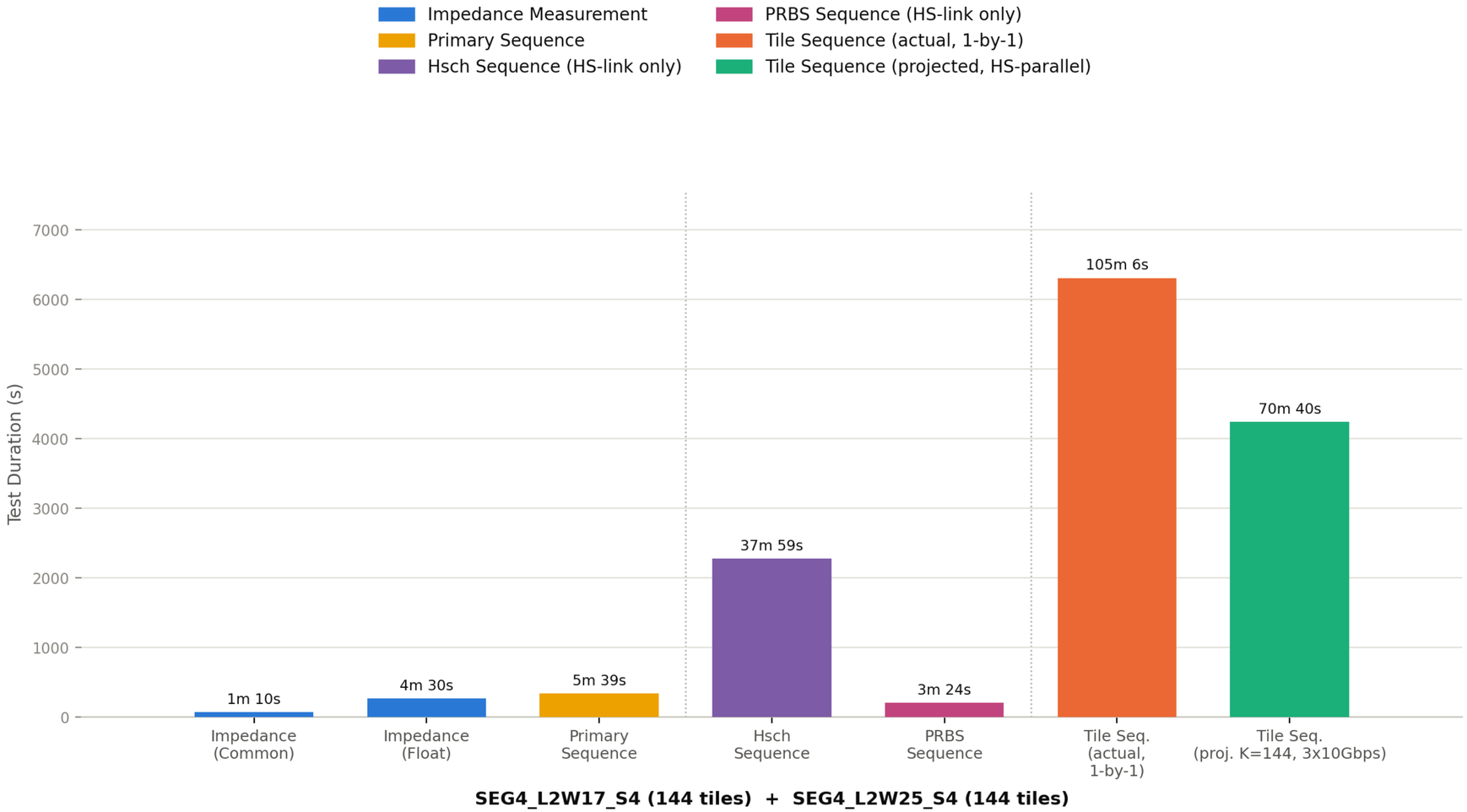
babyMOSAIX: 1x RSU
MOSAIX: 12x RSU
(RSU: Repeated Sensor Unit)





LAS: 5-6x RSU
(Design in progress)

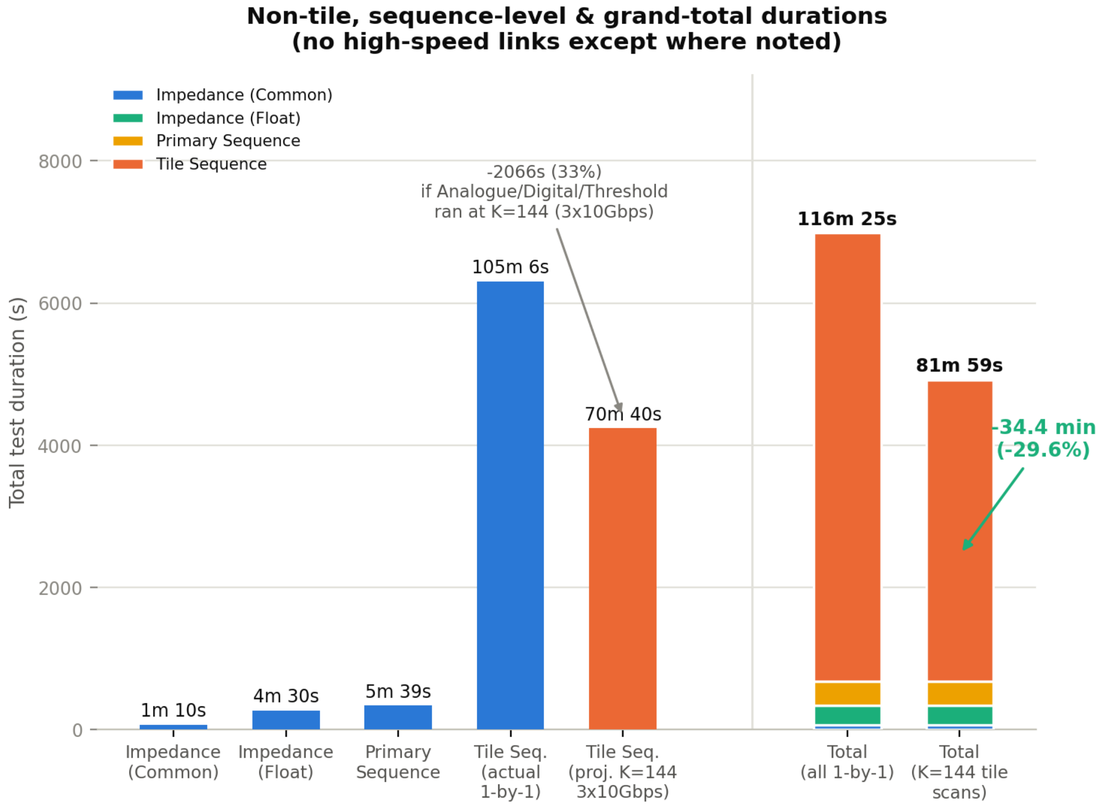
Testing time breakdown

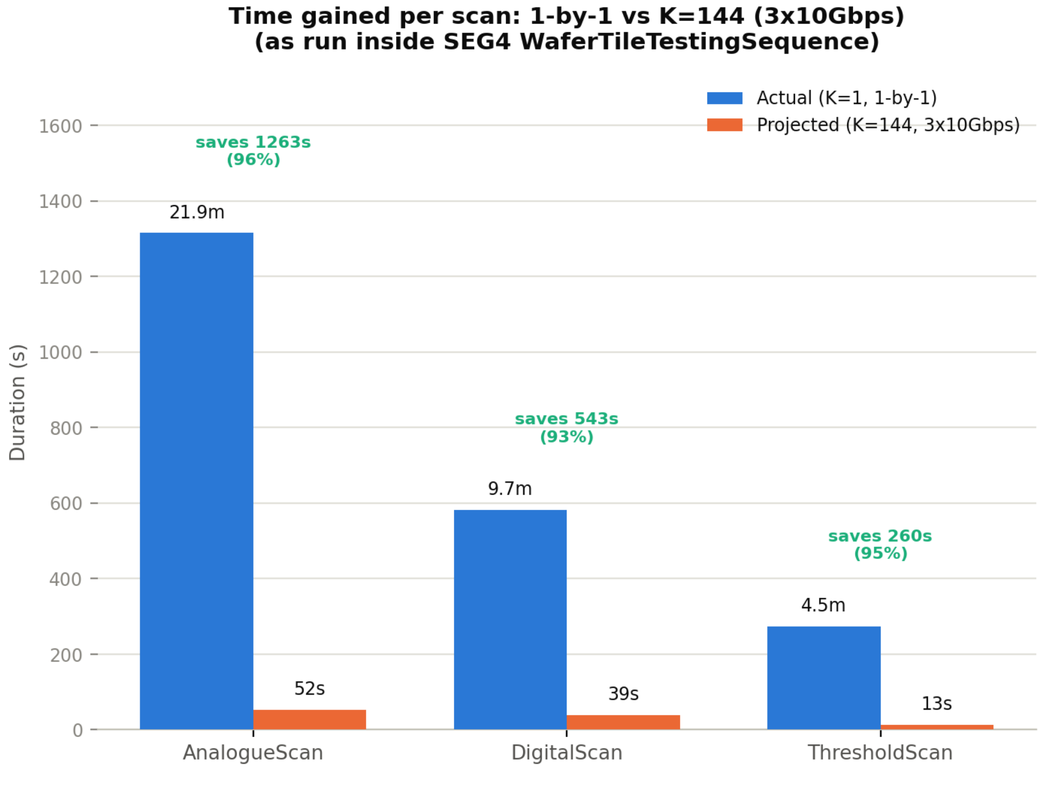


Time optimization still possible adjusting the matrix parameters scan and pushing parallelization forward (next slide)

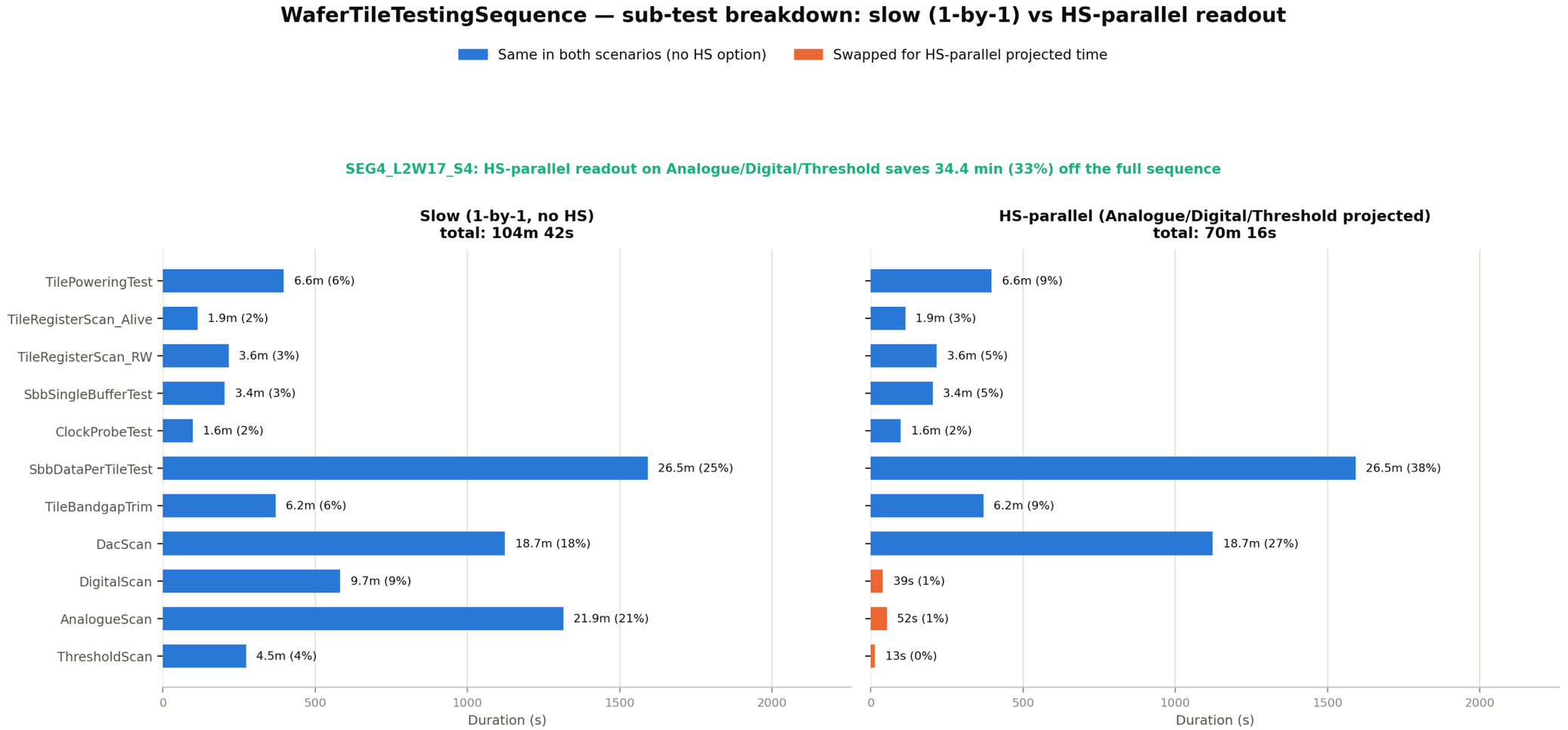
Testing time breakdown

SEG4_L2W17_S4 — Impedance measurement & production sequence timing





Testing time breakdown



(Few) Throughput Scenarios – Functional Testing

Number of Wafers: 400, Number of Sensors (MOSAIX / LAS) per Wafer: 5 / 16, ~ 5300 Sensors to test

Relying only on Cantilever Probing looks prohibitive for both Testing time and Testing Capabilities
Vertical Probing from both LEC and REC enables full testing capabilities

MOSAIX Wafers	LAS Wafers	Technology	Test Capabilities	MOSAIX/LAS Test Time (h)	Prober-busy (h)	Prober utilisation	Calendar days
100	300	**Cantilever**	Inomplete (Missing HS Testing)	3 / 2	11500	55%	**839**
100	300	**Cantilever (LEC + REC)**	Inomplete (Missing HS Testing)	3 / 2	11500	55%	**839**
100	300	**Vertical**	Almost Complete (Missing Full Powering & Readout)	1.5	8350	59%	**559**
100	300	**Vertical (LEC + REC)**	**Complete**	0.75	4375	34%	**488**

(Few) Throughput Scenarios

Number of Wafers: 400, Number of Sensors (MOSAIX / LAS) per Wafer: 5 / 14, ~ 5600 Sensors to test

Multipoint: multiple sensors probed in parallel on the wafer
Automatic: Fully automatic wafer loading and continuous operation without operator

Too Slow

Optimistic

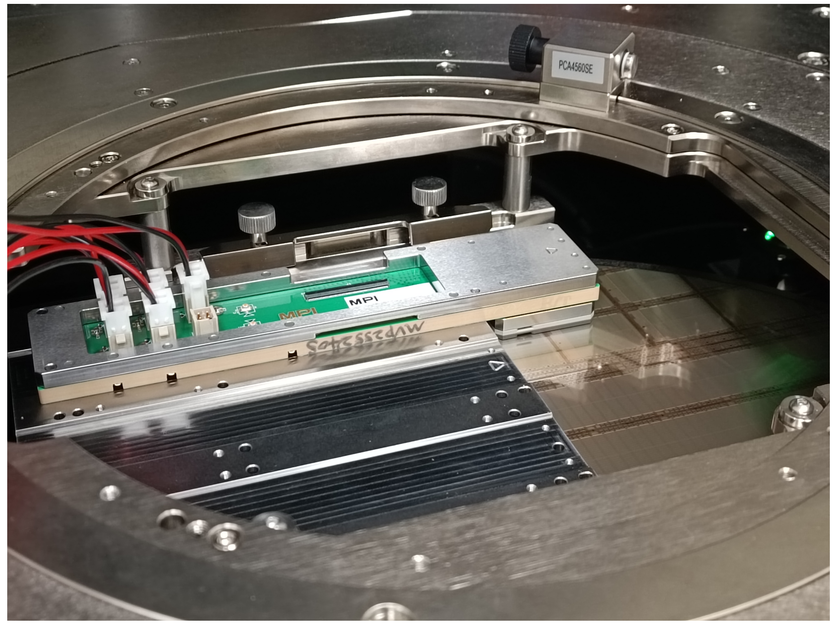
Technology	Test Time per Sensor	Handling Time (hours)	Sites	QC Time (hours/site)	QC Time (working days/site)
Cantilever	12 hours	100	3	22433	2804 (8h/day)
Vertical	1 hour	100	1	5700	712 (8h/day)
Vertical	1 hour	100	3	1900	237 (8h/day)
Vertical - Multipoint	1 hour	100	1	1966	245 (8h/day)
Vertical - Automatic	1 hour	8	1	5608	233 (24h/day)
Vertical - Multipoint/Automatic	1 hour	8	1	1874	78 (24h/day)

Approaching Production QC **relying only on Cantilever Probing looks prohibitive**,
Multi-site Vertical, Multi-point Vertical, Automatic Vertical would guarantee the fastest throughput

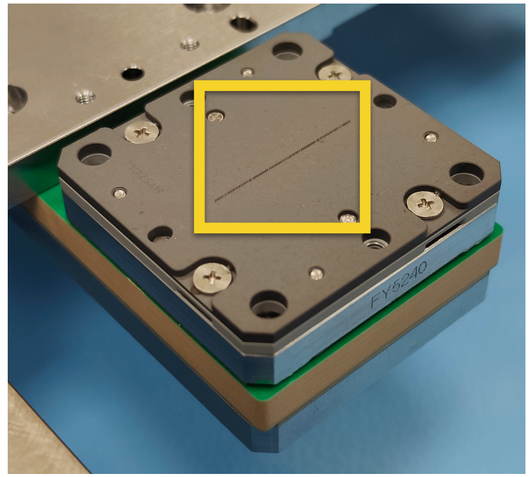
MOSAIX / LAS Modular Vertical Probe Card

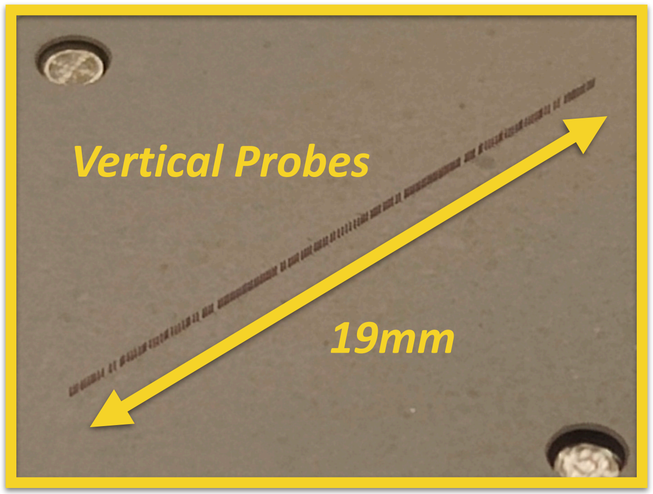
Custom Vertical Probe Card:
Concept by PixElφ Lab

- *Compact & Modular design*
- Custom plate allows
  installation of multiple Probe Cards
  for parallel testing on Wafer
- 18 Layers High Speed MLO
  34 Layers High Speed PCB (Megtron6)
  Compact & Modular design



Used for ITS3 MOSAIX large scale full characterization,
In this talk, focus on what is unique about this setup:
High Speed & Automatization capabilities





https://indico.cern.ch/event/1643631/contributions/7151920/
https://indico.cern.ch/event/1643631/contributions/7151927/
https://indico.cern.ch/event/1643631/contributions/7152045/

Simulations: HS channels S-parameters

System simulations include all interconnects:
Needles, Wirebonds, PCBs, Connectors, Cables

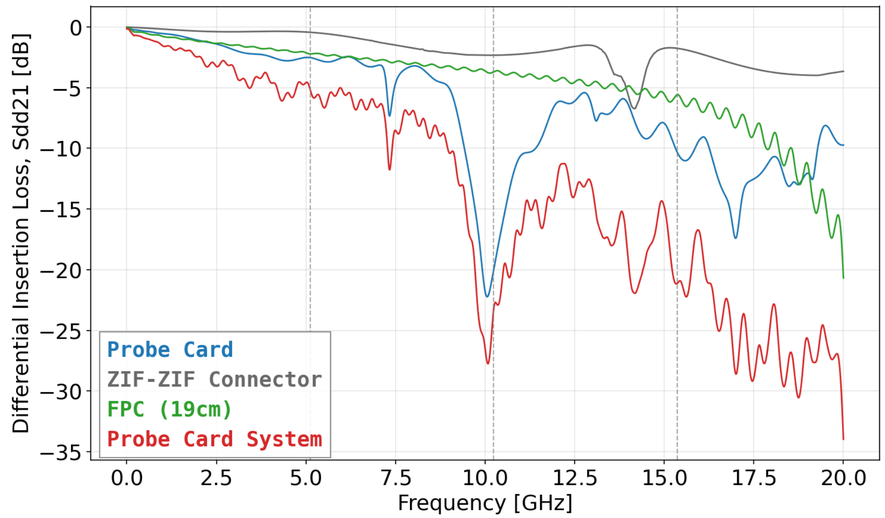
Methodology:

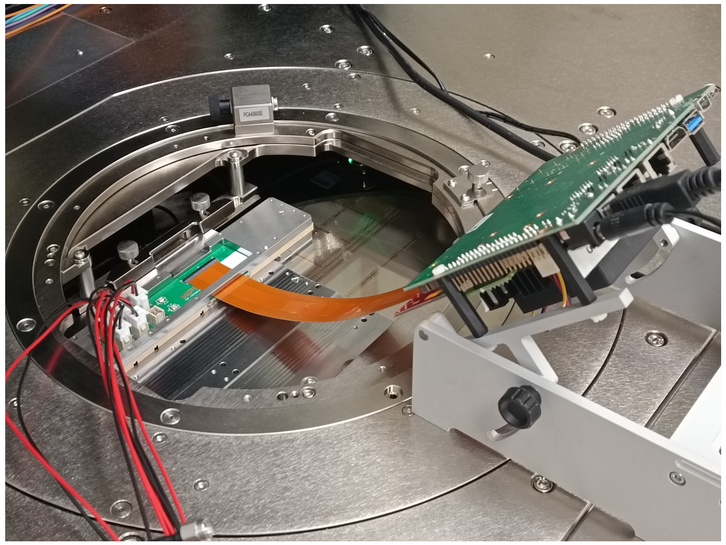
- Ansys HFSS simulation of PCBs, interconnects
- System S-parameters cascading multiple blocks

Carrier Card system as reference of established technology

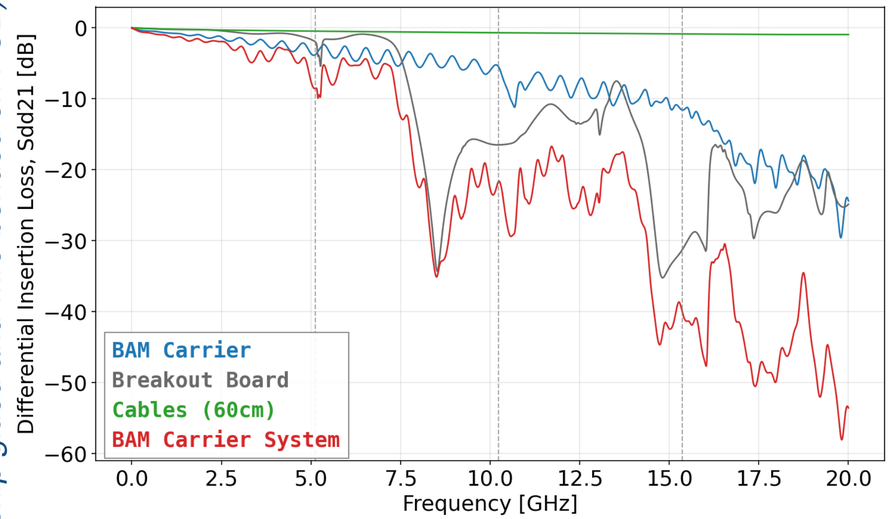
Simulation of individual blocks allows to identify bottlenecks for system optimization

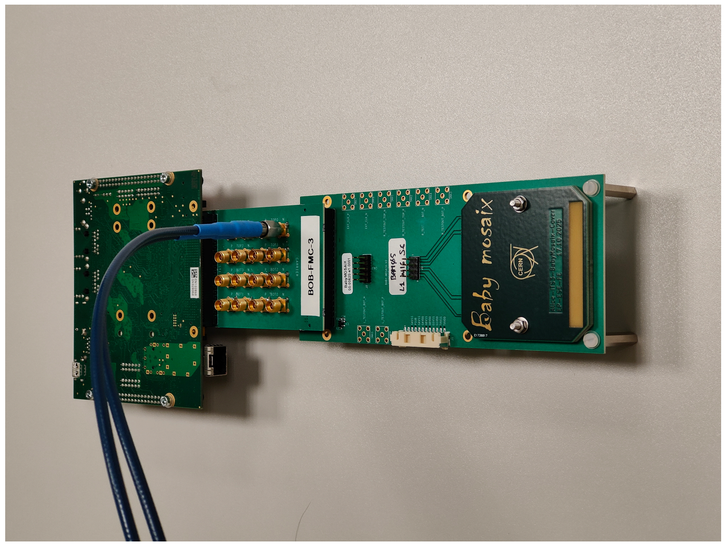
Vertical Probing System





babyMOSAIX Carrier System *(chip glued and wire-bonded on PCB)*



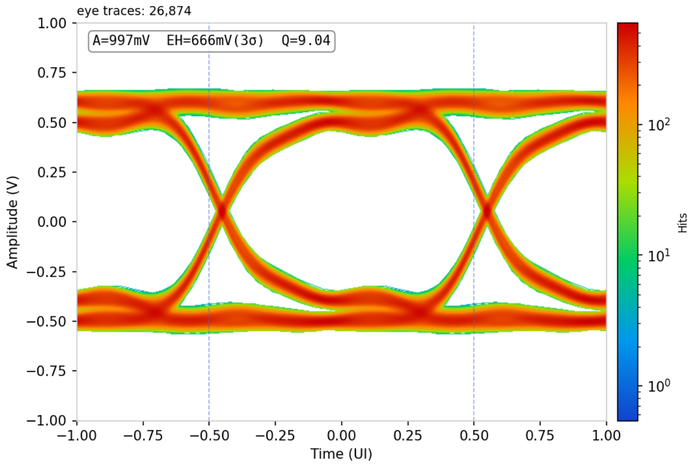


Simulations: Eye Diagrams

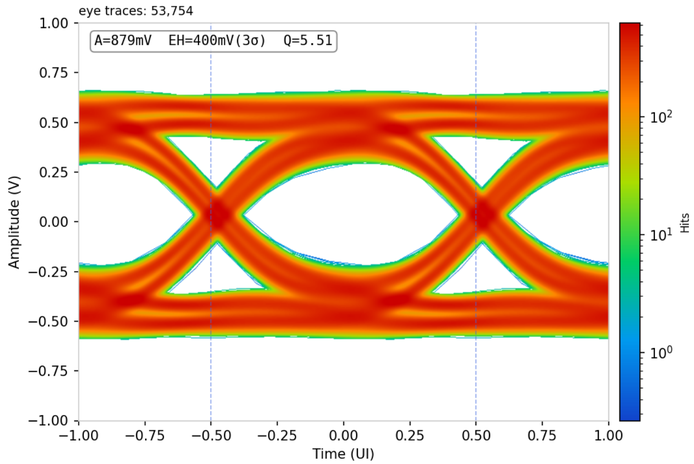
Missing from simulations:
Instrumentation induced jitter, real transmitter behavior (IBIS model)

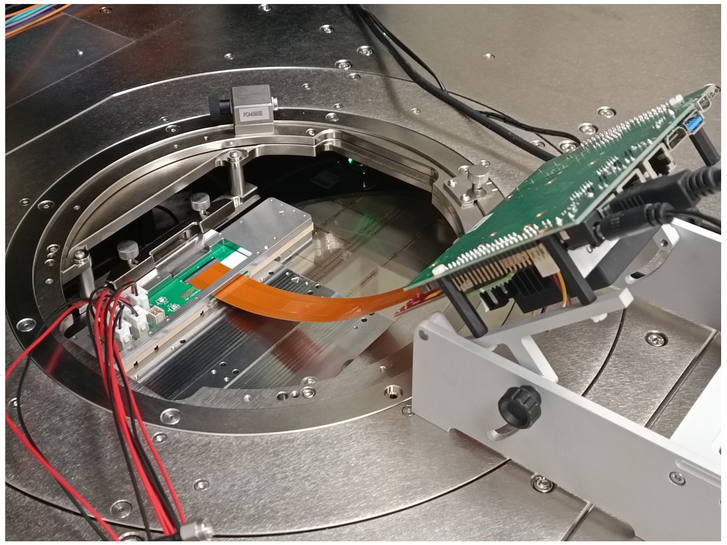
Vertical Probing System

5.12 Gbps

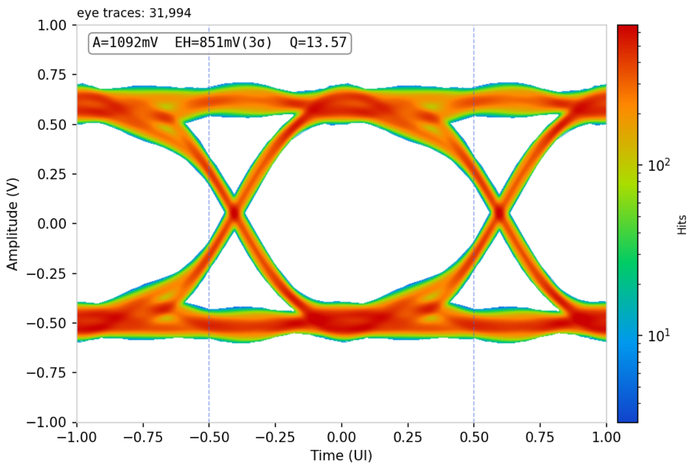


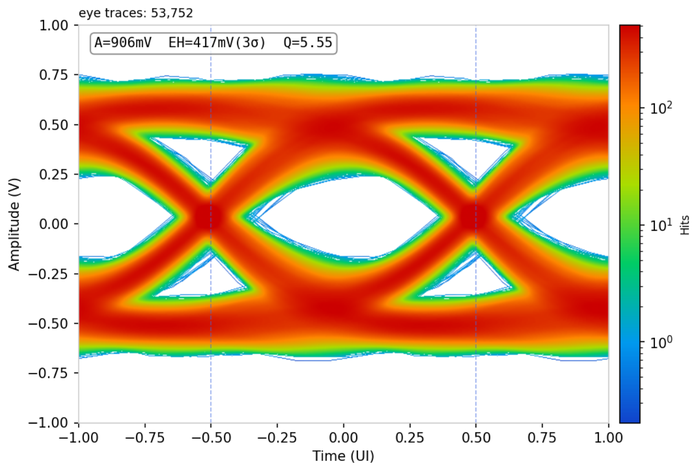
10.24 Gbps

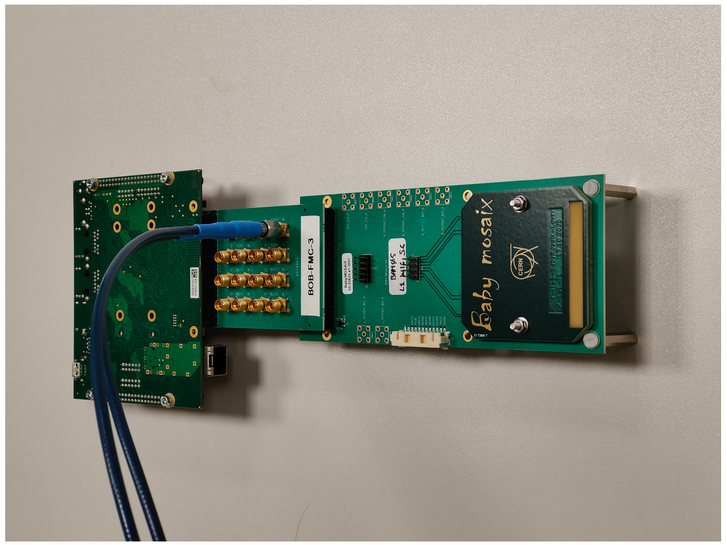




babyMOSAIX Carrier System







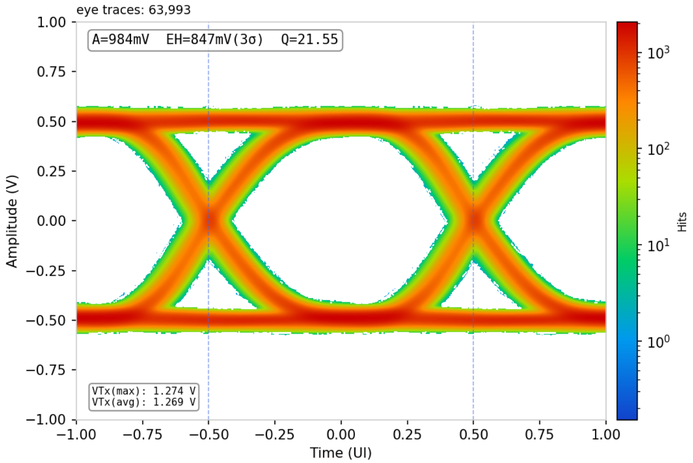
Eye Diagrams @ 5.12 Gbps

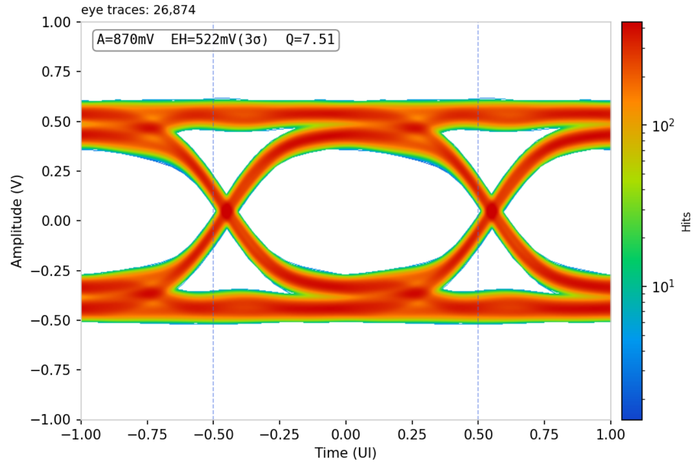
Vertical Probing System can perform closely to the Carrier Card System

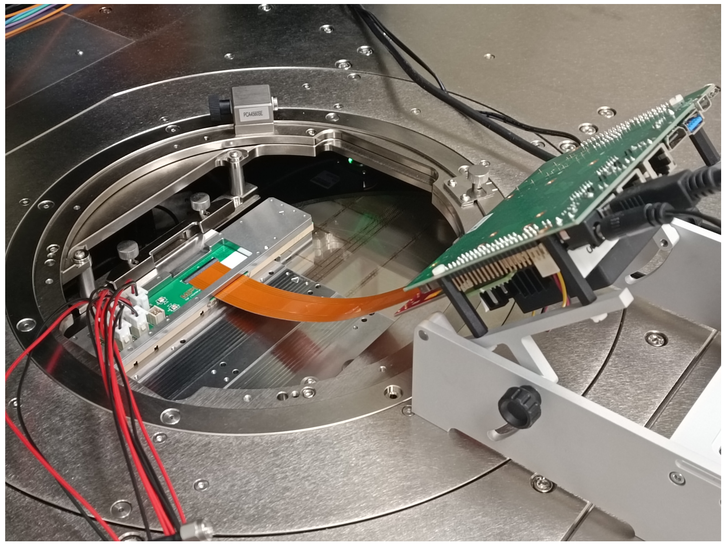
Measurements

Simulations

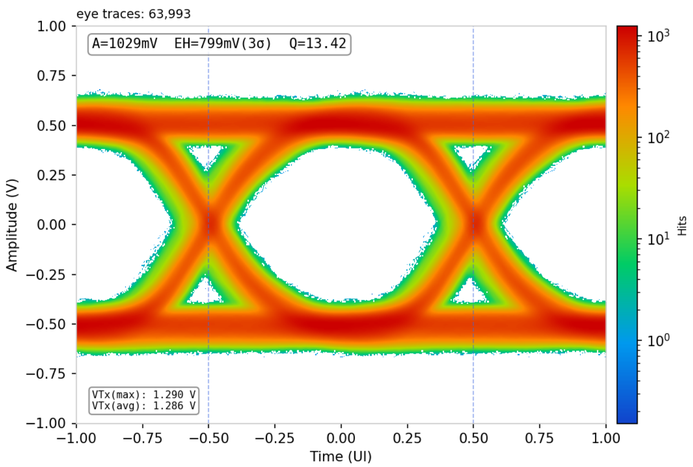
Vertical Probing System

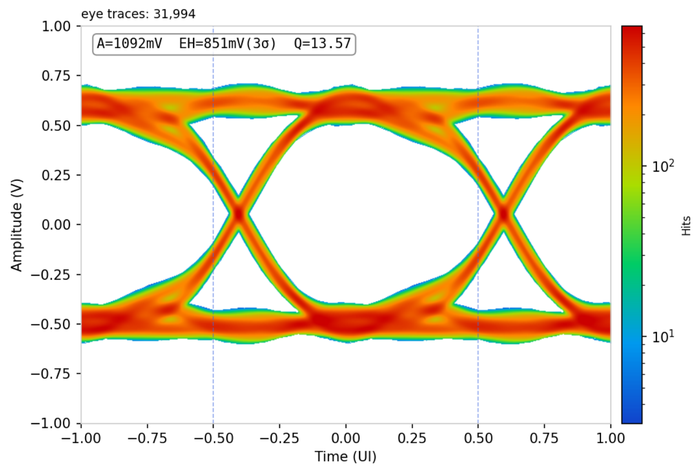


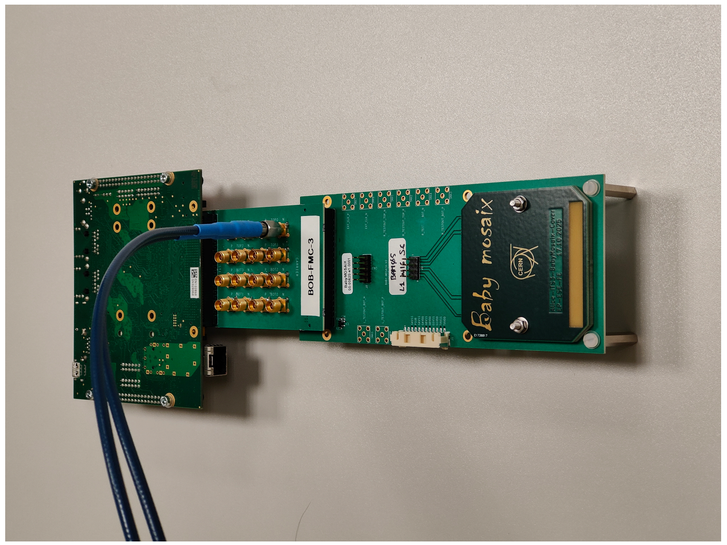




babyMOSAIX Carrier System







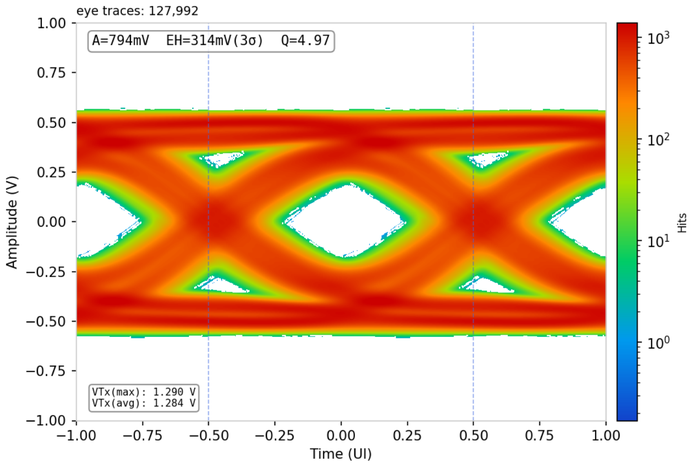
Eye Diagrams @ 10.24 Gbps

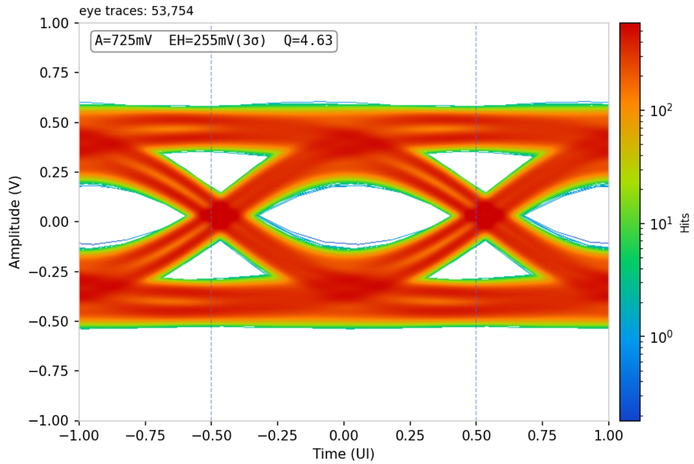
Vertical Probing System can perform closely to the Carrier Card System

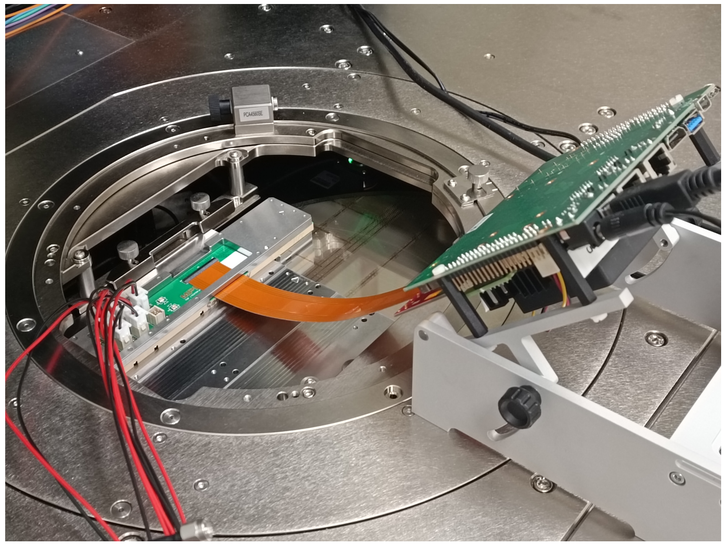
Measurements

Simulations

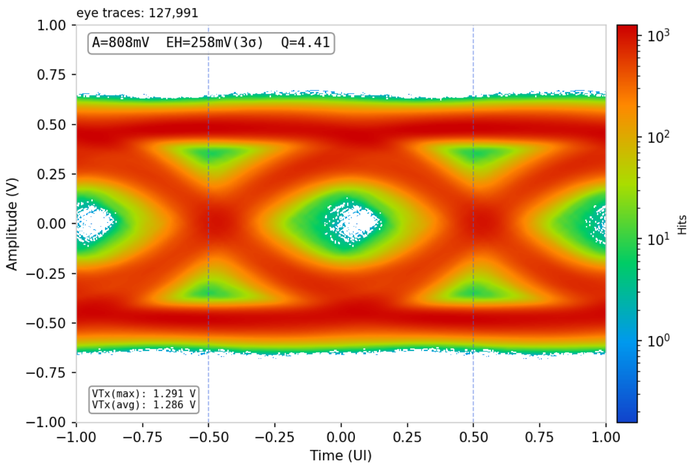
Vertical Probing System

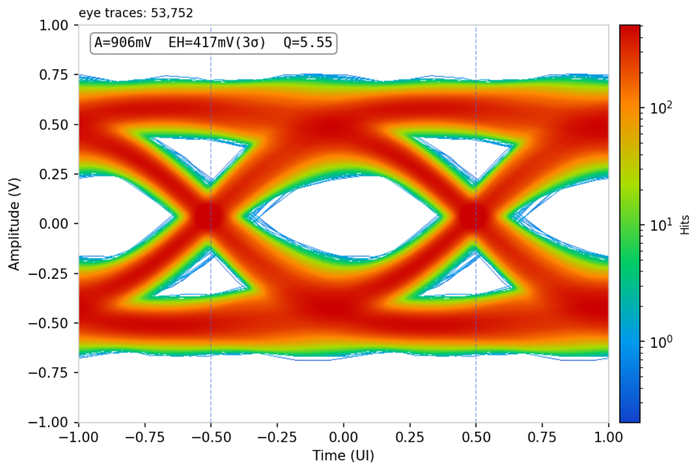


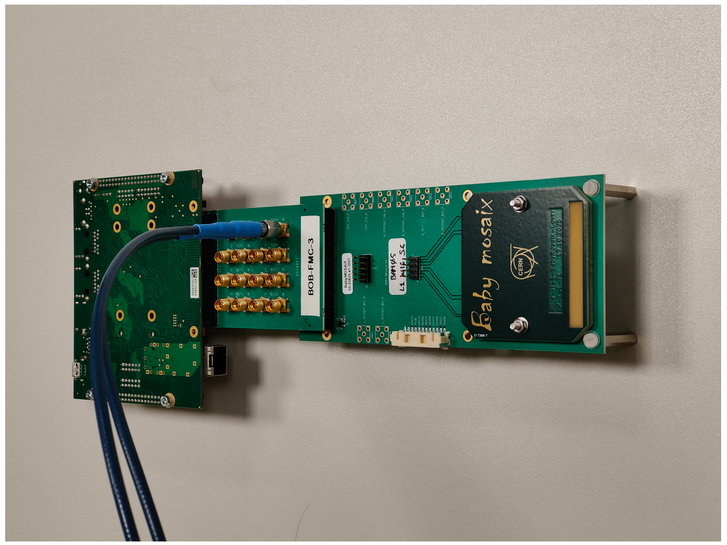




babyMOSAIX Carrier System





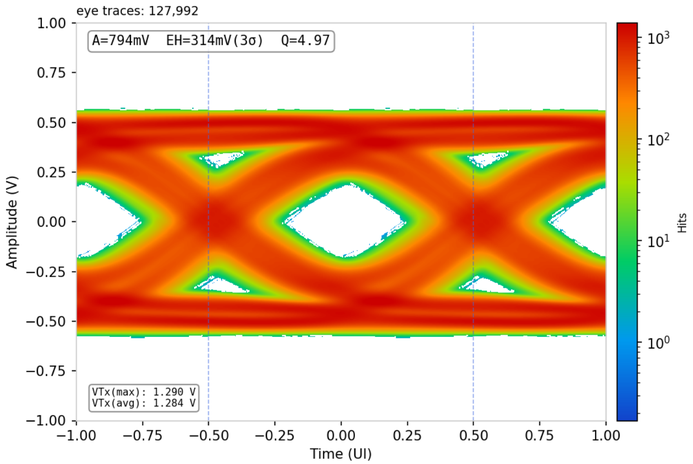


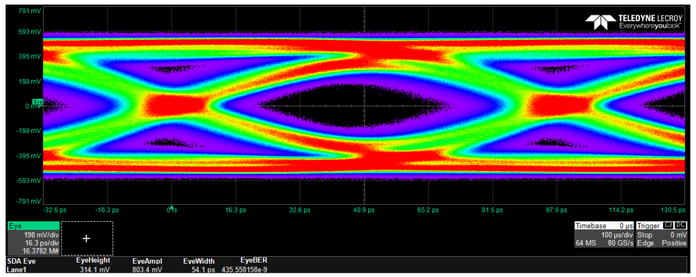
Measurements: Eye Diagrams

Measurements

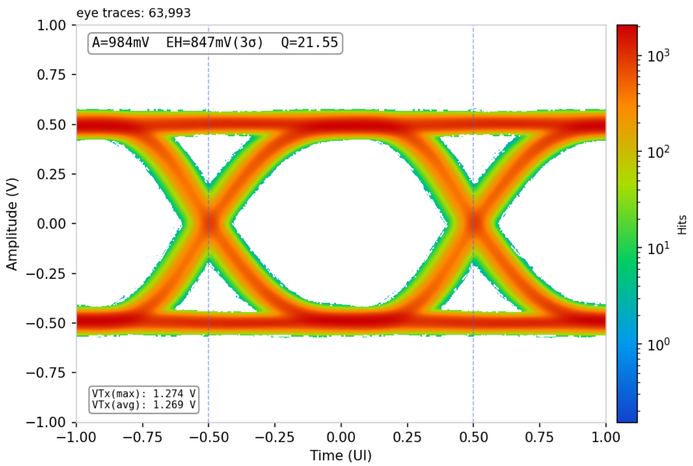
Post-Processing

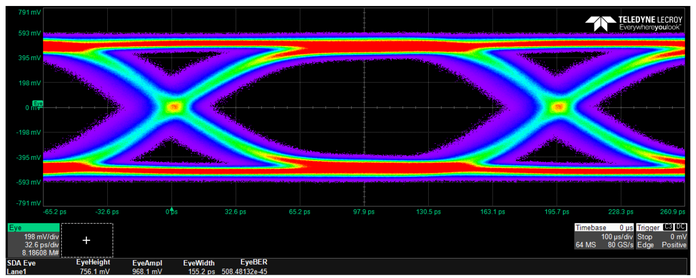
10 Gbps

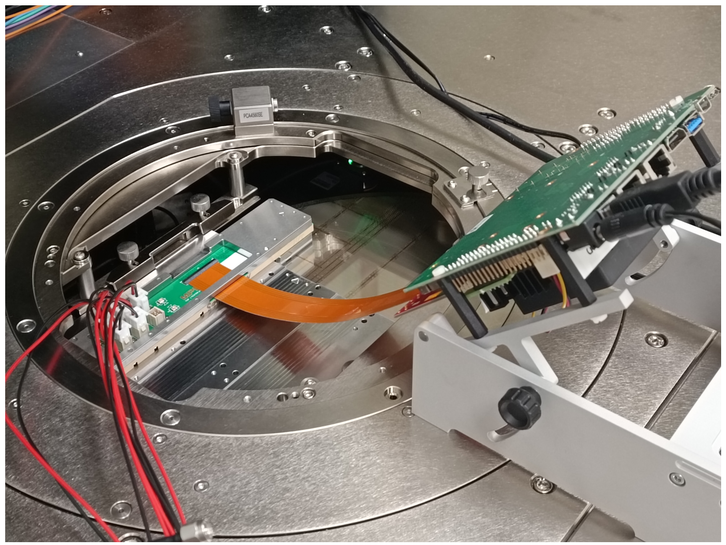




5 Gbps







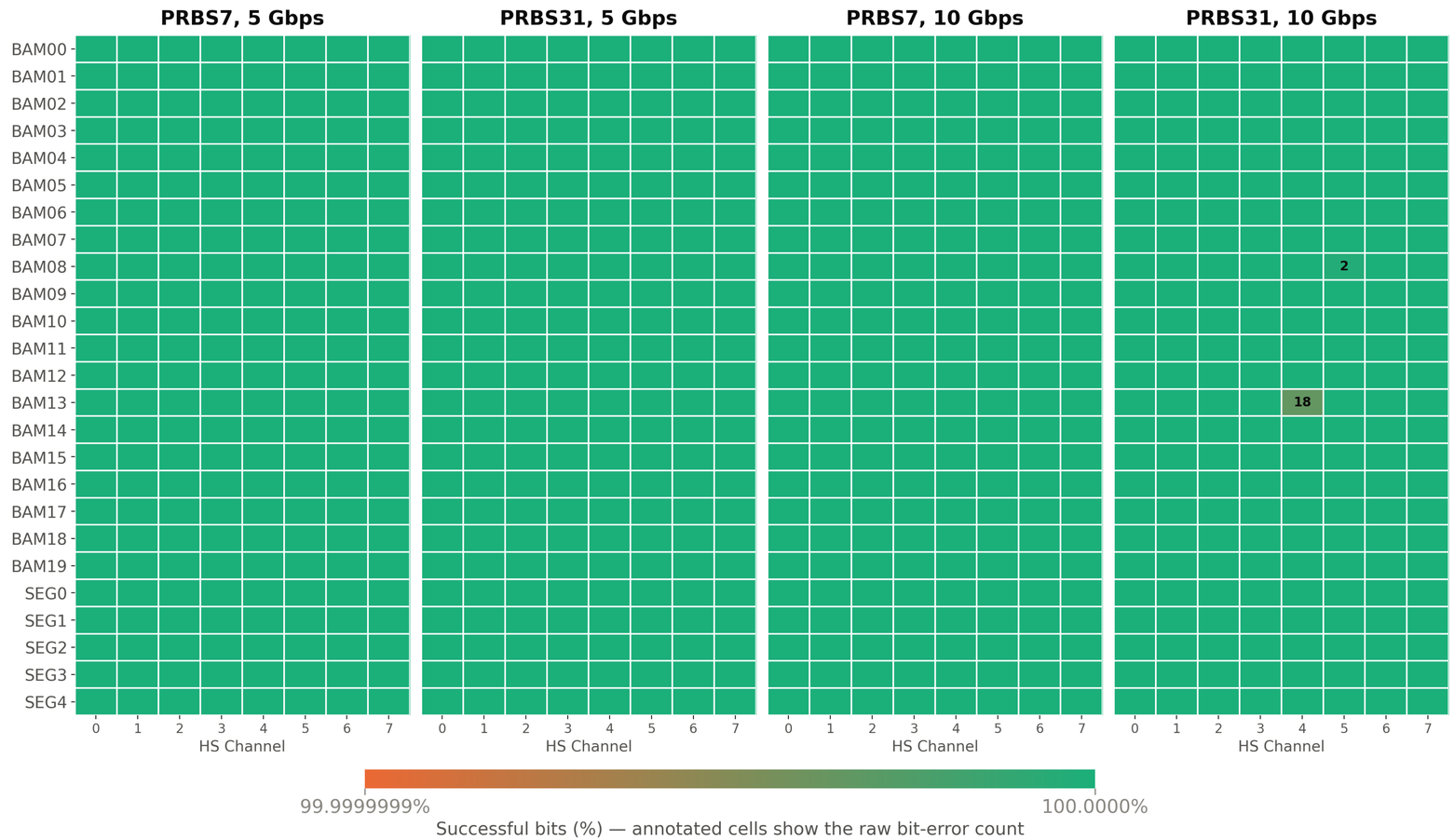
Gathering Statistics: Measuring BER

Using an FPGA receiver, it is also possible to **measure Bit Error Rate on Wafer Prober**, this allows to **study the serializer yield and behavior on the entire silicon production**

PRBS Example Test:

- PRBS @ 5.12, 10.24 Gbps
- Each chip has 8x HS Channels
- **Full Wafer test: 25 Chips**

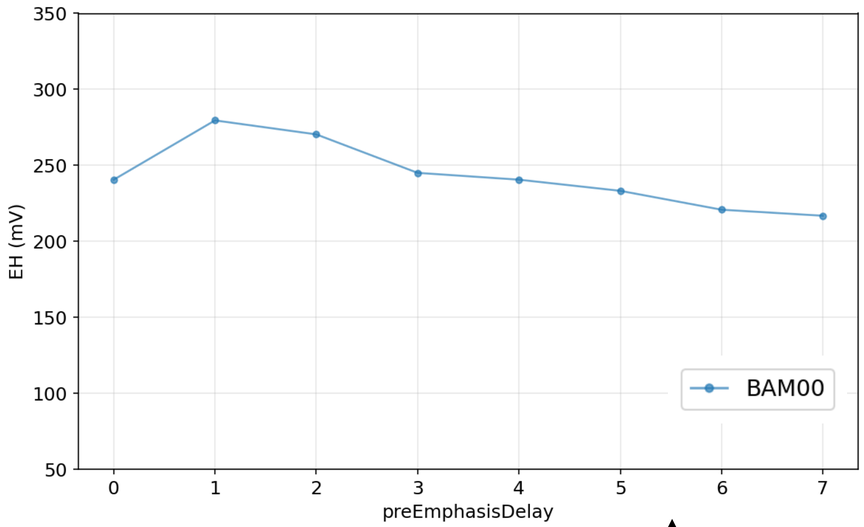
Fully automated system operating at 5 & 10 Gbps allows high speed channels yield test

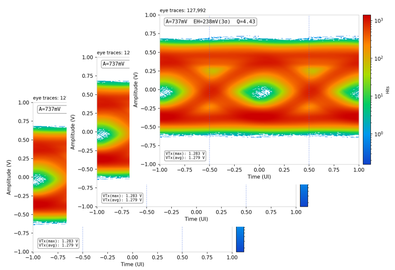


Eye Diagrams: Gathering Statistics

Analog **measurements of High speed links on automated Wafer Prober**
allows to **study & optimize on large samples the transceiver characteristics** *(supply voltage, preEmphasis strength and delay)*

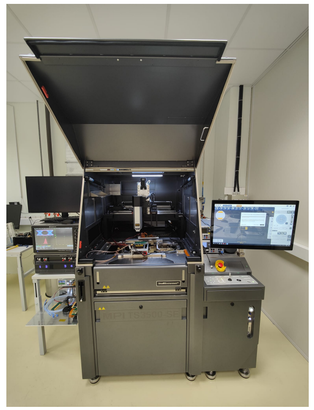
Individual Tx behavior



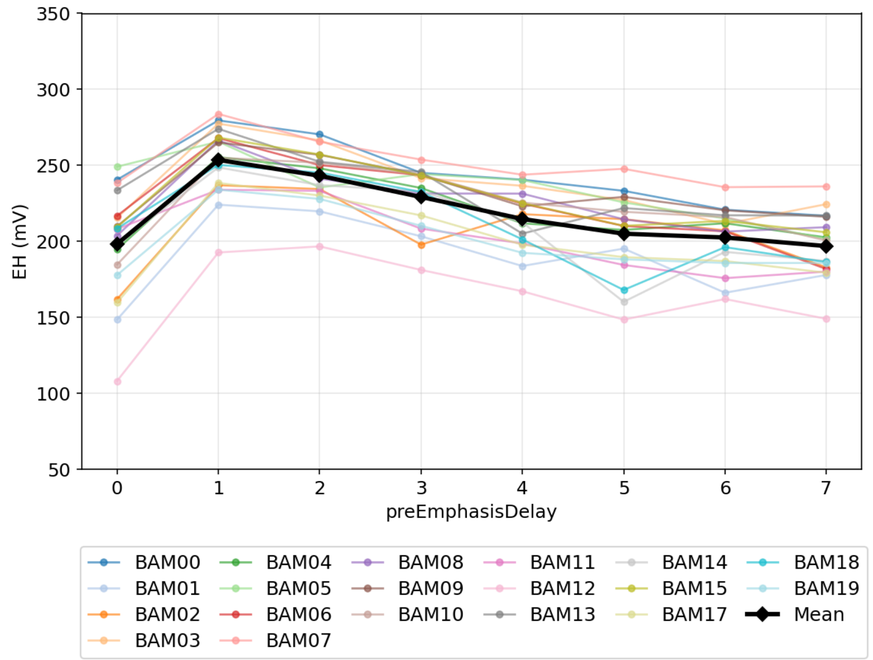


Eye parameters extraction for each Tx setting

Fully automated system allows seamless testing on entire silicon production



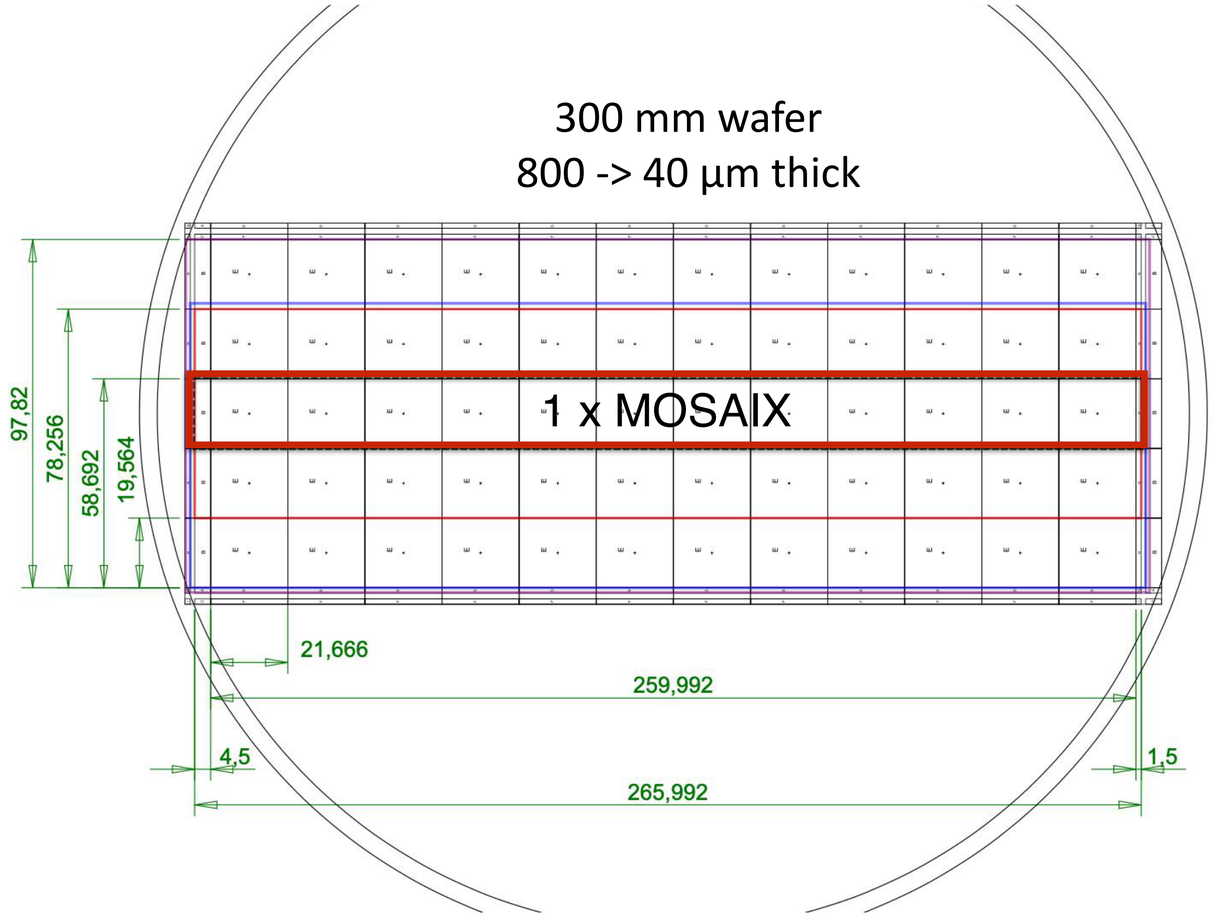
1x HS Channel Full Wafer Test: ~ 3h (only eye parameters scan)

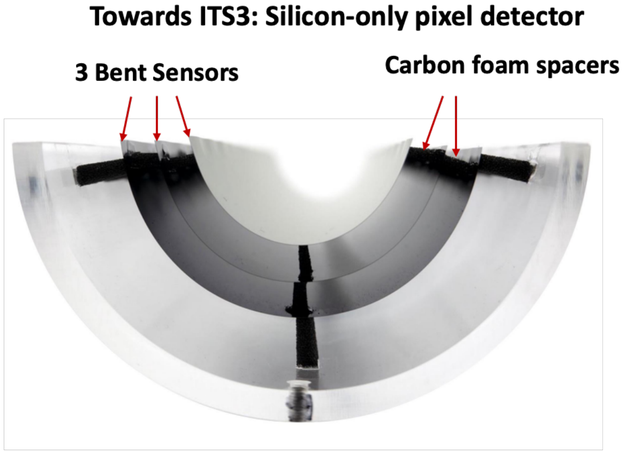


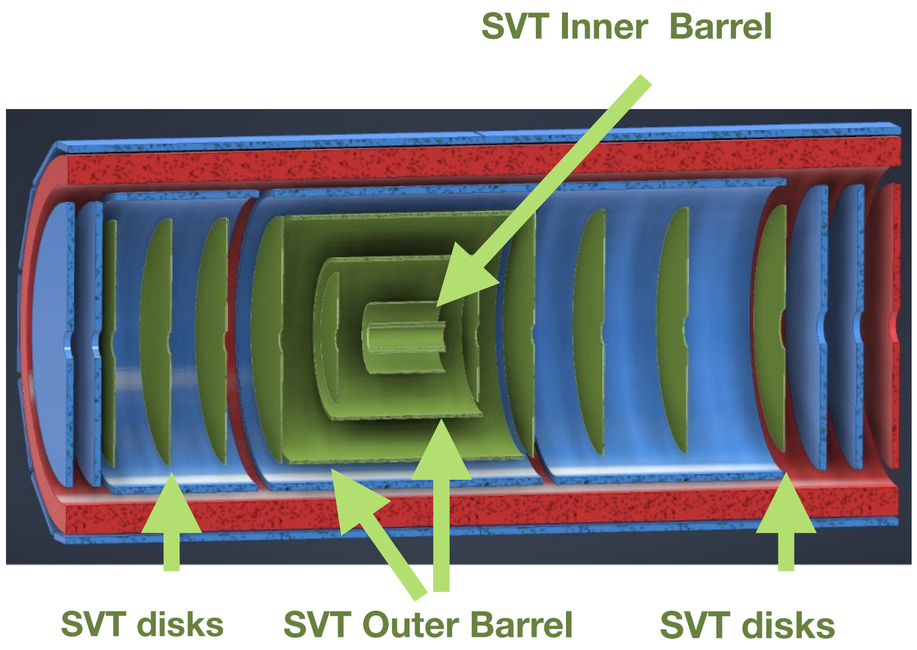
MOSAIX & LAS

- ALICE ITS3 and ePIC SVT Inner Barrel will share the same technology: **MOSAIX**

- SVT will derive from MOSAIX a sensor named **Large Area Sensor (LAS)** to be installed in the Outer Barrel and Disks





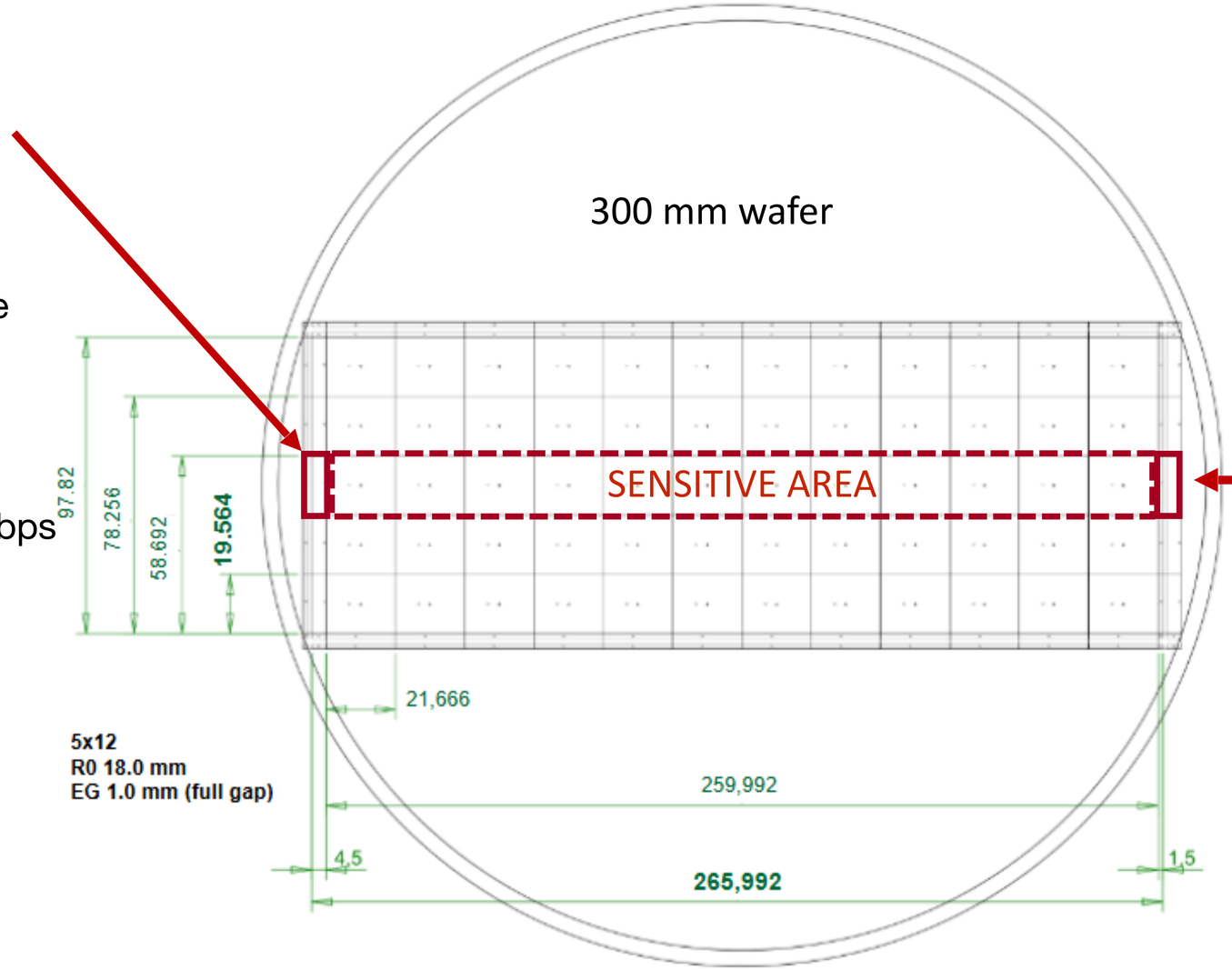


MOSAIX

Left Endcap (LEC)

The LEC hosts all the communication pads to the outside world plus different power domains and substrate biasing

- **152** pads in total:
  - Data Out: 8x 10.24 Gbps differential links
  - Slow Control: 2x 320Mbps differential links
  - Power domains
  - Substrate bias



Right Endcap (REC)

The REC hosts mainly pads dedicated to powering

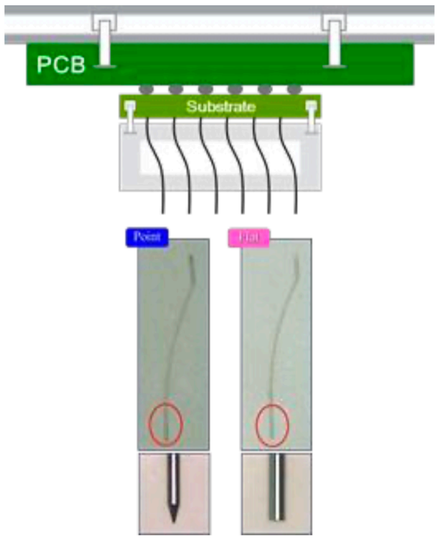
- **161** pads in total:
  - 2x test differential pairs
  - Power domains
  - Substrate bias

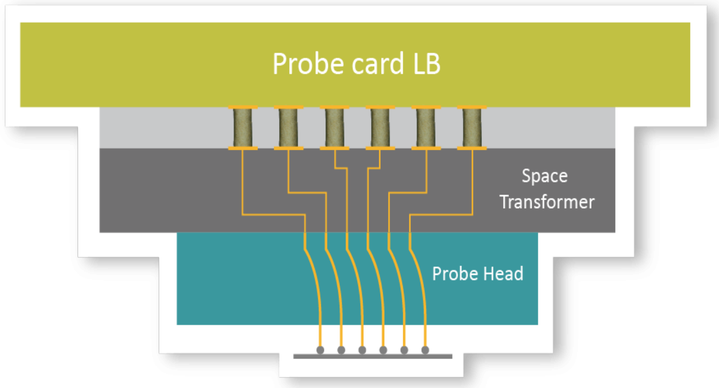
Wafer Probing – Vertical Probe Cards

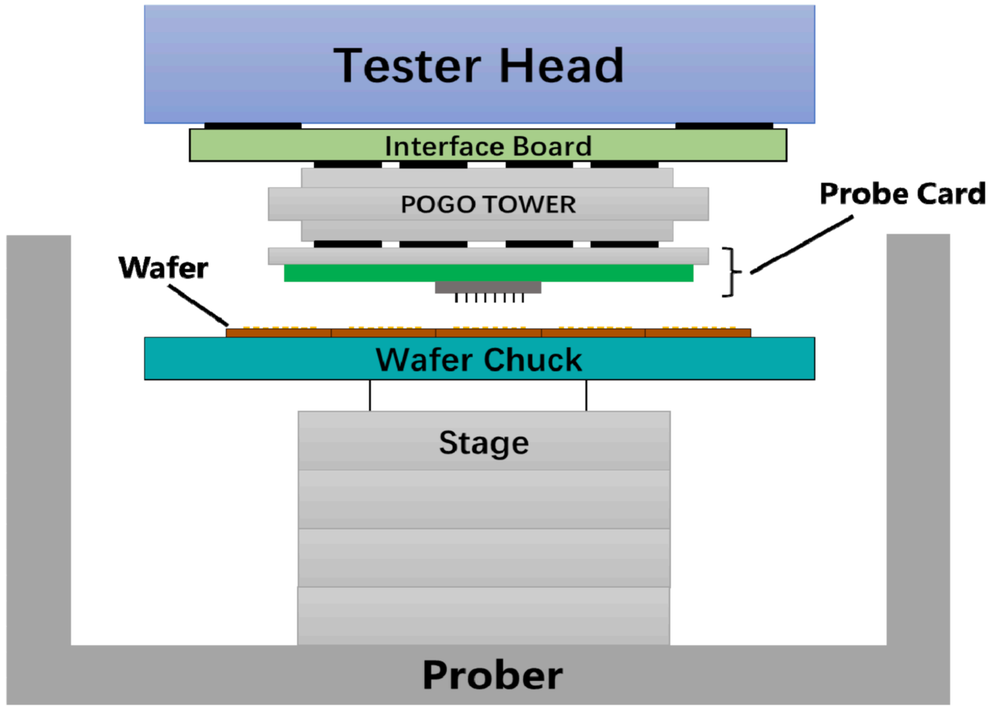
MOSAIX Left Endcap: 152 pads (up to 94x91 µm), 100 µm pitch

Cutting Edge Vertical Probe card approach:

- **Dense interconnects**
- **High speed operation in the multi-Gbps range**
- High power applications







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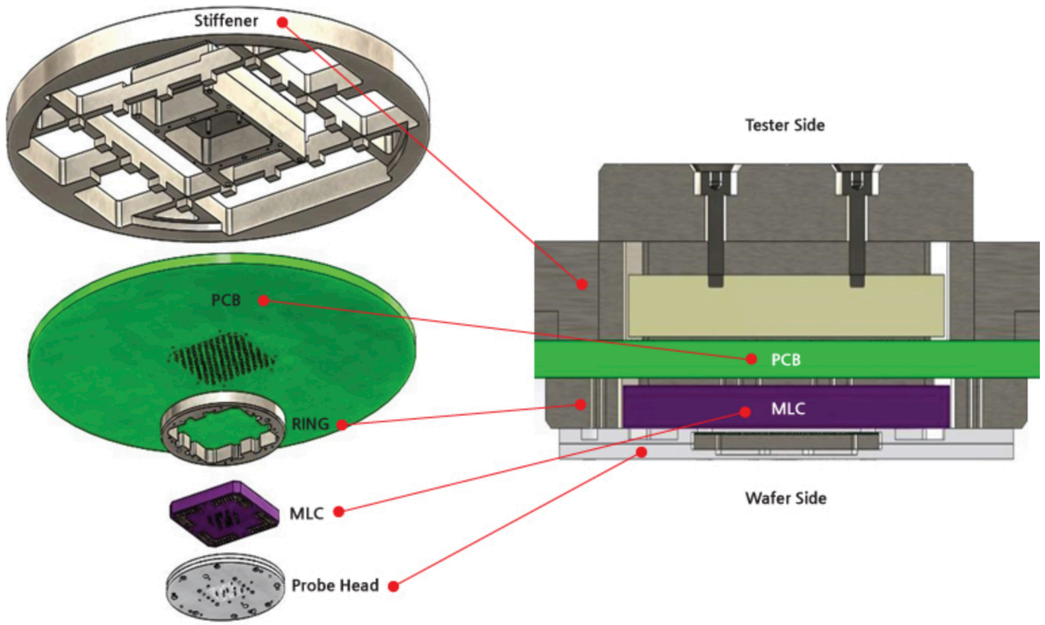
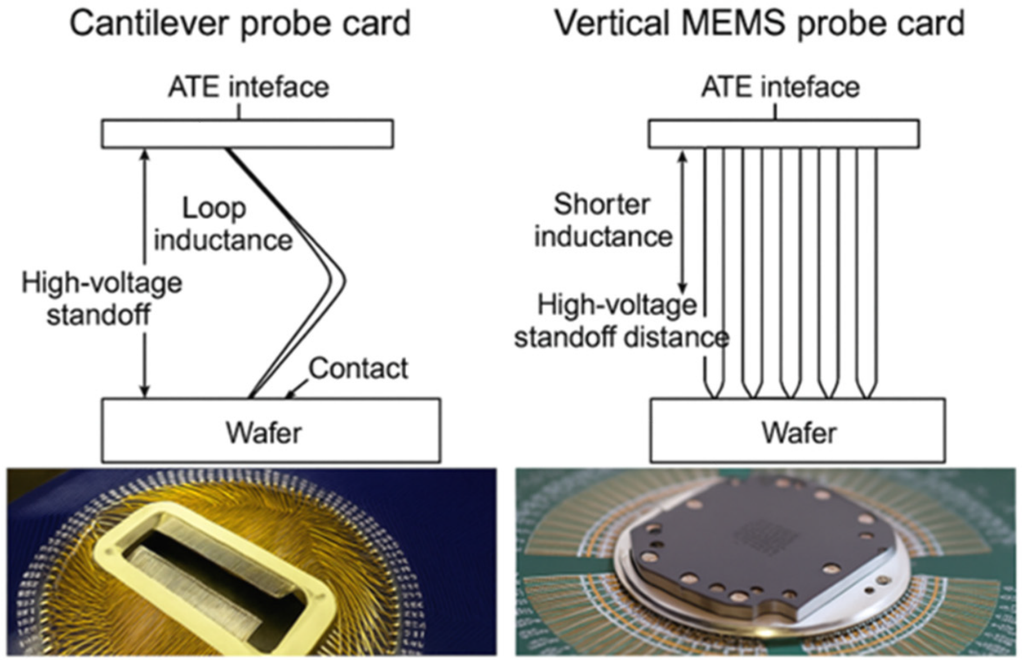


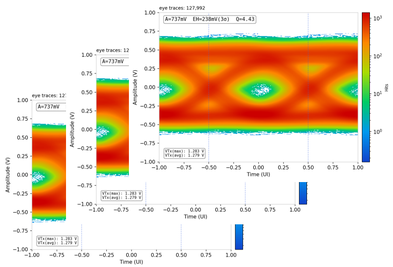


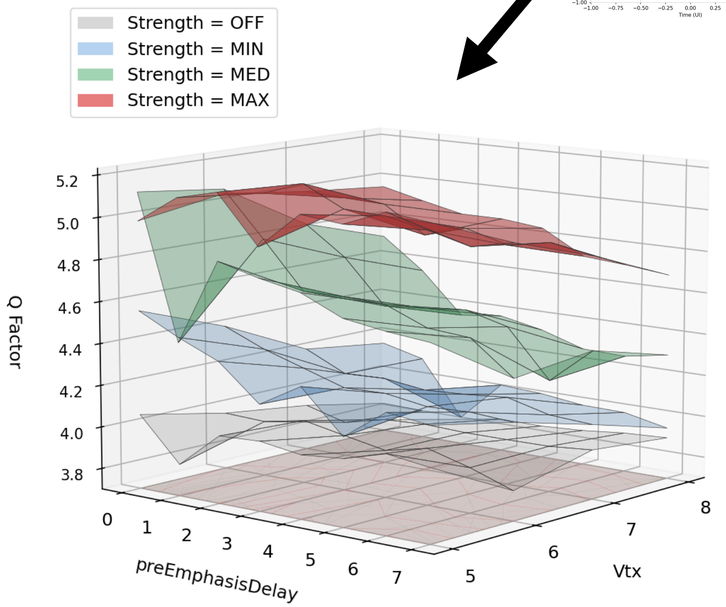
https://doi.org/10.3390/chips5030018

Eye Diagrams: Gathering Statistics

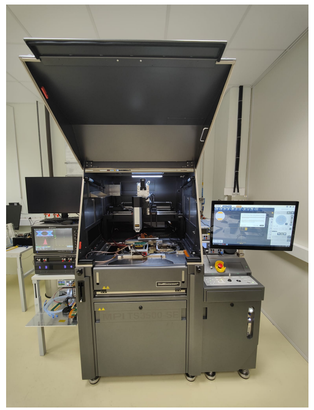
Analog **measurements of High speed links on automated Wafer Prober**
allows to **study & optimize on large samples the transceiver characteristics** *(supply voltage, preEmphasis strength and delay)*

Eye parameters extraction for each Tx setting



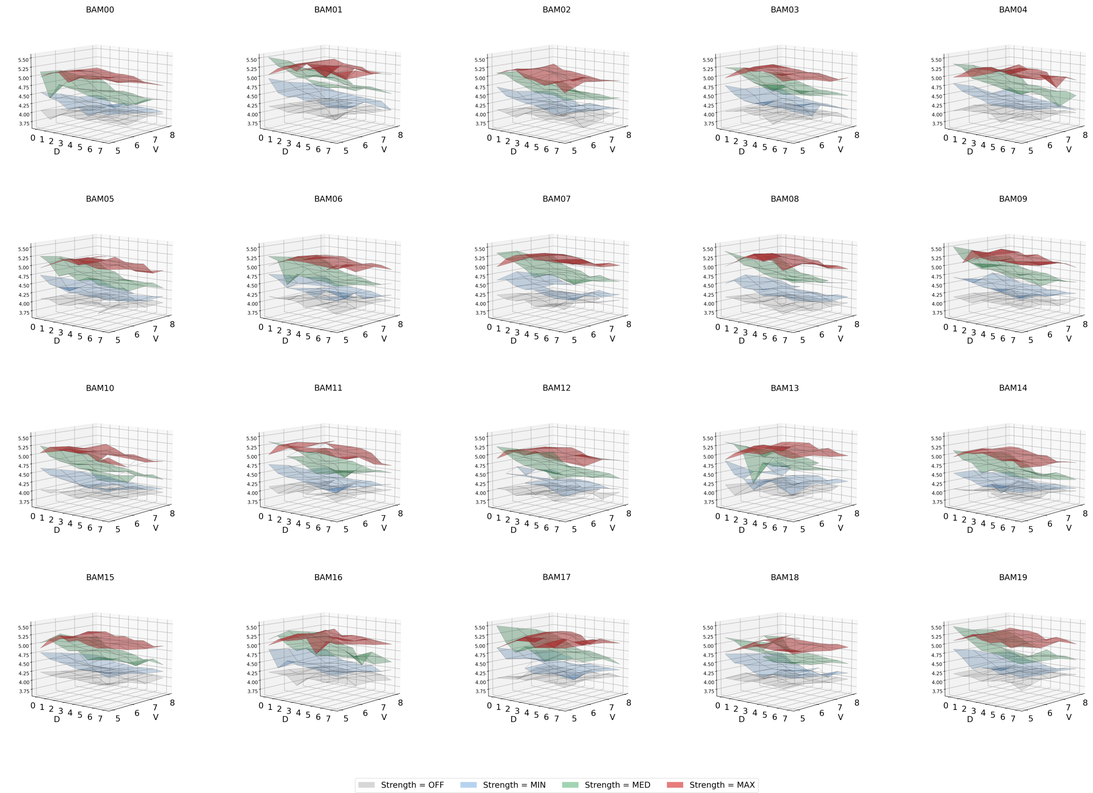


Individual Tx behavior



Fully automated system allows seamless testing on entire silicon production

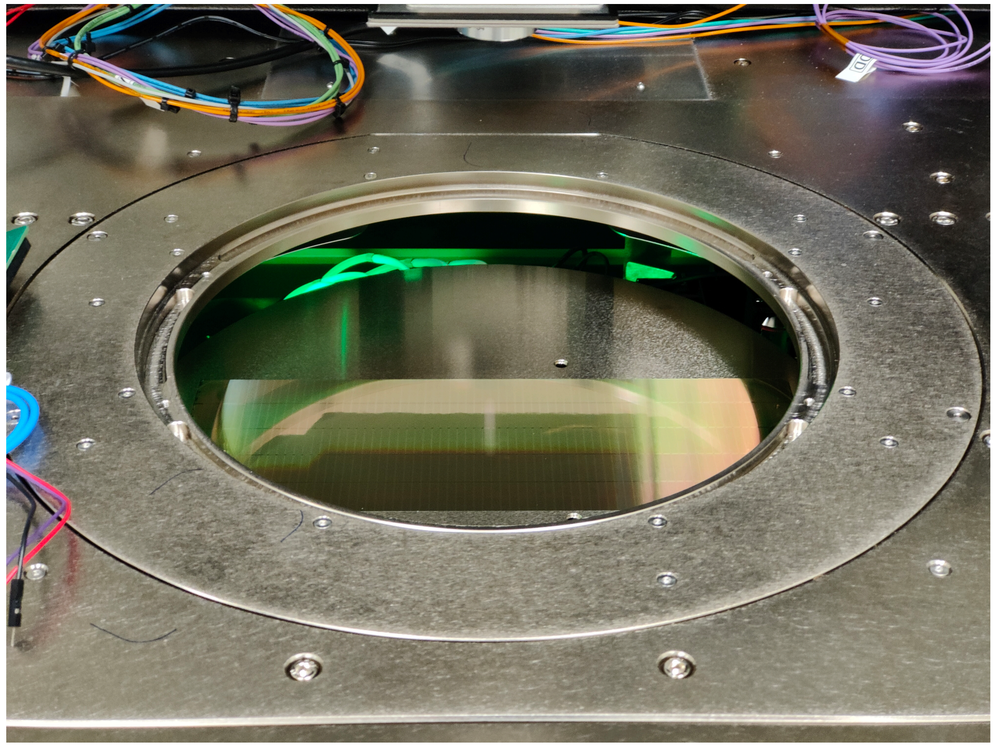
1x HS Channel Full Wafer Test: ~ 3h
(only eye parameters scan)

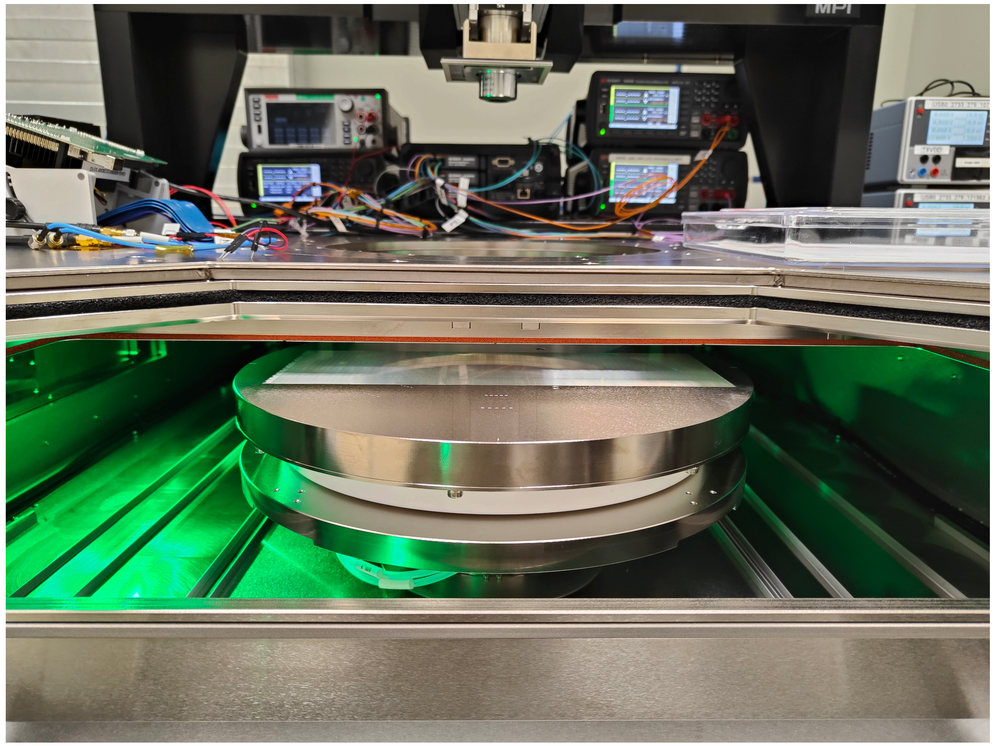


MIT Wafer Prober at CERN

Custom Wafer Prober Upgrades:
Concept by PixElφ Lab targeting HEP specific applications

- Micro-holes (200 µm) chuck for **thin (50µm) wafers handling**

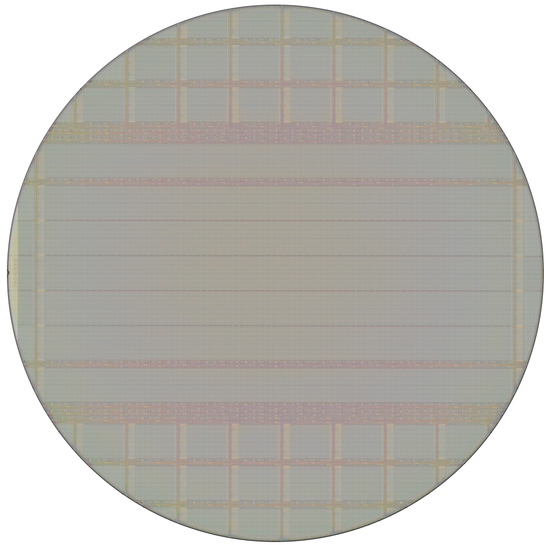


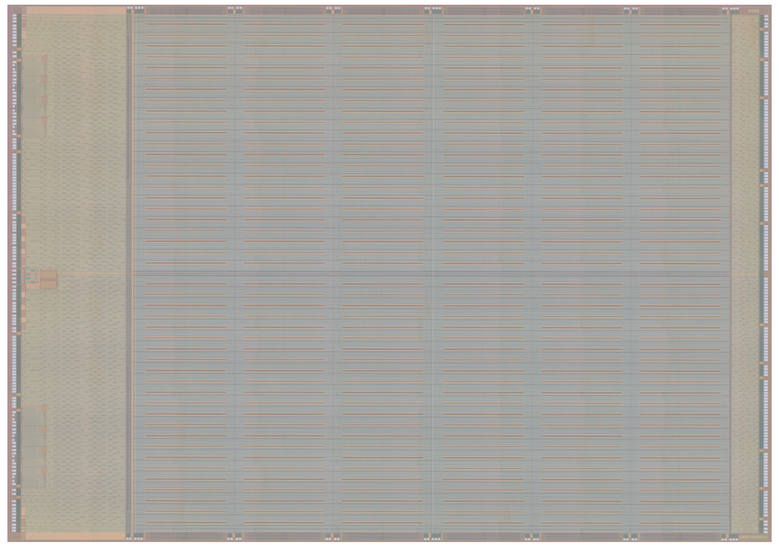


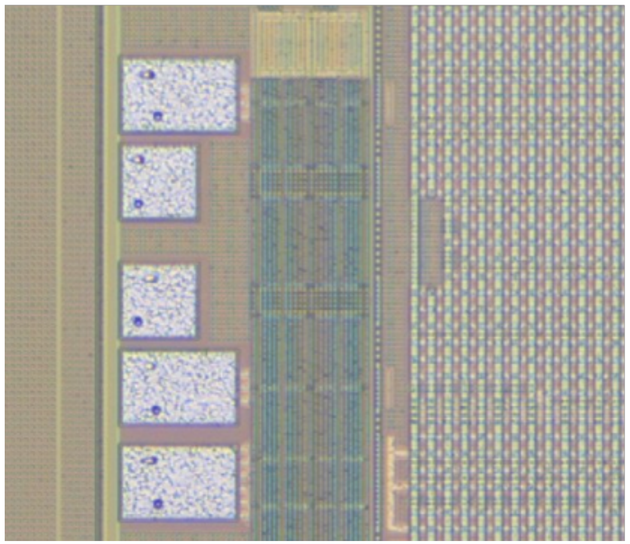
MIT Wafer Prober at CERN

Custom Wafer Prober Upgrades:
Concept by PixElφ Lab targeting HEP specific applications

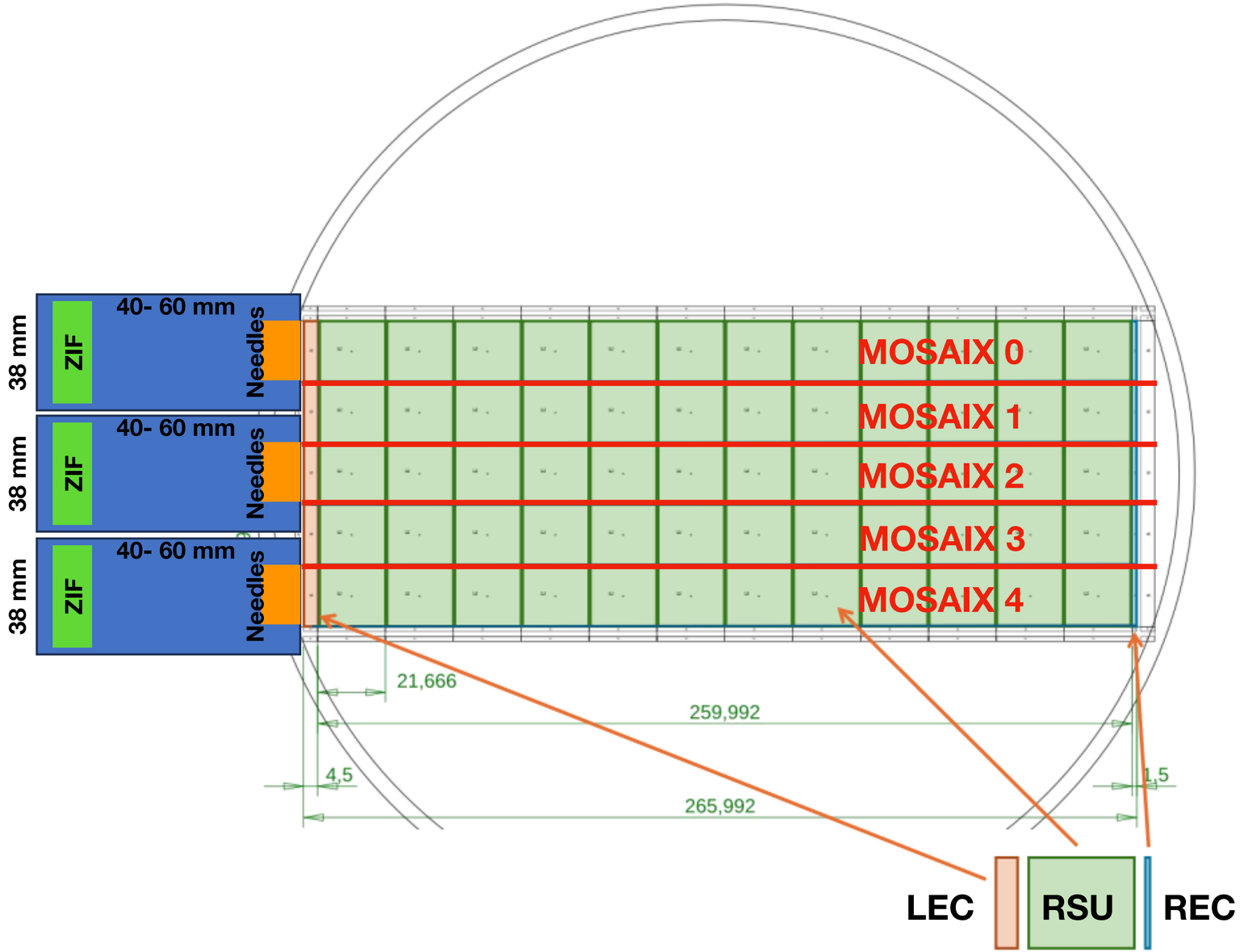
- Wafer Prober cameras and movement programmed to:
  acquire and stitch arrays of images to reconstruct **pads or full wafer high resolution images**



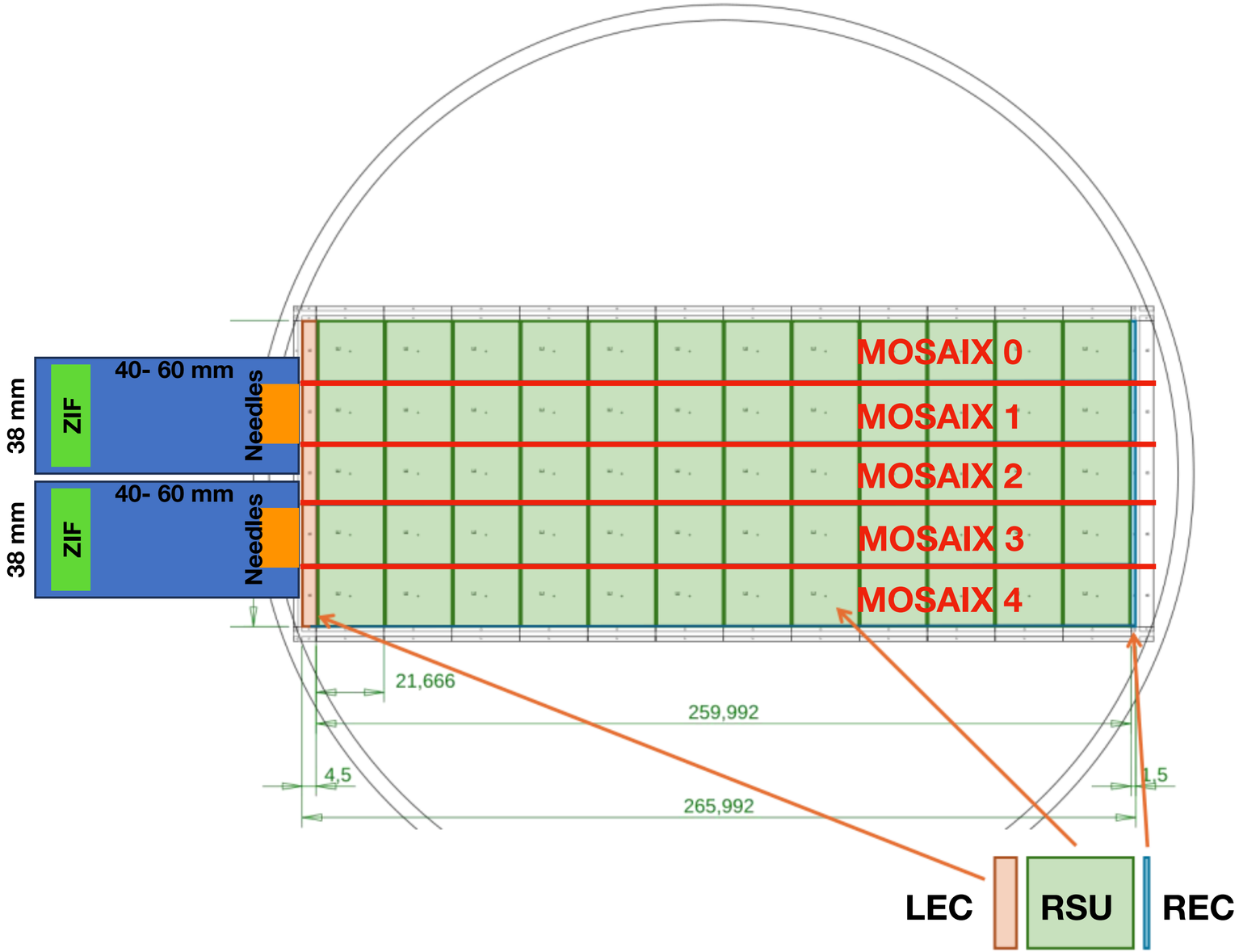
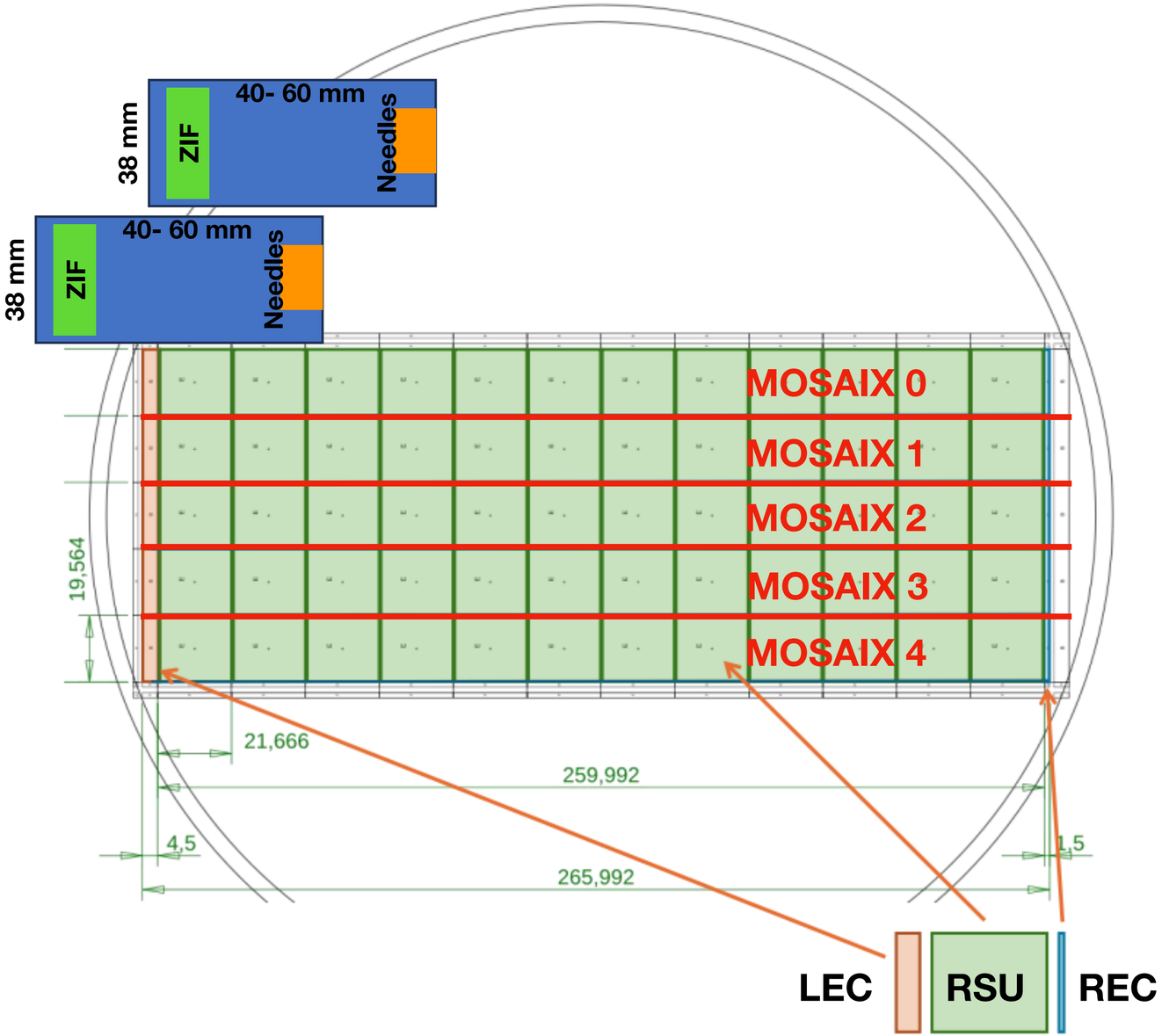




MOSAIX (LEGO) Probe Card



MOSAIX (LEGO) Probe Card



MOSAIX (LEGO) Probe Card