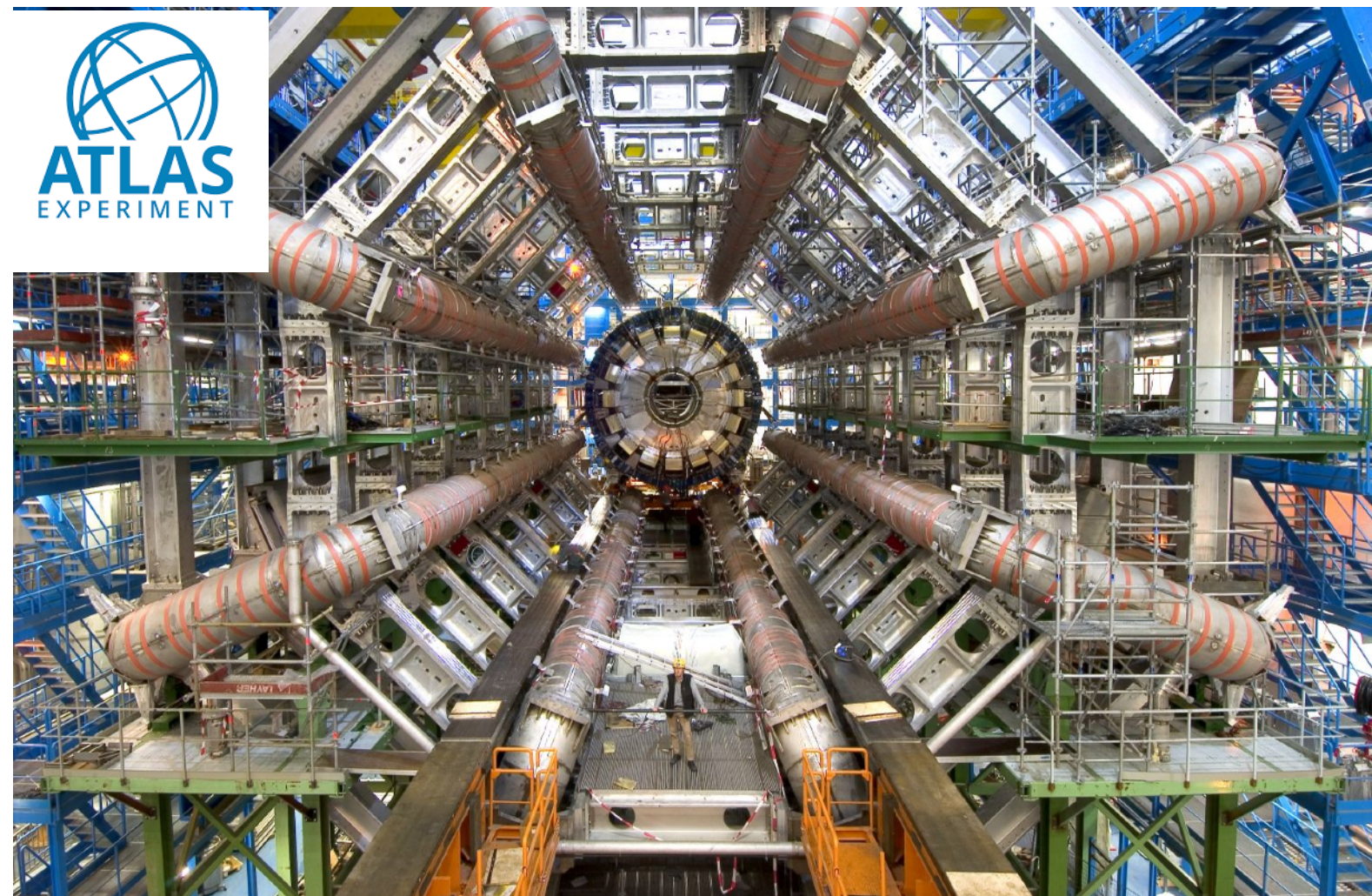


Sensor QA thoughts

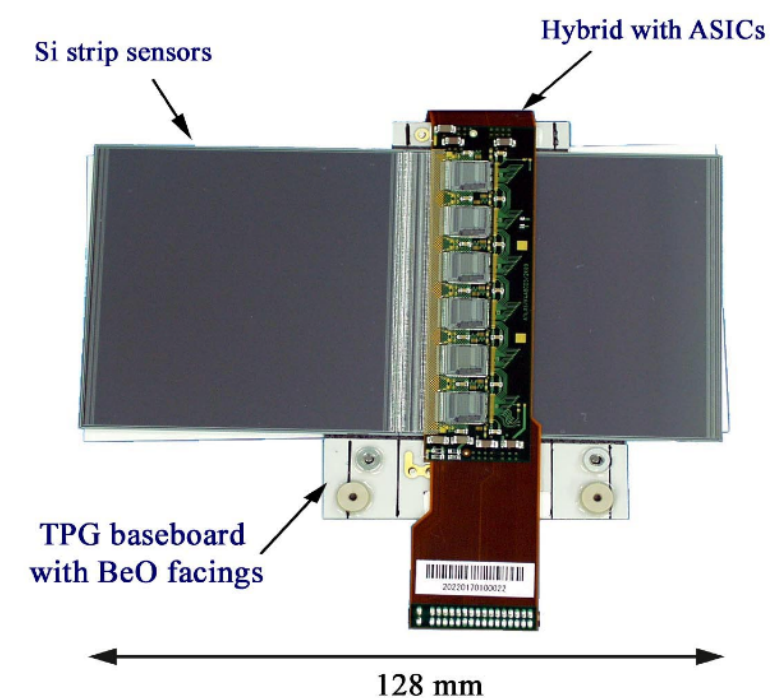
Tomohiro Inada and Hidetoshi Otono
(Kyushu University)

tomohiro.inada@cern.ch

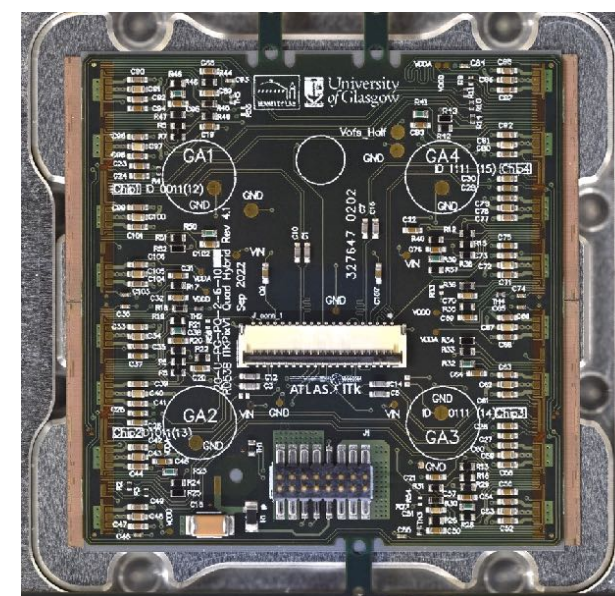
Recap: Silicon detector experience



- Strip-based tracker (Operation)
- ITk (Inner Tracker) Detector (Production)



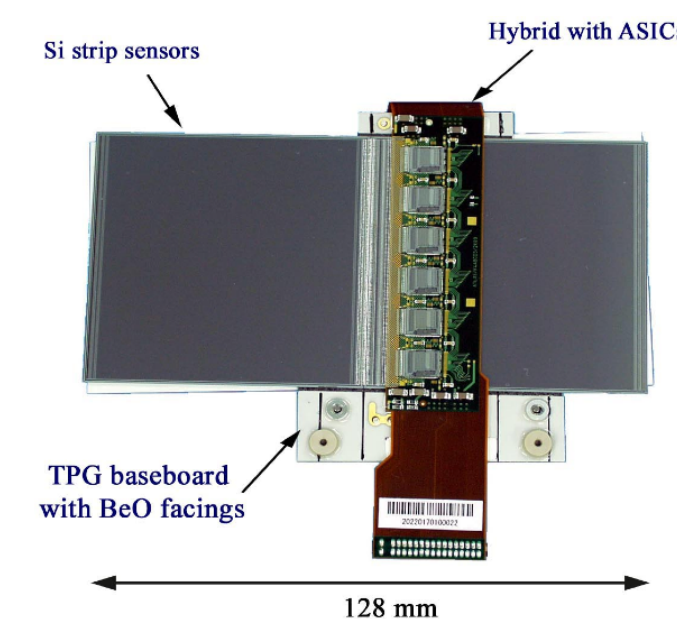
Silicon strip



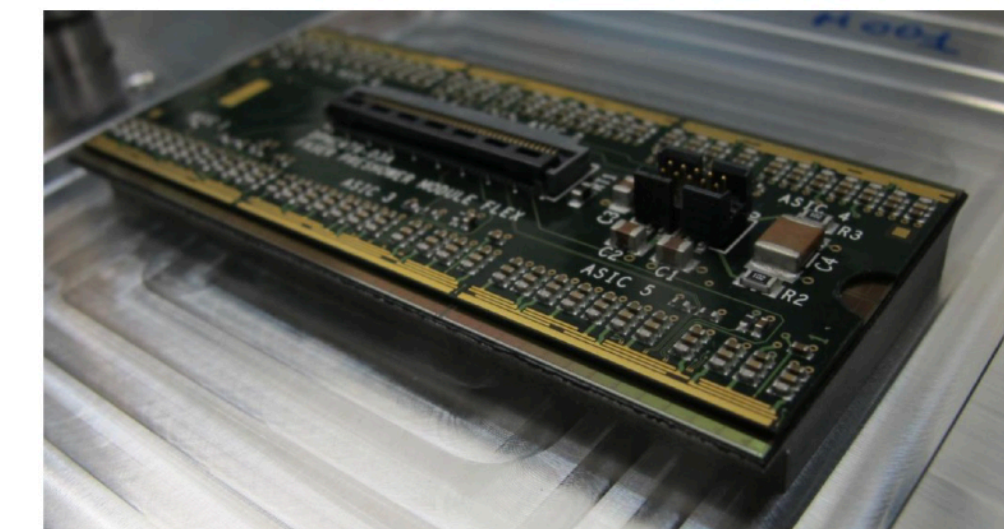
ITk pixel quad-module



- Strip-based tracker (Assembly/Operation)
- MAPS-based Pixel preshower detector (Production/Assembly/Operation)



Silicon strip



MAPS Pixel detector

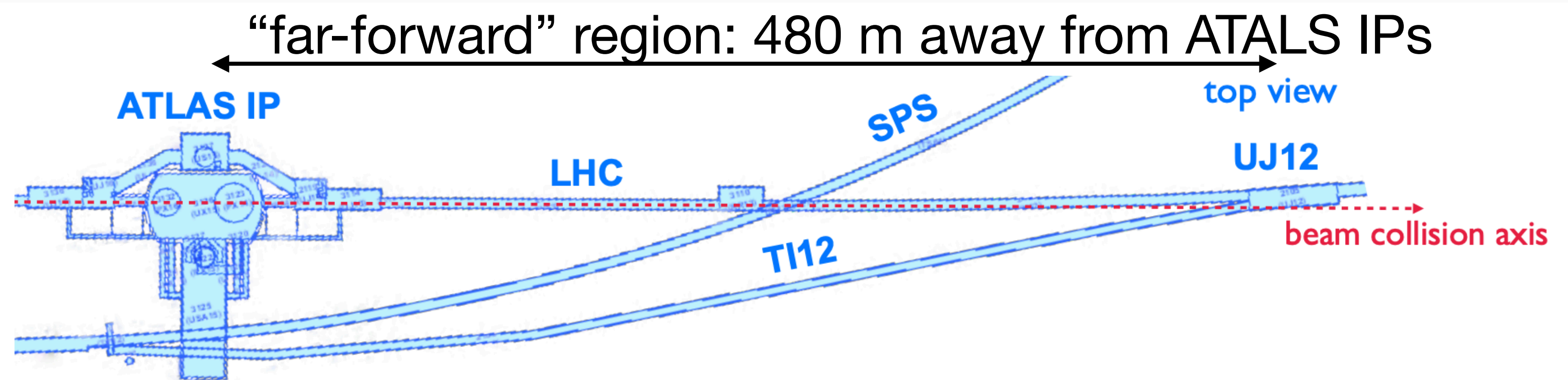
In this talk, we would like to review the recent QA experience with FASER and ATLAS

ForwArd Search Experiment (FASER)

Operation since July 2022

LHC beamline

2018

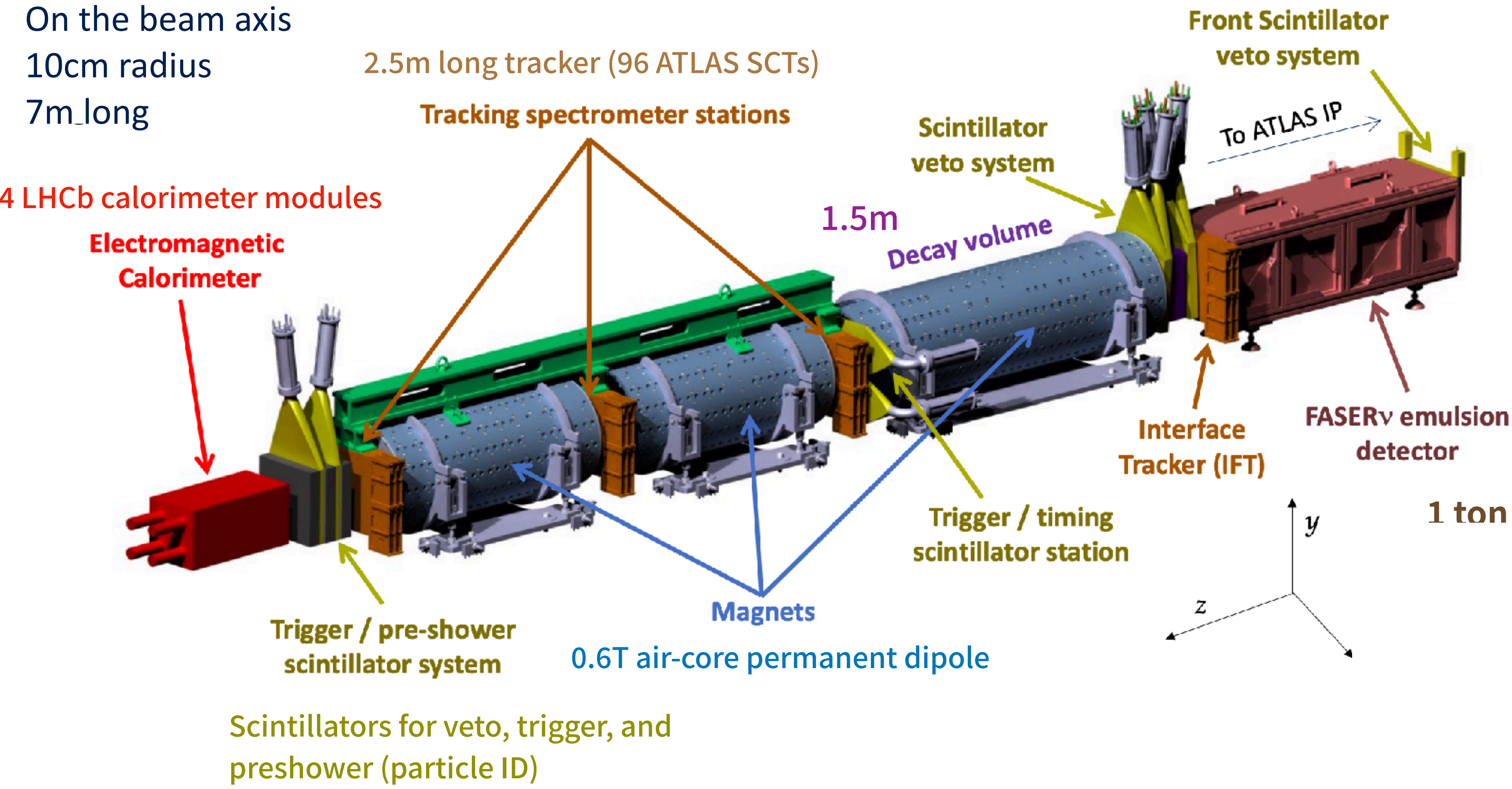


The **far forward region** has an extremely **hard radiation environment**, making continuous detector operation challenging
→ An unused tunnel was renovated, enabling a viable environment for the experiment

FASER detector

JINST 19 (2024), P05066

On the beam axis
10cm radius
7m long

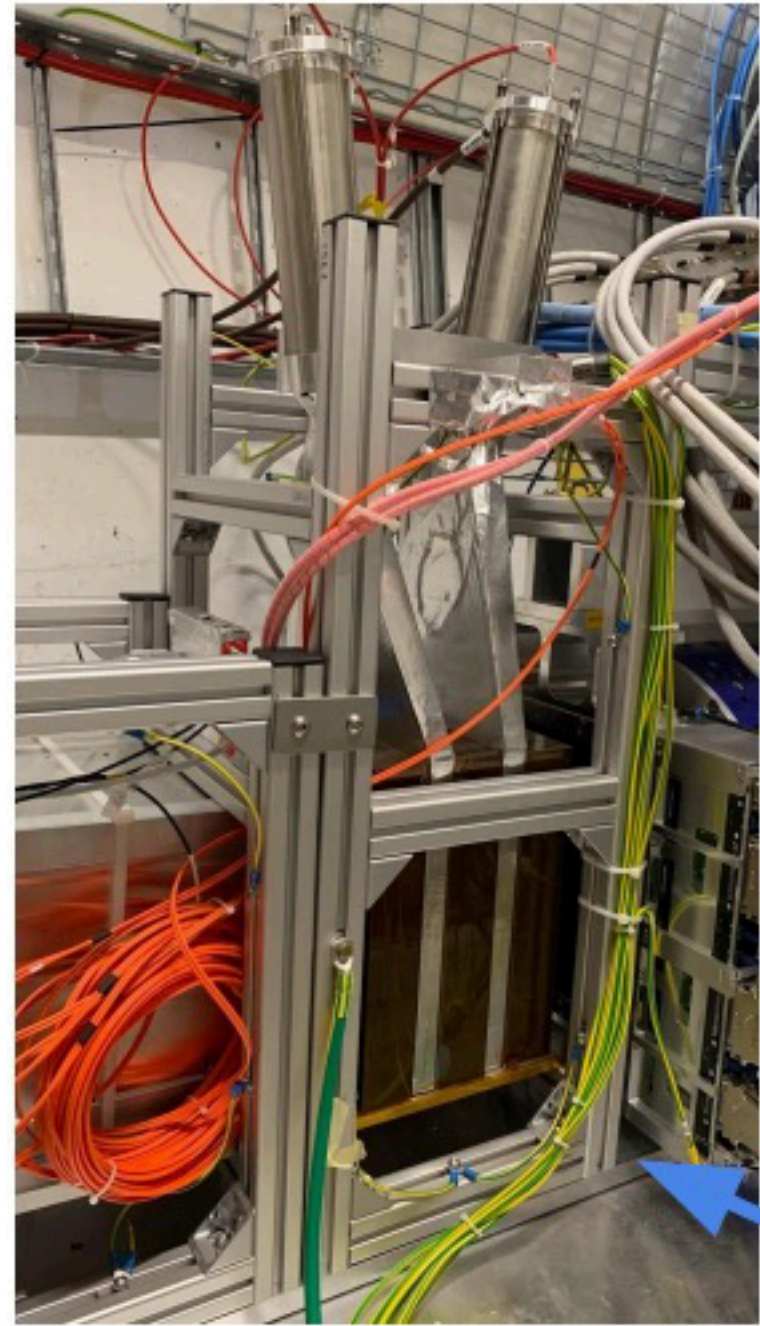


All detector components are successfully installed in T12 in March 2022

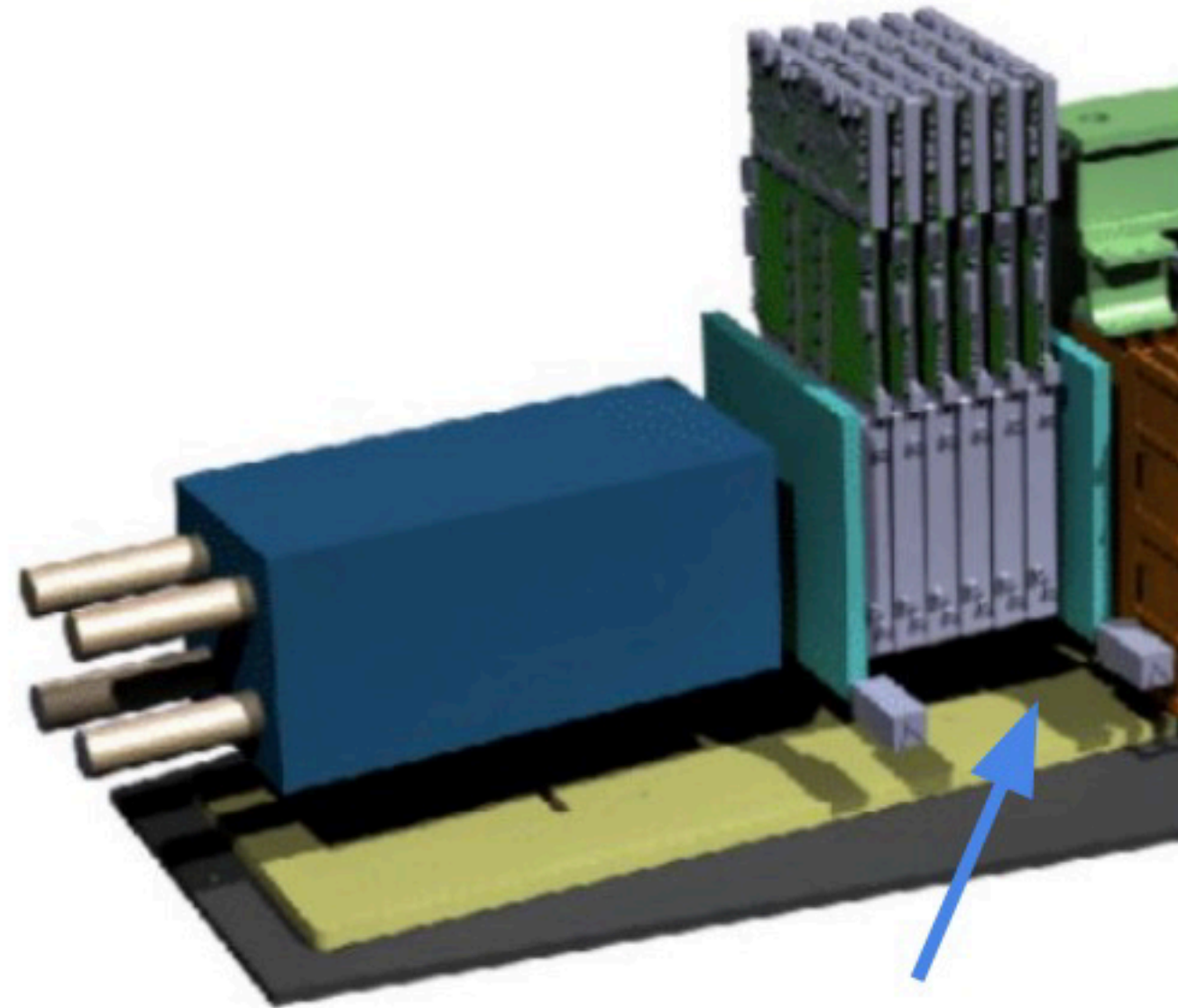
Particles from
ATLAS



FASER preshower upgrade



The first Preshower



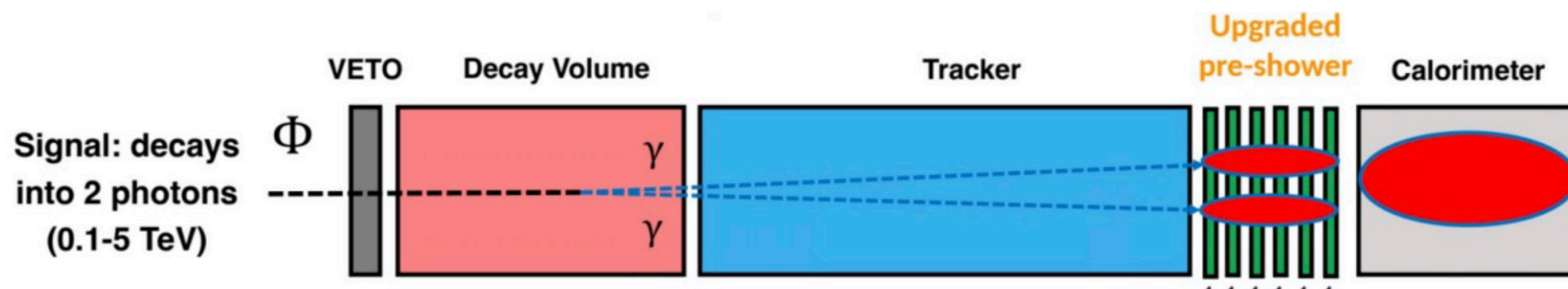
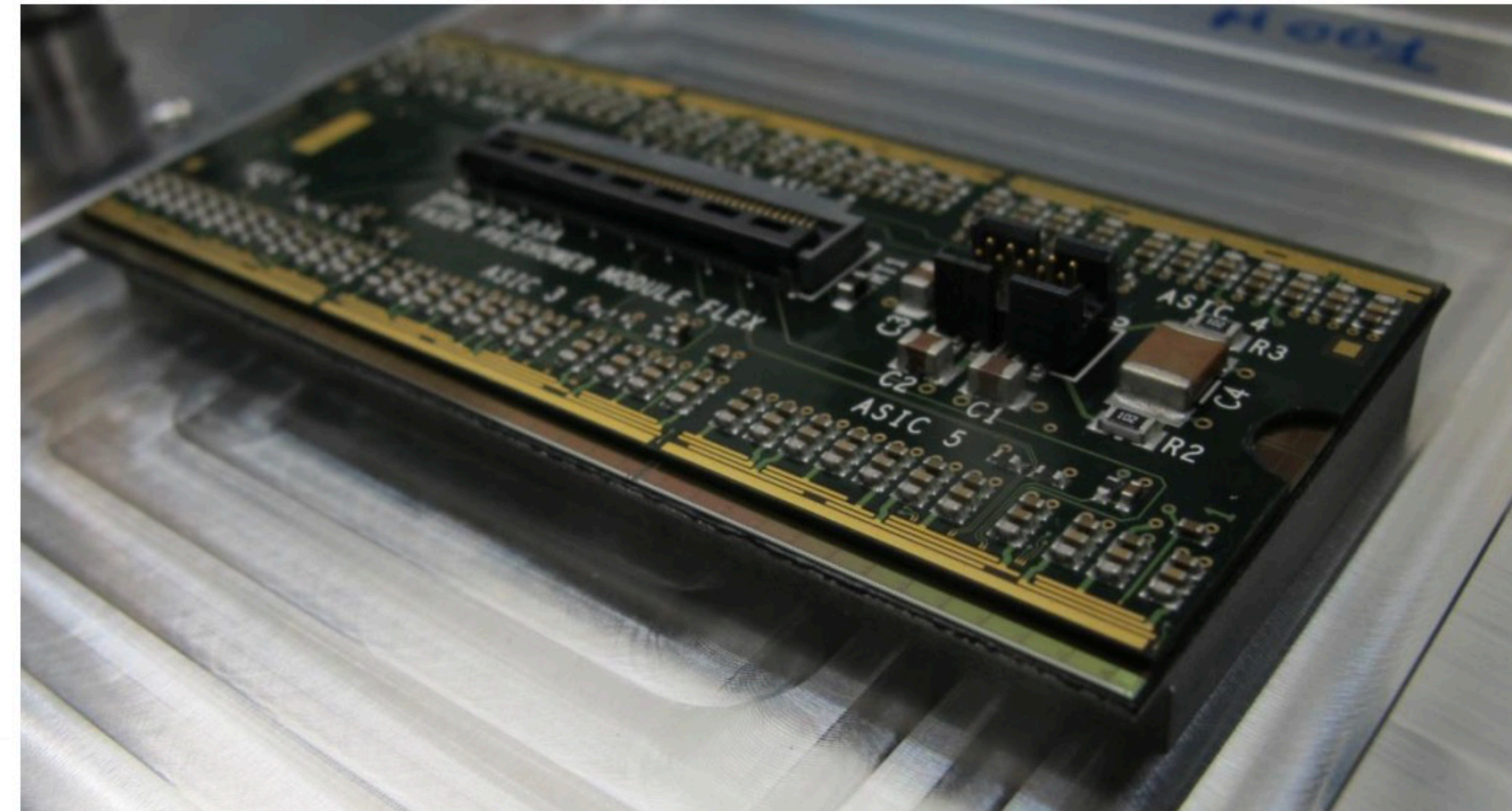
Planned upgrade (YETS 2024) The current Preshower

Preshower sub-detector upgrade

- Improve ability to resolve diphoton events with high X-Y granularity
- Improve sensitivity and background suppression in ALPs searches

FASER approved to run in Run 4

- Large dataset with upgraded FASER at HL-LHC

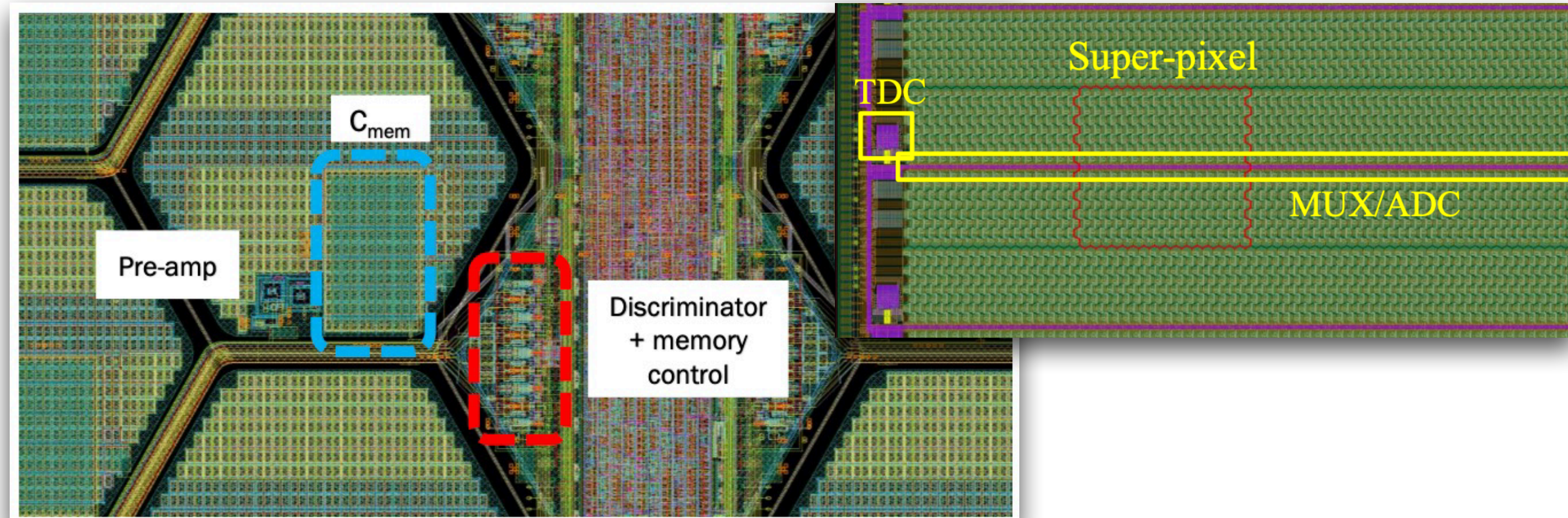
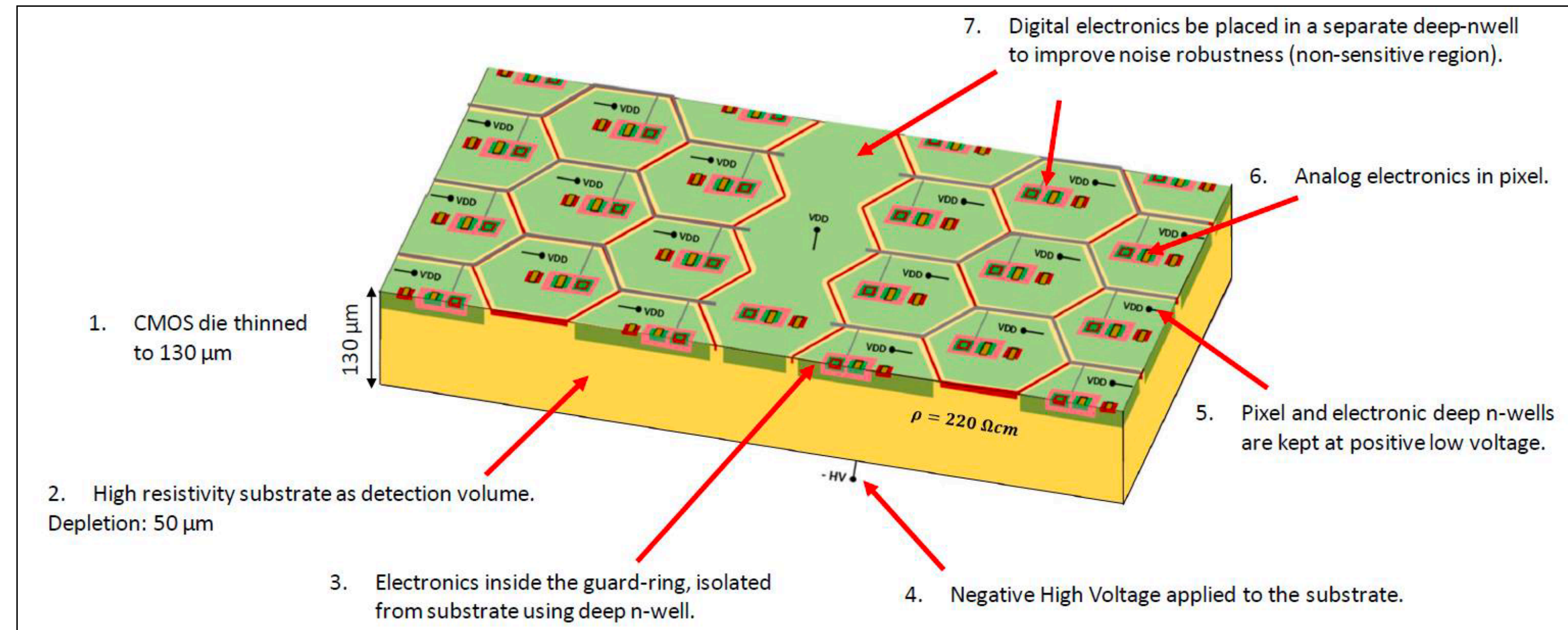


Preshower upgrade with 130 nm SiGe BiCMOS technology

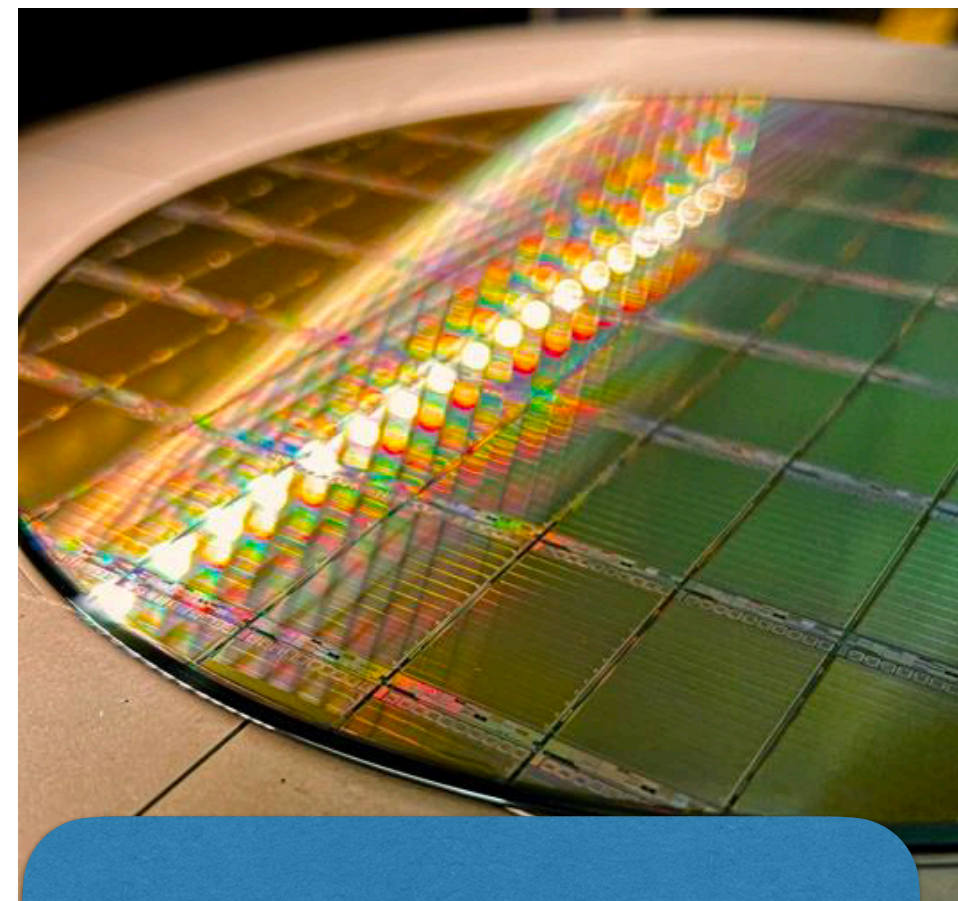
- **Monolithic Active Pixel Sensor**

130 nm SiGe BiCMOS technology (SG13G2 by IHP microelectronics)

- 8-inch wafer
- Laser dicing
- n-on-p planar sensor architecture
 - good radiation hardness
 - Good timing resolution
- Sensor size: $2.2 \times 1.5 \text{ cm}^2$
- Pixel size: $65 \mu\text{m}$ hexagonal
- Front-end architecture: preamplifier + discriminator + memory control
- Readout scheme:
 - 4-bit flash ADC per 256 pixels
 - 7-bit TDC per 2048 pixels
 - Super-pixel structure with shared MUX/ADC
- Time resolution: $< 300 \text{ ps}$



Preshower Project Development



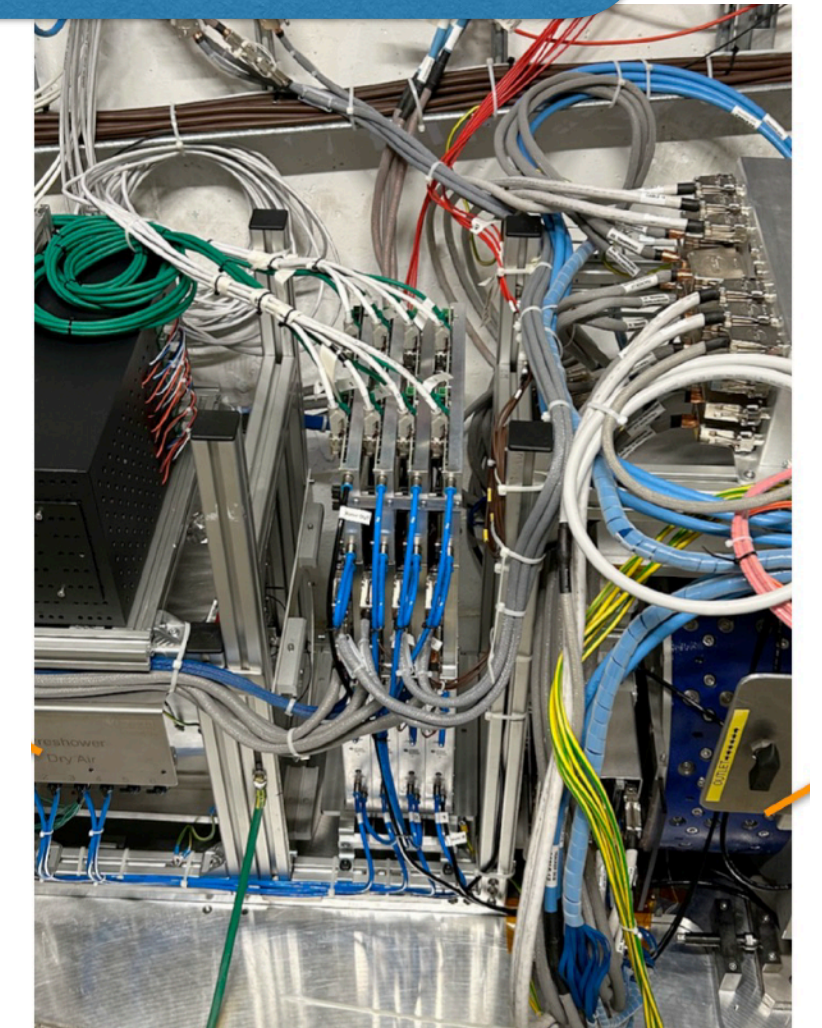
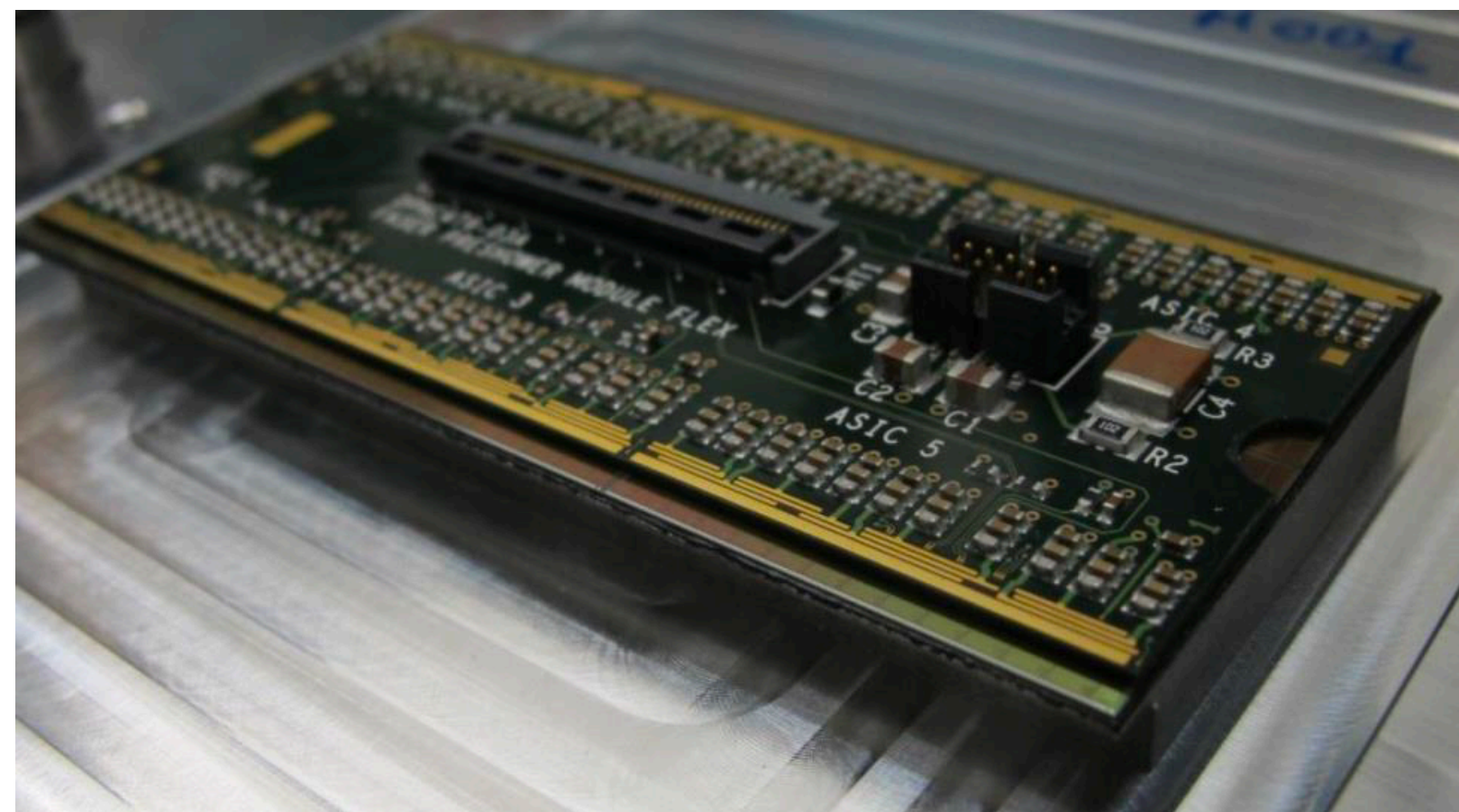
ASIC
qualification

Module
qualification

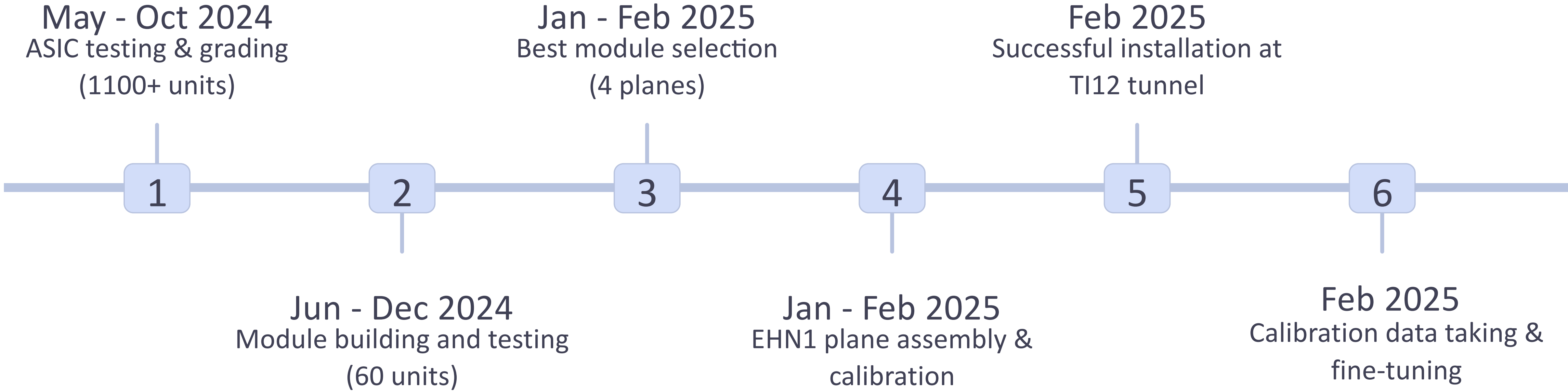


Plane assembly

Commissioning,
installation, and
operation



Project timeline



ASIC Testing procedure

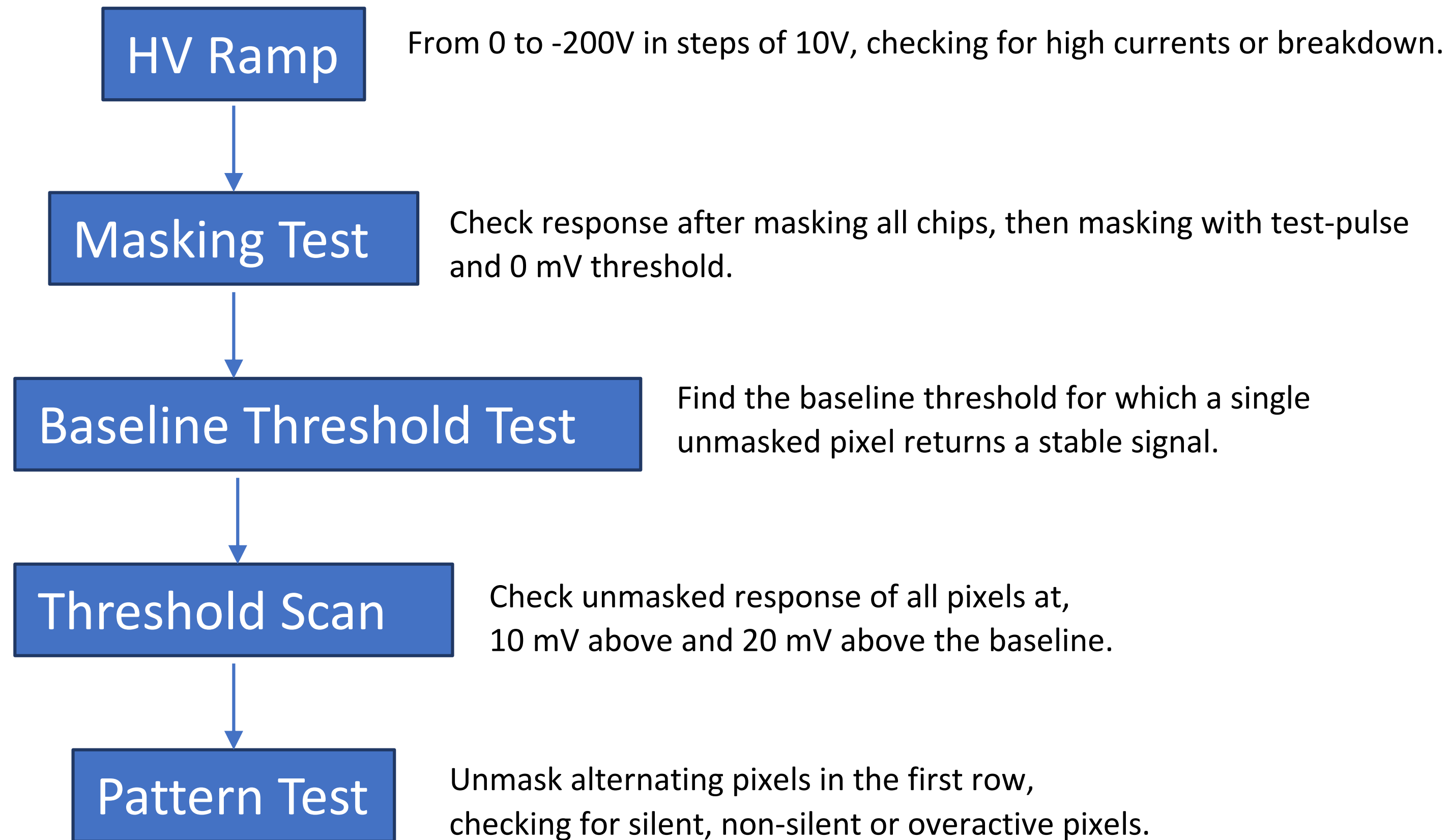
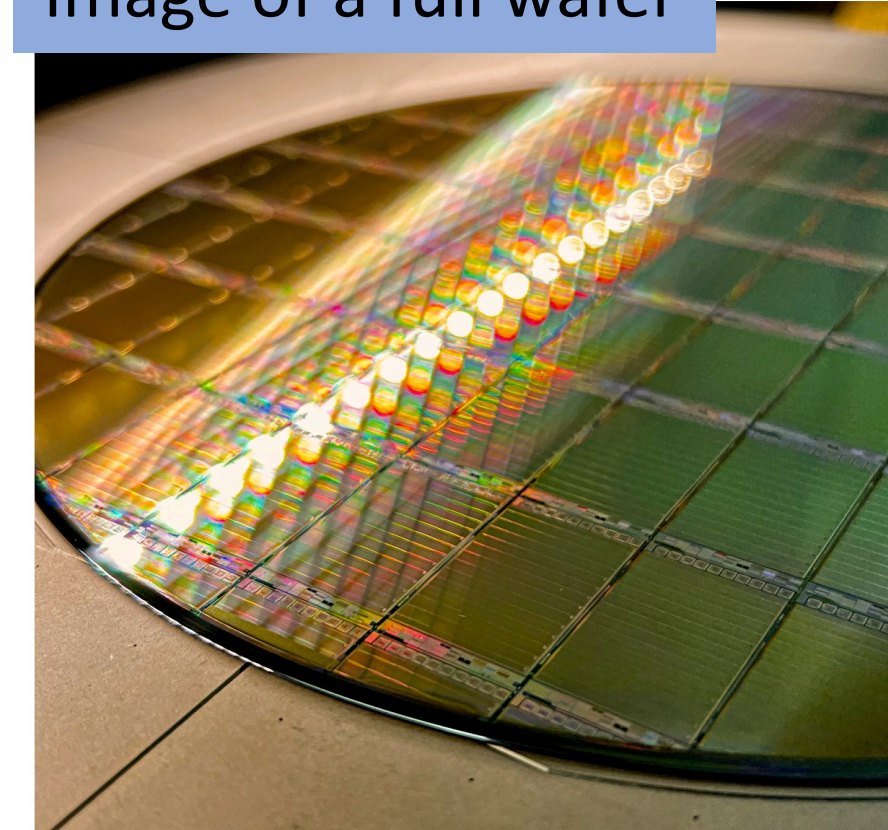
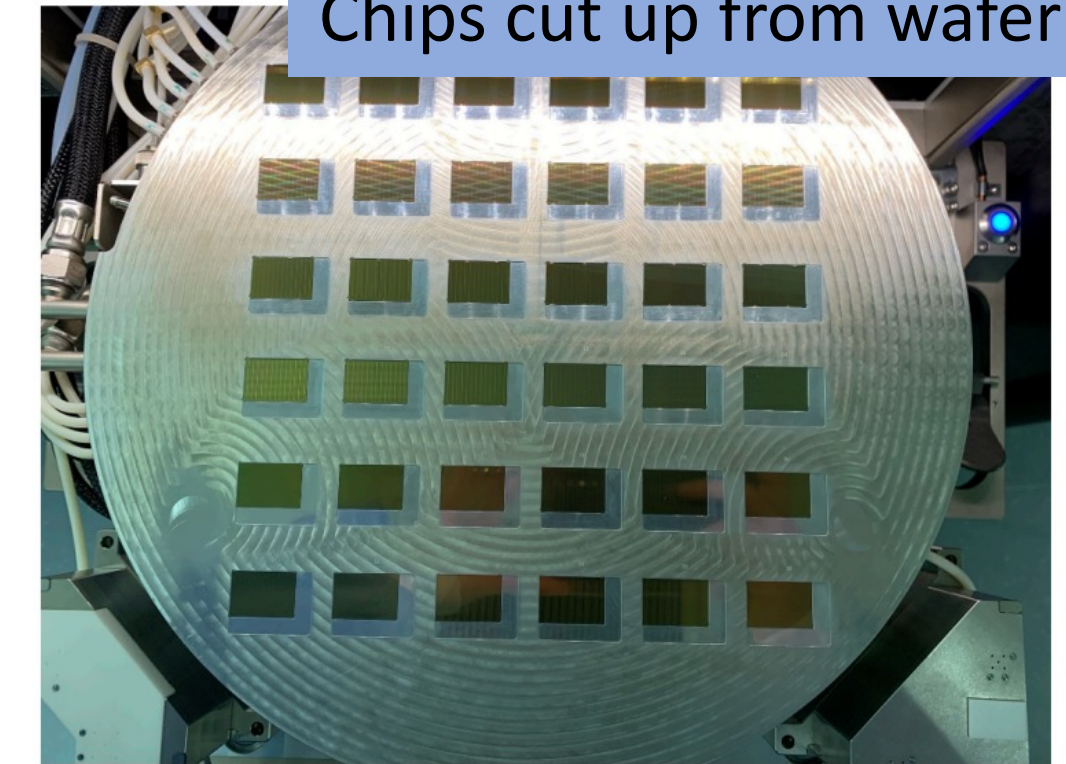


Image of a full wafer

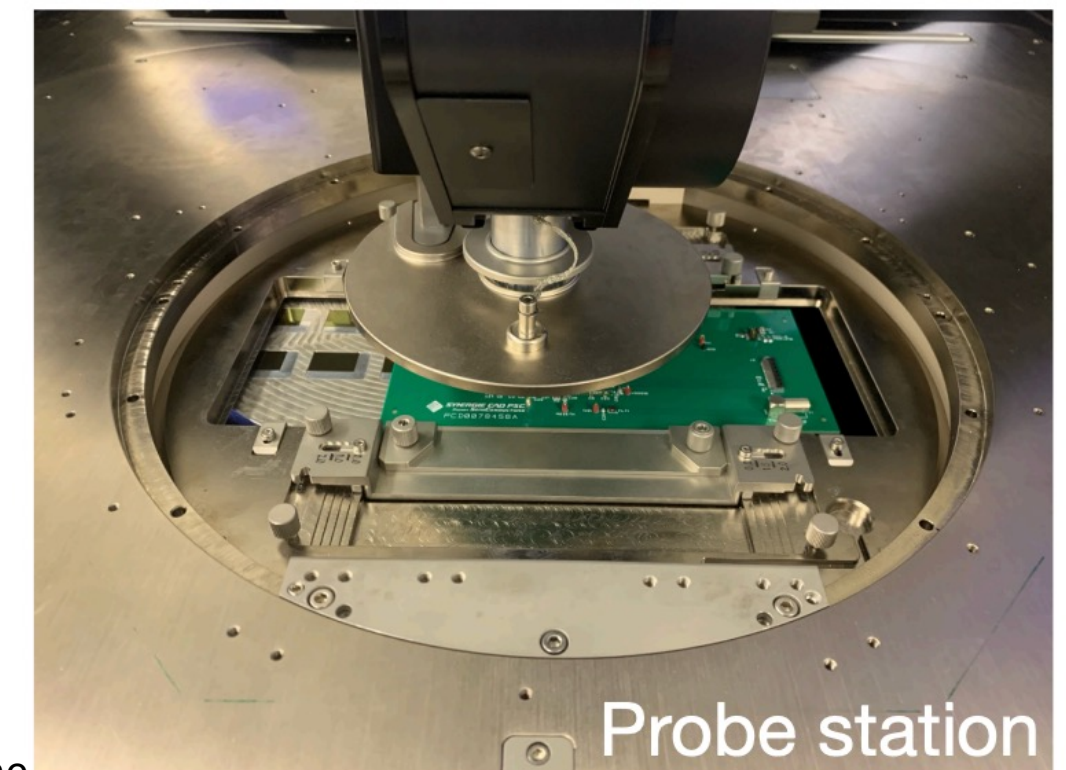


Chips cut up from wafer

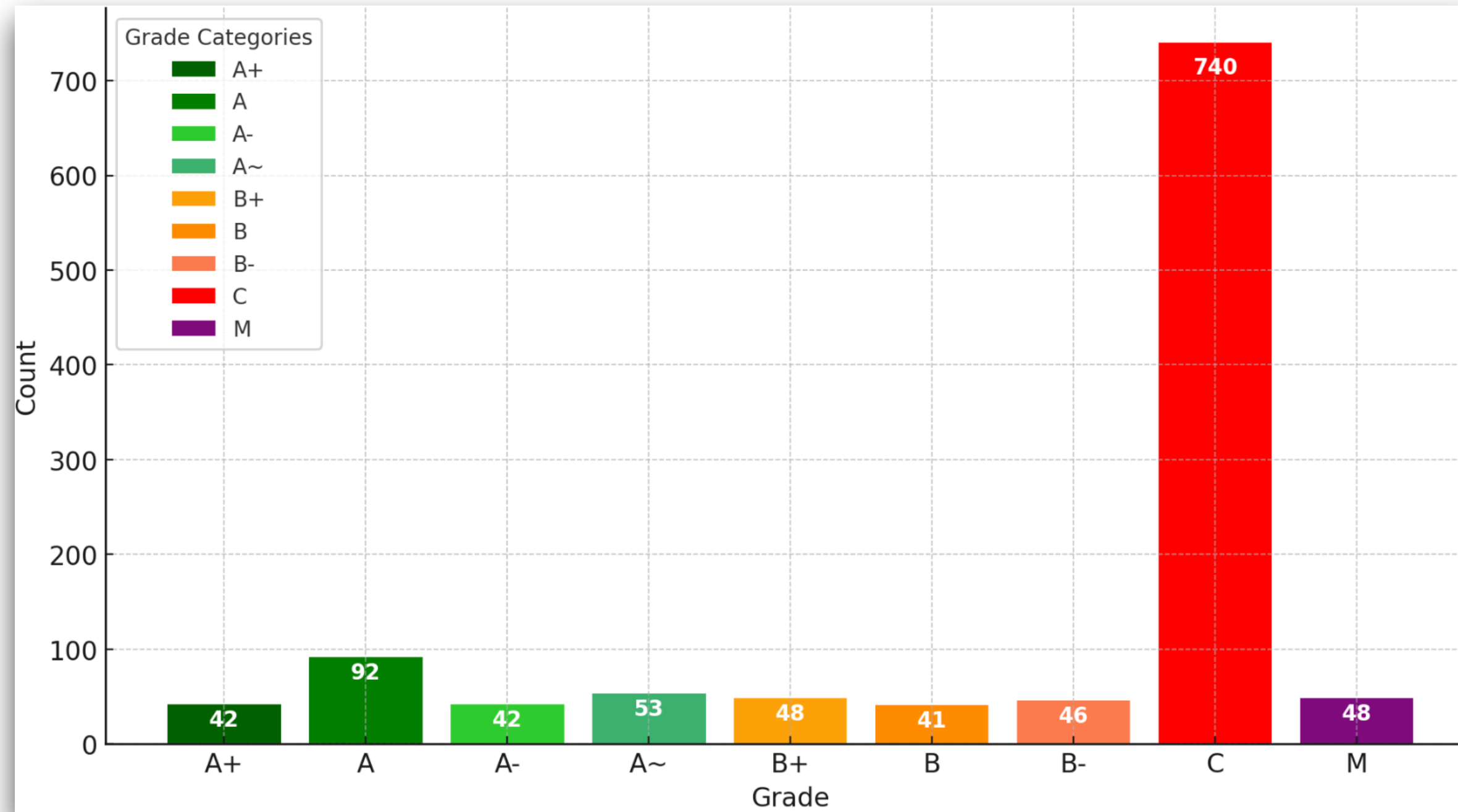


ne.

Probe station



ASIC qualification



Grading System: ASICs

After testing, the ASICs are graded based on their performance and compliance with specifications. They are categorized as follows:

- Grade A: Fully functional ASICs with optimal performance. These are ideal for use in modules where maximum reliability and performance are required.
- Grade B: ASICs that exhibit minor issues but are still functional within acceptable limits. These may be used in modules where slight deviations from optimal performance are tolerable.
- Grade C: ASICs with significant issues that render them unsuitable for use in standard modules. These are either set aside for further testing or discarded.

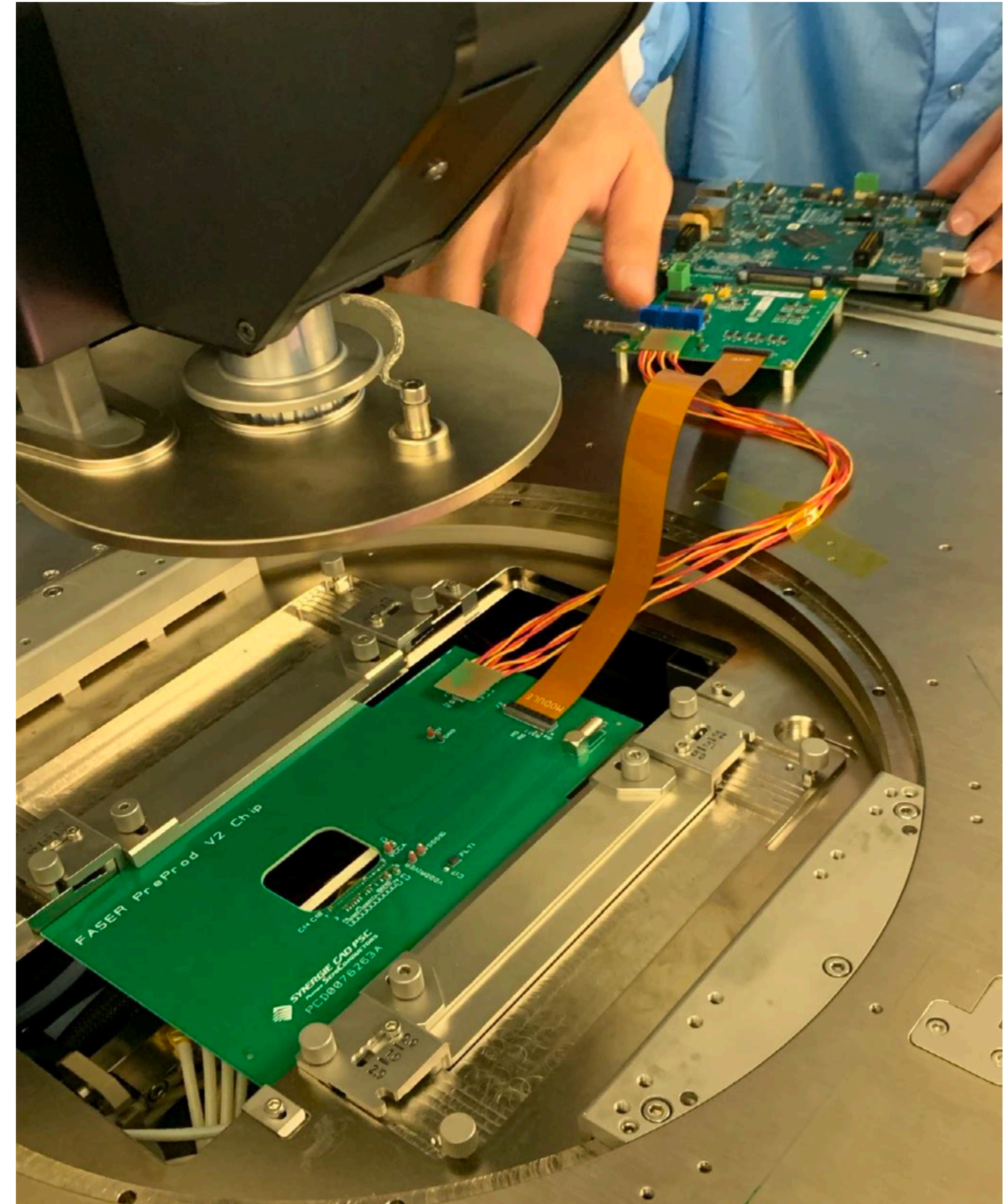
A total of 1,101 chips were tested, yielding an efficiency of 29% of chips usable for module assembly. The breakdown is as follows:

- 42 A+ chips were flawless, showing no issues.
- 187 chips graded as A, A-, and A~ had only minor issues, such as overly active or missing pixels in the pattern test.
- 48 B+ chips exhibited structural problems affecting less than 8% of the chip area.
- 41 B chips had more significant issues, with up to 4 SCs of the chip being problematic.
- 46 B- chips are not maskable when the threshold is set to zero; however, they appear to be properly maskable at higher thresholds with the test pulse enabled, suggesting they may remain silent and operable under specific conditions.
- 740 C chips had configuration, masking issues, or failed LV/HV tests.
- 48 missing (M) chips were ASICs lost during transport or assembly.

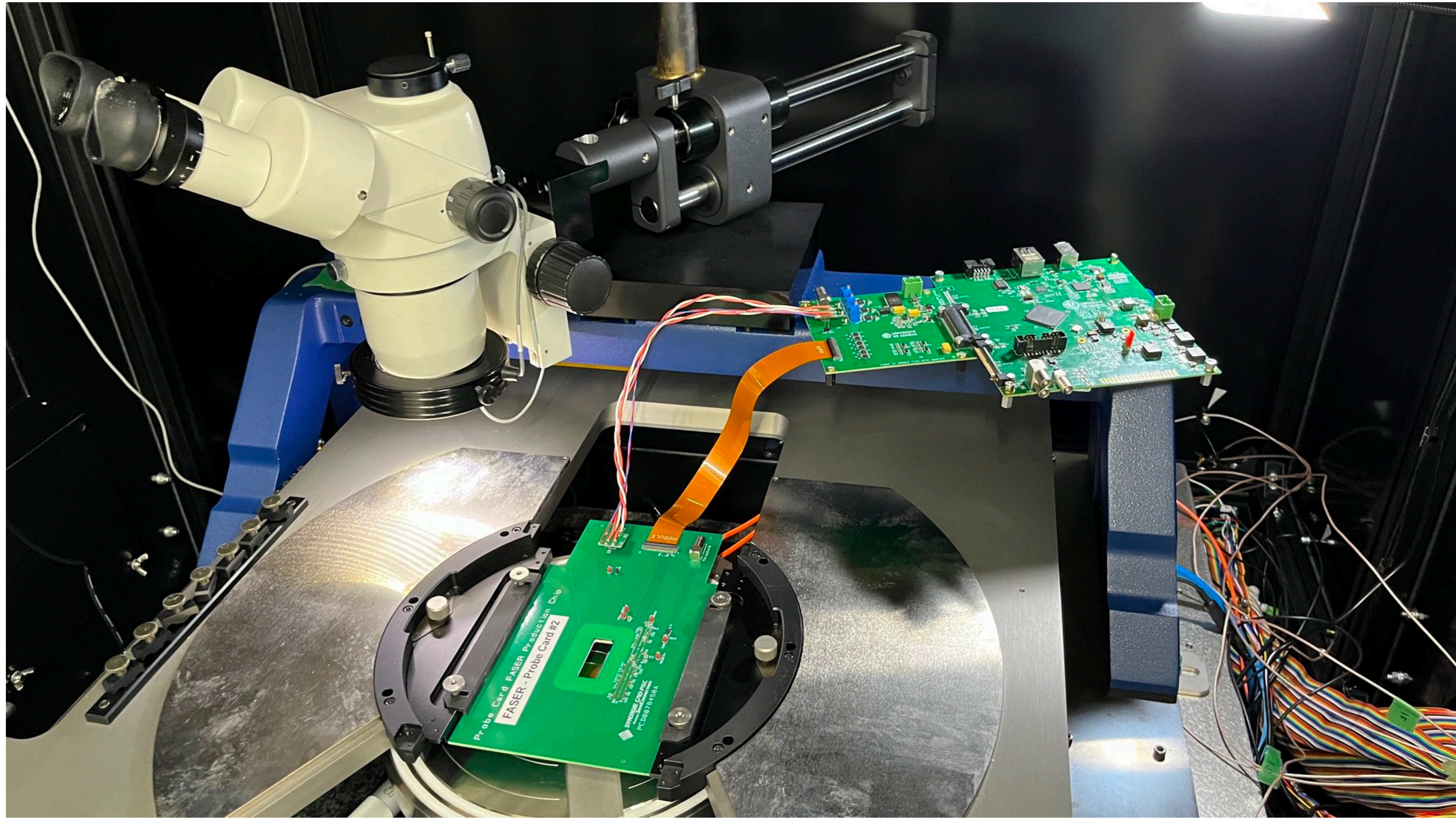
Chip testing - setup in Kyushu U.

Although the main QA/QC site was UNIGE, after ASIC characterization at UNIGE has finalized, we have been maintaining communication with colleagues at Kyushu University to provide a full working probe card setup for future chip testing.

- Probe Card
- Adaptor Board with pigtail and ribbon cable
- GPIO board with firmware installed as well as front-end software
- 9 chips to validate procedure.

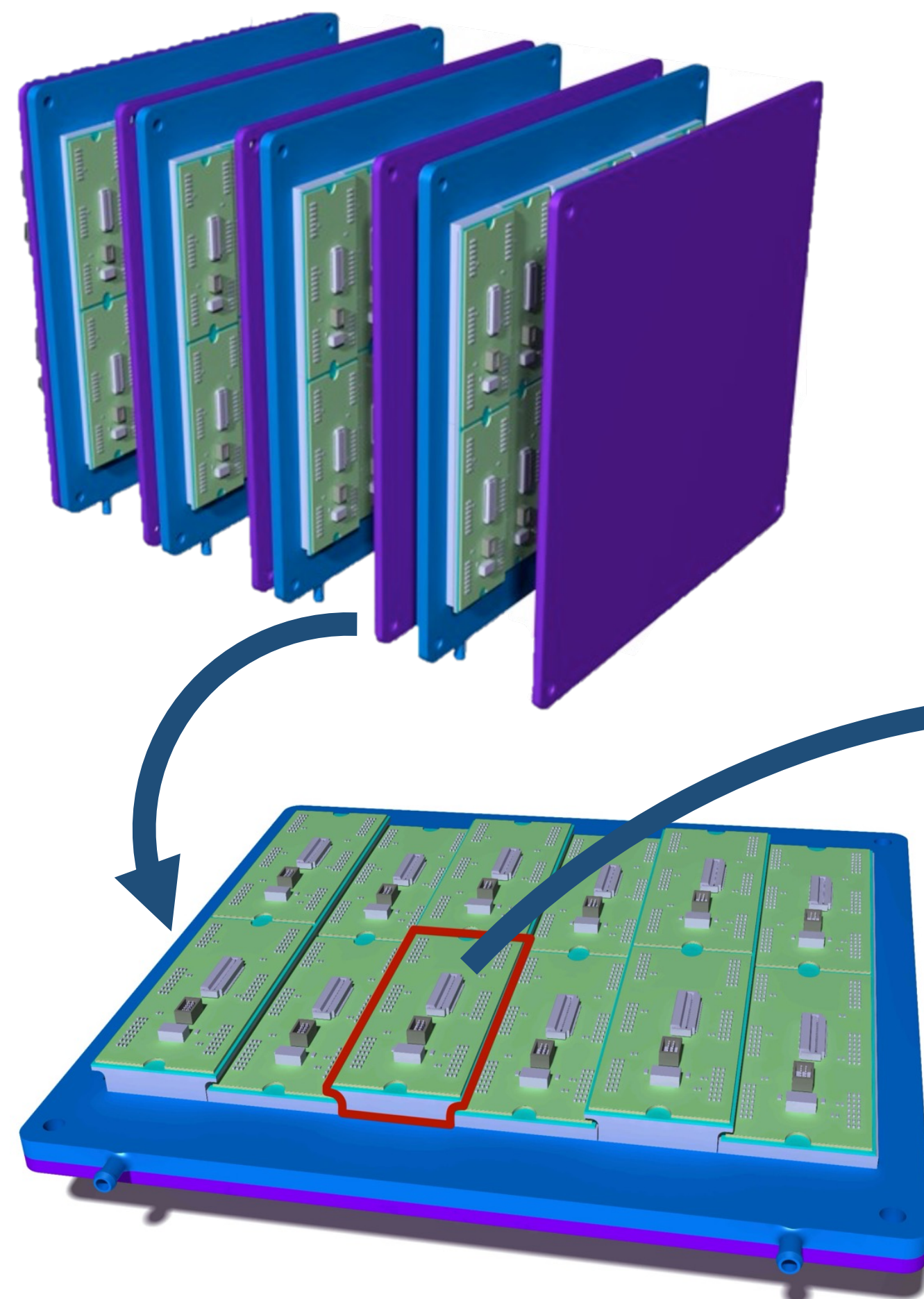


Chip testing - setup in Kyushu U. and installed



Module assembly

4 planes in total (silicon + W plates)

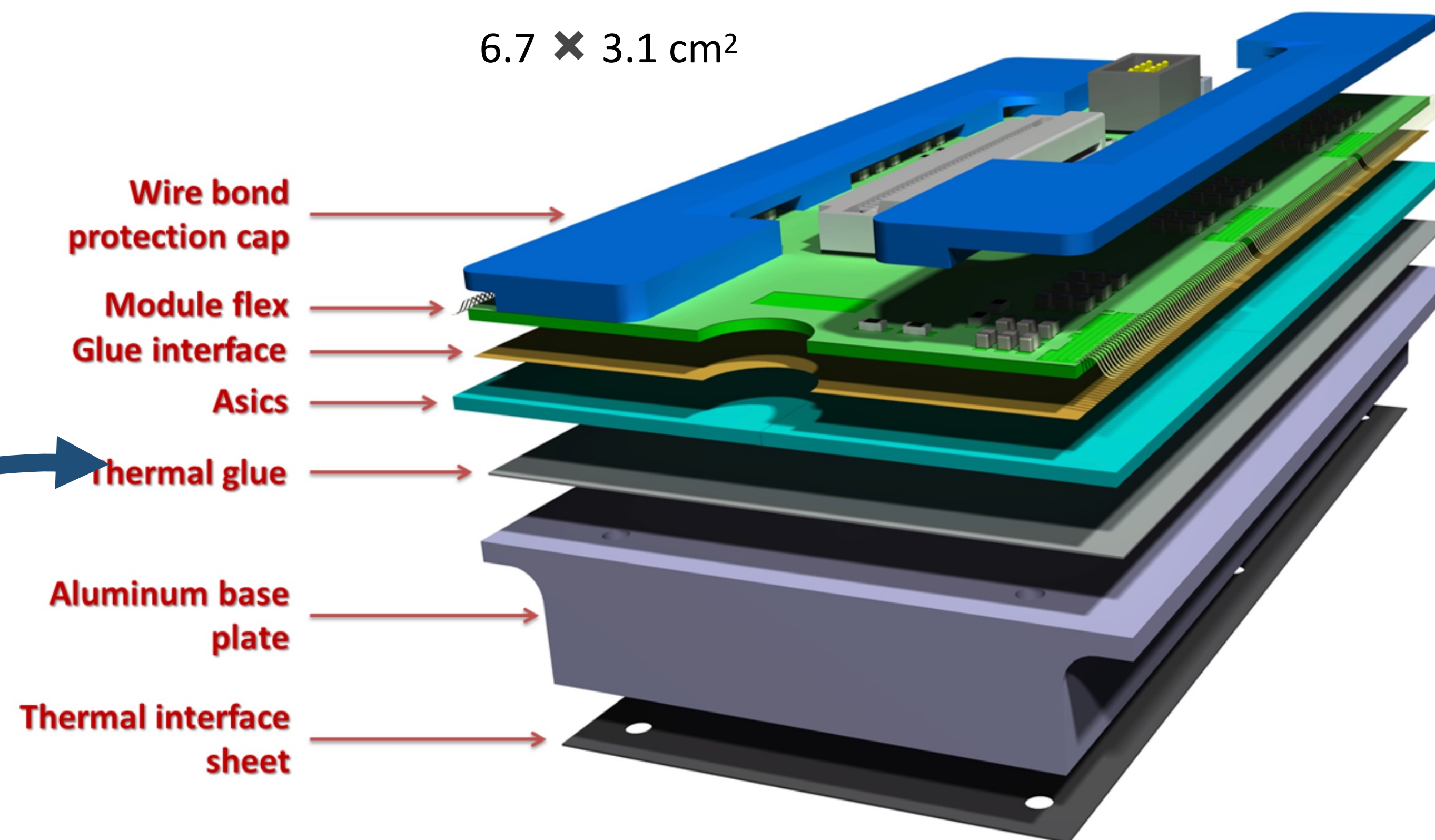


20 × 20 cm² (5 mm thickness)

6 ASICs per module, 208x128 pixels each

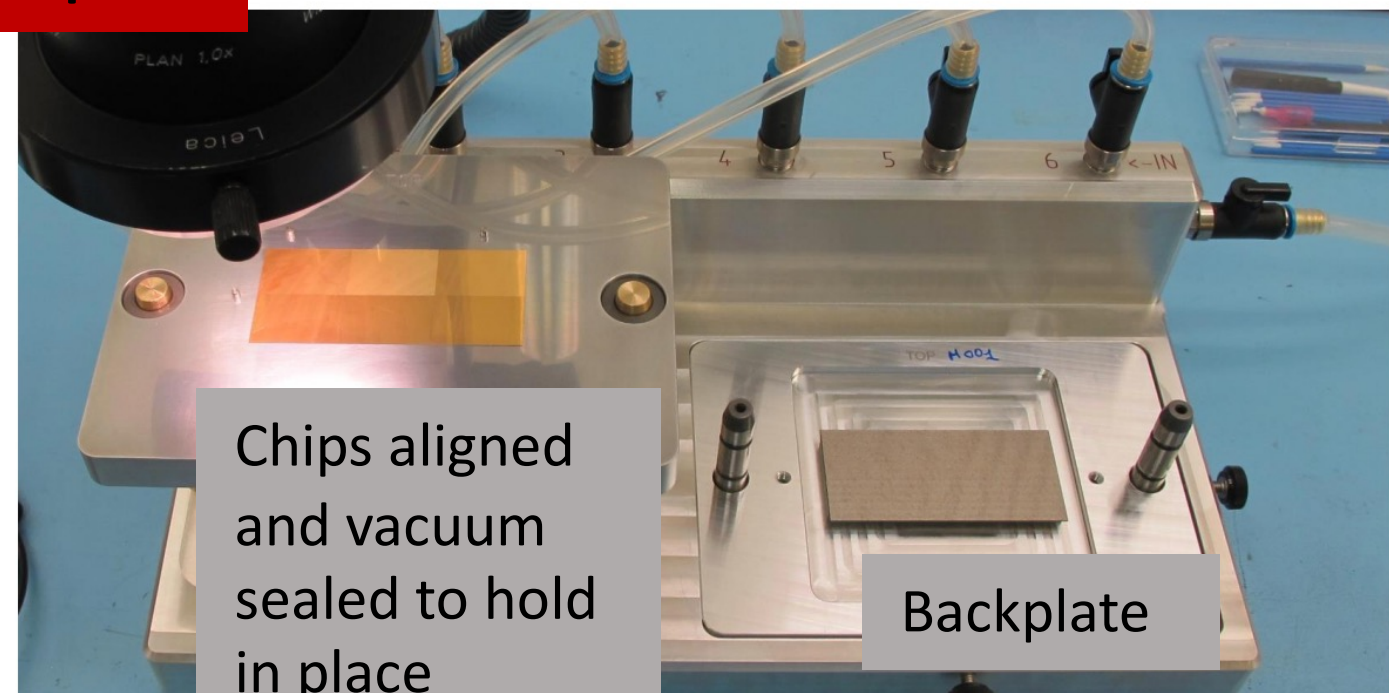
↪ 100 μm pitch hexagonal pixels

6.7 × 3.1 cm²



Chips to Module

Step 1

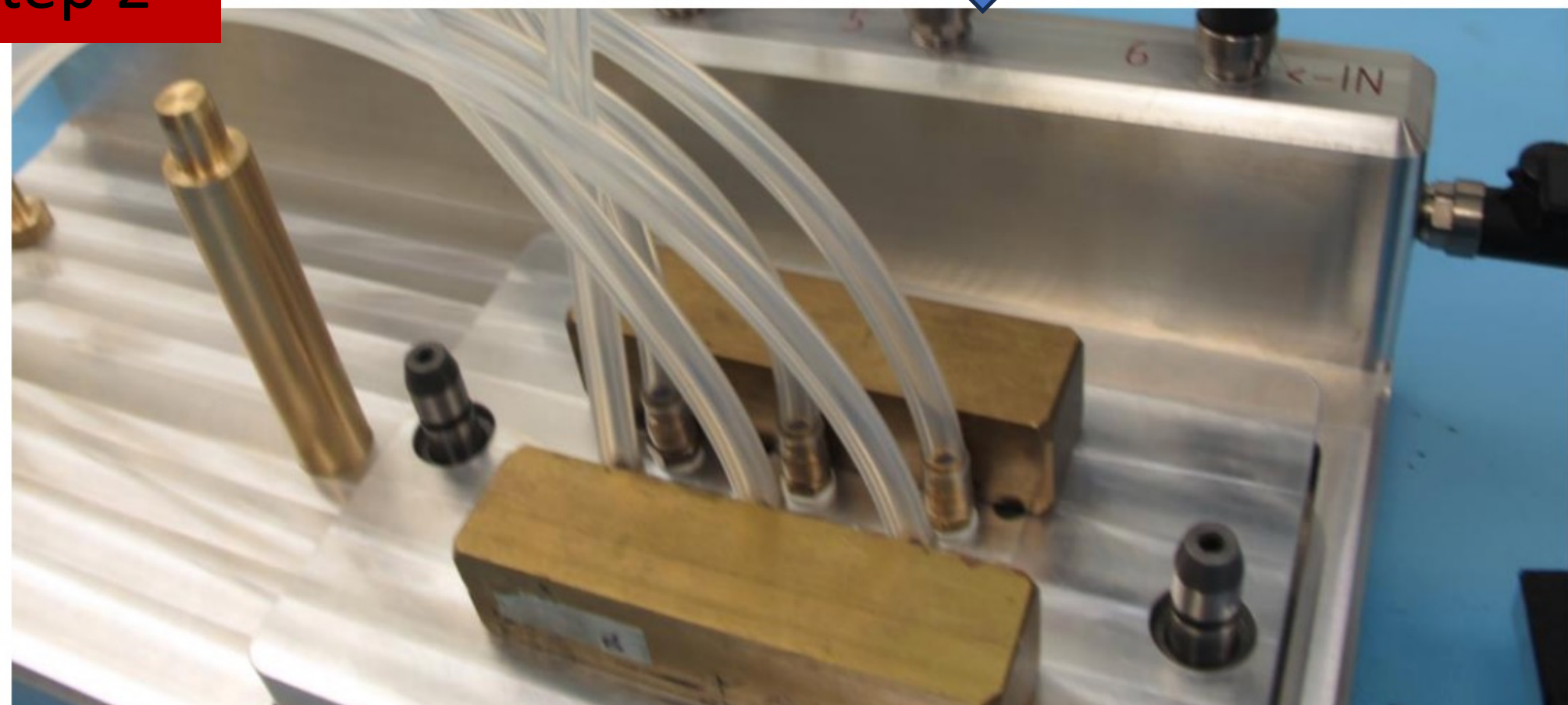


Chips aligned and vacuum sealed to hold in place

Backplate

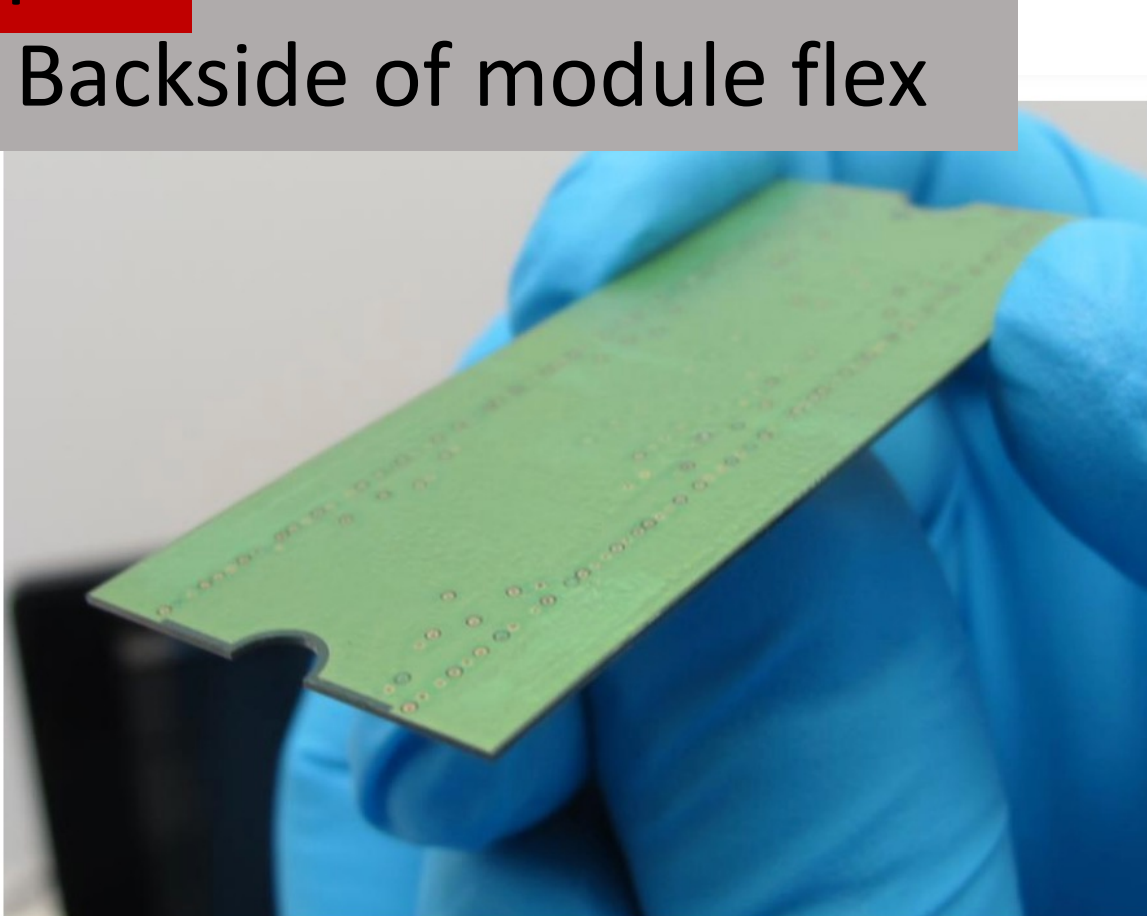
Chips are aligned and backplate set up

Step 2



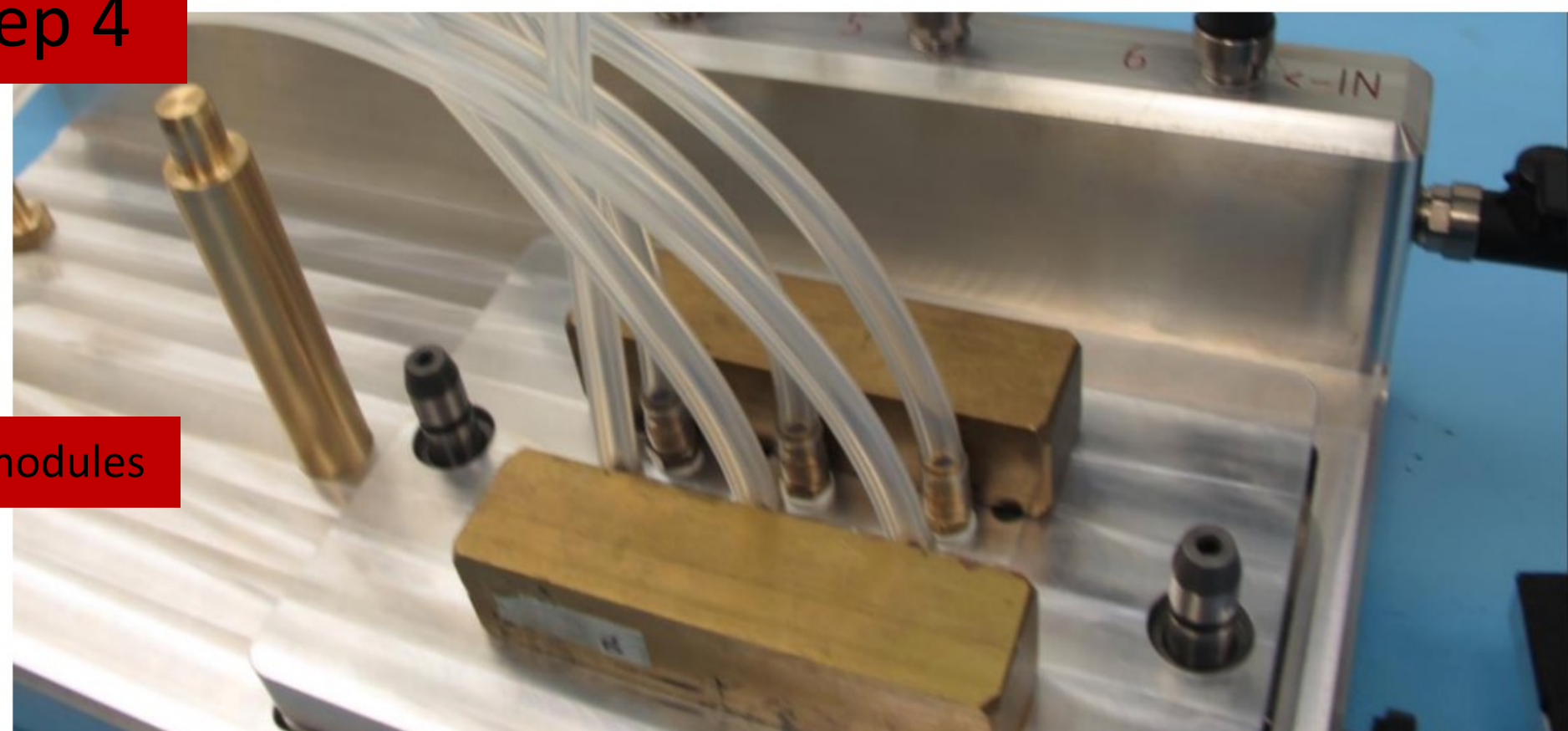
Chips are flipped and glued onto the backplate

Step 3

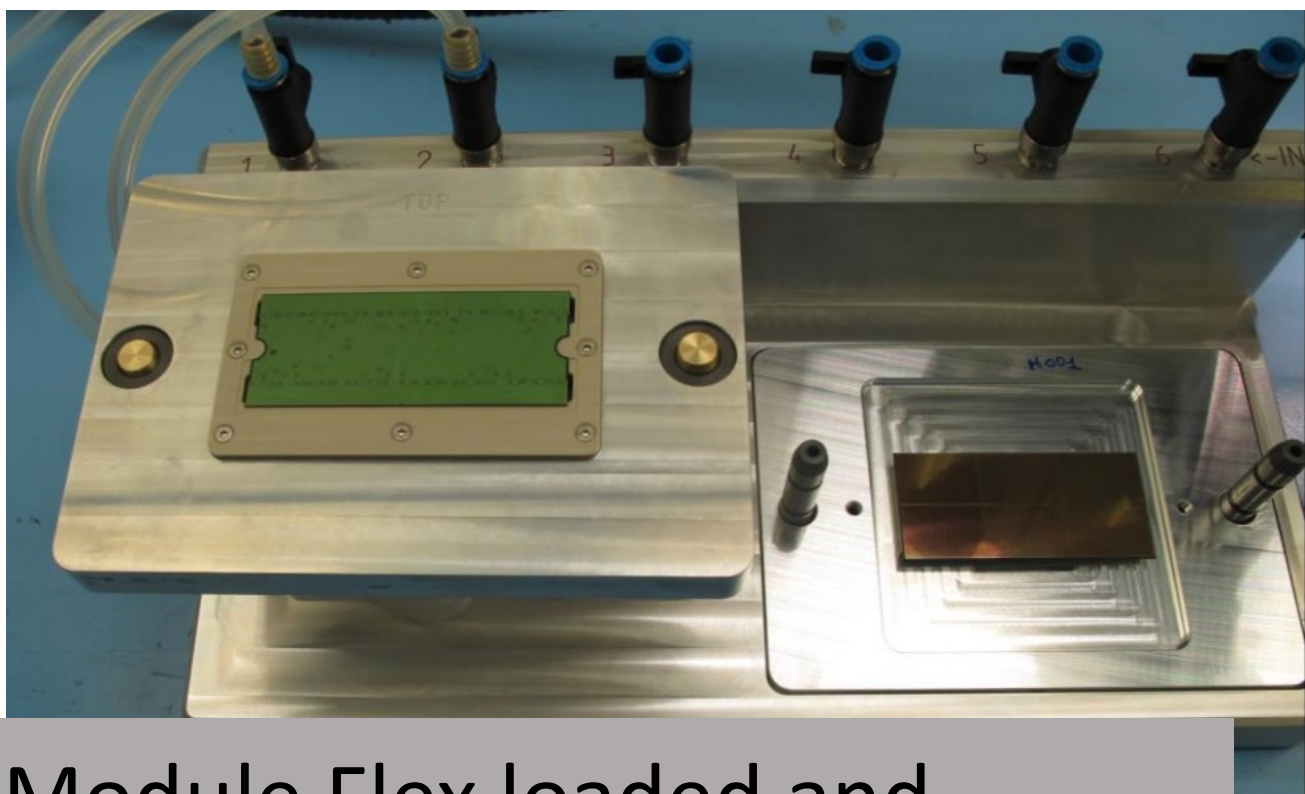


Backside of module flex

Step 4

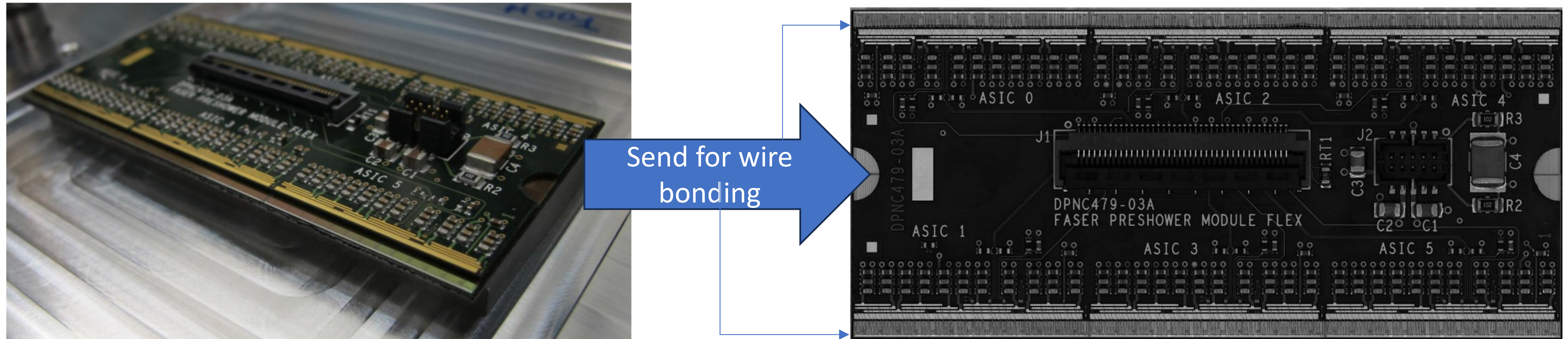


Module Flex is flipped and glued onto the chip + backplate



Module Flex loaded and vacuum sealed to hold in place

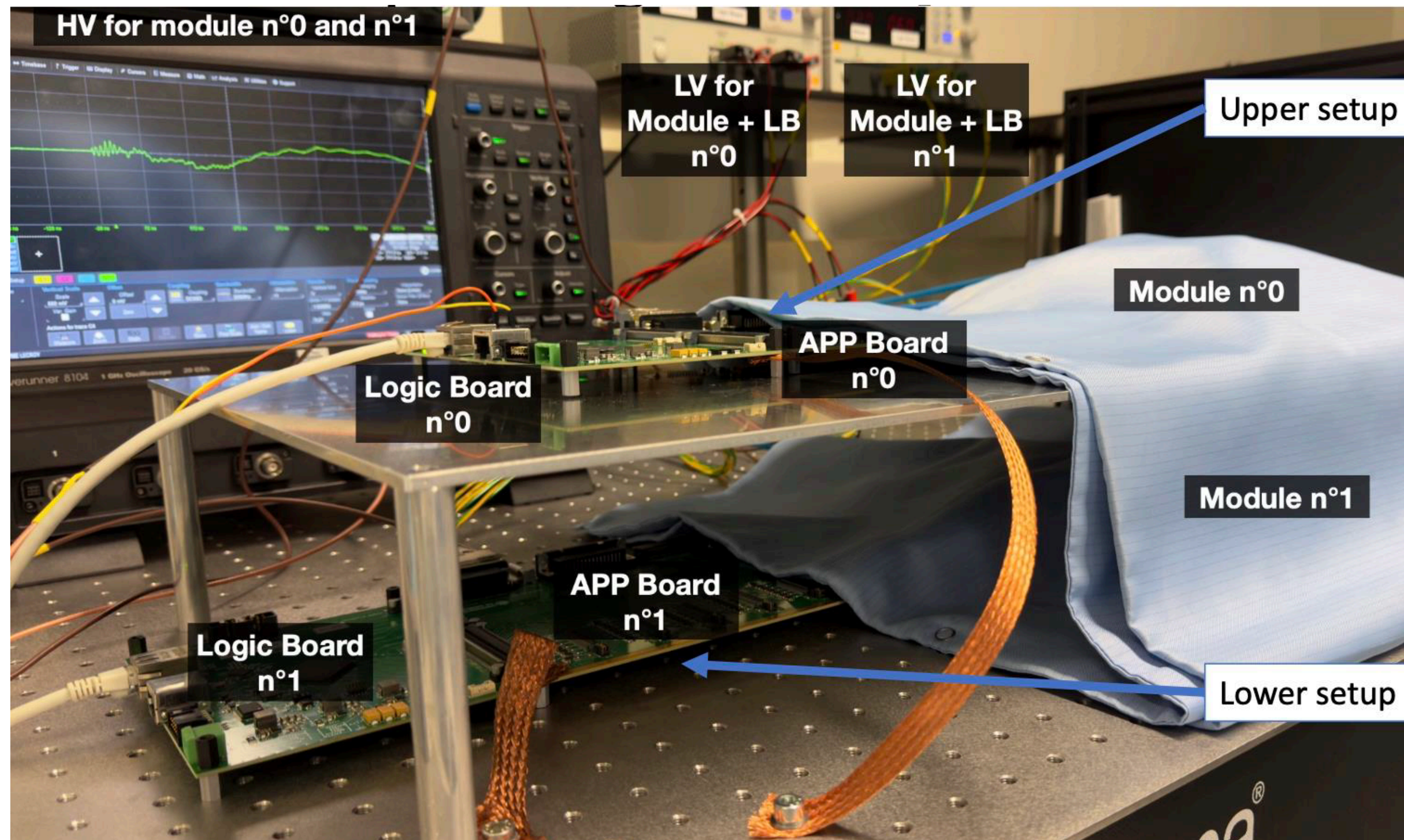
Once mounted



1. Once the ASICs are assembled onto a module, they are ready to be wire bonded
2. Once wire bonded, the electrical modules are ready to be tested
3. The tests are being carried out at the UNIGE clean room as shown on the next slide

Module testing

Module qualification was done in the clean rooms at UNIGE, with our usual dual setup.



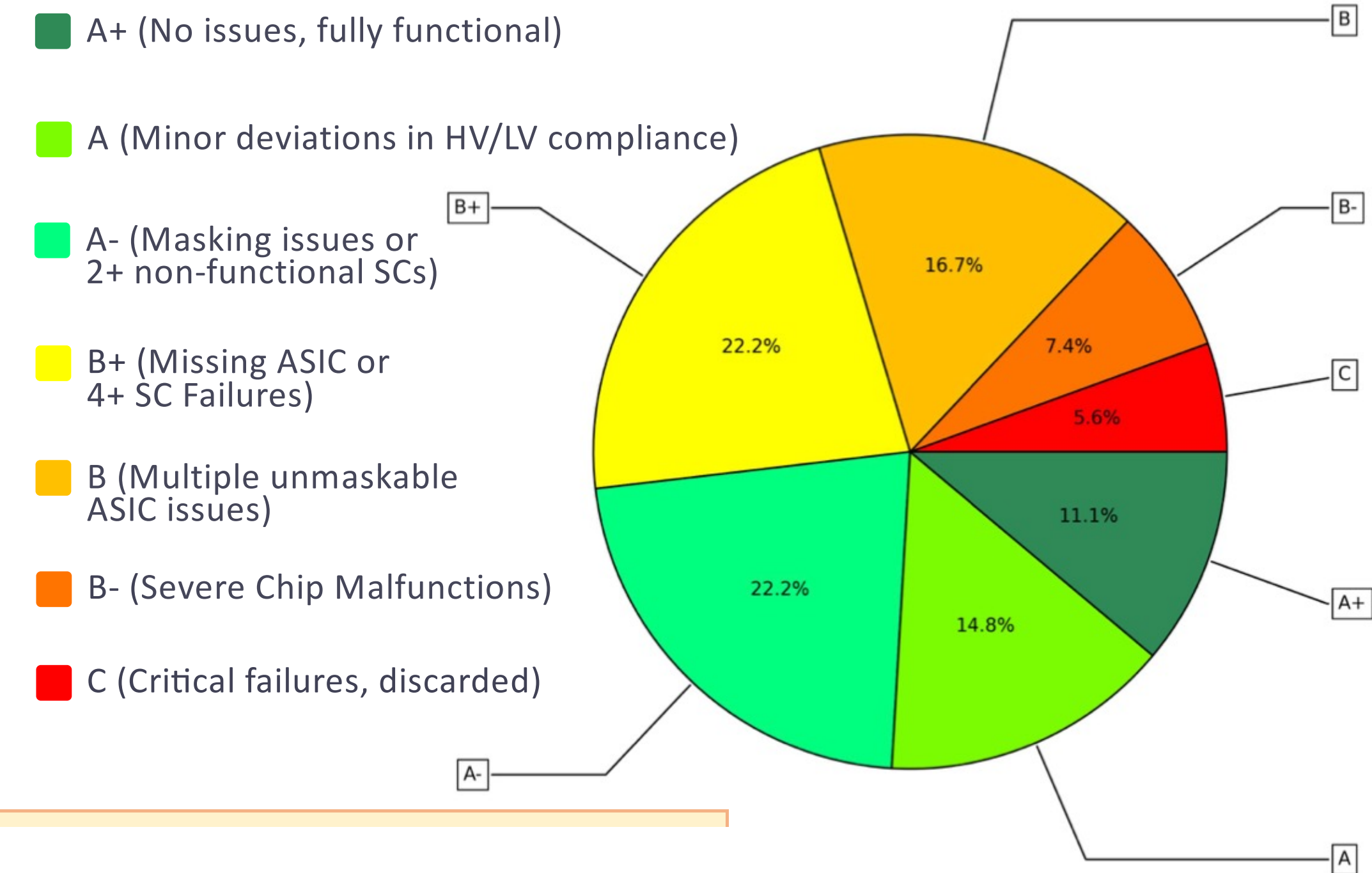
Tests Performed for Each Module

- **Electrical test**
 - Monitor HV and LV currents
- **Threshold scan to set the optimal thresholdP**
 - perform broad and fine scans to determine the best DAC value (± 1)
- **Noise scan to mask noisy pixels**
 - Use 1 s, 5 s, and 60 s scans to identify even low-rate noisy pixels
- **Test pulse scan to measure sensitivity and identify problematic regions**
 - Inject test pulses in predefined patterns

Module and plane assembly

In order to qualify, planes 1, 2, 3, 0 are assembled avoiding problematic regions to overlap

- The best 48 were selected to build 4 planes
- Yield of first 54 assembled modules:



Plane 1
≈1% dead area

	5	3	1	5	3	1	
ELECT08 (thin)	4	2	0	4	2	0	ELECT13 (thin)
	5	3	1	5	3	1	
ELECT10 (thick)	4	2	0	4	2	0	ELECT15 (thick)
	5	3	1	5	3	1	
ELECT09 (thin)	4	2	0	4	2	0	ELECT21 (thin)
	5	3	1	5	3	1	
ELECT11 (thick)	4	2	0	4	2	0	ELECT19 (thick)
	5	3	1	5	3	1	
ELECT12 (thin)	4	2	0	4	2	0	ELECT17 (thin)
	5	3	1	5	3	1	
ELECT14 (thick)	4	2	0	4	2	0	ELECT22 (thick)

Plane 2
3 - 6 % dead area

	5	3	1	5	3	1	
ELECT24 (thin)	4	2	0	4	2	0	ELECT20 (thin)
	5	3	1	5	3	1	
ELECT31 (thick)	4	2	0	4	2	0	ELECT35 (thick)
	5	3	1	5	3	1	
ELECT04 (thin)	4	2	0	4	2	0	ELECT37 (thin)
	5	3	1	5	3	1	
ELECT23 (thick)	4	2	0	4	2	0	ELECT27 (thick)
	5	3	1	5	3	1	
ELECT16 (thin)	4	2	0	4	2	0	ELECT42 (thin)
	5	3	1	5	3	1	
ELECT43 (thick)	4	2	0	4	2	0	ELECT36 (thick)

Plane 3
5 - 8% dead area

	5	3	1	5	3	1	
ELECT48 (thin)	4	2	0	4	2	0	ELECT02 (thin)
	5	3	1	5	3	1	
ELECT39 (thick)	4	2	0	4	2	0	ELECT47 (thick)
	5	3	1	5	3	1	
ELECT41 (thin)	4	2	0	4	2	0	ELECT34 (thin)
	5	3	1	(to be tested) 5	(to be tested) 3	(to be tested) 1	
ELECT03 (thick)	4	2	0	(to be tested) 4	(to be tested) 2	(to be tested) 0	ELECT44 (thick)
	5	3	1	5	3	1	
ELECT29 (thin)	4	2	0	4	2	0	ELECT28 (thin)
	5	3	1	5	3	1	
ELECT18 (thick)	4	2	0	4	2	0	ELECT49 (thick)

Plane 0
10 - 20% dead area

	5	3	1	5	3	1	
ELECT45 (thin)	4	2	0	4	2	0	ELECT52 (thin)
	5	3	1	5	3	1	
ELECT40 (thick)	4	2	0	4	2	0	ELECT54 (thick)
	5	3	1	5	3	1	
ELECT53 (thin)	4	2	0	4	2	0	ELECT50 (thin)
	5	3	1	5	3	1	
ELECT05 (thick)	4	2	0	4	2	0	ELECT07 (thick)
	5	3	1	5	3	1	
ELECT01 (thin)	4	2	0	4	2	0	ELECT38 (thin)
	5	3	1	5	3	1	
ELECT30 (thick)	4	2	0	4	2	0	ELECT06 (thick)

Plane assembly and installation

224 A chips

↳ ≈ 2.5 planes

73 B+ and B

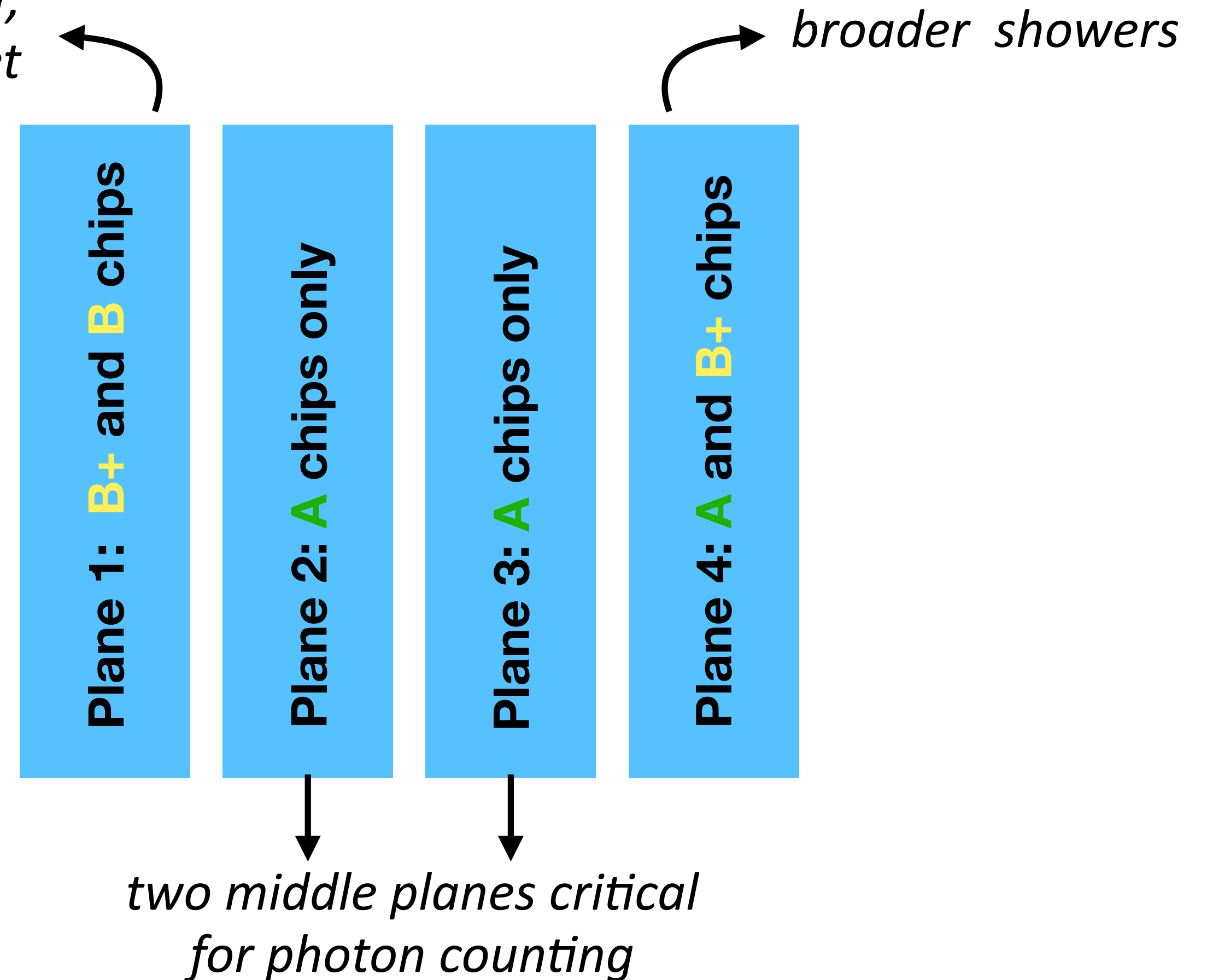
↳ ≈ 1.5 planes

746 C chips

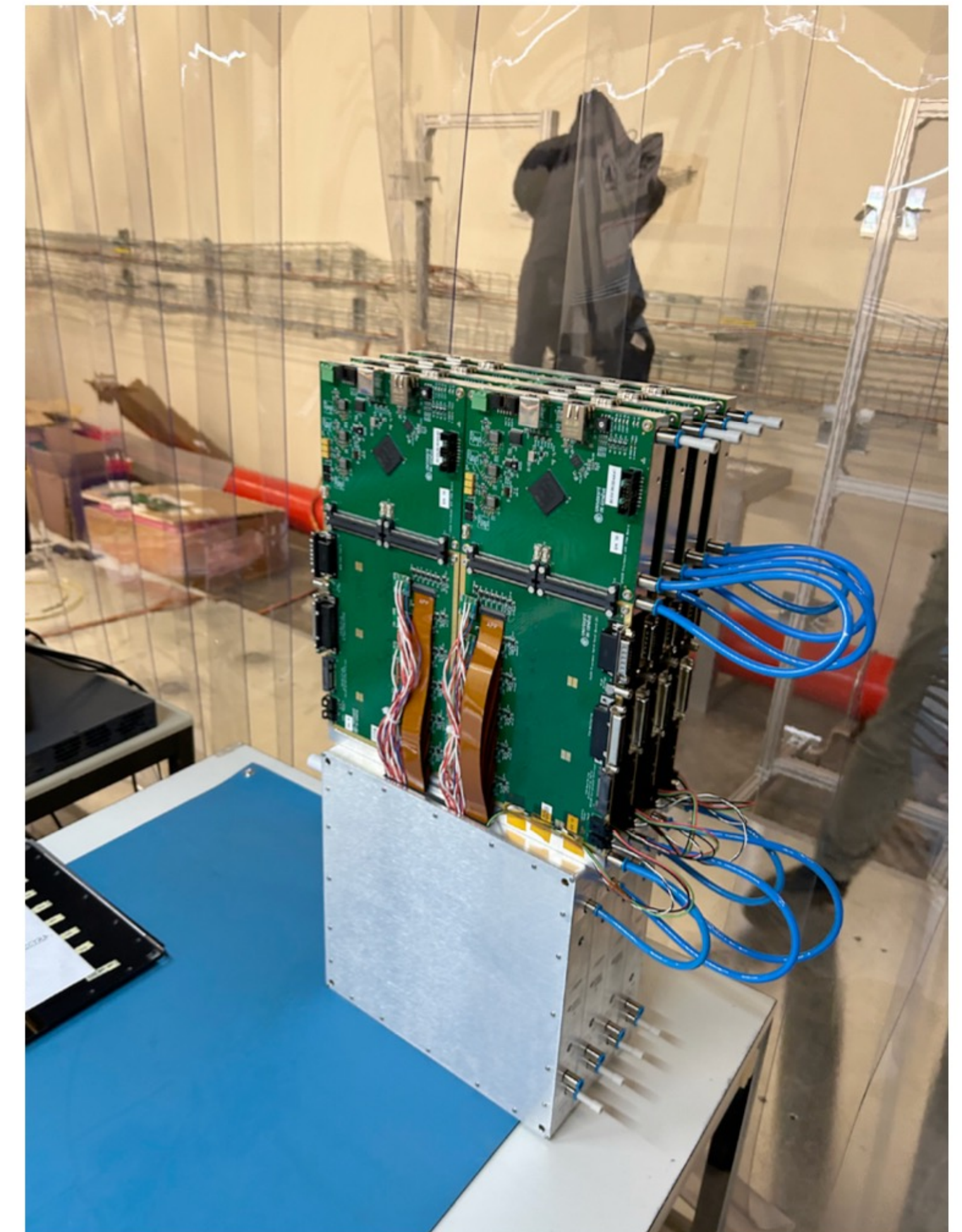
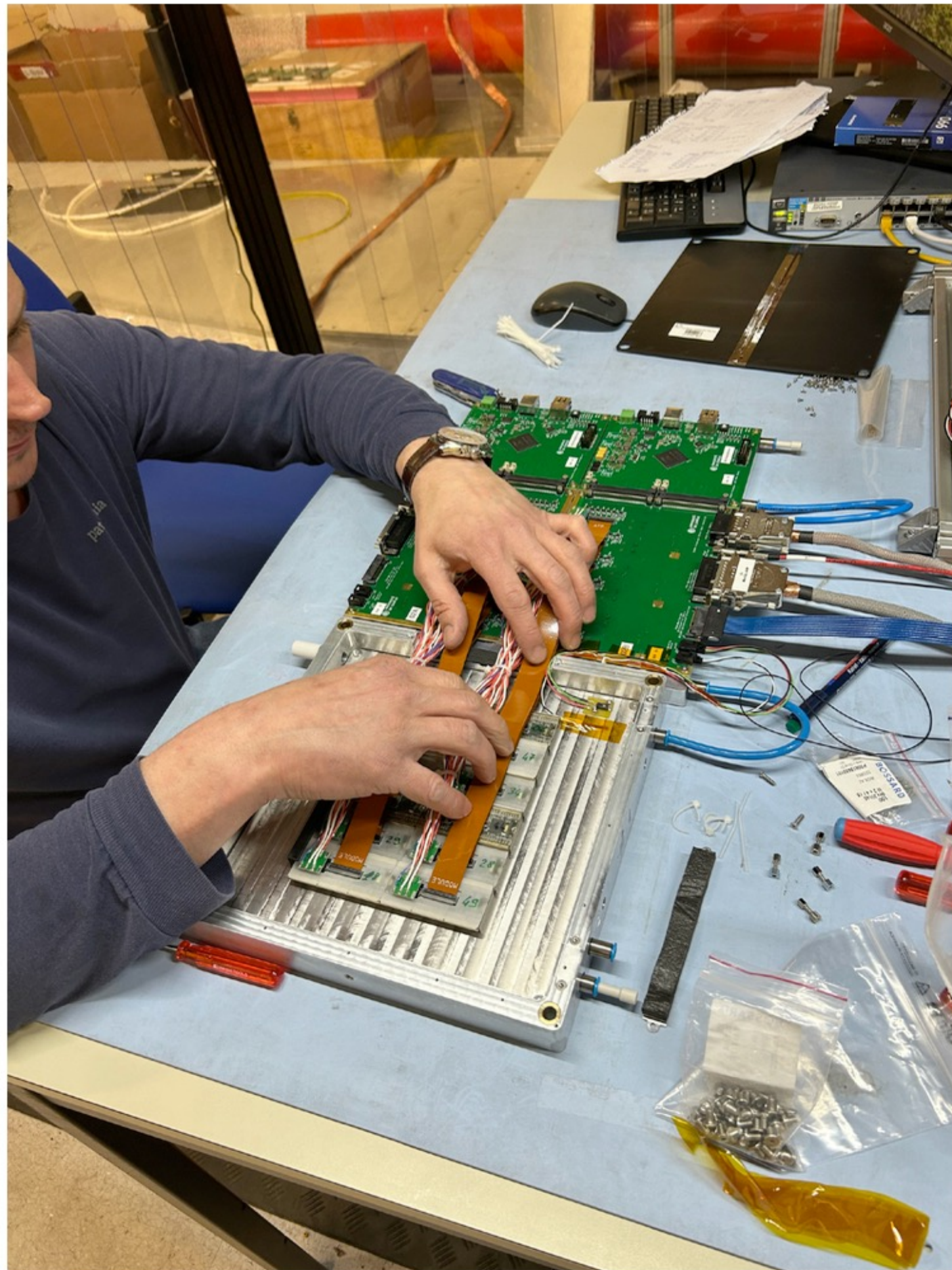
↳ discarded / left
for future tests

*showers are narrower,
not all photon converted yet*

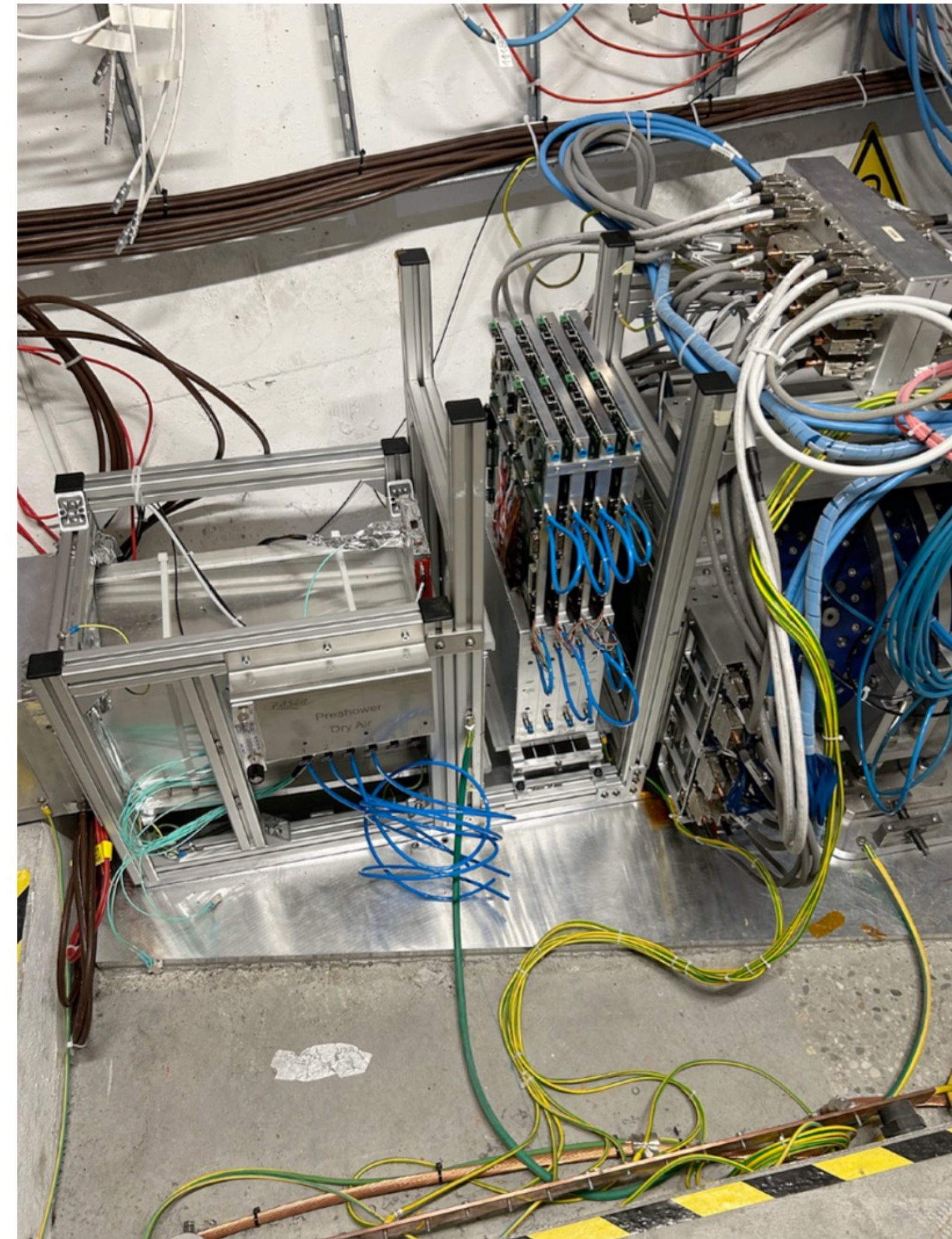
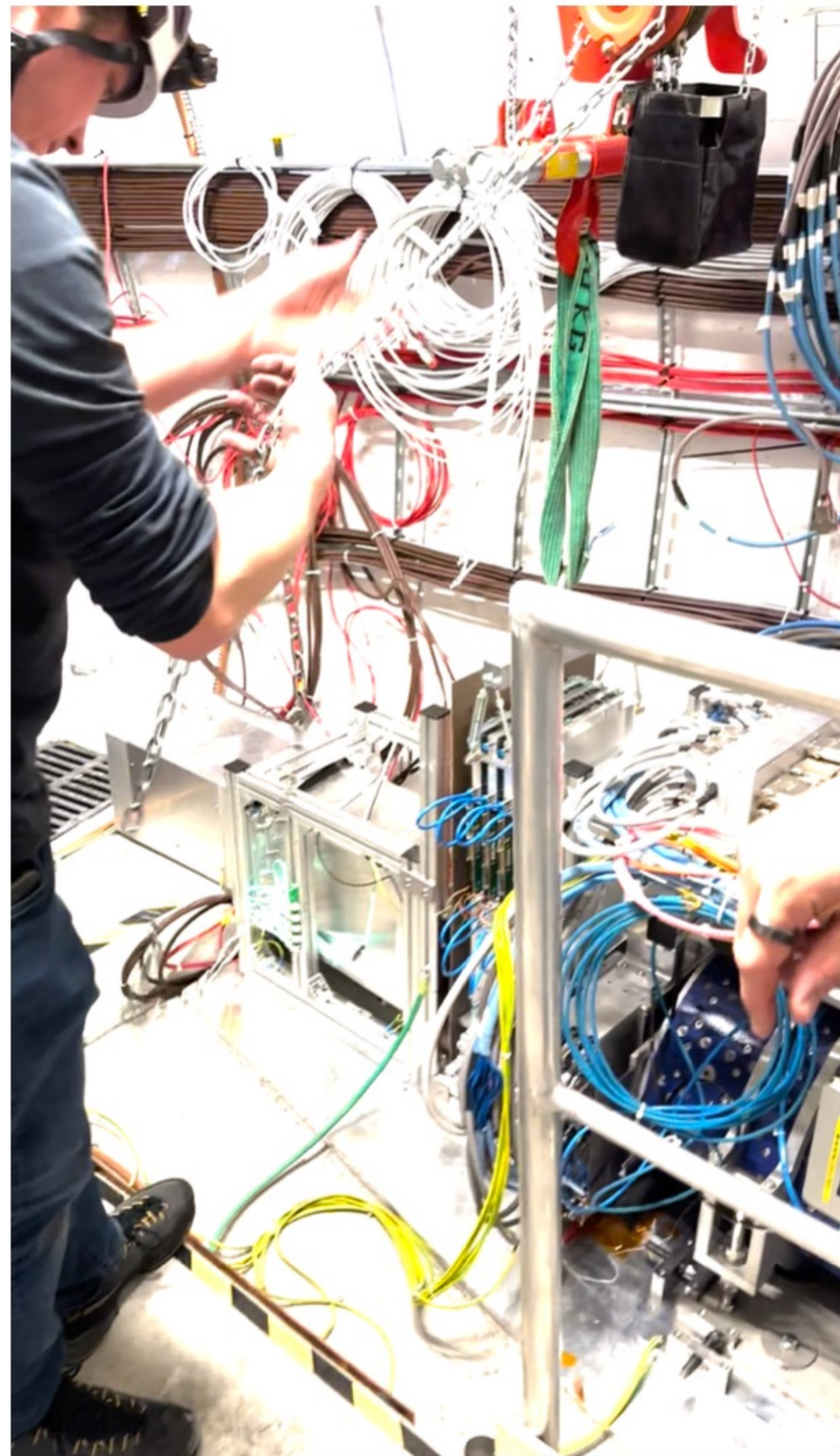
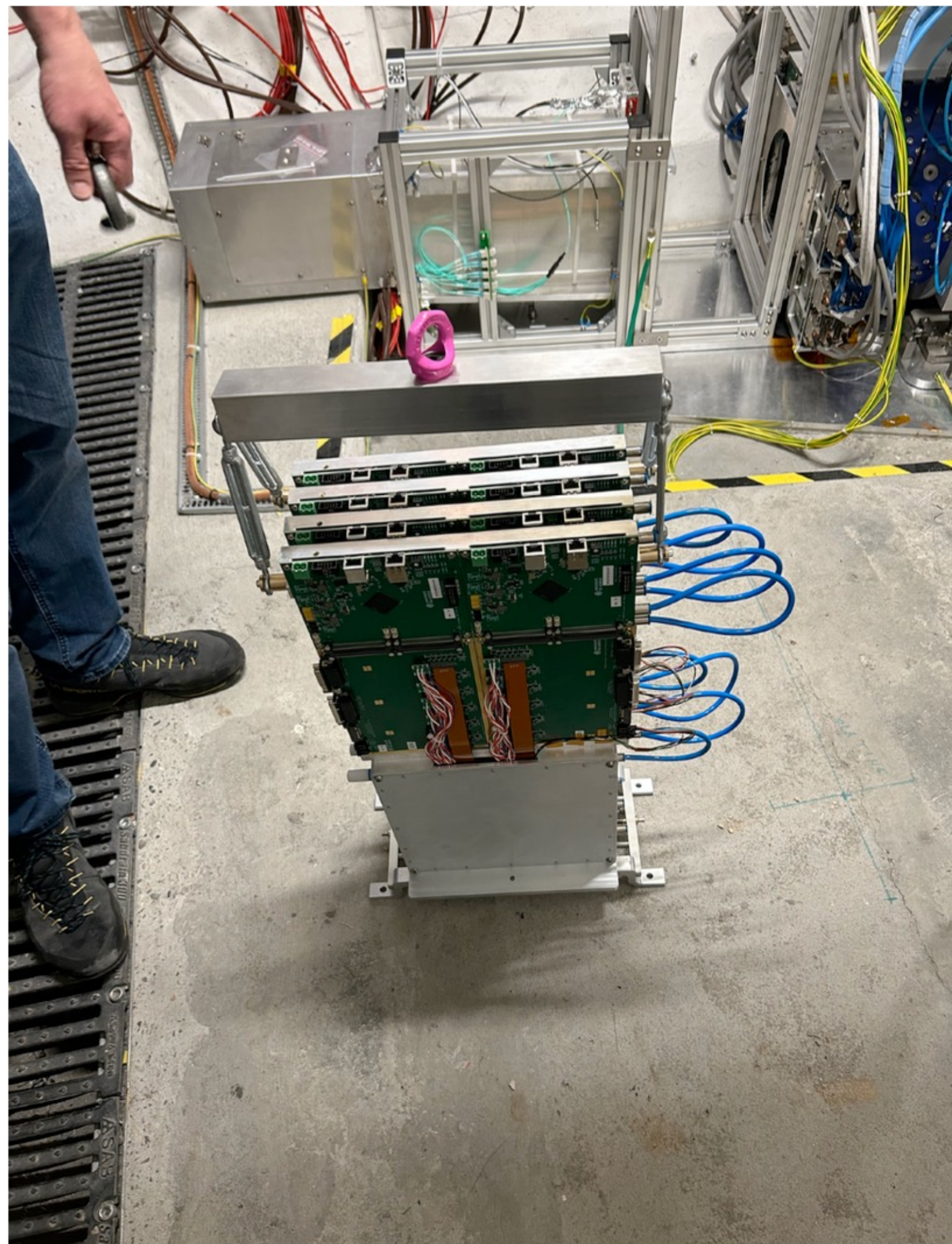
incoming ALPs



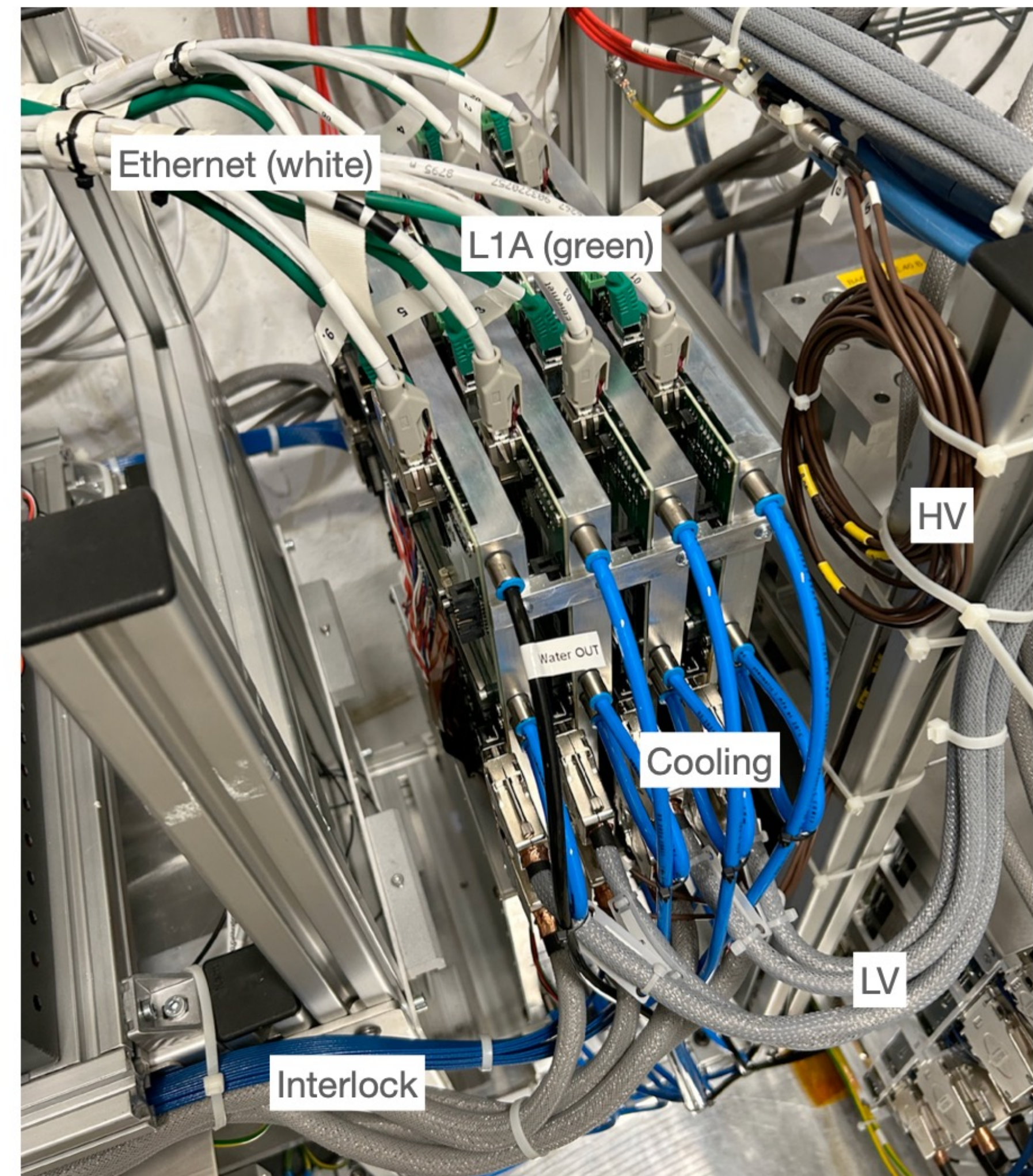
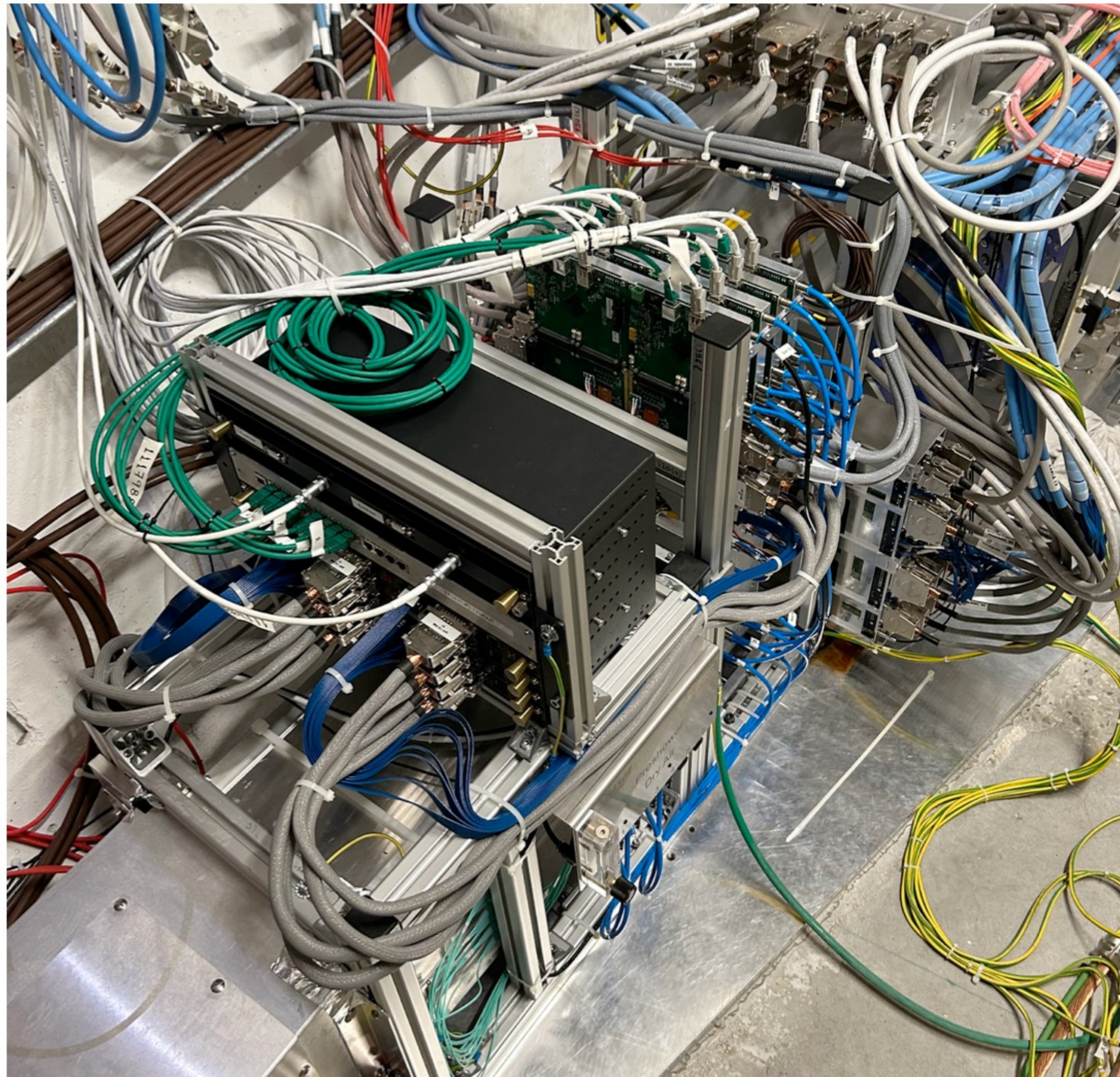
Assembly of planes at EHN1 (the FASER lab)



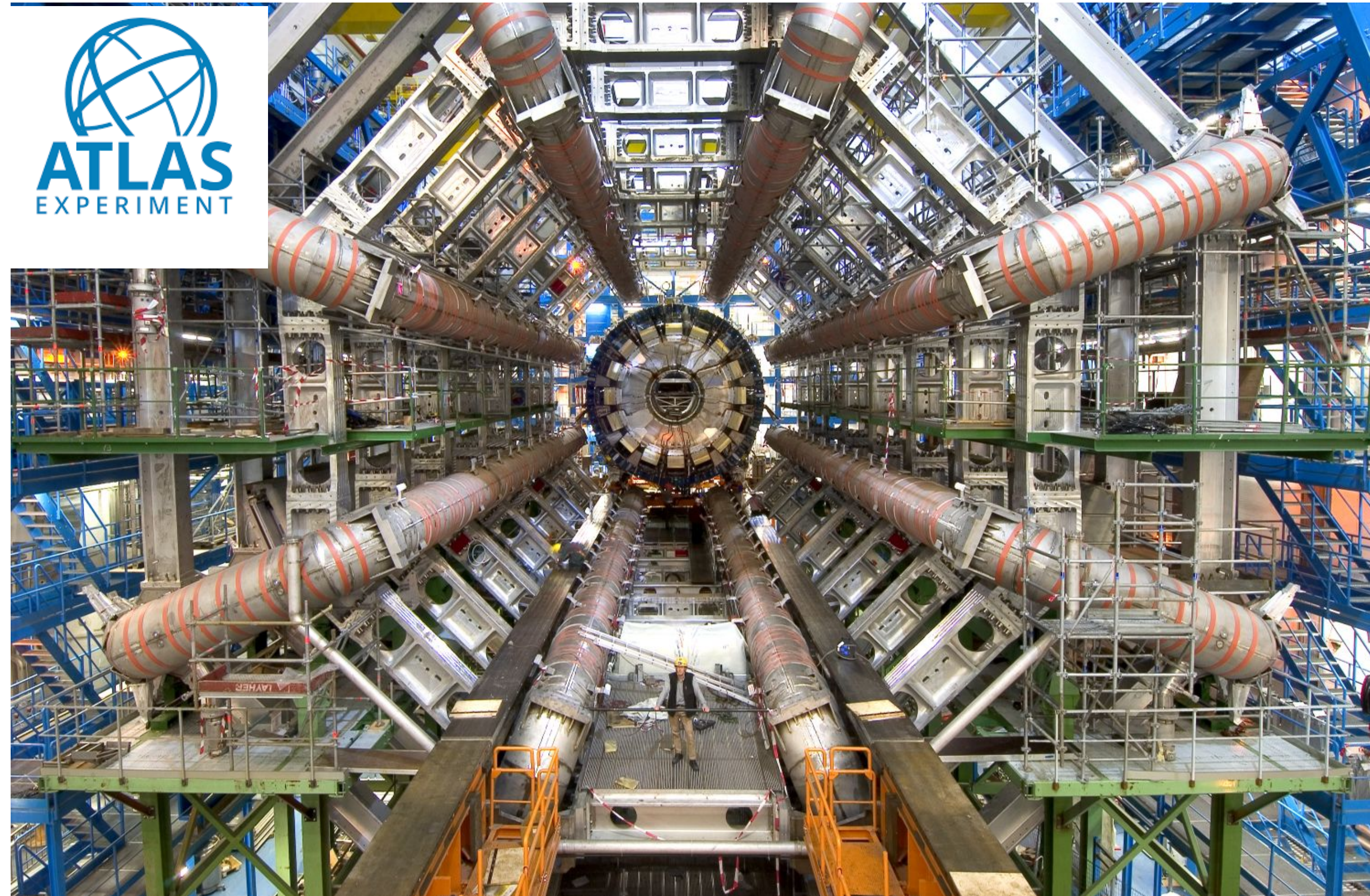
Installation at TI12



Installation at TI12



ATLAS ITk experience



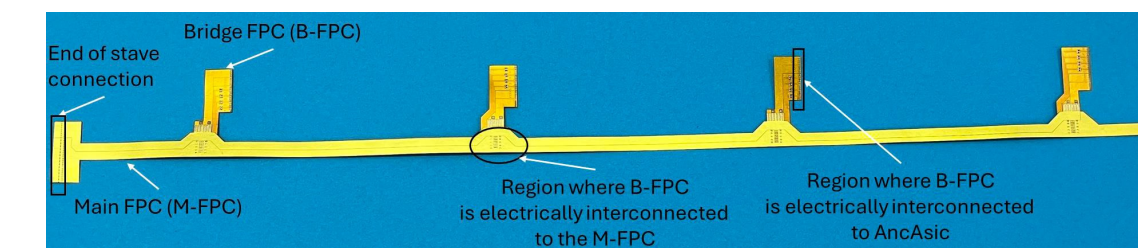
Potential FPC idea

Potential OB/Disk FPC ideas

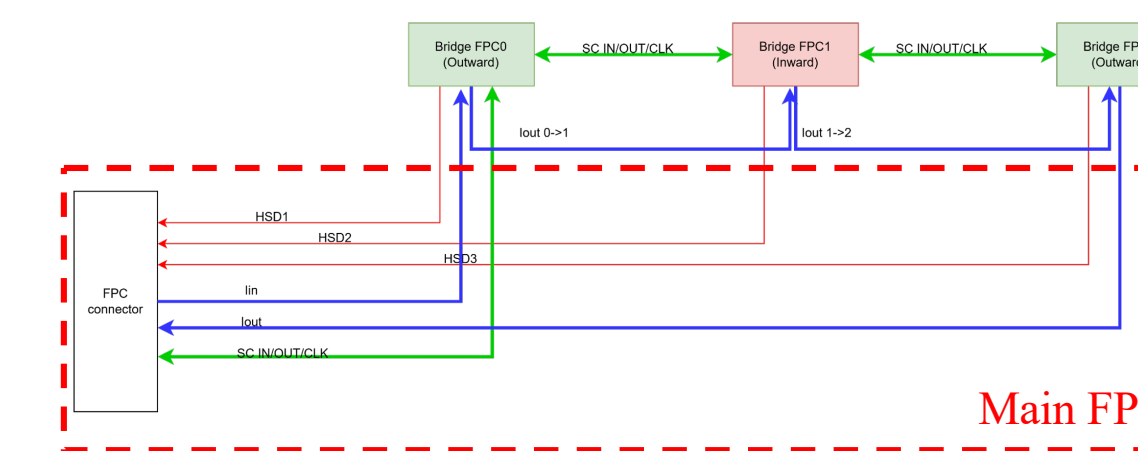
- Investigating an (nearly) available FPCs
 - Communicating with colleagues in BelleII
 - Study Aluminum FPCs for Low-Material-Budget
 - Want to have a prototype within a-year timescale
- Progress in Aluminum Via Metallization
 - Combined PVD and copper electroplating: successful through-hole metallization
 - Fully wet plating: zincate pretreatment and Ni/Cu metallization
- Hybrid Al/Cu Flex study is also ongoing
 - Copper signal layers and aluminum power layers
 - Ultrasonic Al–Cu bonding through polyimide
 - +10 % material budget from only Al case

Low-mass Al Flexible Printed Circuits for OB/Disks

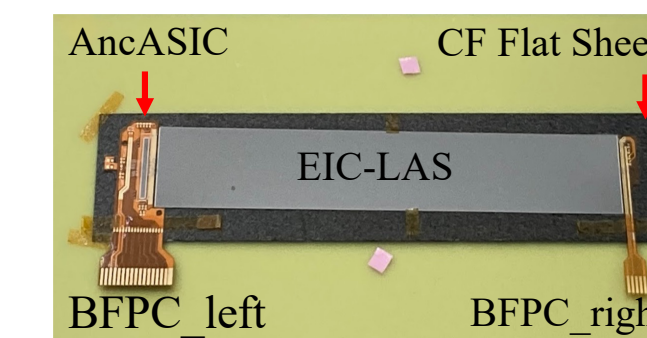
Prototype FPCs produced by LTU for OB



- OB and disks: 1) bridge FPCs connect to the EIC-LAS endcaps; 2) main FPC connects multiple sets of bridge FPCs.
- Challenges: Al for low mass; high-speed (5.12/10.24 Gbps) transmission over 40 cm distance.



Disk Module

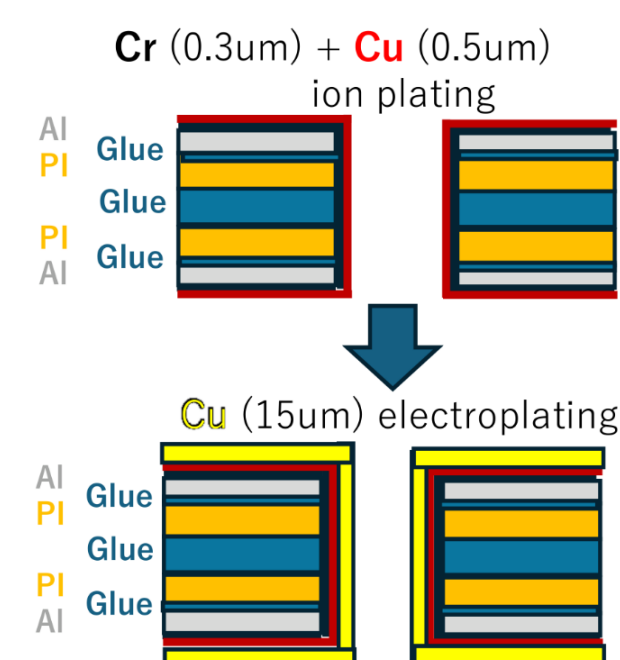


Disk Main FPC by JLC ~40 cm

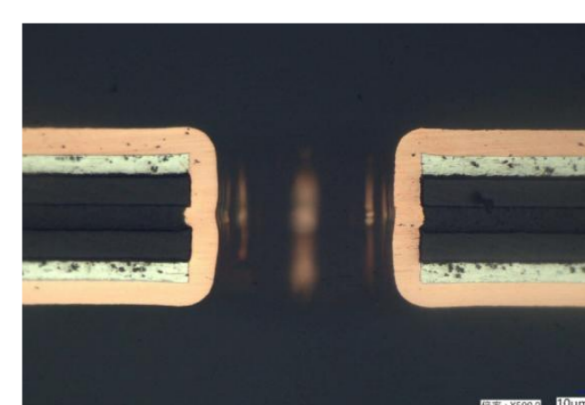
Zhenyu's slide for PIXEL 2026 [\[link\]](#)

Photos and plots from Y. Onuki [\[link\]](#)

1 Combined PVD and electroplating



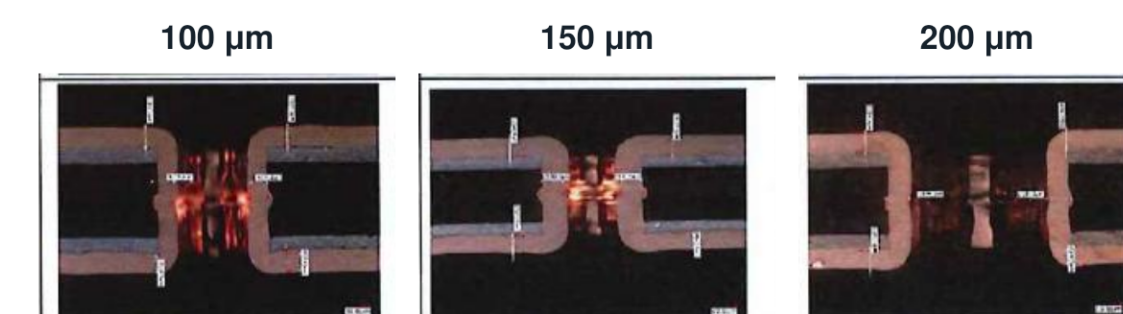
0.2 mm via cross-section



- CERN/ATLAS IBL reference process
- Via metallization demonstrated in Japan
- High PVD cost, limited economies of scale

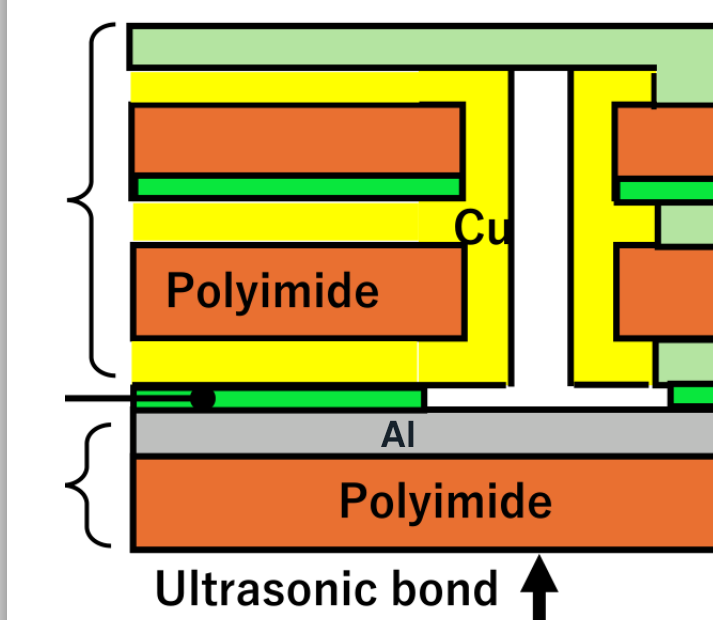
2 Fully wet plating

Via cross-sections

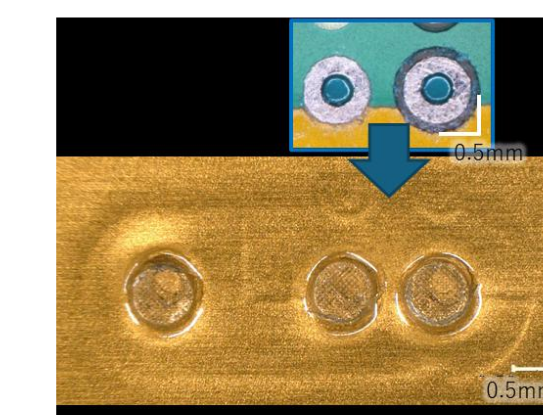


- Zincate pretreatment, electroless Ni/Cu, then copper electroplating
- Beaker-scale demonstration, with potential for lower production cost
- Next: circuit etching and multilayer process integration

3 Ultrasonic Al–Cu bonding



Prototype Al–Cu joints



- Cu signal routing with Al power/ground
- Initial Al–Cu connections demonstrated
- Next: thermal-shock tests and production setup

Summary and Prospects

Lessons Learned for from ATLAS/FASER QA/QC

- **Design QA/QC together with production.**
 - Keep manufacturing, testing, and troubleshooting closely connected.
- **Build resilience into the workflow.**
 - Minimize critical dependencies on external components, services, and transport.
- **Agree on common acceptance criteria early**
 - Coordinate test procedures across sites to ensure comparable results and reduce duplicated development.
- **Validate local optimizations with data**
 - Even small differences in procedures or standards can require substantial effort to justify.
- **Use pilot production to support decisions**
 - Demonstrate repeatability and throughput, and let decision-makers see practical constraints firsthand.
- **Build close partnerships with industry**
 - Stable quality depends on technical expertise, continuous feedback, and sustained cooperation.



Backup