

AncASIC Test - Updates

Shirsendu Nanda (LBNL)

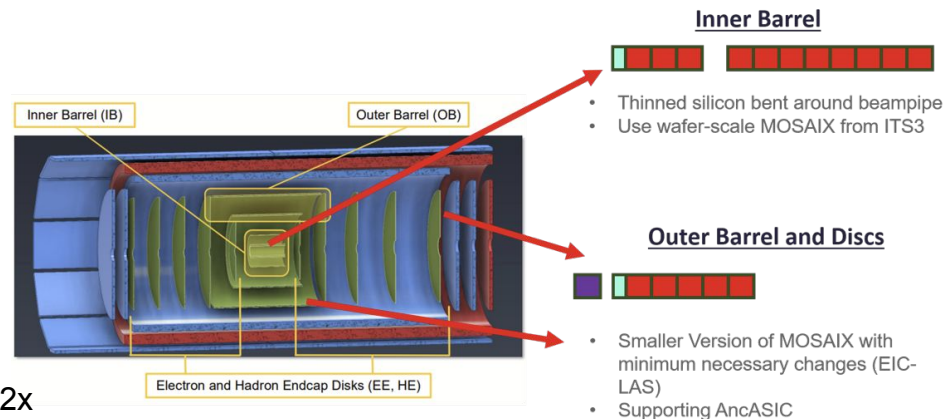
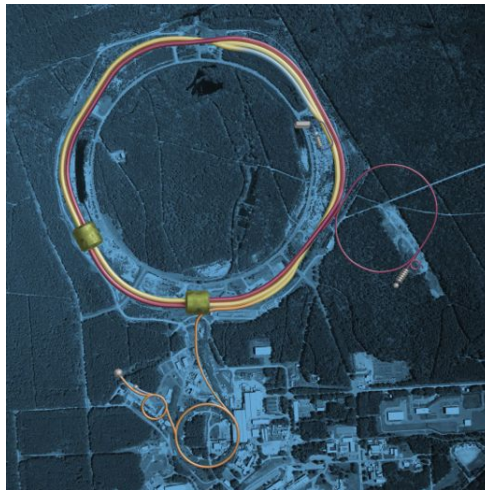
SVT Working Meeting (8 - 9 October, 2026)

*Thanks to the BNL design team, Amanda Krieger at LBL for useful suggestions/discussions and the UK team for the MPW2 design and test results

Introduction

EIC, ePIC and MOSAIX

- EIC is currently under construction at BNL
 - First beams expected ~ 2037
 - Detector is called the electron Proton Ion Collider (ePIC). Inner tracker is called the Silicon Vertex Tracker (SVT).
 - SVT plans to use **MOSAIX for IB**, and **EIC-Large Area Sensor for OB and Disks**. **EIC-LAS** will be modified from **MOSAIX**:
- Reduce number of RSUs from **12** to **5-6**
- Reduce number of high-speed data links from **8** to **1**
- Reduce the clock frequency and high-speed data rate by $\geq 2\times$



AncASIC Overview

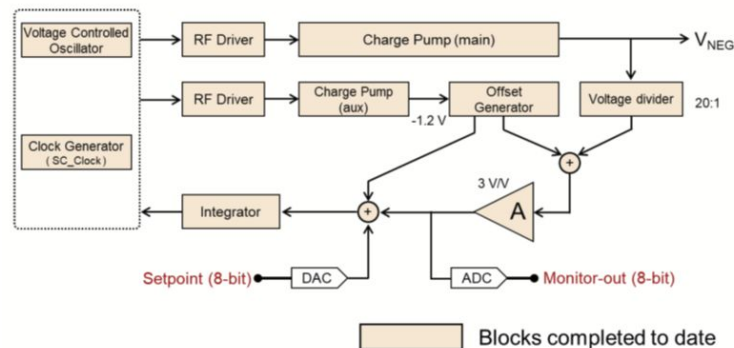
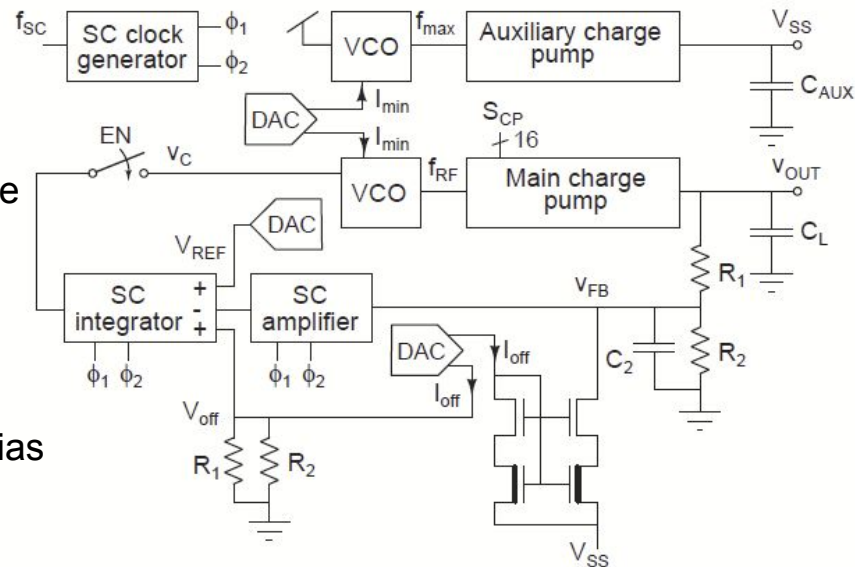
- [illegible]

DOI:[10.1109/MWSCAS53549.2025.11244383](https://doi.org/10.1109/MWSCAS53549.2025.11244383)

- Dickson charge pump for on-chip negative-voltage generation
- Clock-driven switched-capacitor architecture
- Programmable negative output for sensor back-bias

Programmable control parameters

Parameter	Description
linteg	bias current for the SC integrator
lvco	bias current for the VCO
loff	bias current for the offset generator
EN_{CP}	enable branches of the main charge pump and RF driver
EN<2>	selects VCO control voltage (V_c) - 0 = external control voltage - 1 = output of the SC integrator
EN<1>	Enable RF clock for main charge pump
EN<0>	Enable RF clock for aux. charge pump



MPW1: NVBG

Specifications

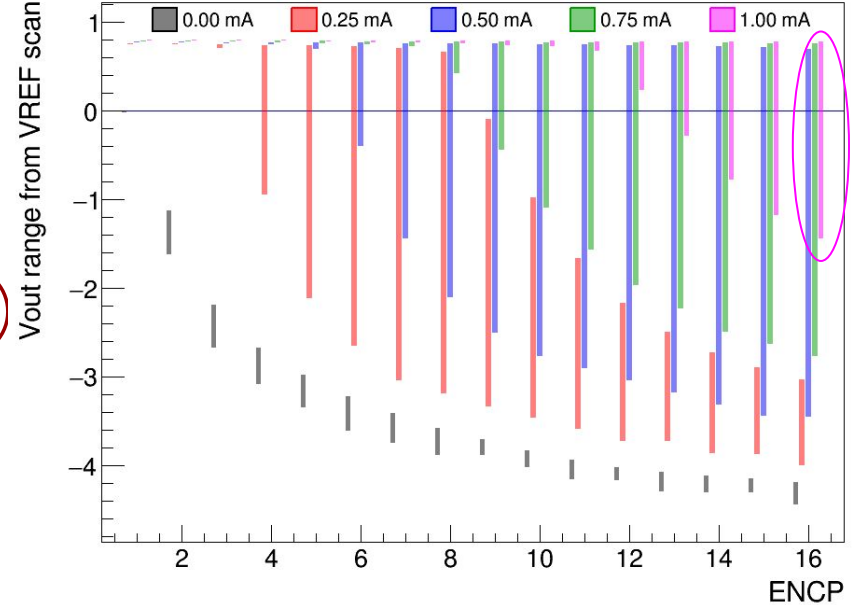
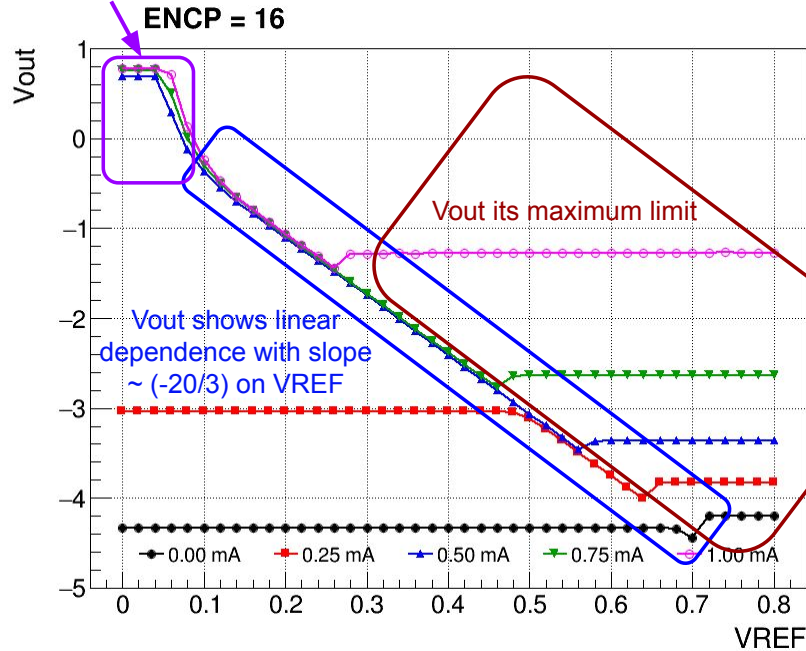
- Specifications driven by the EIC-LAS back-bias requirements.
- Wide programmable negative-voltage range to accommodate different sensor operating conditions
- Parallel charge-pump architecture to scale the available output current
- Designed for low-ripple, low-power operation to minimize impact on sensor performance

Parameter	Value reported in the draft
Supply	1.2 V $\pm$ 10% (provided by 1 st SLDO)
Output range	<-1 up to -5 V relative to local ground
Reference DAC	8 bit for V_{ref}
Output-current capability	$\approx$ 1 mA / section (6 sections: 1 Main + 5 Auxiliary) ; $\approx$ 200 μ A nominal reference load/section
Output ripple	<0.15 mV; simulated
Power consumption	<15 mW; $\approx$ 11 mW at -1.5 V
Main charge pump	16 selectable parallel branches / section

MPW1: NVBG

VOUT - VREF dependence and VOUT range

Vout becomes positive and clamped to $< \sim 1$ V by ESD diodes

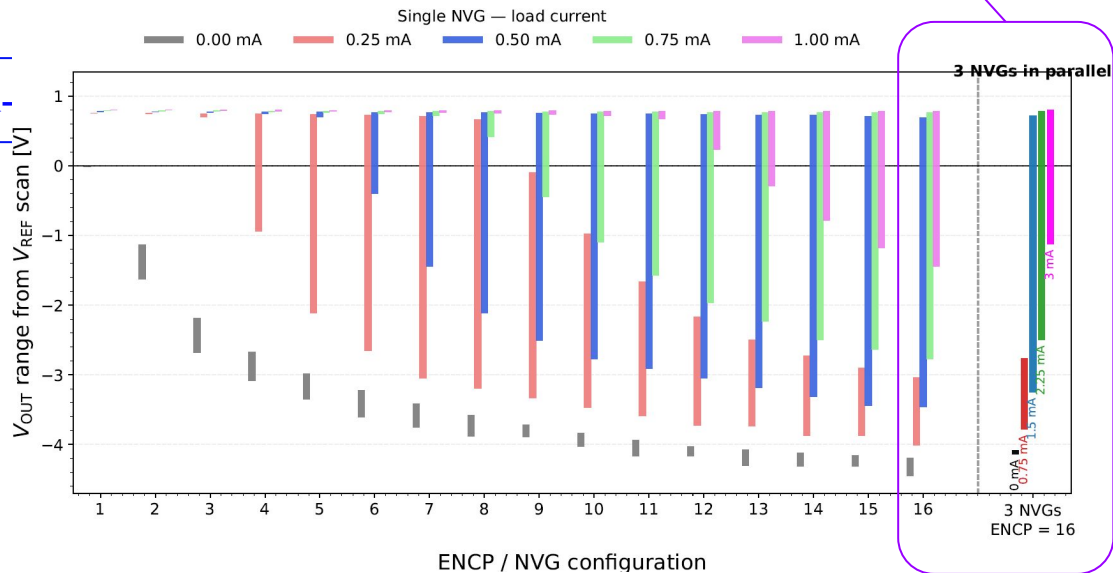
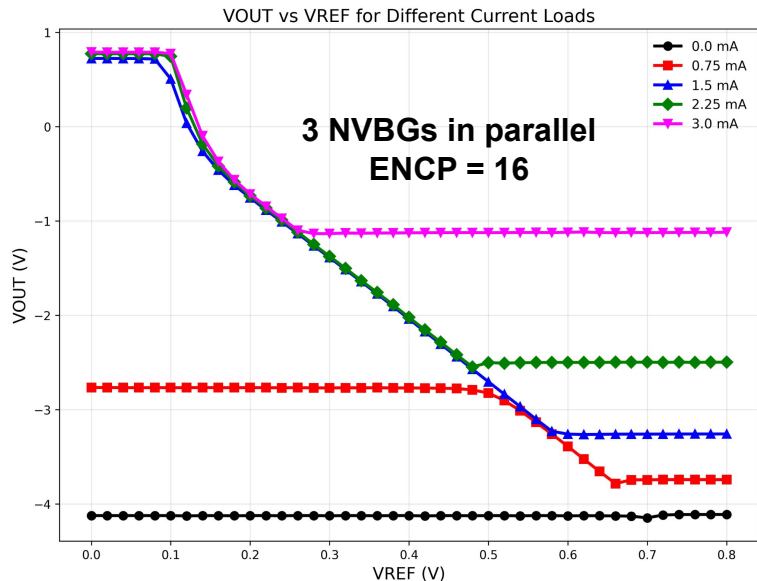


- Vout range from V_{REF} (0 - 0.8V) scan for each ENCP (different load currents)
- With 1 mA current load, for highest ENCP, Vout reach ~ -1.5 V

MPW1: NVBG

VOUT - VREF dependence and VOUT range

1 Closed-loop and 2 opened loop NVGs in parallel

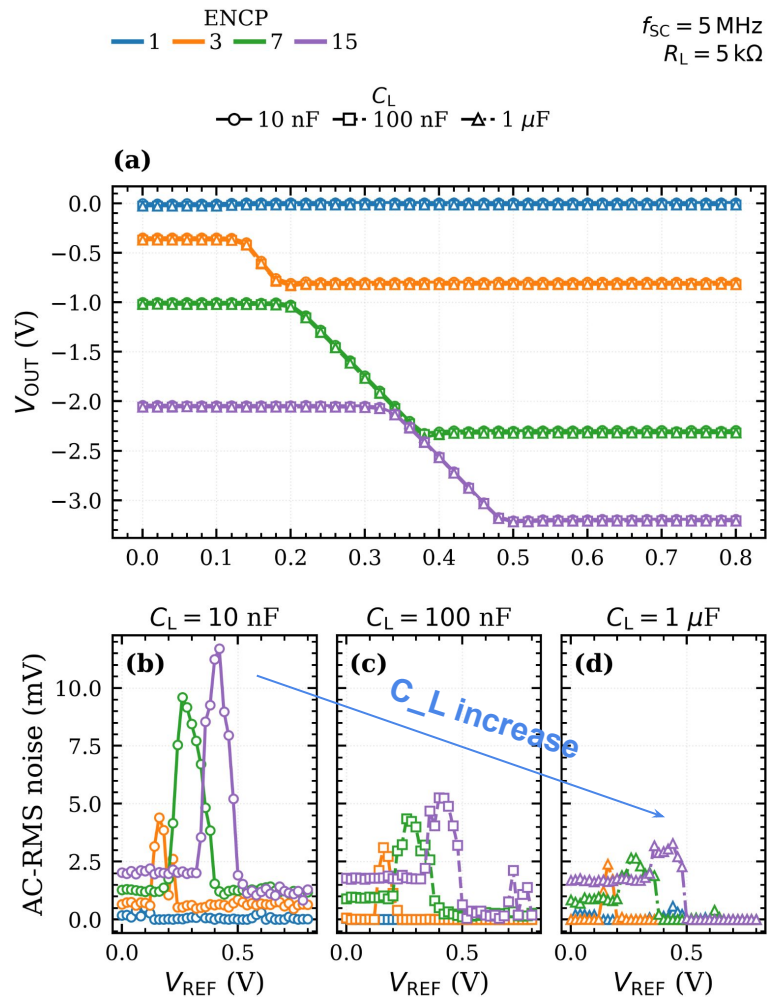
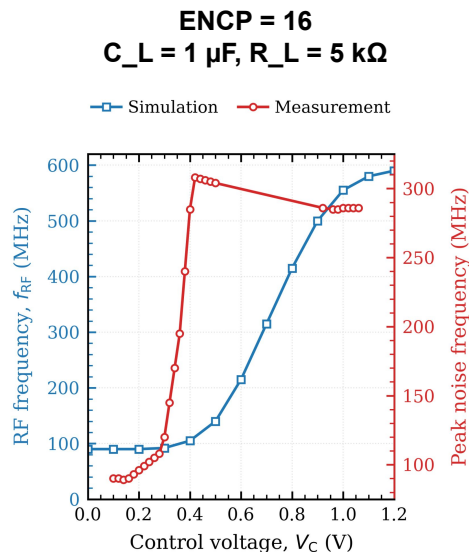


- Parallel operation of three NVBGs extends the load-current capability by 3X while maintaining a VOUT range comparable to a single NVBG
- 6 NVBGs in parallel are implemented in the new chip submission to support up to ~6 mA of load current ⁷

MPW1: NVBG

Noise

- V_{OUT} independent of C_L but varies with ENCP
- NVBG Noise ENCP and C_L dependent
- $\sim 2\text{-}3\text{ mV}$ for $C_L = 1\text{ }\mu\text{F}$
- Peak noise frequency follows the simulated trend, reaching $\sim 300\text{ MHz}$ in measurements
- Confirms the on-chip VCO as the dominant NVG noise source



MPW1: NVBG + babyMOSS

NVBG and babyMOSS Integration Testing

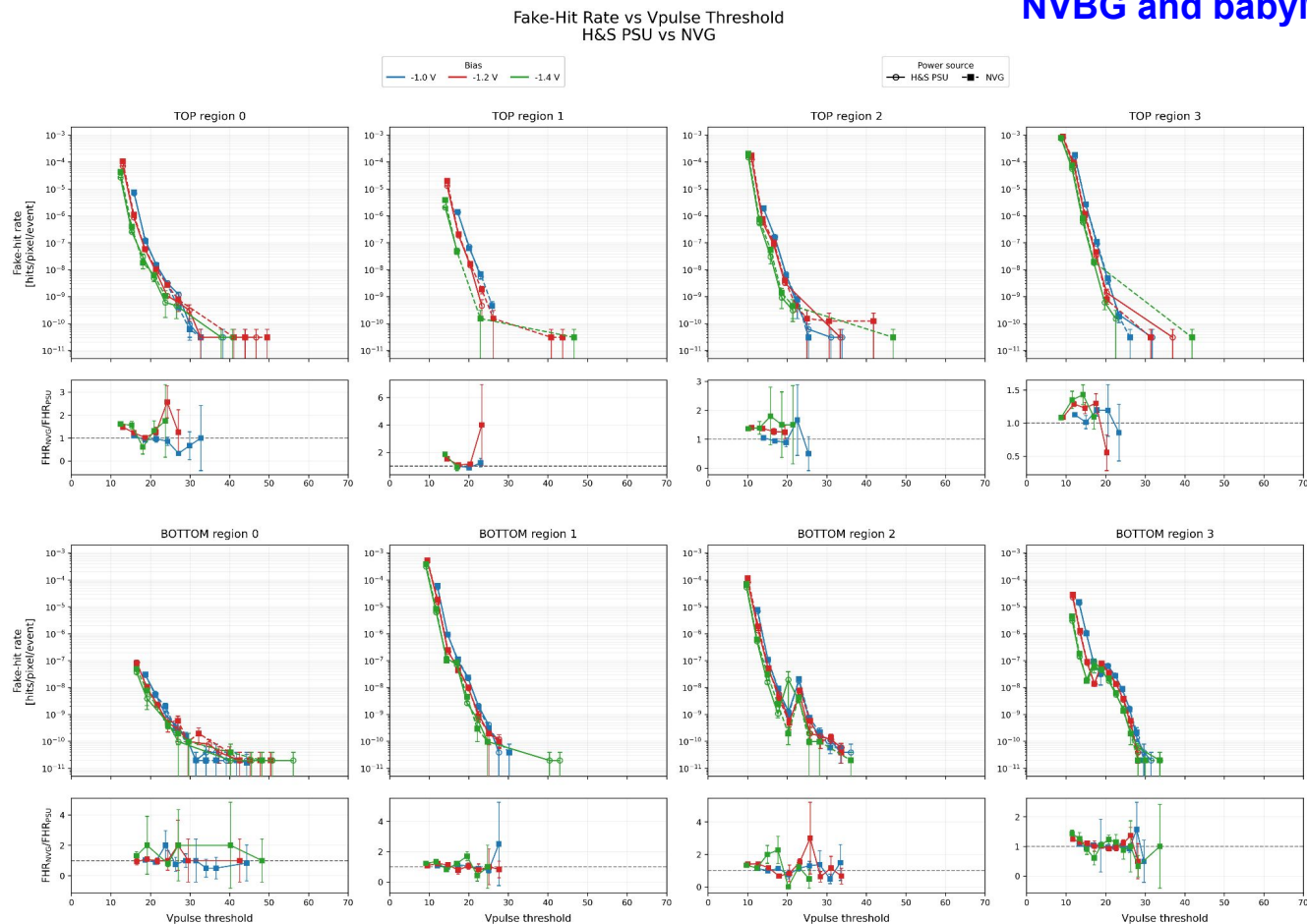
First babyMOSS operation with on-chip negative bias generation



- Compared the fake hit rate (FHR) of babyMOSS using the **R&S HMP4040** and **NVG** power supplies.
- Measurements performed at a stable 20°C in an environmental chamber to minimize temperature effects on FHR.
- FHR measured for three bias voltages (-1.0 , -1.2 , and -1.4 V)
- FHR also measured for different capacitive loads at the Vout node

MPW1: NVBG + babyMOSS

NVBG and babyMOSS Integration Testing

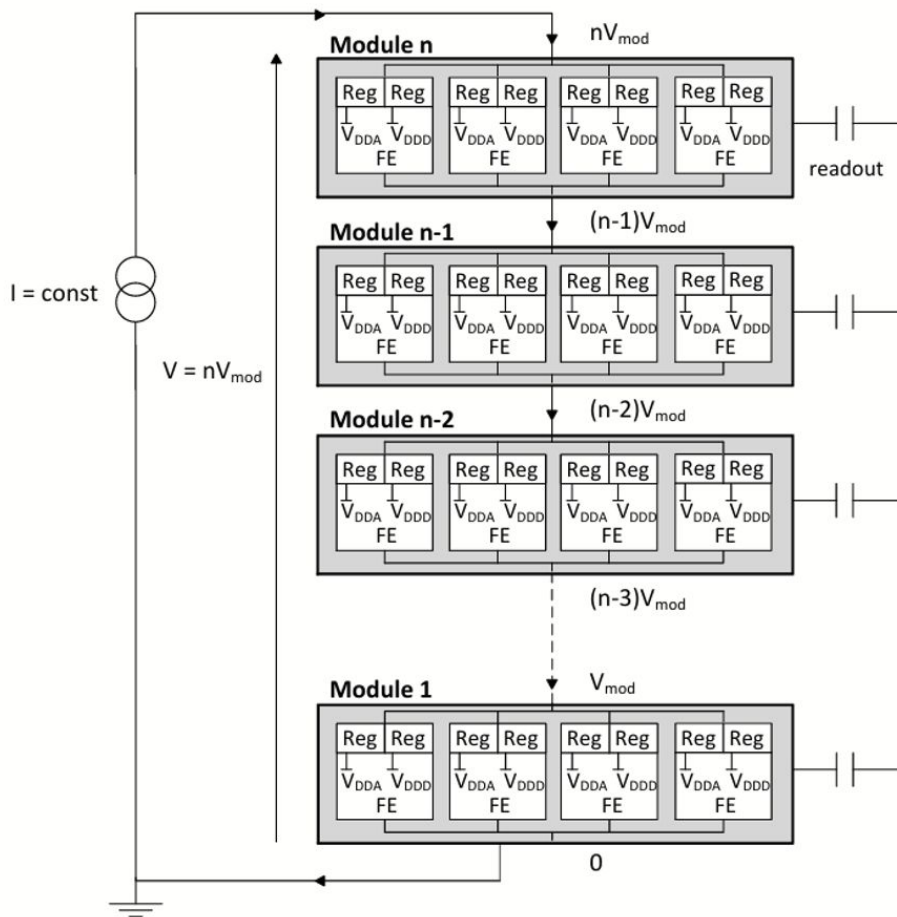


- Fake hit rate (FHR) plotted as a function of Vpulse thresholds for different bias voltages.
- FHR measured with the NVG is in good agreement with that obtained using the R&S HMP4040

MPW2: SLDO

Serial Powering

- Goal is to reduce cable requirements but routing a single current through multiple serial regulators
- Requires a circuit that:
 - Can shunt current to the next stage
 - Can regulate the output voltage
 - Can be paralised in case of multiple supplies i.e. has a resistive characteristic



MPW2: SLDO

Circuit Overview

- Overcurrent protection – triggers when shunt current drops below 10mA
- Tri-state output can also be used for power sequencing
- Also DAC to control output voltage

LDO Loop:

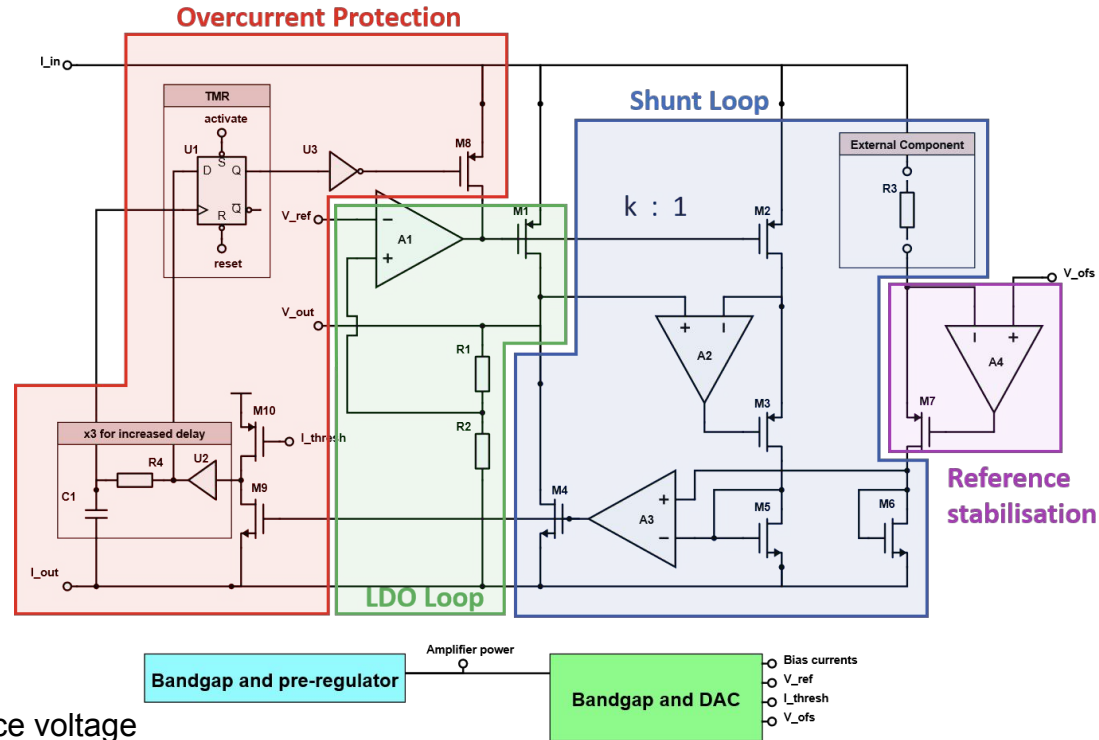
→ Regulates and stabilizes the output voltage

Shunt Loop and reference stabilization:

→ Maintains stable shunt operation and reference voltage

Overcurrent protection:

→ Protects against excessive load current



$$I_{in} = k \frac{V_{in} - V_{offset}}{R3}$$

$$R_{eq} \approx \frac{R3}{k}$$

MPW2: SLDO

Specifications

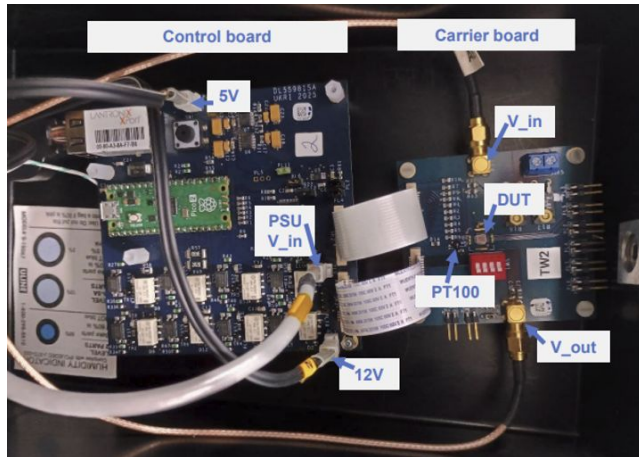
- Current specifications driven by expected EIC-LAS consumption based on published MOSAIX data
- Temperature range significantly exceeds expected ePIC temperatures
- SLDO to cover the large current range. Area inefficient, some performance degradation

Specification	Unit	Value
Temperature	Degrees Celsius	-20 to 105
Voltage Range	V	1.0 – 1.4
Current capacity	mA	0.04 - 900
Load Capacitance	F	10n – 10u
Shunt current overhead	%	10
Shunt power	% of load power	<35
Total Ionising Dose	Rad	< 1M
Neutron Flux	n_{eq}/cm^2	10e12
Additional features		• Tri-state output • Over-current protection

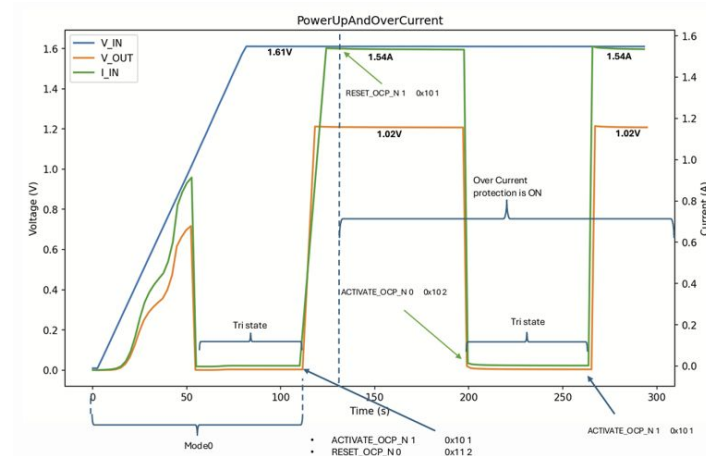
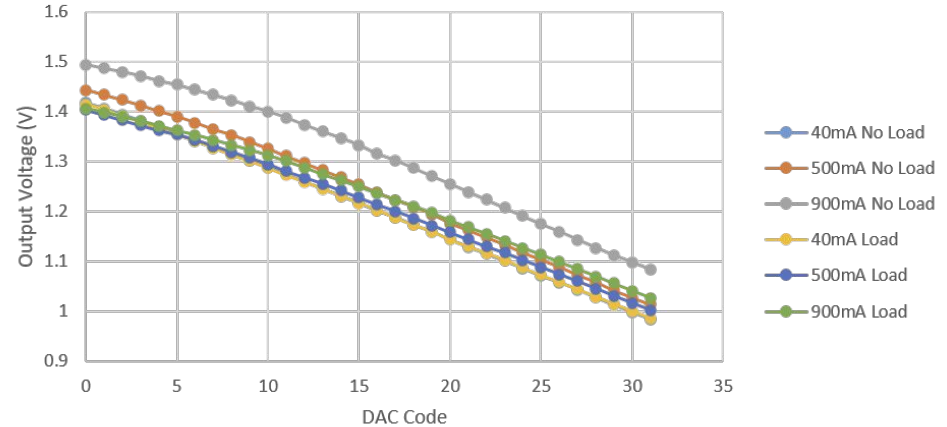
MPW2: SLDO

Device Testing

- Fully functional over full range of load currents and shunt conditions. -20 and 27 degrees, all load caps.
- Tri-state output functional



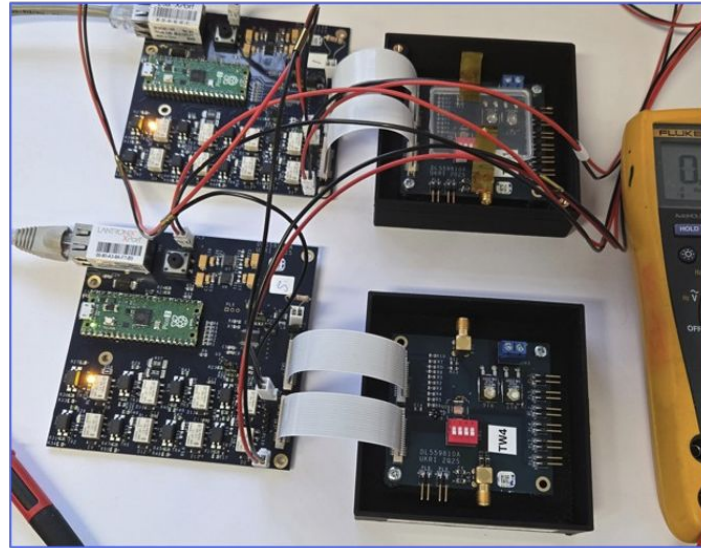
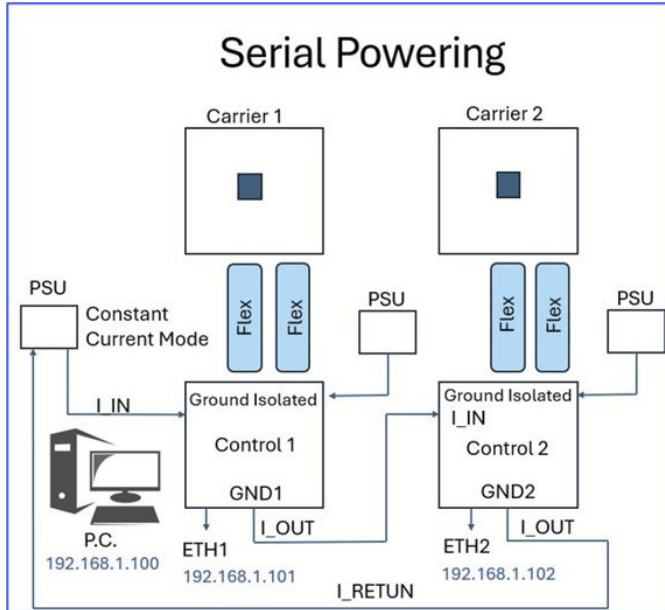
Output Voltage vs. DAC Code for 3 Maximum Current Conditions With Full Load Applied and Zero Load Applied



MPW2: SLDO

Serial Powering Chain Testing

First serial powering chain constructed



PSU V_OUT 3.2V 0.06A CC Mode
Board 1 V_IN = 1.556V
Board 2 V_IN = 1.641V
Overall V_Drop = 0.003V

No Load test:-

Board 1 Dac set to 0 $\therefore$ V_out = 1.416V
Board 2 Dac set to 0 $\therefore$ V_out = 1.479V
PSU V_out = 3.2V 0.06A CC Mode

Board 1 Dac set to 31 $\therefore$ V_out = 0.984V
Board 2 Dac set to 31 $\therefore$ V_out = 1.055V
PSU V_out = 3.2V 0.06A CC Mode

With Load test:-

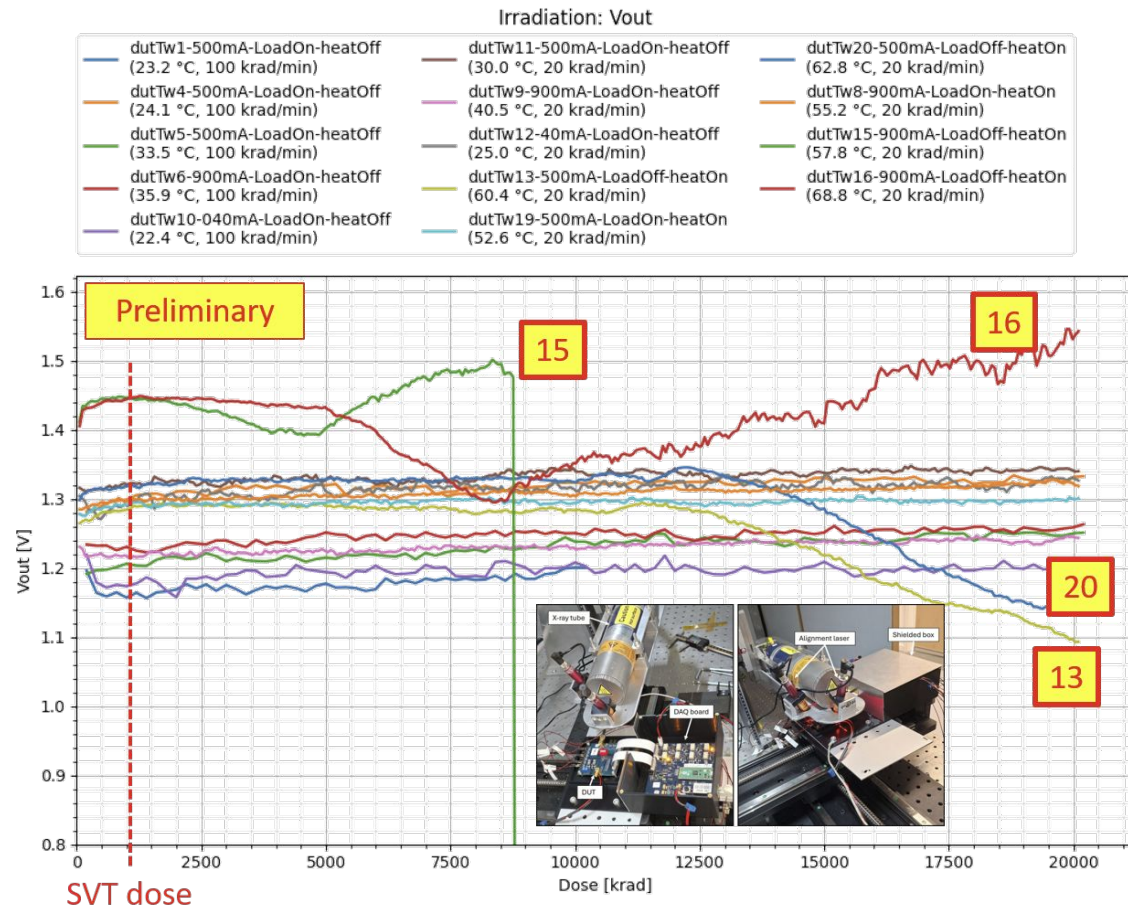
Board 1 Dac set to 0 $\therefore$ V_out = 1.414V
Board 2 Dac set to 0 $\therefore$ V_out = 1.478V
PSU V_out = 3.2V 0.06A CC Mode

Board 1 Dac set to 31 $\therefore$ V_out = 0.985 V
Board 2 Dac set to 31 $\therefore$ V_out = 1.058V
PSU V_out = 3.2V 0.06A CC Mode

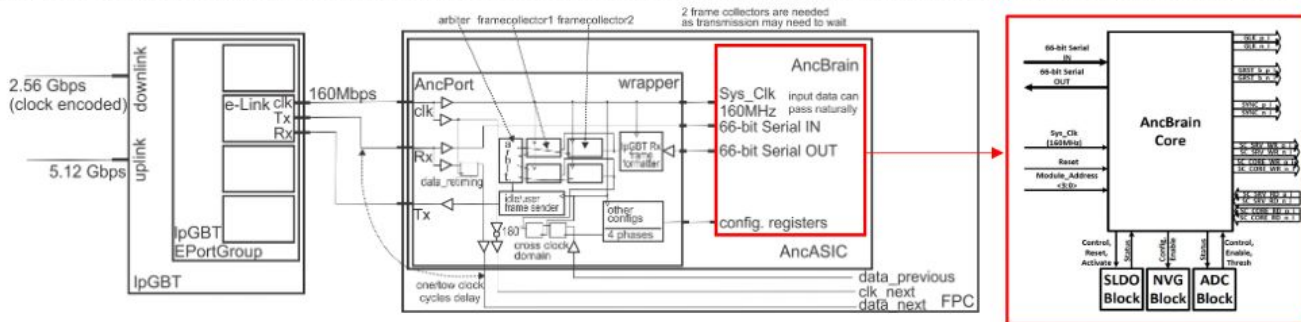
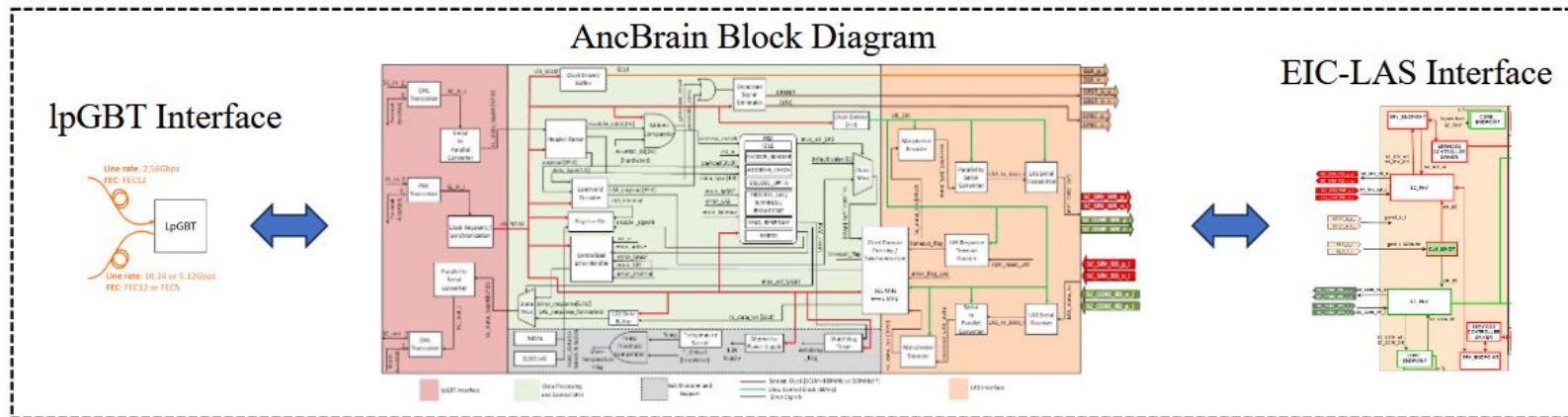
MPW2: SLDO

TID Testing

- Irradiated multiple devices up to 20 MRad (EIC expected dose <1 MRad)
- Irradiated under multiple conditions
- High heat, high current with all current shunted shows some failure conditions at multi-Mrad doses
- 4 chips: 13, 15, 16, 20, but in any case, all meet EIC dose



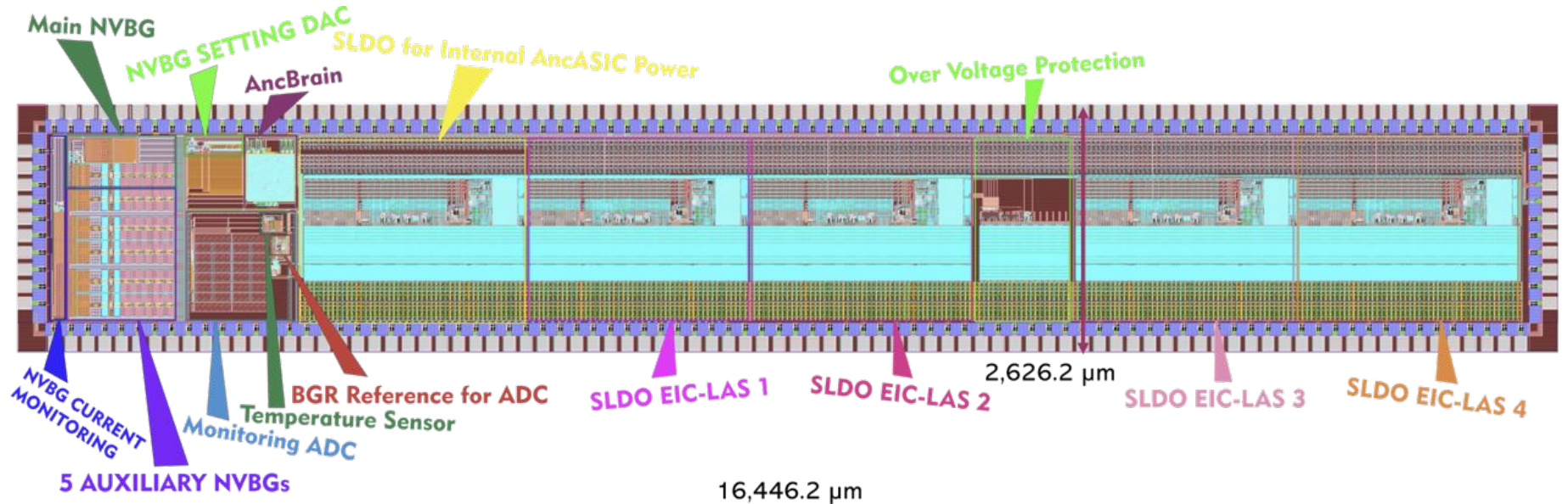
AncBrain for Slow Control



AncBrain is designed to control and monitor the NVBG and SLDOs in the AncASIC, and to provide a slow control hub for the EIC-LAS

MPW3: NVBG + Shunt-LDO + AncBrain for Slow Control

- MPW3 submission in September 2026; expected delivery mid-February 2027
- 5 SLDOs are included in the AncASIC MPW3 submission
- 6 NVBG design to increase the supply current limit to 6mA@-1.2V is included in AncASIC MPW3
- AncBrain is included in the AncASIC MPW3



Summary and Future Work

Summary

- Presented results for Negative Voltage Bias Generator and Shunt-LDO in a 110nm SOI process
- The functions and characteristics of the NVBG have been extensively tested, and the test results match close to the design expectation.
- A SLDO was included in MPW2 submission and underwent extensive tests, e.g. temperature and total irradiation dose measurements.
- MPW3 submitted in September 2026, expected to delivery mid-February 2027

Future Work

- Starting preparation for characterization for MPW3

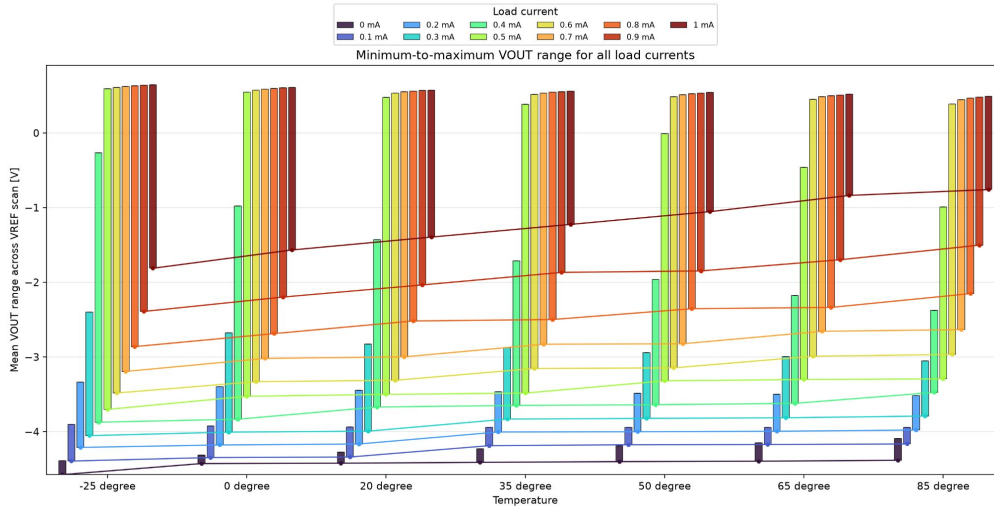
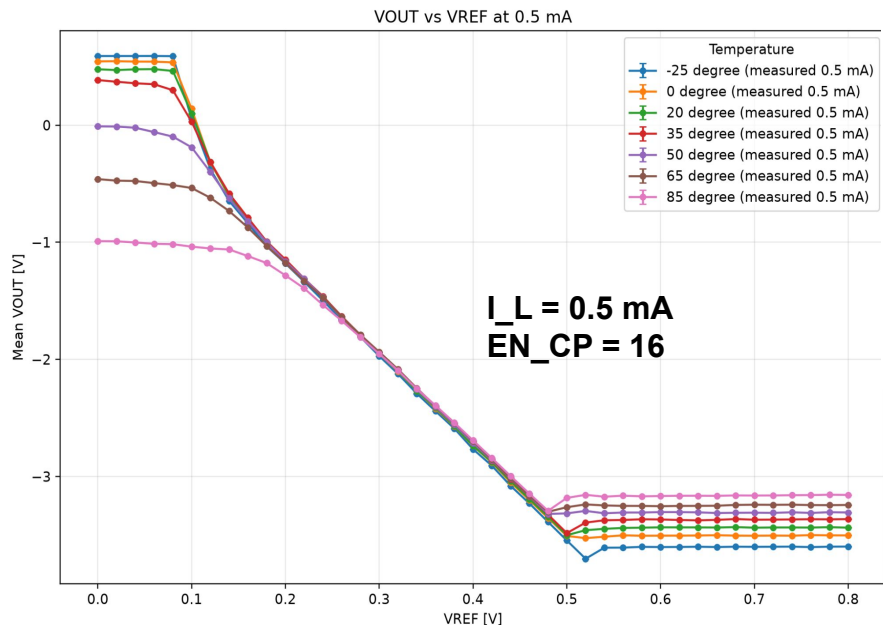
Extra slides

I2C Configuration: EN_CP = 16
 EN = 111, loff, lvco, lint = 0000111
 CLK_SC: 1.2Vpp Square
 Power: GNDi = -5 V, VDDi = -5 V
 CLK_SC: f_SC = 5 MHz
 C_L = 1 uF

Negative Voltage Generator

Temperature dependence

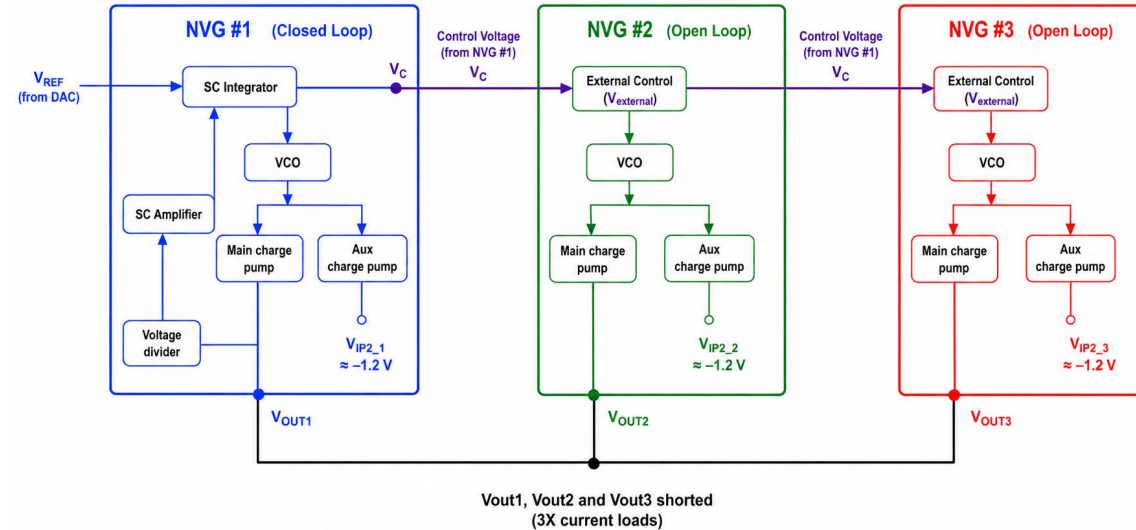
Single chip: CHIP1



- NVG output range was measured over a temperature range from -25°C to 85°C .
- VOUT-VREF transition region narrows as temperature increases while all other parameters are kept constant.

Negative Voltage Generator

Three NVBGs in parallel



- To handle higher load currents multiple NVBGs can be connected in parallel
- Three NVBGs in parallel (one in closed loop and another two in open loop)
- v1p2 outputs of all NVBG separate, but Vout shorted together
- V_c from the closed-loop NVBG $\rightarrow$ external control for the open-loop NVBGs
- Test with load current increased up to 3 times the single-NVBG to evaluate parallel operation performance

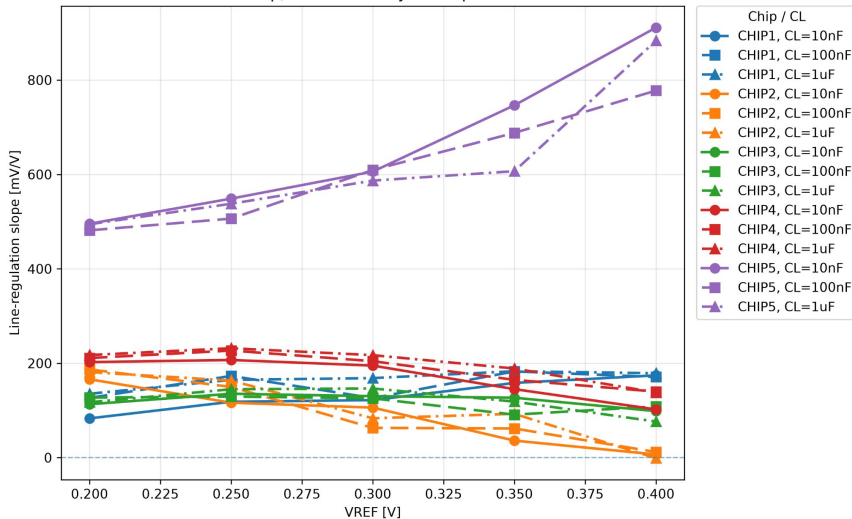
I2C Configuration: EN_CP = 16
 EN = 111, loff, lvco, lint = 0000111
 CLK_SC: 1.2Vpp Square
 Power: GNDi = -5 V, VDDi = -5 V
 CLK_SC: f_SC = 5 MHz

Negative Voltage Generator

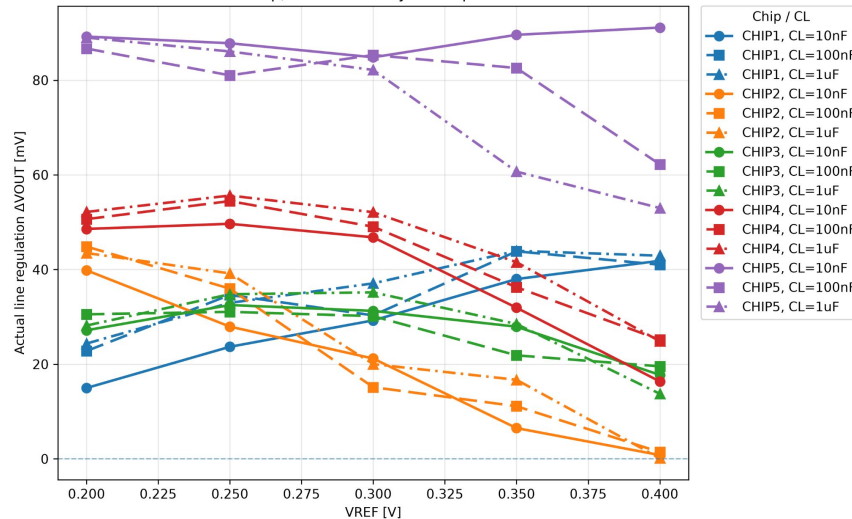
Chip to chip variation

Line regulation

Line-Regulation Slope vs VREF — CHIP1 to CHIP5
 fCLK=5MHz, IL=0.500 mA, Rload=0 Ω
 Color = chip; marker/line style = capacitive load



Actual Line Regulation vs VREF — CHIP1 to CHIP5
 ΔV_{OUT} = slope $\times \Delta V_{DD}$ of fitted flat region; fCLK=5MHz, IL=0.500 mA, Rload=0 Ω
 Color = chip; marker/line style = capacitive load



- Line regulation shows no strong dependence on VREF or load capacitance.
- CHIP5 exhibits larger line regulation than the other chips under the same measurement conditions.
- ΔV_{OUT} = line-regulation slope $\times$ regulated VDD range estimates the overall VOUT variation within the regulated region, ranging from 0–50 mV across the measured chips.

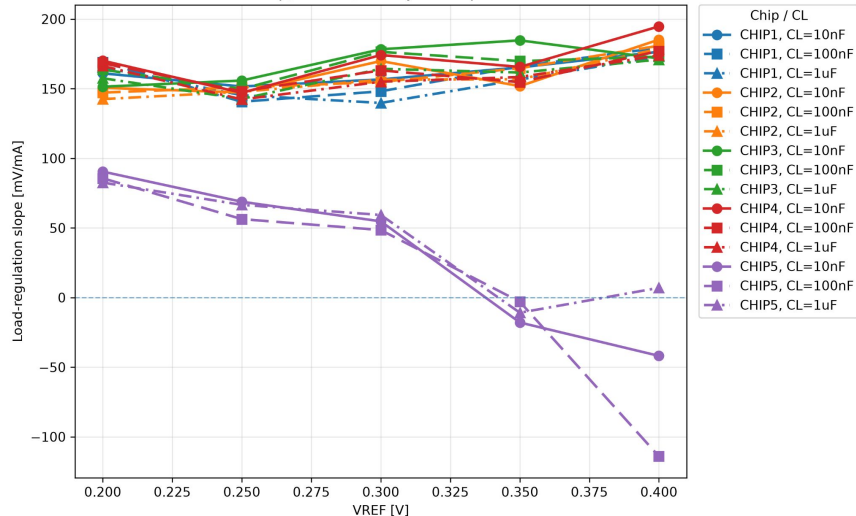
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 CLK_SC: 1.2Vpp Square
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 CLK_SC: f_SC = 5 MHz

Negative Voltage Generator

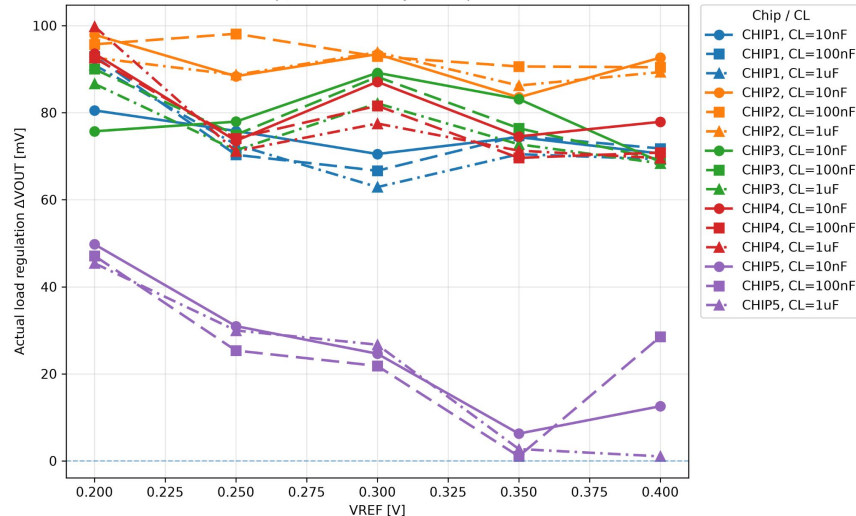
Chip to chip variation

Load regulation

Load-Regulation Slope vs VREF — CHIP1 to CHIP5
 fCLK=5MHz, VDD=1.200 V, Rload=0 Ω
 Color = chip; marker/line style = capacitive load



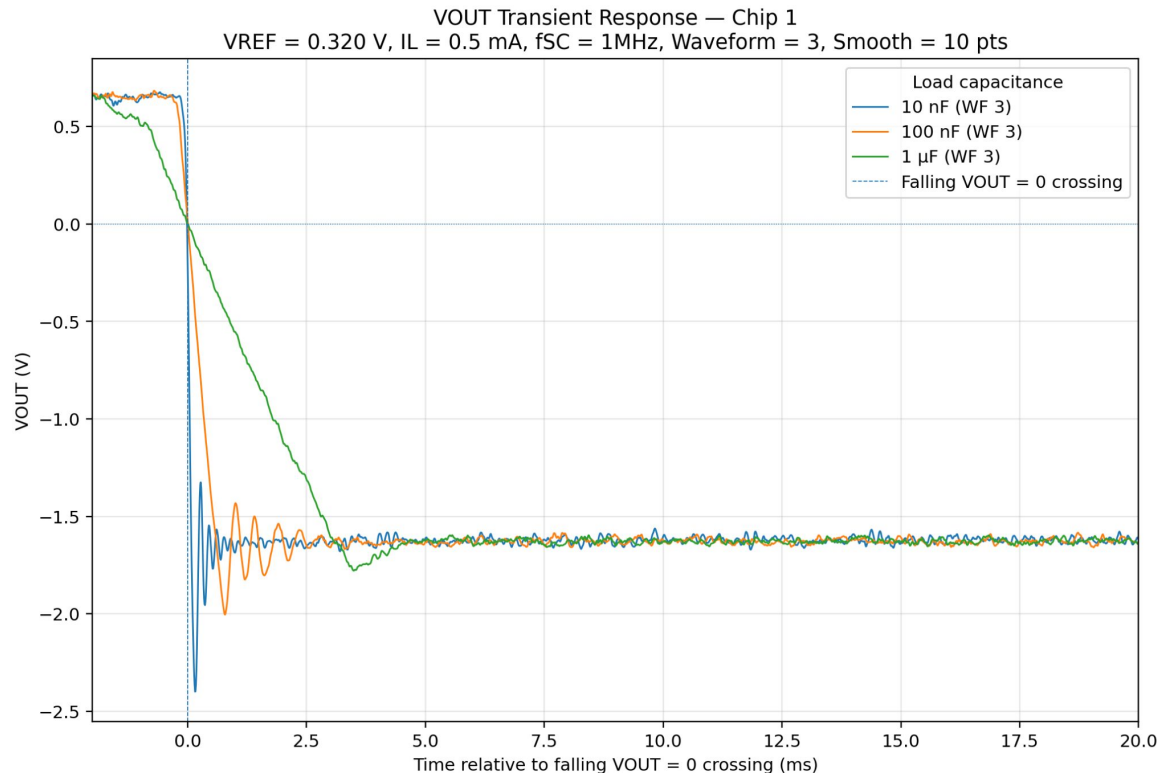
Actual Load Regulation vs VREF — CHIP1 to CHIP5
 ΔV_{OUT} = slope $\times$ ΔI_L of fitted flat region; fCLK=5MHz, VDD=1.200 V, Rload=0 Ω
 Color = chip; marker/line style = capacitive load



- Load regulation shows no strong dependence on VREF or load capacitance.
- CHIP5 exhibits smaller line regulation than the other chips under the same measurement conditions.
- ΔV_{OUT} , defined as the load-regulation slope $\times$ regulated IL range, is used to estimate the overall VOUT variation across the regulated region and ranges from 60–100 mV across the measured chips.

I2C Configuration: EN_CP = 16
EN = 111, loff, lvco, lint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V

Negative Voltage Generator



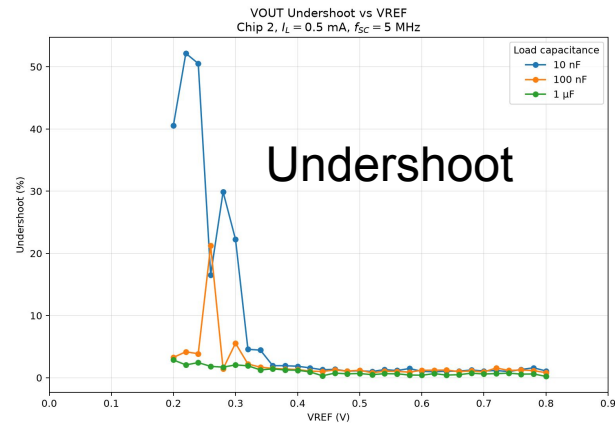
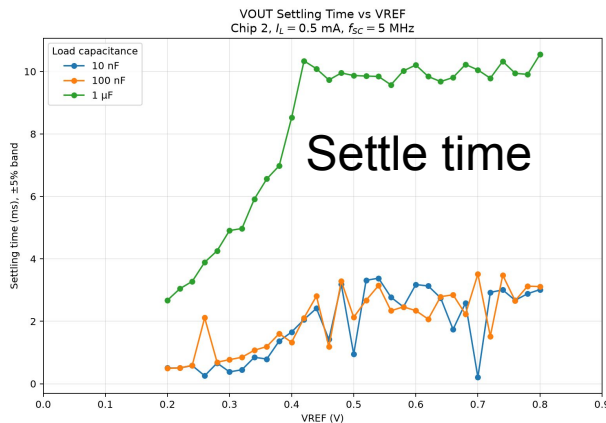
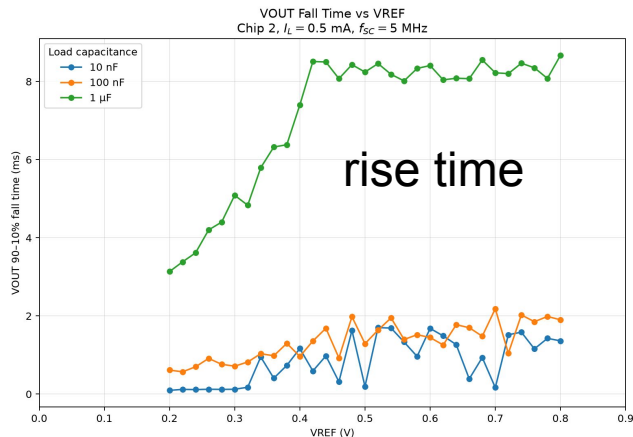
- Smaller C_L provides a faster VOUT transition, but results in larger undershoot and stronger ringing.
- Increasing C_L damps the transient response, significantly reducing undershoot and oscillations.
- This improved stability comes at the cost of a slower transition and longer settling time for larger C_L .

I2C Configuration: EN_CP = 16
EN = 111, loff, lvco, lint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V

Negative Voltage Generator

10 -90 % of the falling edge

5% band +/- VOUT (steady state)

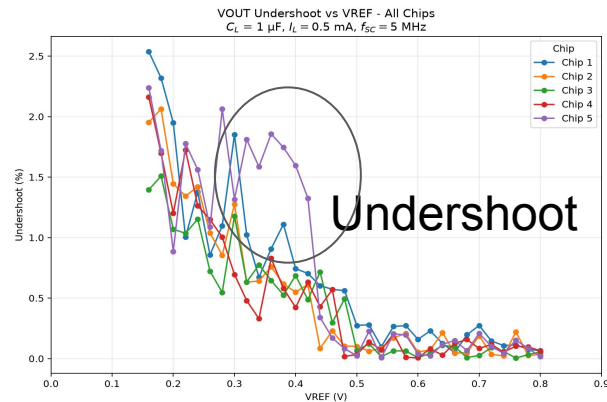
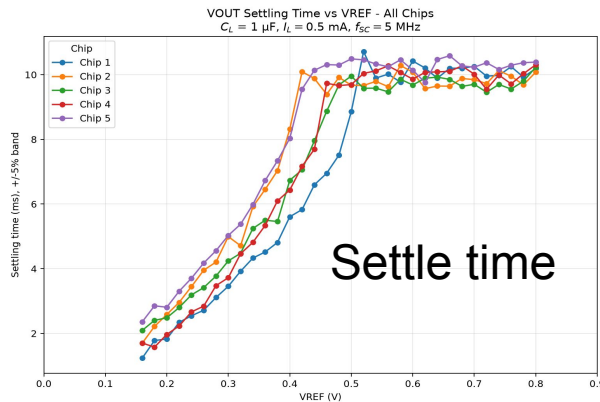
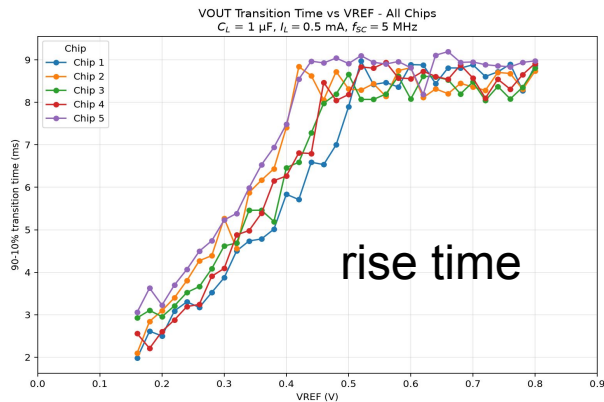


- Larger C_L increases both the 10–90% transition time and settling time, resulting in a slower transient response.
- Smaller C_L provides a faster response, but produces significantly larger undershoot, particularly near the onset of the VOUT–VREF transition region.
- Increasing C_L strongly suppresses the undershoot and oscillatory behavior, giving a more stable output response.

I2C Configuration: EN_CP = 16
EN = 111, loff, lvco, lint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
Load: C_L = 1uF
CLK_SC: f_SC = 5 MHz

Negative Voltage Generator

Chip to chip variation

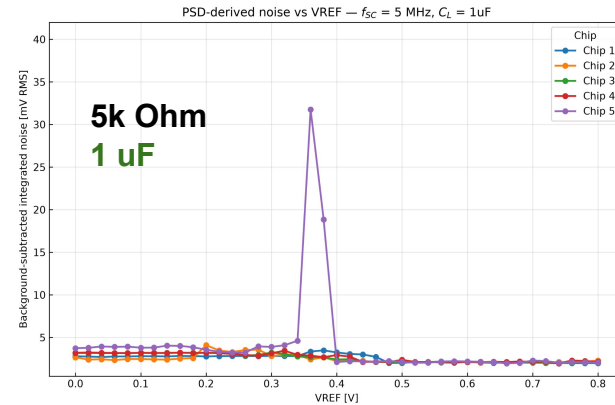
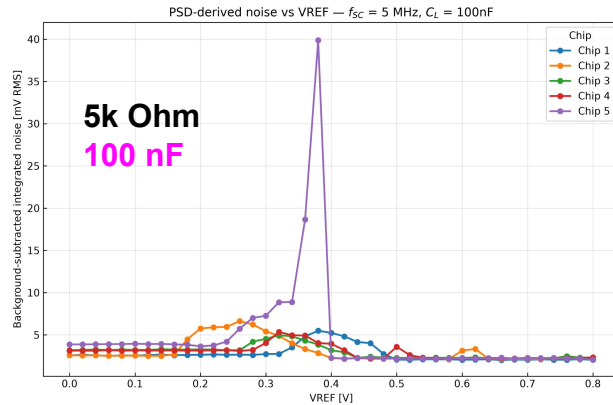
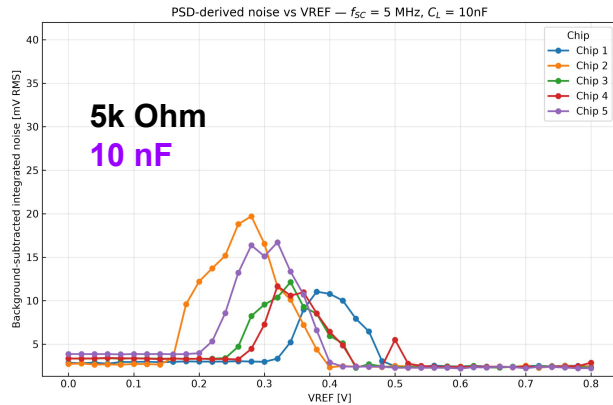


- Rise and settling times show consistent behavior across multiple chips for fixed I_L and $C_L = 1 \mu F$, reaching approximately 8–9 ms and 10 ms, respectively, at higher VREF.
- Undershoot decreases with increasing VREF and becomes minimal at higher VREF, indicating an increasingly stable VOUT
- CHIP5 exhibits a larger undershoot than the other chips in the transition region.

I2C Configuration: EN_CP = 16
EN = 111, loff, lvco, lint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz

Negative Voltage Generator

Chip to chip variation



- Noise increases within the VOUT–VREF transition region for all tested chips.
- Increasing C_L strongly suppresses the noise enhancement, from ~10-20 mV at 10 nF to only a few mV at 1 μ F
- CHIP5 shows larger noise value for both 100 nF and 1 uF capacitive loads
- At 10 nF, larger chip-to-chip variation is observed in both the peak noise and its VREF position.
- With larger C_L , the noise behavior becomes more uniform across chips, with only small chip-to-chip variation at 1 μ F.

I2C Configuration: **EN_CP = 16**
Load: **C_L = 1uF, R_L = 5k Ohm**
CLK_SC: **f_SC = 5 MHz**
20 MHz hardware bandwidth limit: **OFF**

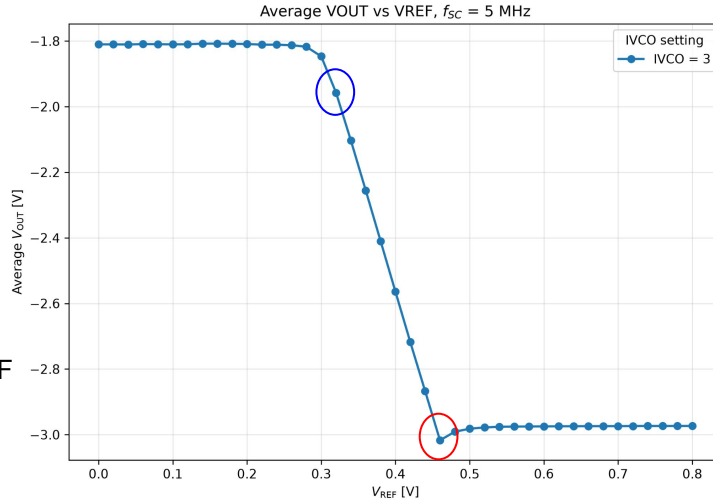
Negative Voltage Generator

R&S ZVL Network Analyzer

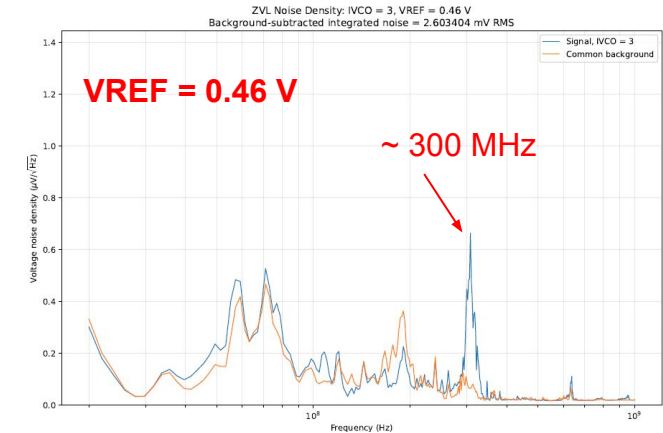
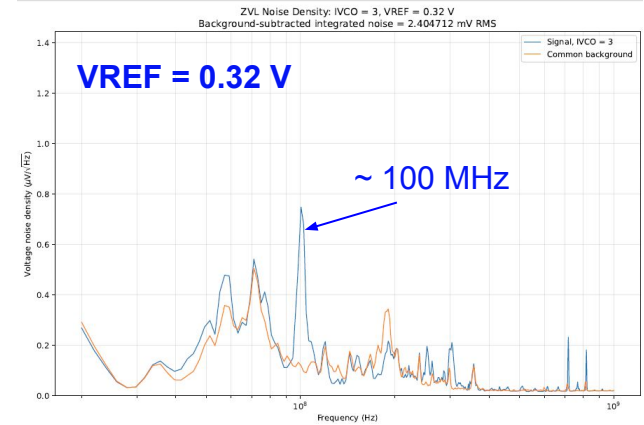
Measured 20 MHz - 1GHz
RBW = 3 MHz

Tektronix P6201

Bandwidth 900 MHz
Attenuation $\times 1$
Output impedance 50 Ω
Input impedance 100 k Ω // 3 pF



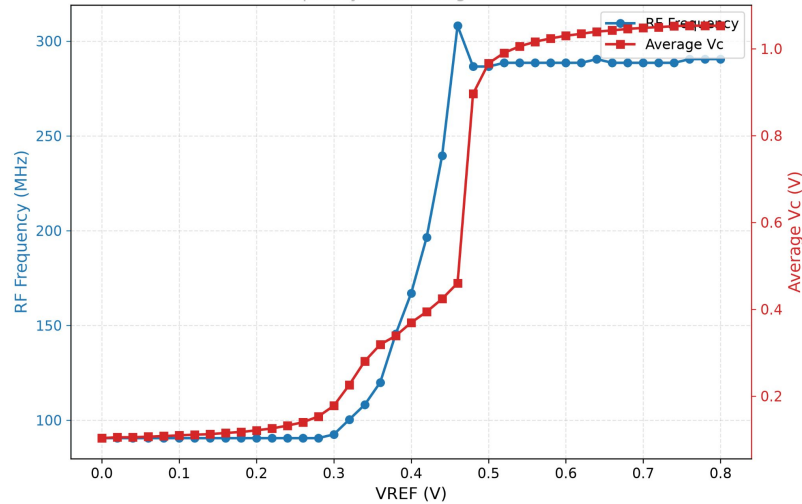
- R&S ZVL Network Analyzer used for noise spectral density measurements (20 MHz–1 GHz).
- Peak noise frequency shifts with VREF in the VOUT–VREF transition region.



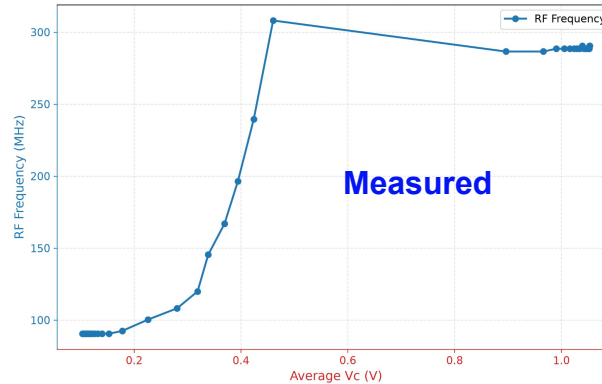
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Load: **C_L = 1uF**, **R_L = 5k Ohm**
CLK_SC: **f_SC = 5 MHz**
20 MHz hardware bandwidth limit: **OFF**

Negative Voltage Generator

Peak noise frequency and Vc vs VREF

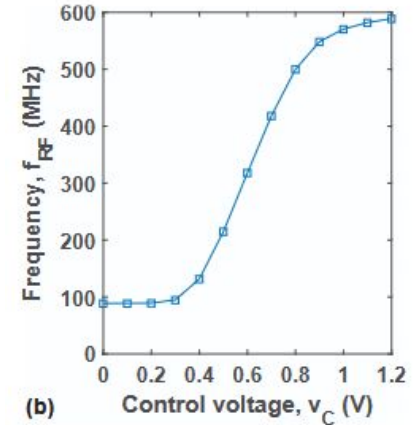


Peak noise frequency vs VREF



simulated tuning curve of VCO

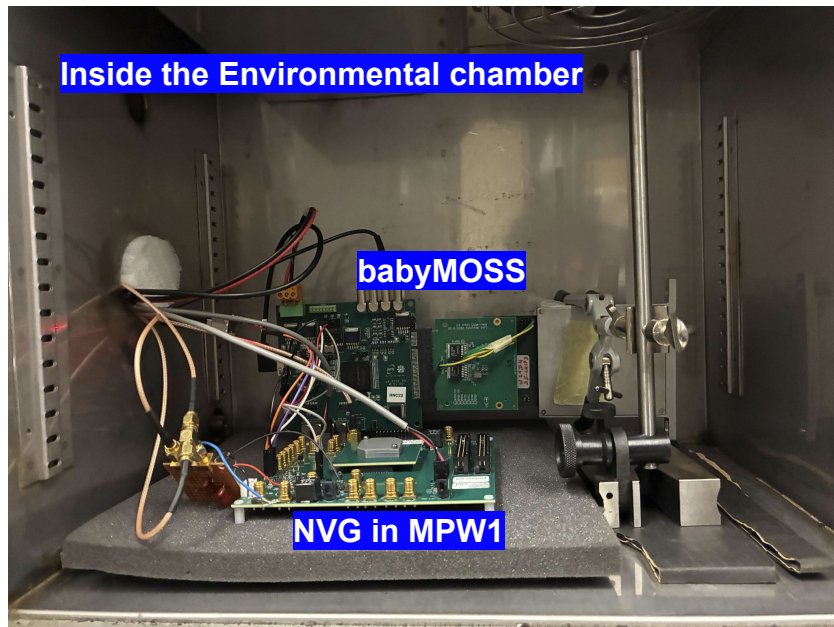
DOI: [10.1109/MWSCAS53549.2025.11244383](https://doi.org/10.1109/MWSCAS53549.2025.11244383)



- Peak noise frequency follows a trend similar to simulation results but is limited up to ~300 MHz in the measurement.
- This supports that the dominant peaks observed in the NVG measurement originate from the on-chip VCO.

I2C Configuration: EN_CP = 11
EN = 111, loff, lvco, lint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz
C_L = 1 uF

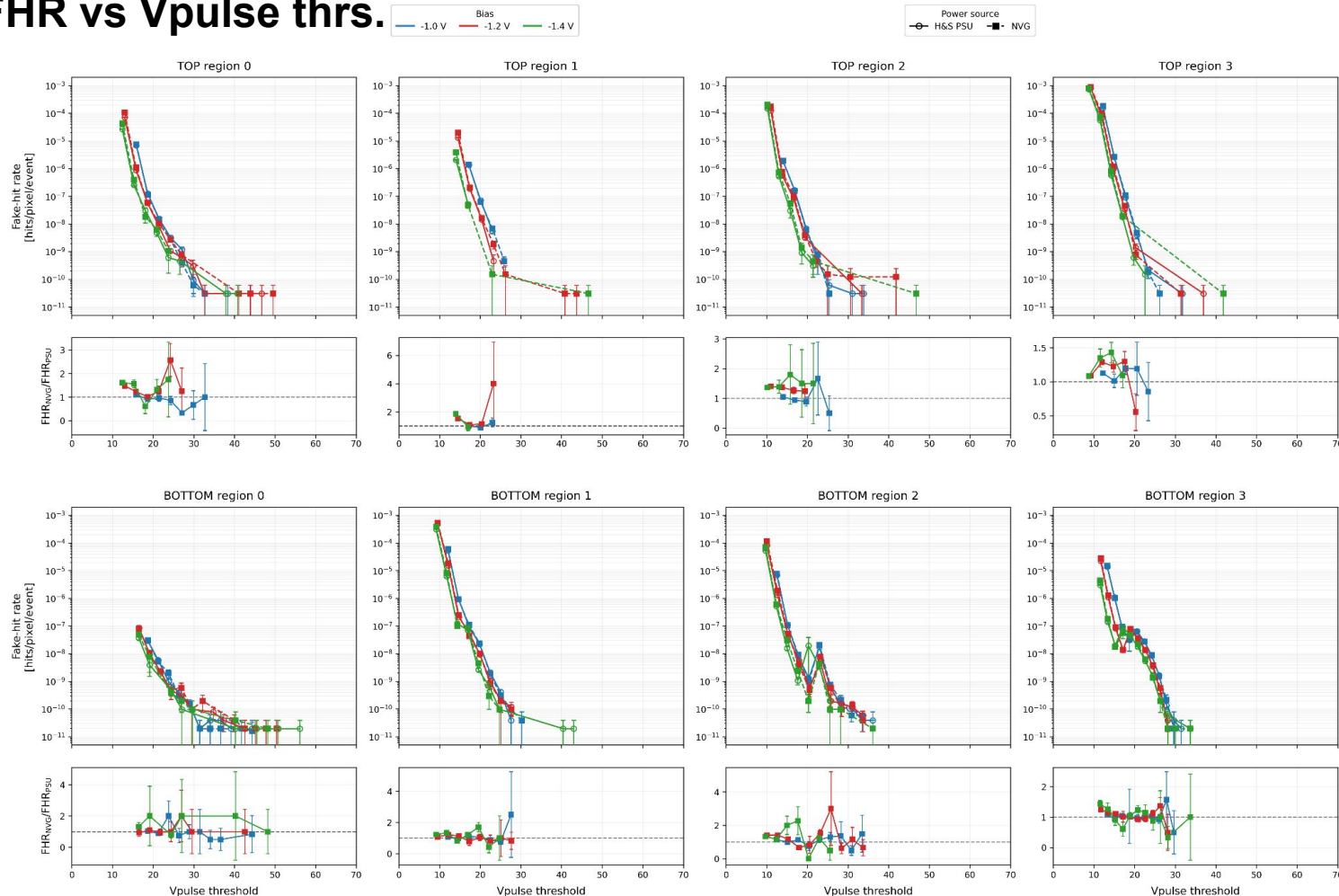
Negative Voltage Generator



- Compared the fake hit rate (FHR) of babyMOSS using the **R&S HMP4040** and **NVG** power supplies.
- Measurements performed at a stable 20°C in an environmental chamber to minimize temperature effects on FHR.
- DC output monitored using an oscilloscope, and noise spectral density monitored using a network analyzer.
- FHR measured for three bias voltages (-1.0, -1.2, and -1.4 V)
- FHR also measured for different capacitive loads at the Vout node.

FHR vs Vpulse thrs.

Fake-Hit Rate vs Vpulse Threshold
H&S PSU vs NVG



I2C Configuration: EN_CP = 11
EN = 111, loff, lvco, lint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz
C_L = 1 uF

- Fake hit rate (FHR) plotted as a function of Vpulse thresholds for different bias voltages.
- FHR measured with the NVG is in good agreement with that obtained using the R&S HMP4040

FHR vs Vpulse thr.

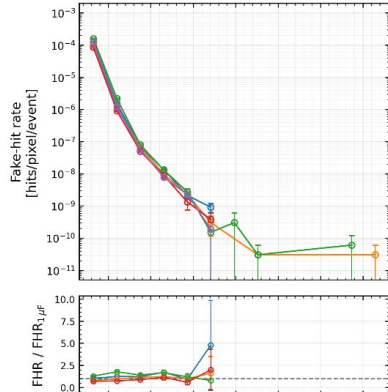
Capacitive load

- No cap
- 1 nF
- 10 nF
- 100 nF
- 1000 nF

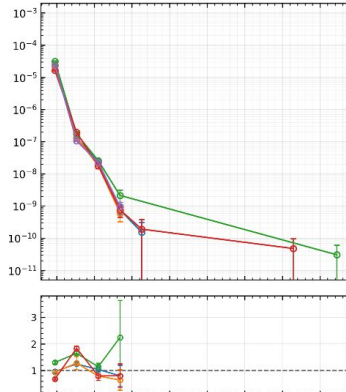
I2C Configuration: EN_CP = 11
EN = 111, loff, lvco, lint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz

TOP

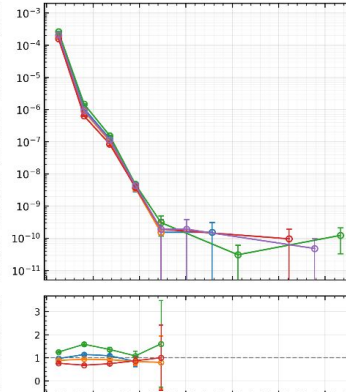
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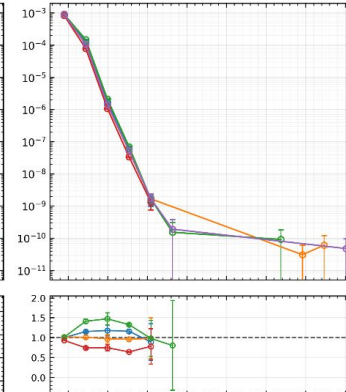
TOP region 1



TOP region 2

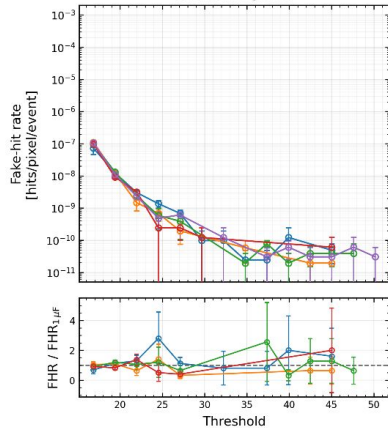


TOP region 3

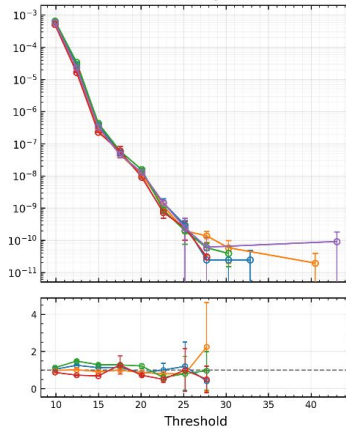


BOTTOM

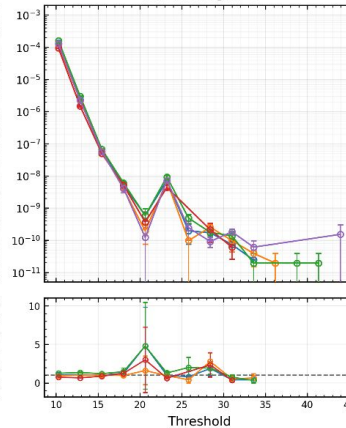
BOTTOM region 0



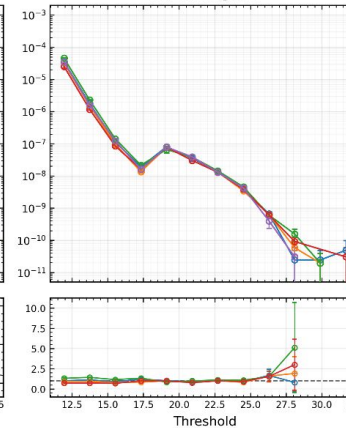
BOTTOM region 1



BOTTOM region 2



BOTTOM region 3



- FHR measured as a function of Vpulse threshold using the NVG for different capacitive loads.
- FHR remains consistent across the tested capacitive loads, indicating negligible dependence on C_L.