

Developing Flexible Printed Circuits for SVT Disks

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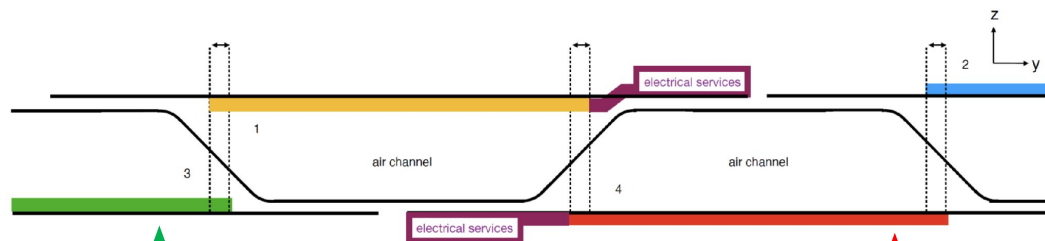
October 9, 2026`

Monthly SVT WP3 meeting: <https://indico.bnl.gov/category/548/>

Mailing list: <https://lists.bnl.gov/sympa/info/epic-svt-wp3-l>

FPCs for SVT Disks

Requirements: provide electrical interfaces for low voltage power, slow control and high-speed data between **sensor, AncASIC, and FPC Interface Board (FIB)**; transmit high-speed data up to 10.24 Gbps over 40 cm distance; minimum power loss; minimum material budget (Al-based FPC)



Sensor Inward Facing Module

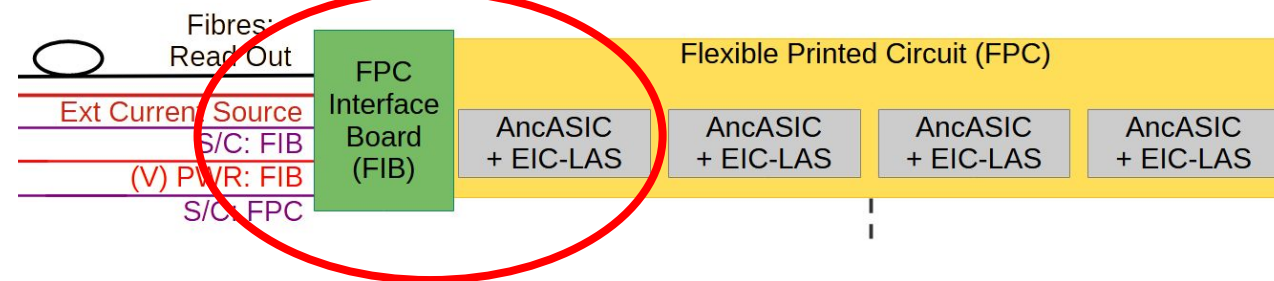
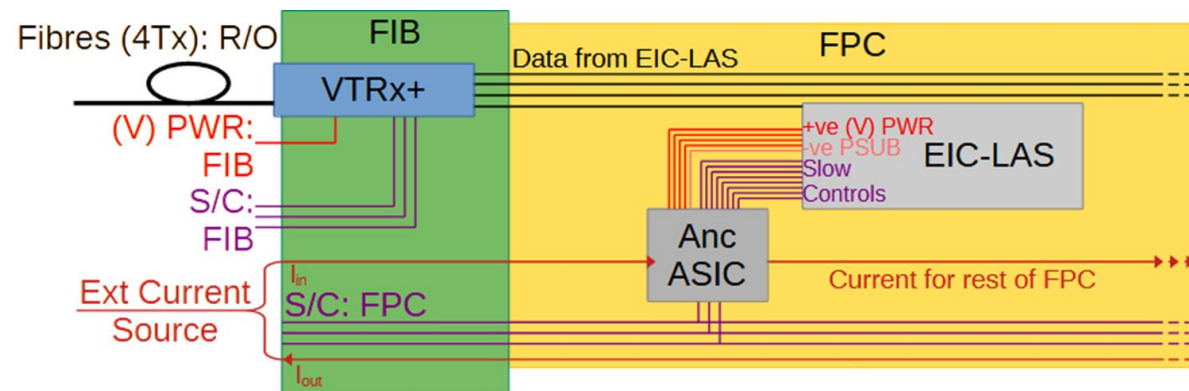
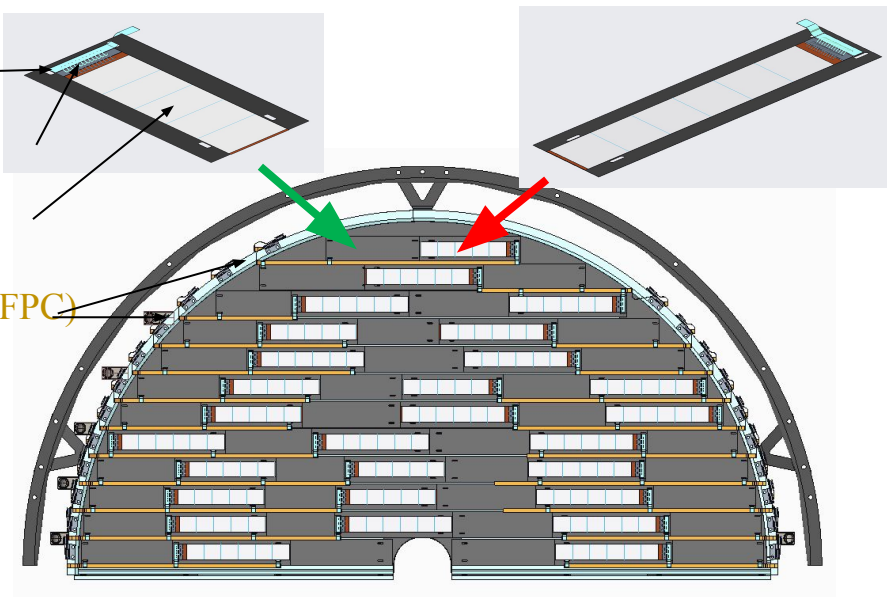
Sensor Outward Facing Module

Bridge FPC(BFPC)

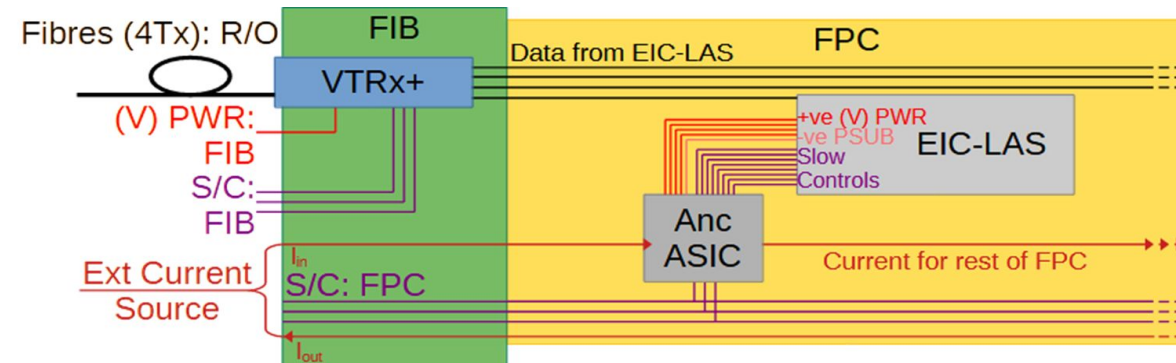
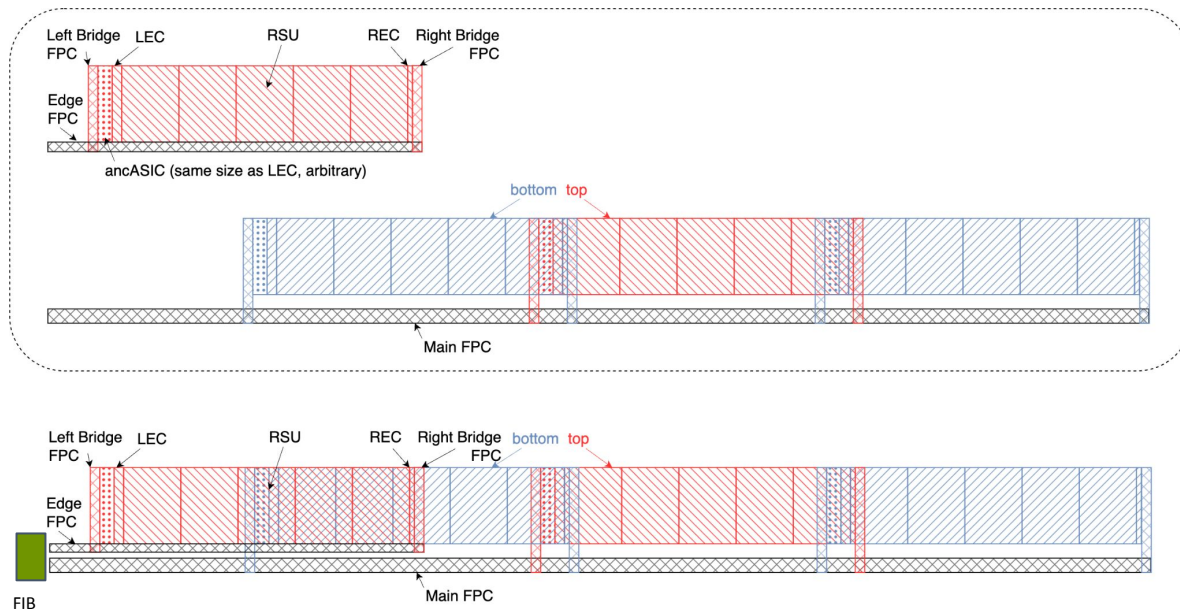
AncASIC

EIC-LAS

Main FPC(MFPC)



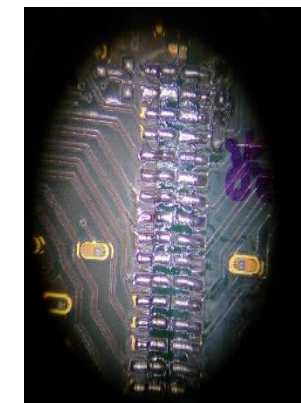
FPC Interconnections for SVT Disks



bold: preferred option

	FIB	Main FPC	Bridge FPC	AncASIC
Main FPC	Connector, Soldering			
Bridge FPC		soldering, wire/TAB-bonding		
AncASIC			wire-bonding, TAB-bonding	
EIC-LAS			wire-bonding, TAB-bonding	wire-bonding

soldering



wire bonding



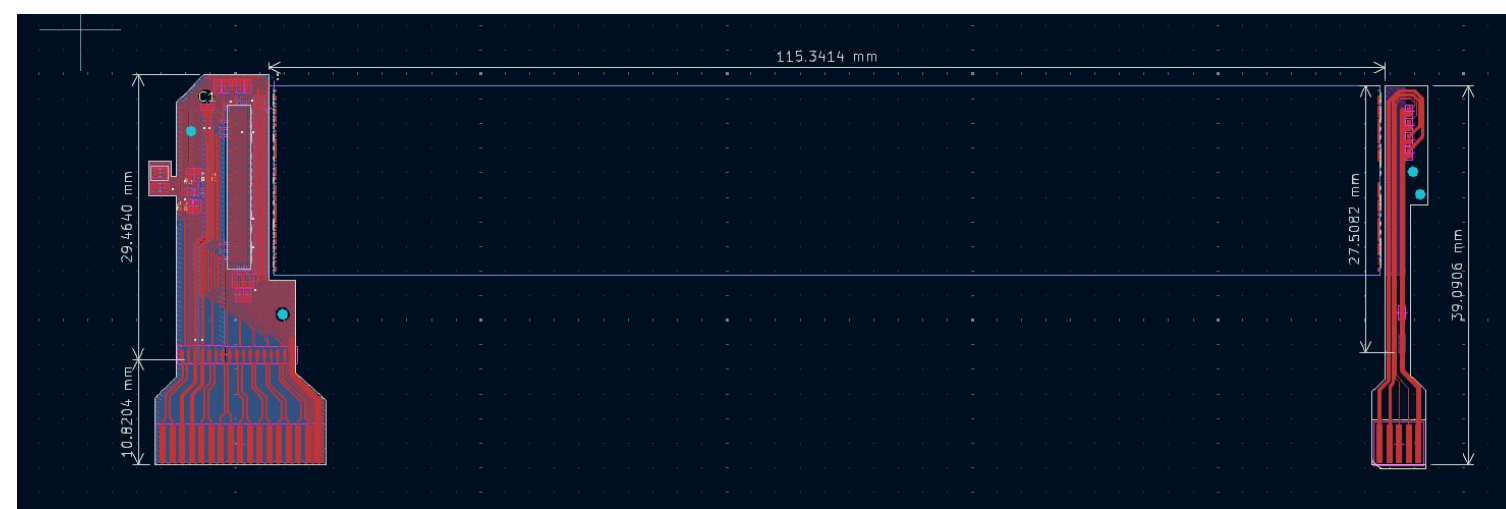
TAB bonding



Mechanical Prototype FPCs for Disk Module Assembly

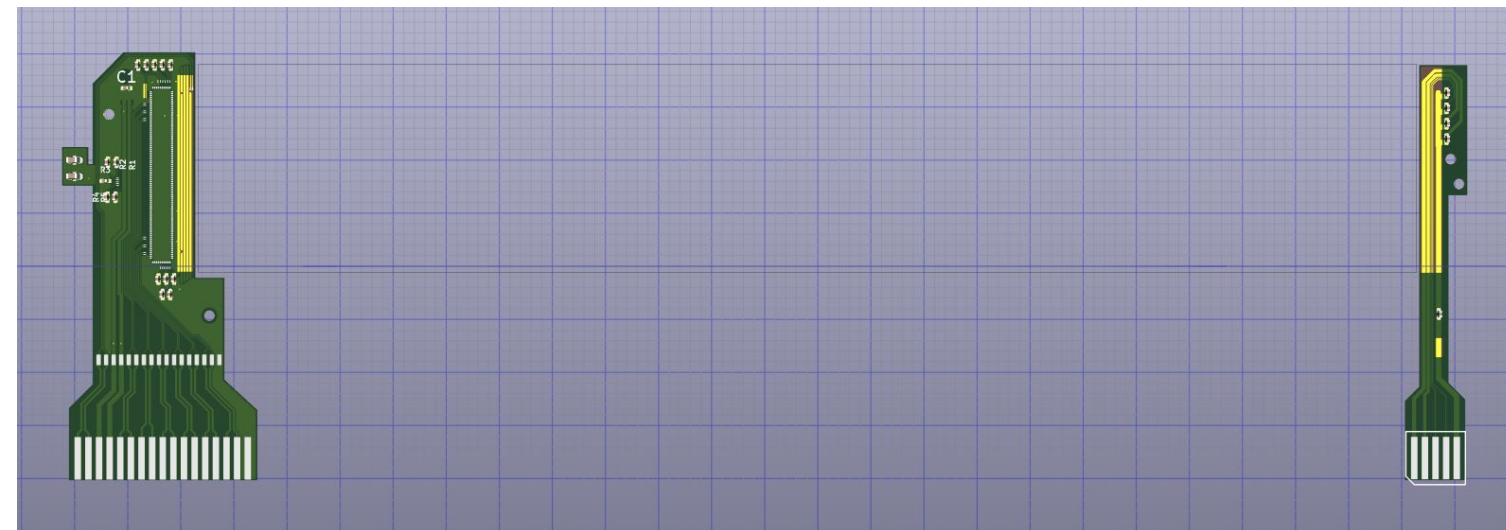
Considering the latest info about EIC-LAS and AncASIC dimensions
and pad assignments

Bridge FPCs (JLCv1)



- **Left bridge FPC with AncASIC** will handle **EIC-LAS** LEC power, slow control, high-speed data transmission.

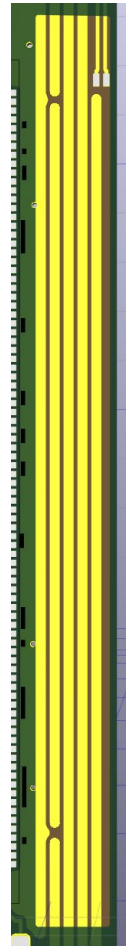
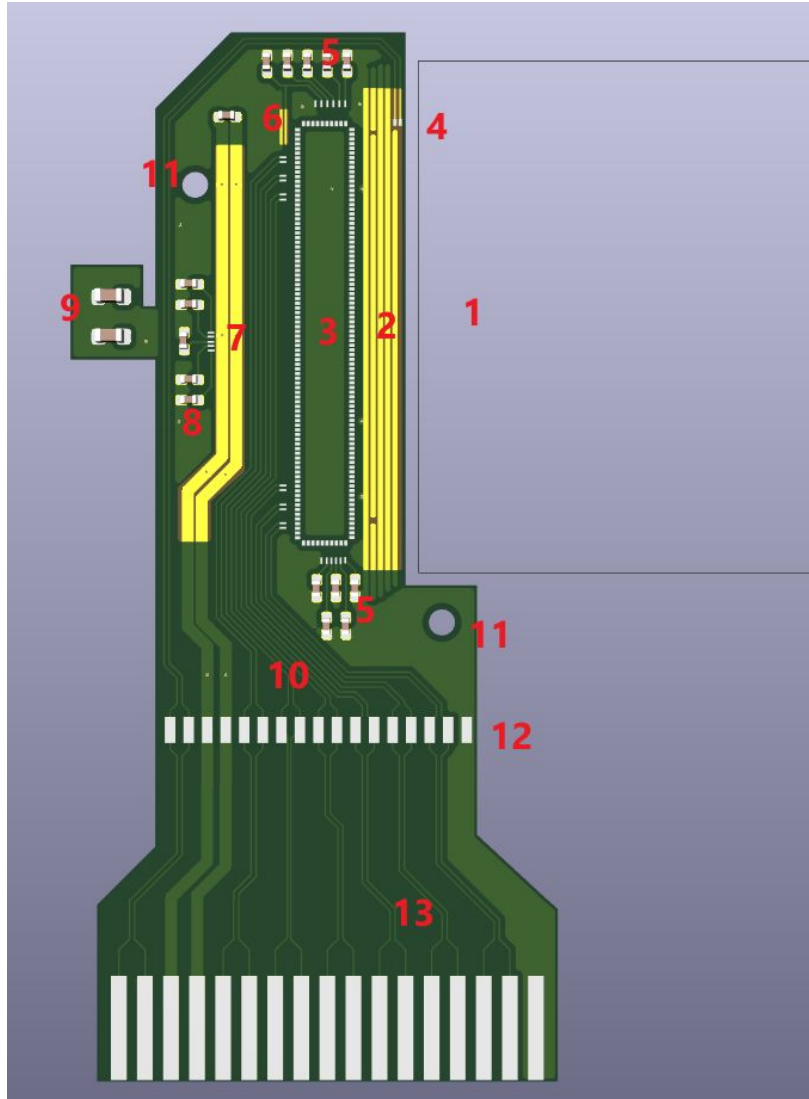
	Area (mm ²)	Metal area (mm ²)	Fill factor
Top Layer	278.2	190	0.69
Bottom Layer	278.2	260	0.94



- **Right bridge FPC** with power buses connected to GND through decoupling capacitors will connect to the **EIC-LAS REC**.

	Area (mm ²)	Metal area (mm ²)	Fill factor
Top Layer	78.9	32.9	0.42
Bottom Layer	78.9	0	0

Left Bridge FPC (JLCv1)



1. Left side of EIC-LAS

The distance between LAS and the FPC is **0.508 mm**. The size of the LAS is assumed as **114.330 * 19.564 mm**.

2. Power Bus

Net name from left to right: GND, PSUB, TXVDD, GSVDD, GAVDD, GDVDD.
Each trace is **8 mil width with 3 mil spacing**.

3. AncASIC

The distance between the edge of AncASIC and LAS is **2.4 mm**. The size of the ASIC is assumed as **16.434 mm × 2.388 mm**.

4. Pads of the HSD

width/space = 55um / 140 um. Since the pads of the HSD on LAS haven't been confirmed, I choose the HS_DATA<0> of MOSAIX as the HSD pad in this design.
Length of HSD_P = 48.4mm, HSD_N = 48.9mm.

5. Decoupling Capacitors

All of the Decoupling Capacitors are in the 0201 footprint.

6. AncASIC address

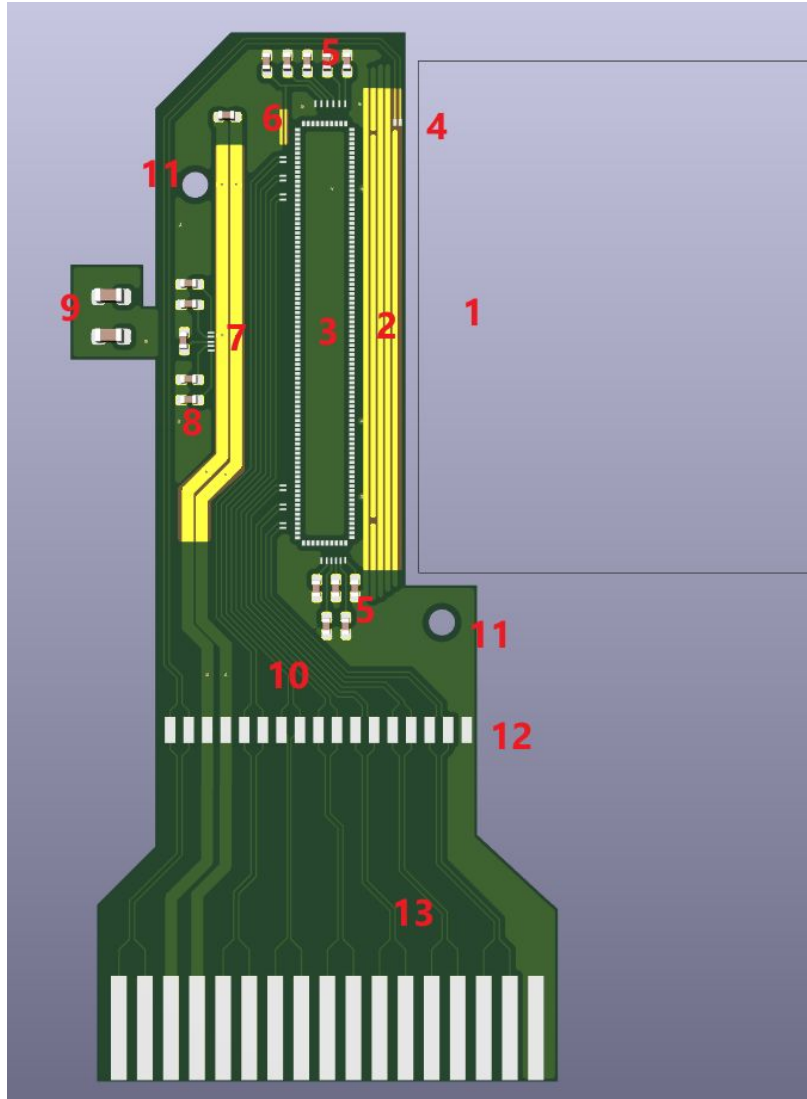
There is an open window on the soldermask, so the address pads of AncASIC can be wire-bonded to ABVDD or GND.

Note 1: The 55um / 140um dimensions are empirical parameters for achieving $Z_{diff} = 100\Omega \pm 10\Omega$, which need to be validated through sample production and testing.

Note 2: The dimensions of the AncASIC are calculated as follows: (pad number - 1) × pitch (180 μm) + pad width (assumed to be 5 mil) + Corner Cell Width (300 μm) × 2. The theoretical dimensions are 16.385 mm × 2.345 mm. Due to the precision limitations of the design software, the final dimensions are 16.434 mm × 2.388 mm. These dimensions only serve solely as a reference for the placement and routing of other components on the FPC.

AncASIC/MOSAIX pad lists from Iain
Sedgwick March 2026

Left Bridge FPC (JLCv1)



7. I_{in}/I_{out} bus

Width of I_{in}/I_{out} = 18 mil. To reduce the power consumption, there is another plane for each net on the bottom layer (see power consumption page)

8. SLDO Reference Current Resistor

All of the resistors are in the 0201 footprint.

9. Stiffener test

JLC suggested the FPC designer place a stiffener beneath the device that needs to be soldered. In this prototype, we placed a stiffener on this area to evaluate the impact of stiffener. There are two 0402 pads in this area, with a stiffener placed underneath one of them. We designed this structure to verify whether an FPC without a stiffener can **withstand the high temperatures of soldering**.

10. Slow control signals

Width/Spacing 55 um/140um.

11. Mounting hole

NPTH hole, diameter = 1 mm.

12. FPC Soldering Pads

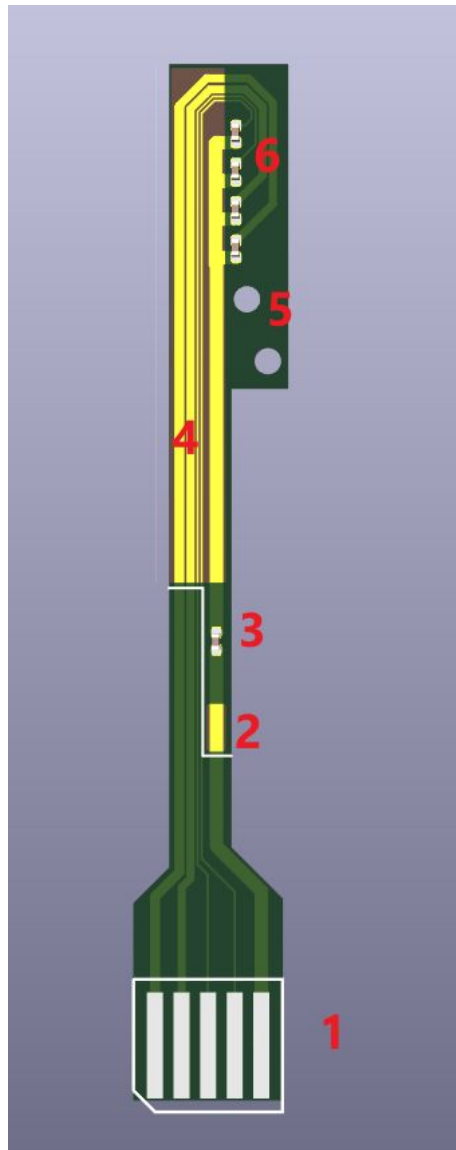
The pads on the bottom edge are used to solder the bridge FPC to main FPC, pad width/spacing (**0.4mm/0.3mm**).

13. FPC wrapper

The FPC wrapper is designed to facilitate connecting this FPC to a test PCB with FPC connector such as 0522711779 Molex to facilitate module electrical test. The wrapper will be removed after QA.

AncASIC/MOSAIX pad lists from Iain
Sedgwick March 2026

Right Bridge FPC (JLCv1)



1. FPC wrapper.

The FPC wrapper is designed to facilitate connecting this FPC to a test PCB with FPC connector such [2005280050 Molex | Connectors, Interconnects | DigiKey](#), to facilitate module electrical tests. The wrapper will be removed afterwards.

2. Solder pads

Solder to the GND net on the Main FPC.

3. AC coupling Capacitors

The ground is AC coupled to the ground on the main FPC.

4. Power/GND Trace:

From left to right, net names and widths are **GDVDD (15mil)**, **GAVDD (12 mil)**, **GSVDD (3 mil)**, and **PSUB (3mil)**.

5. Mounting hole:

NPTH hole, **diameter = 1 mm**.

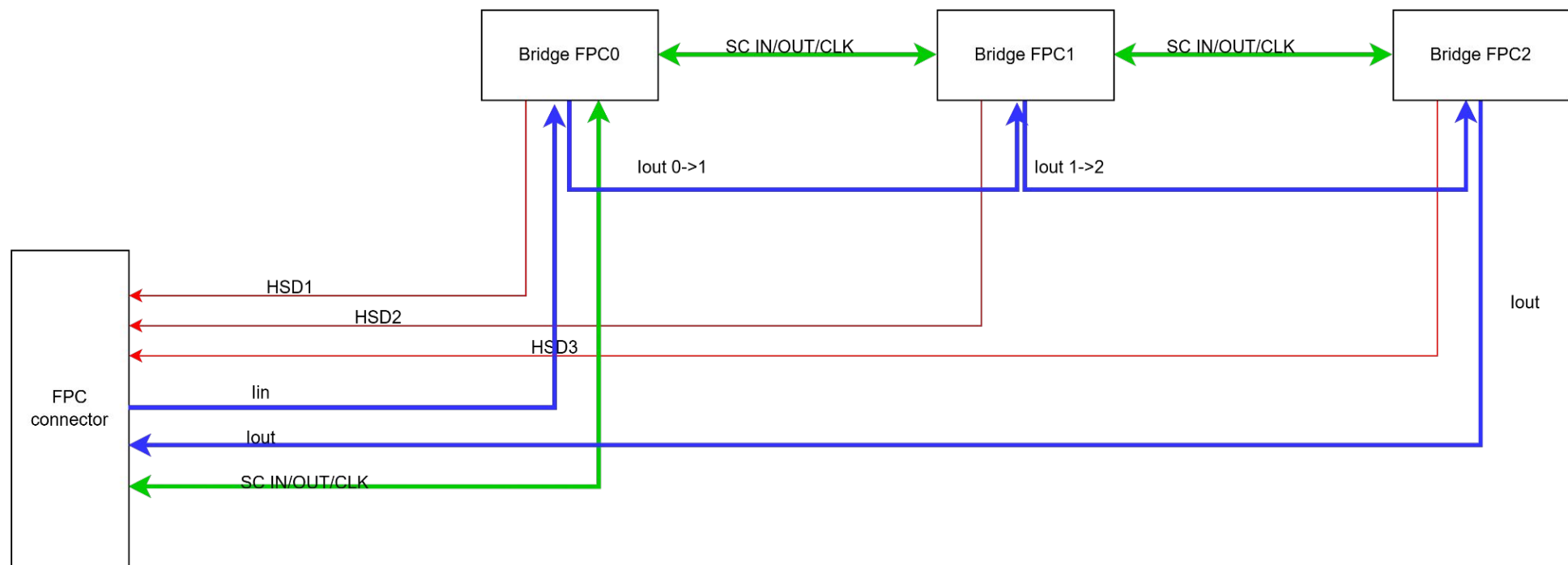
6. Decoupling Capacitor:

All of the resistors are in the 0201 footprint.

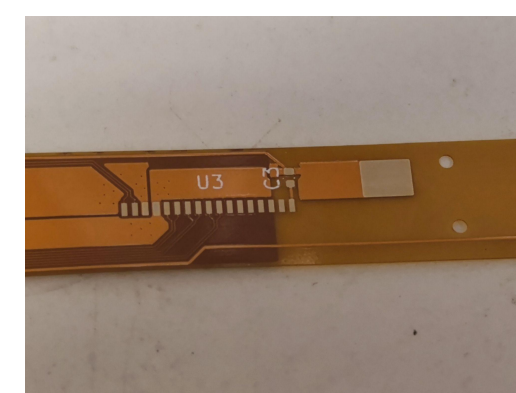
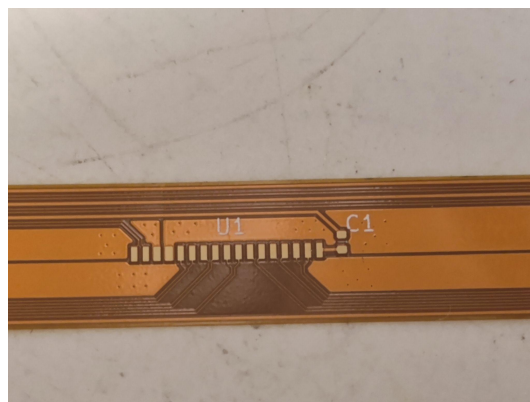
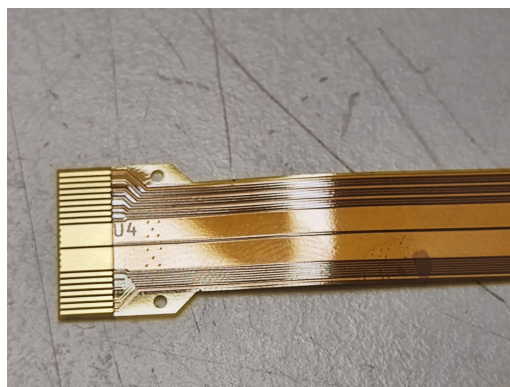
Bridge FPCs (JLCv1)



Main FPC (JLCv1)



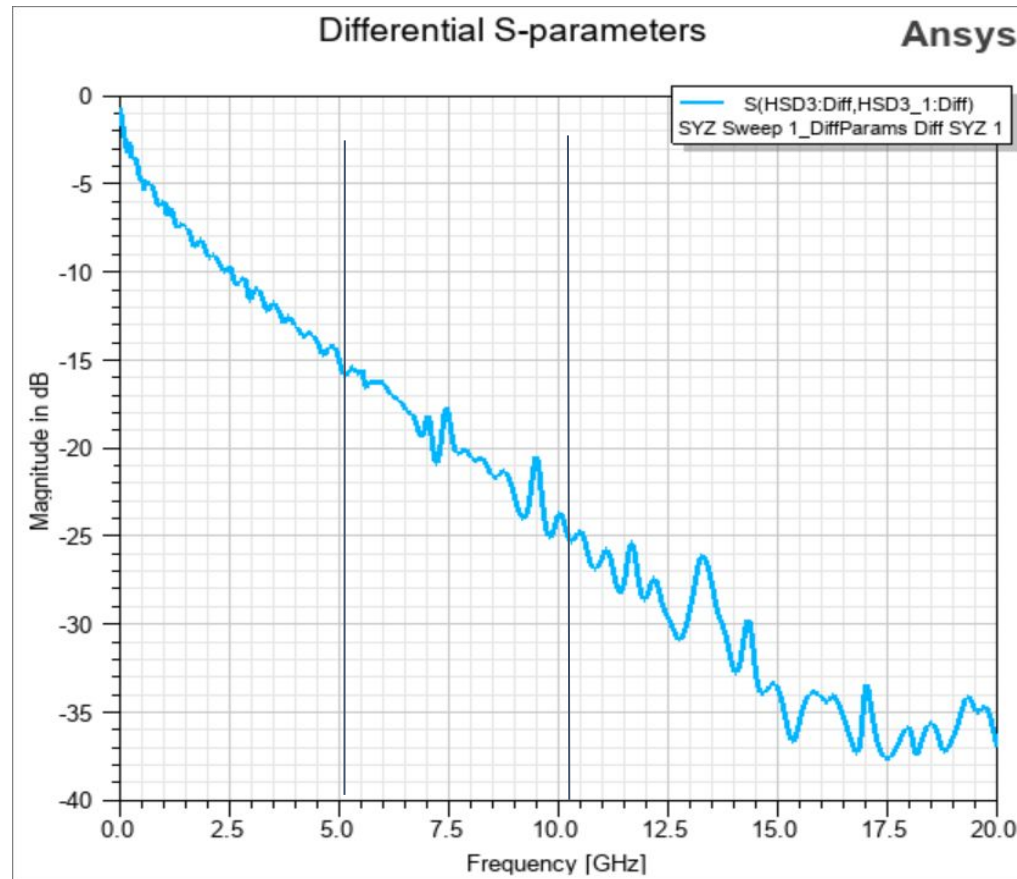
Main FPC (JLCv1)



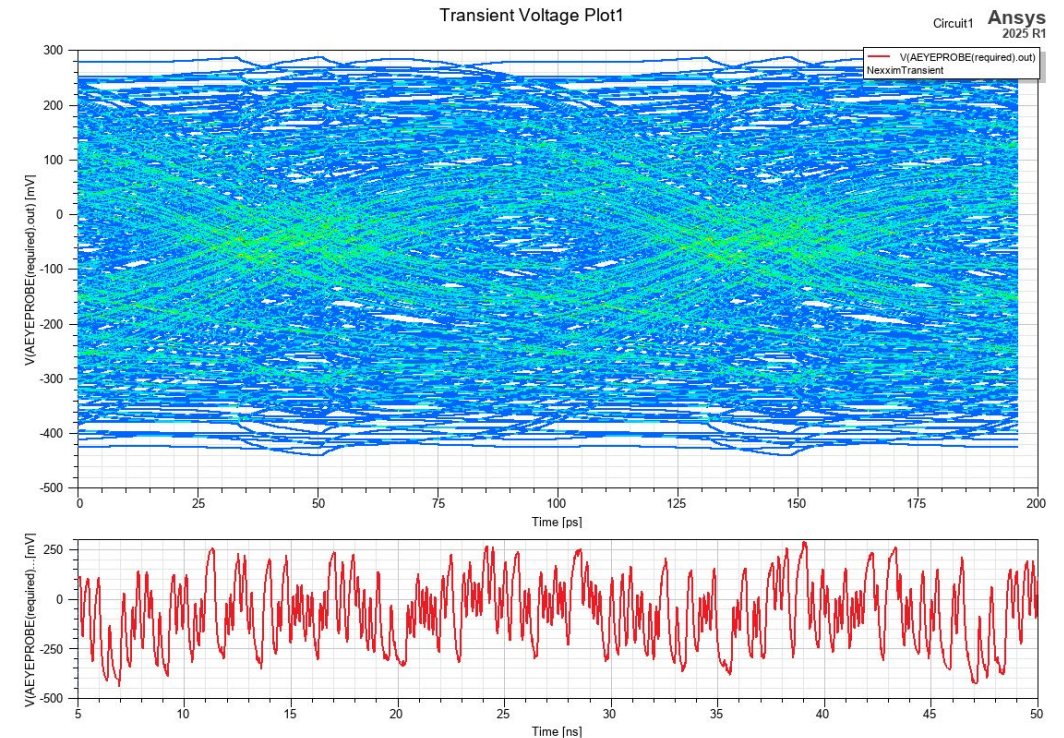
Prototype FPCs for High-Speed Data Transmission

Test structures and simulation to quantify signal loss and cross-talks

S-parameter for JLCv1 FPC



Significant signal transmission loss, eye diagram is unacceptable @10.24Gbps



Test Structures for HS Transmission (JLC)

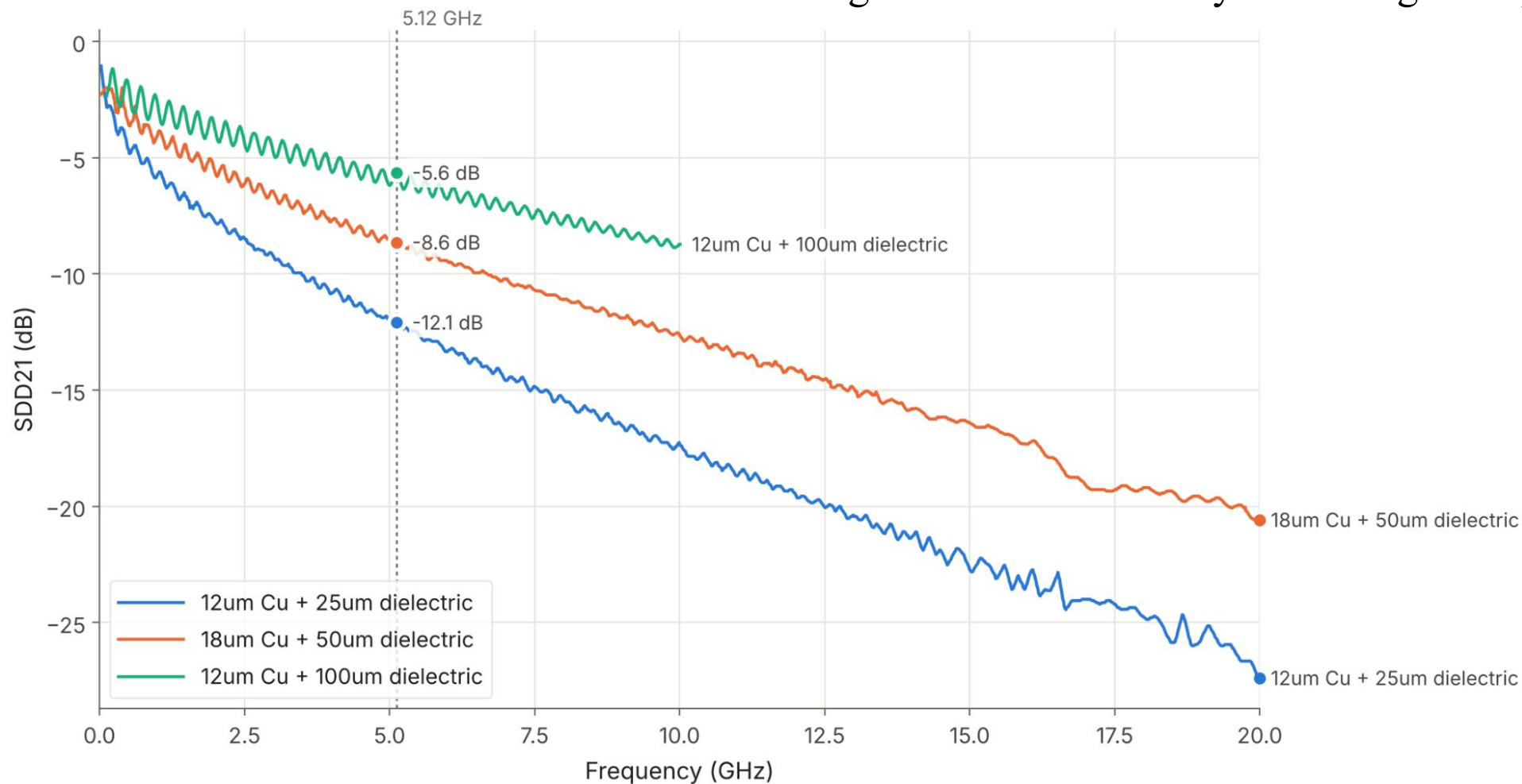
Cover layer thickness (um)	27.5	50	27.5	27.5
Copper thickness (um)	12	18	12	12
Dielectric thickness (um)	25	50	62.5	100
Copper thickness (um)	12	18	12	12
Cover layer thickness (um)	27.5	50	27.5	27.5
Total thickness (um)	104	185	131.5	179
HSD trace width (um)	55	93	110	190
HSD trace spacing (um)	140	152	160	200
HSD perimeter (um)	134	222	244	404
S/C trace width (um)			70	80
S/C trace spacing (um)			60	60
S/C perimeter (um)			164	184

HSD and SC widths and spacings are calculated so that the impedance is around 100 Ohms

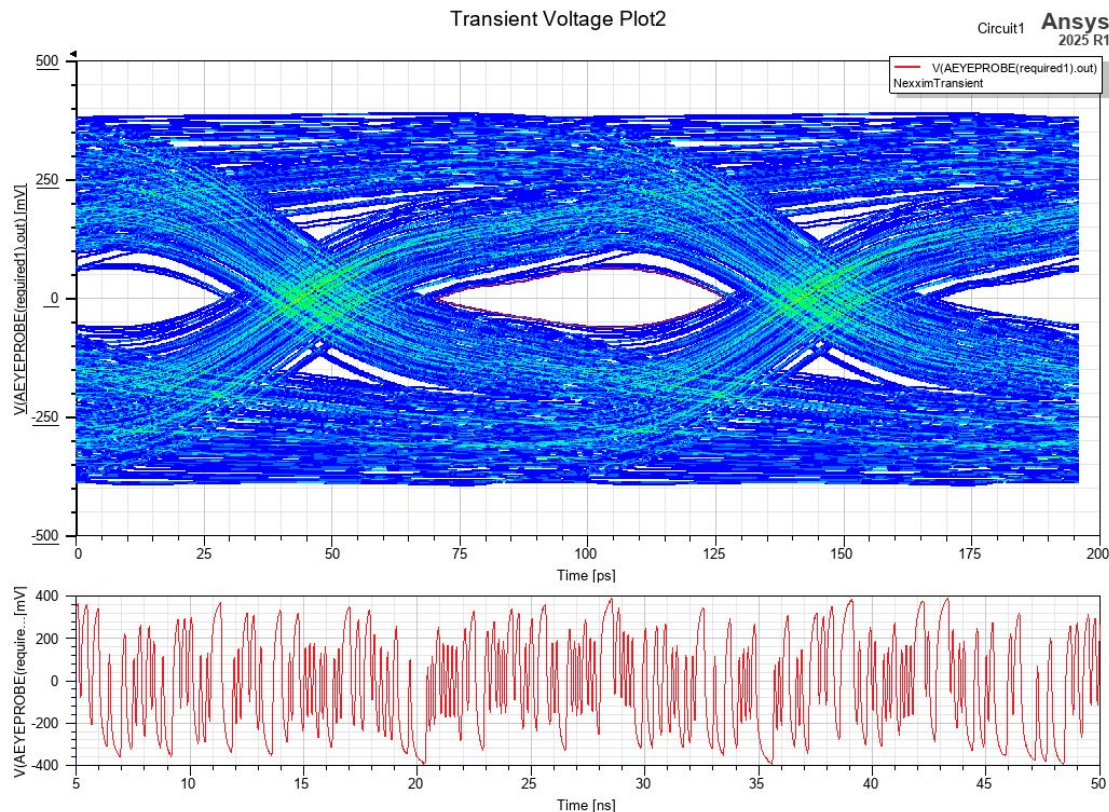
S-parameters from Simulation

Differential insertion loss vs FPC stackup

Signal loss is reduced by increasing trace perimeter



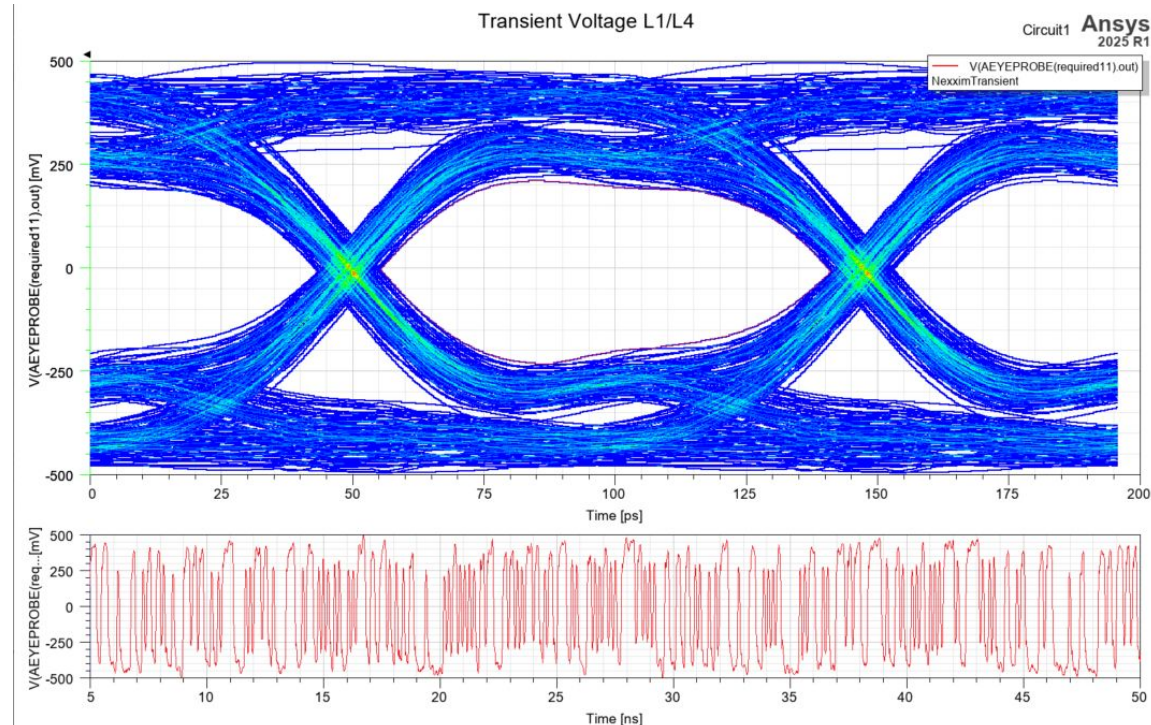
Eye Diagrams @ 10.24Gbps from Simulation



12 um Cu, 25 um dielectric

55 um trace width

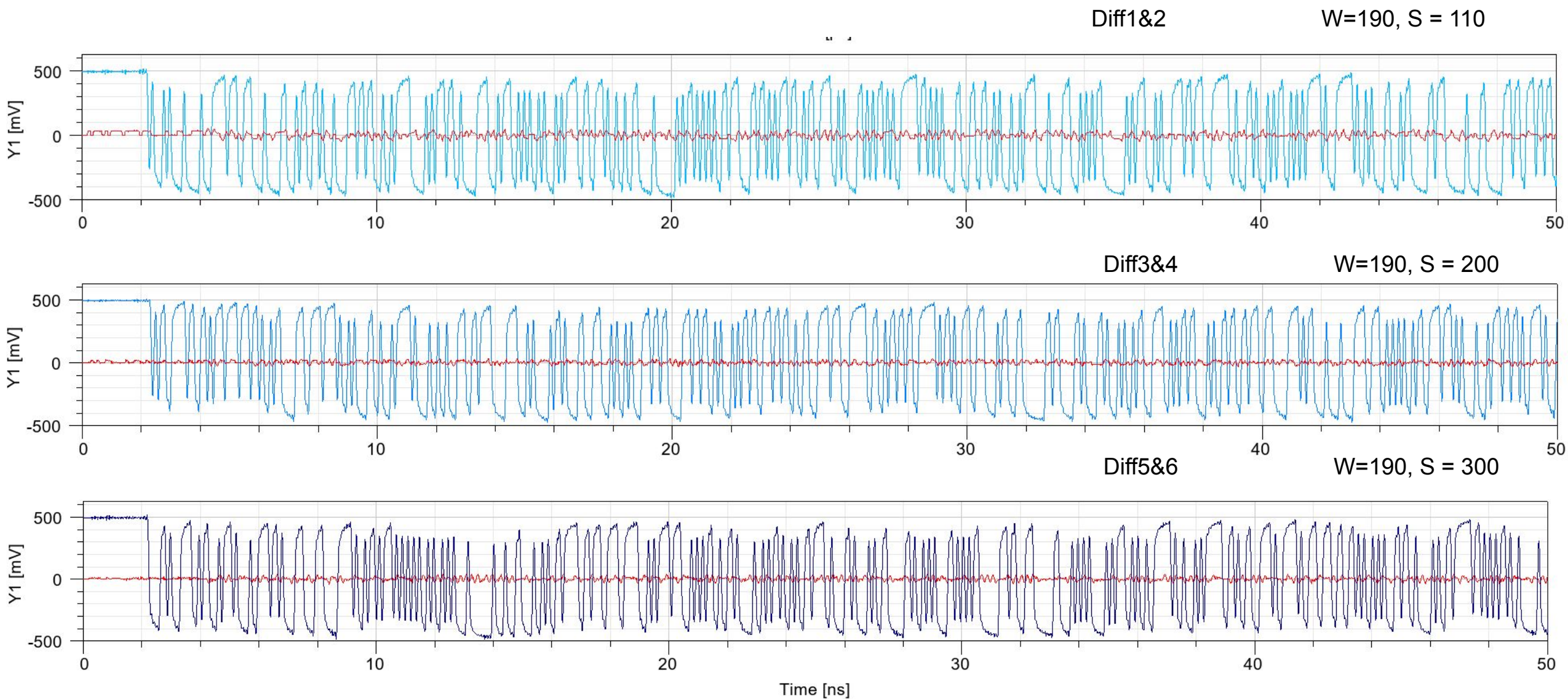
In the same stack-up with the JLCv1(see page 13) and optimized the locations of the impedance discontinuities.



12um Cu, 100 um dielectric

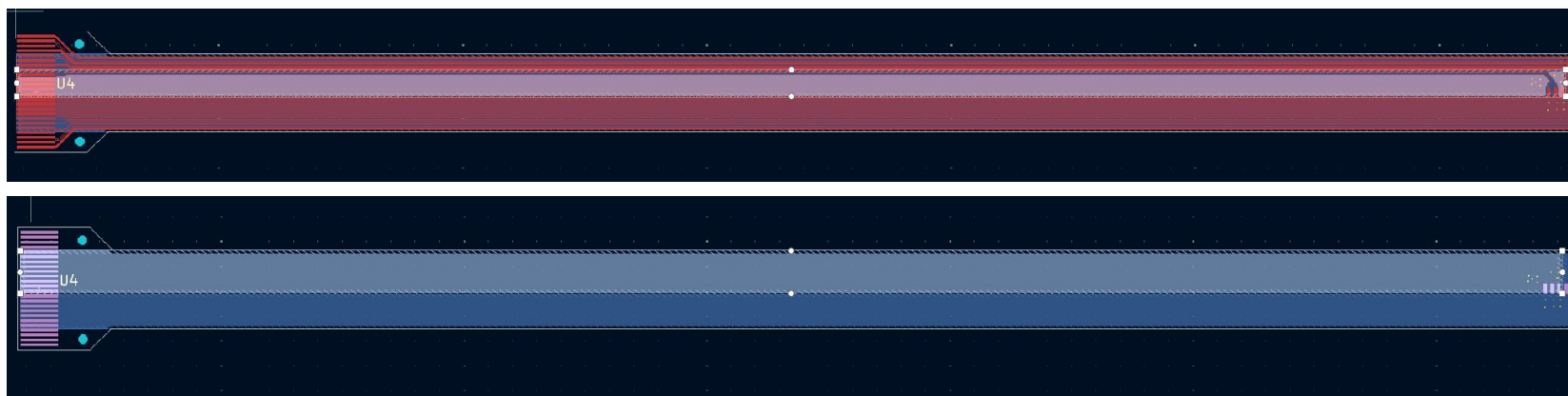
190 um trace width

Cross-Talk vs Spacing from Simulation



W: Trace width; S: Spacing between Differential pairs

Main FPC Power Consumption (JLCv1)



I_{in01} net in the top and bottom layers

Net	From	To	Material	Resistivity@ 20°C (ohm·m)	Thickness (m)	length (m)	Width on top (m)	Width on bottom (m)	Resistance Top	Resistance Bottom	Resistance
I_{in01}	FPC connector	Bridge FPC0	Aluminum	2.65E-08	1.50E-05	0.17	0.00196	0.00460	1.53E-01	6.53E-02	4.58E-02
I_{in12}	Bridge FPC0	Bridge FPC1	Aluminum	2.65E-08	1.50E-05	0.107	0.00282	0.00460	6.70E-02	4.11E-02	2.55E-02
I_{in23}	Bridge FPC1	Bridge FPC2	Aluminum	2.65E-08	1.50E-05	0.107	0.00371	0.00460	5.10E-02	4.11E-02	2.27E-02
I_{out}	Bridge FPC2	FPC connector	Aluminum	2.65E-08	1.50E-05	0.387	0.00228	0.00371	3.14E-01	1.84E-01	1.16E-01

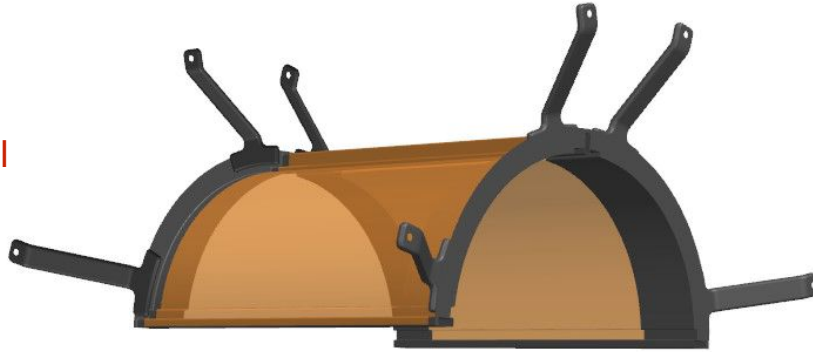
**Assume the I_{in}/I_{out} current is 1.5 A, The power consumption is estimated to be 473 mW.
Including the BFPC, roughly 20% of the total power is dissipated in the FPCs.**

Summary and Outlook

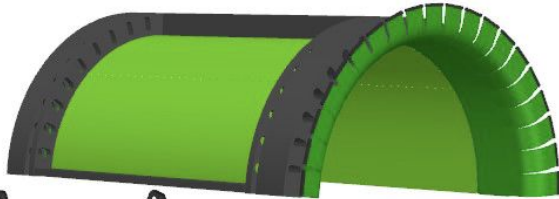
- Low-mass Al FPCs are needed to provide electrical interfaces for SVT disks.
- Designed and fabricated mechanical prototype Cu FPCs to facilitate disk module assembly, considering the current info of EIC-LAS and AncASIC dimensions and pad placements.
- Ongoing studies to optimize FPC design for high-speed data transmission.
 - Simulation studies have indicated that larger perimeter traces have less signal loss.
 - Producing prototype Cu FPCs to study signal transmission and cross-talk with different thickness/width/spacing to validate simulation results.
- Next step: design and fabricate electrically functional Cu and Al FPCs to integrate with AncASIC MPW3 and ER2 sensors and measure the performance.

SVT-IB FPCs

L2 external shell



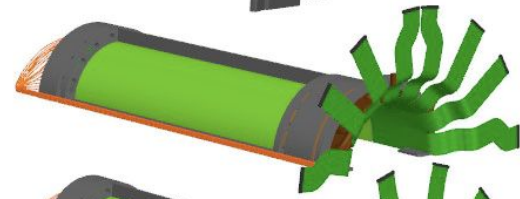
L2



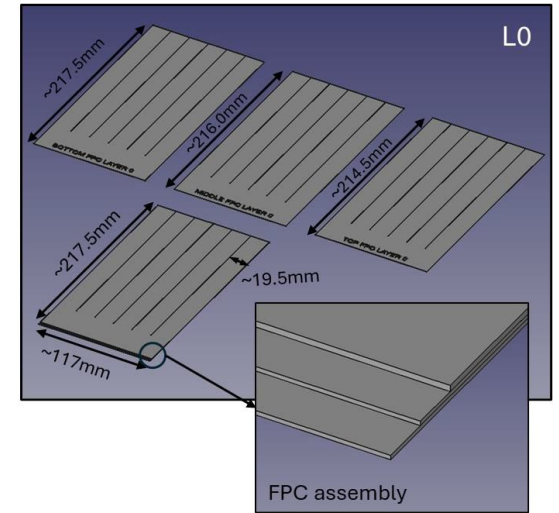
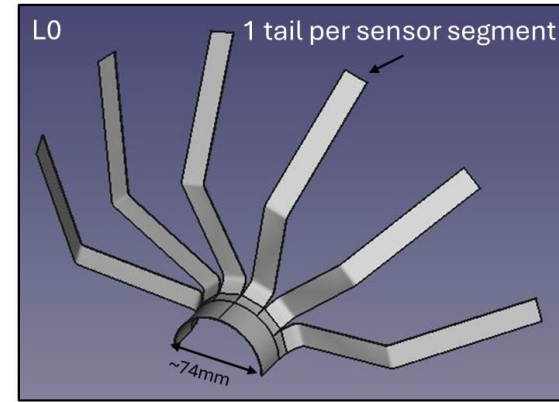
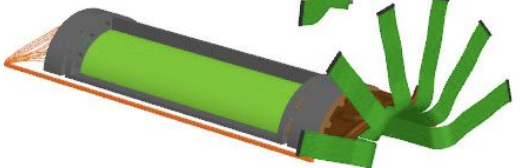
L0-L1
external shell



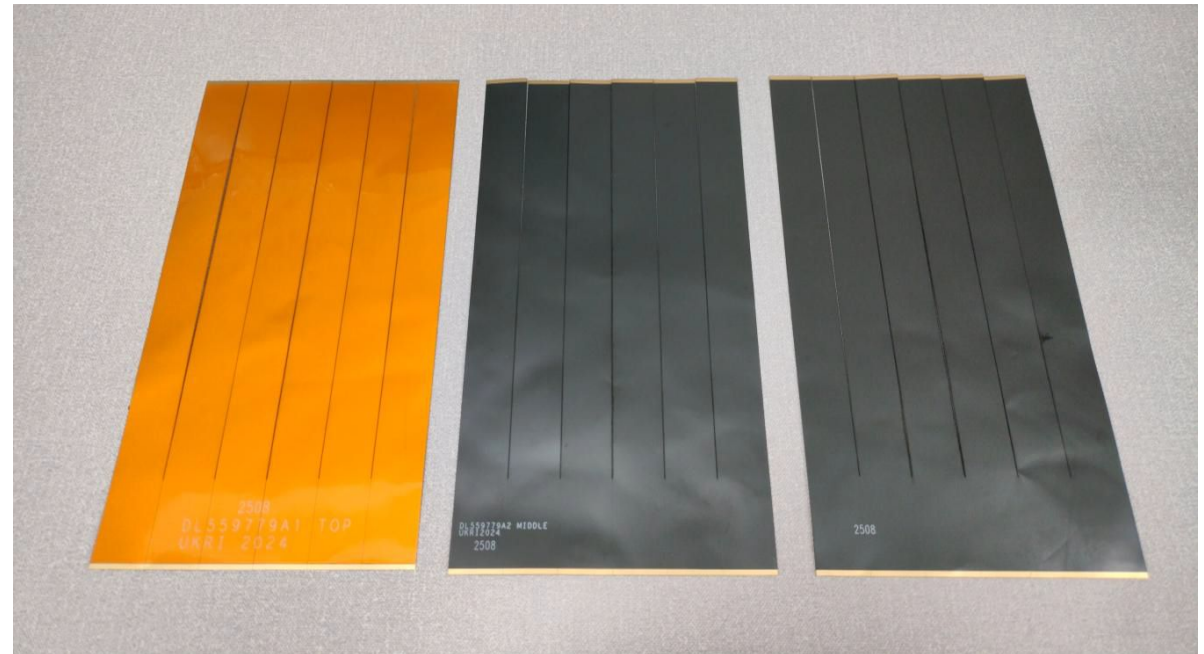
L1



L0

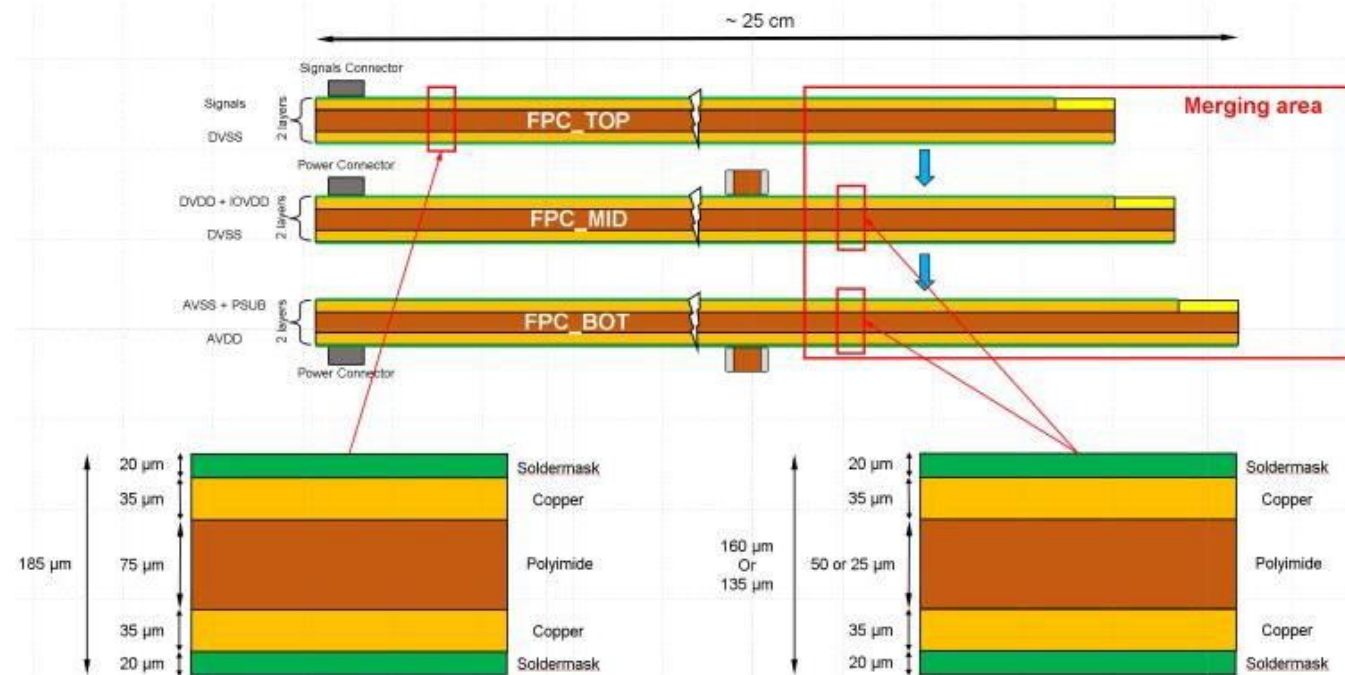
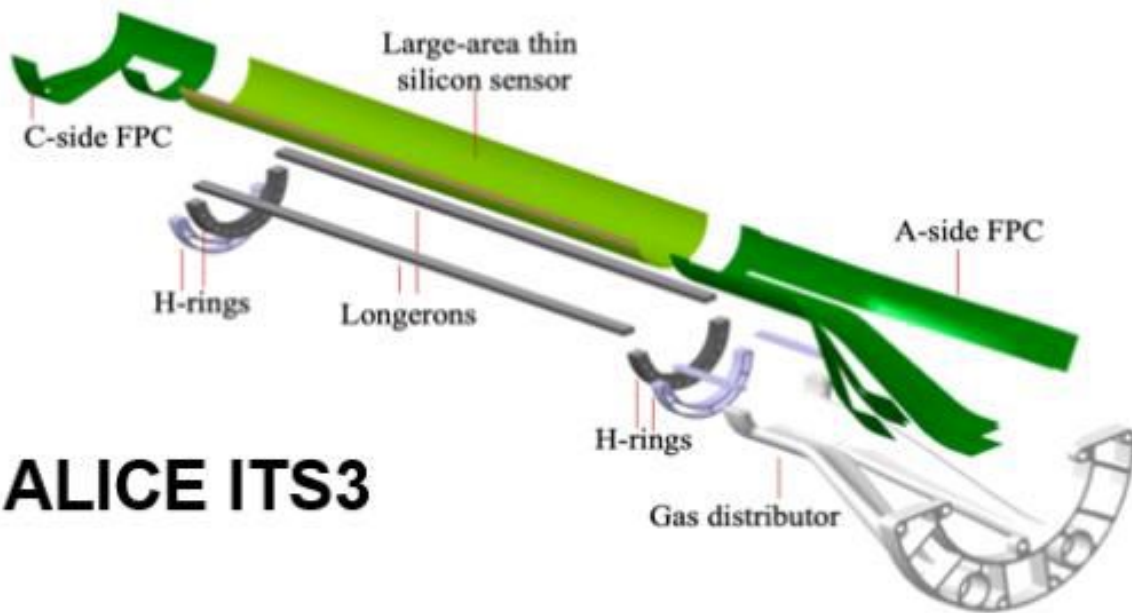


Mechanical FPC prototypes for SVT-IB

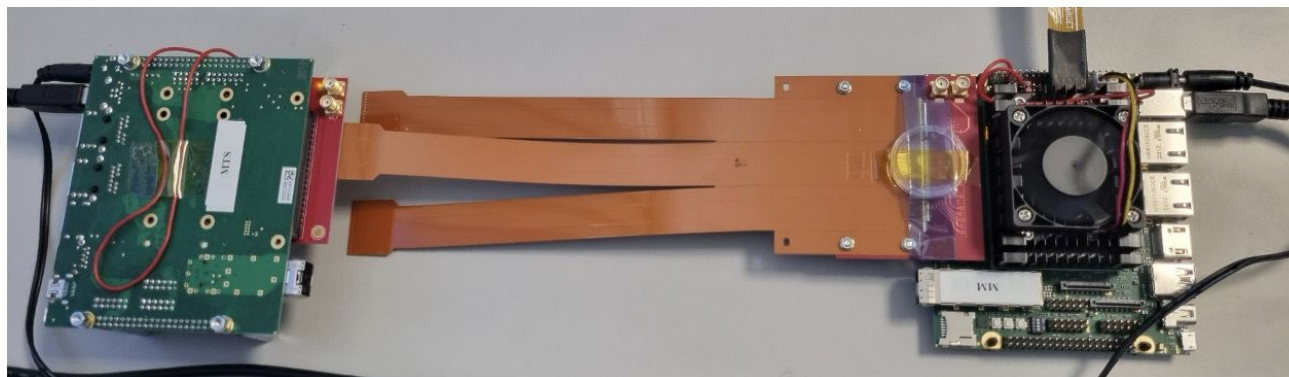


ITS3 FPCs

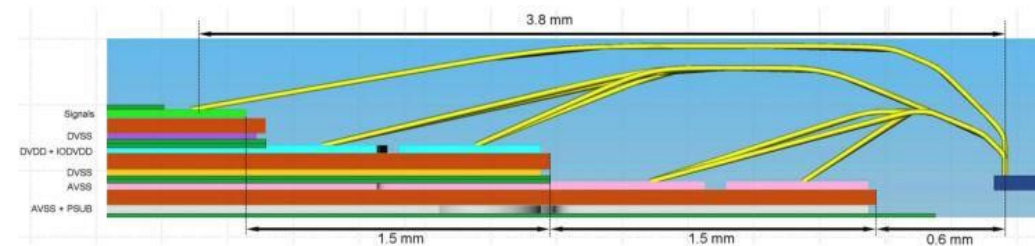
ALICE ITS3

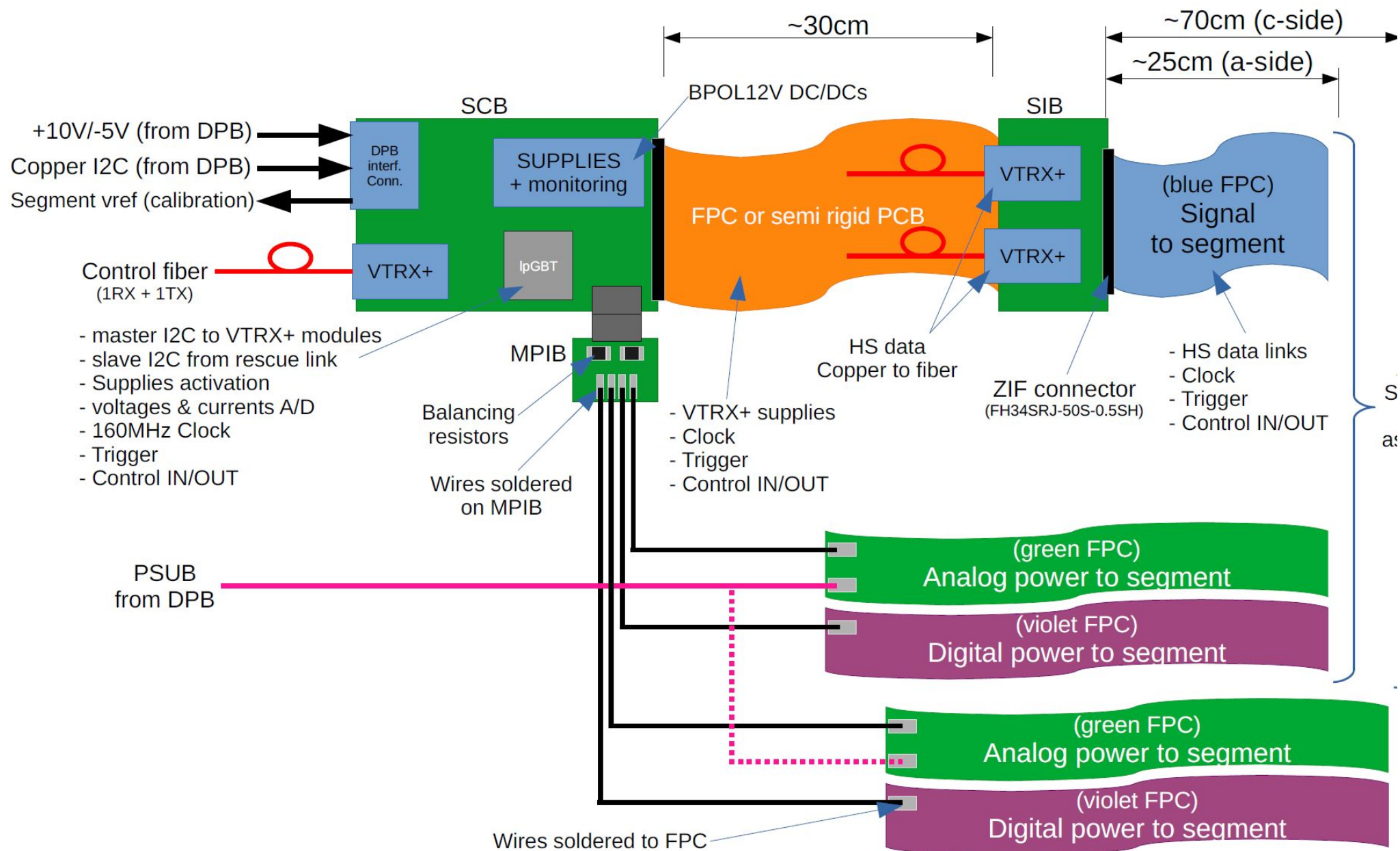


ITS3 test setup

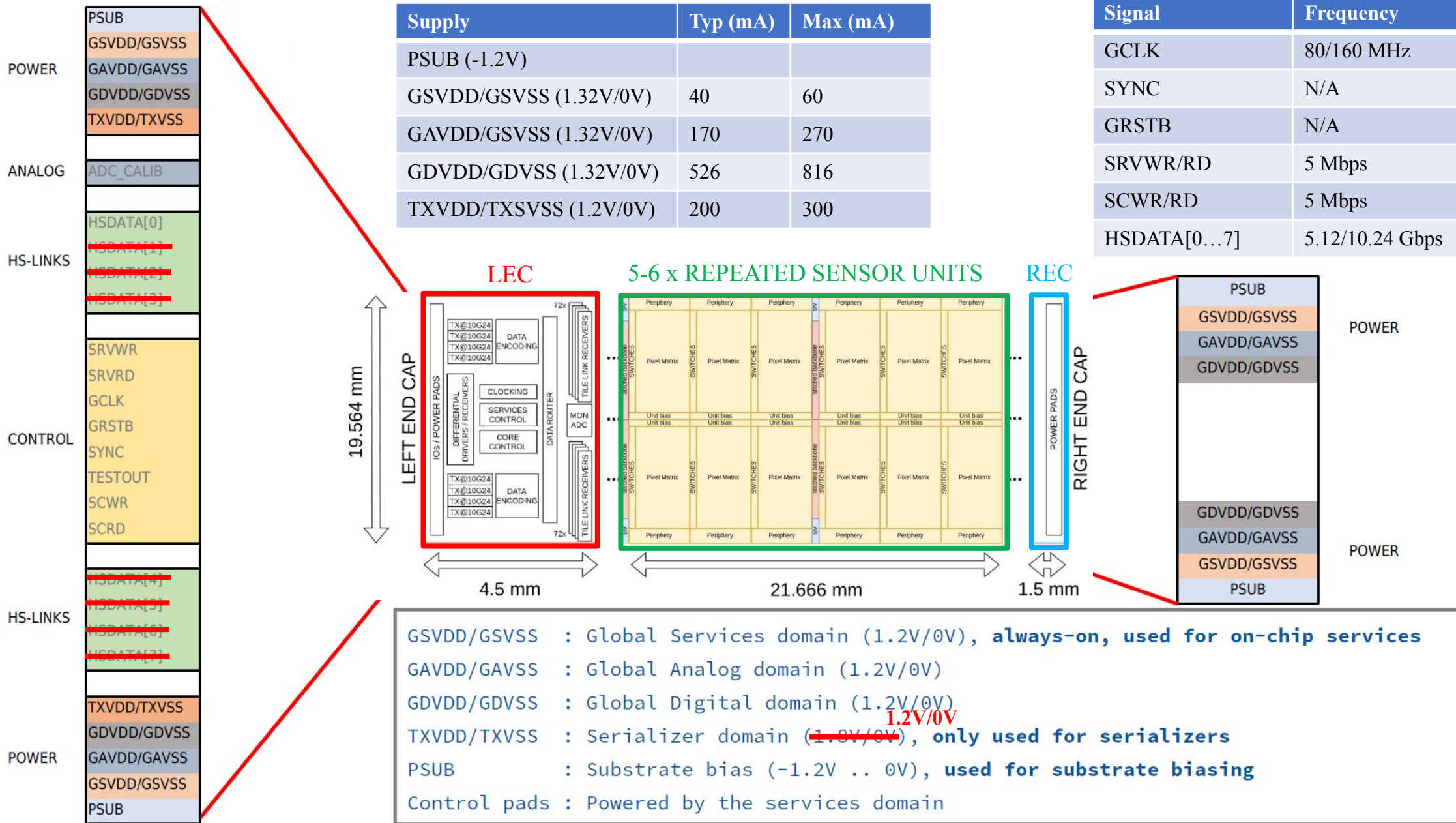


Wire-bond Profile





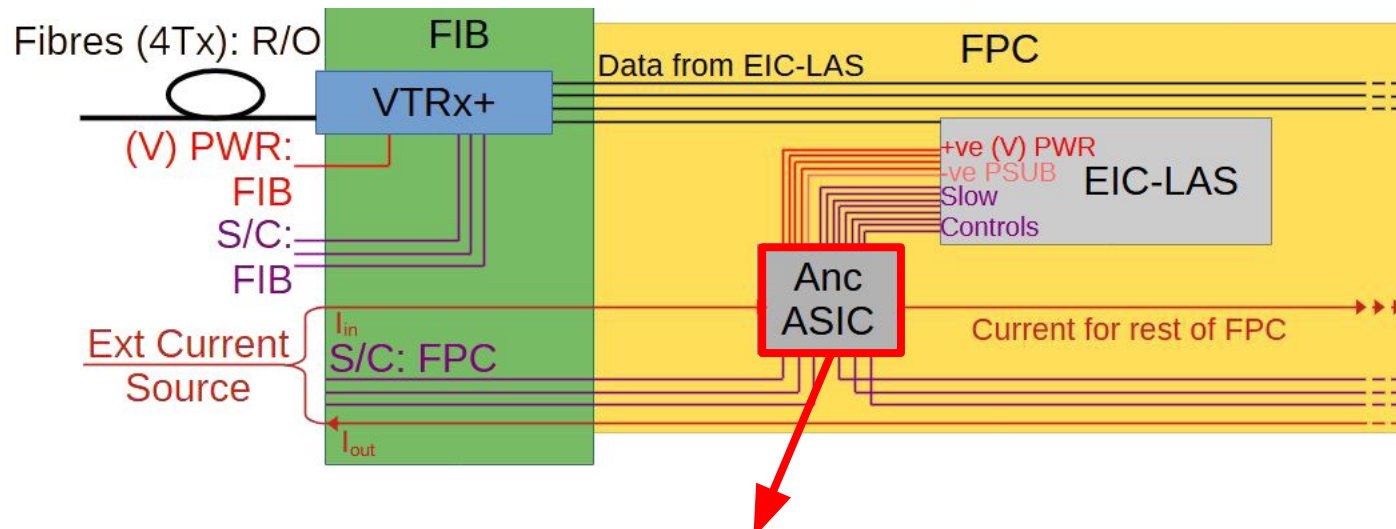
EIC-LAS for SVT OB/Disks



AncASIC and FIB for SVT OB/Disks

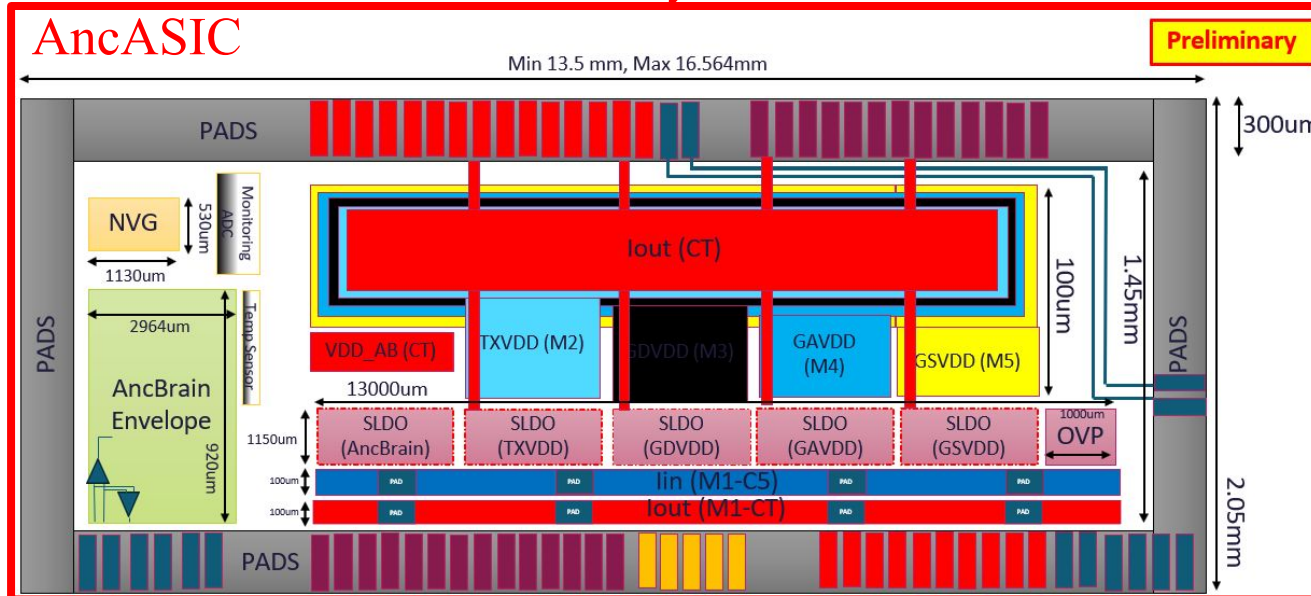
FPC Interface Board

- DC Current for AncASIC to translate to 5 power domains for EIC-LAS.
- S/C for AncASIC to translate to slow control signals for EIC-LAS.
- VTRx+ to receive high-speed data from EIC-LAS and send out by optical fibre

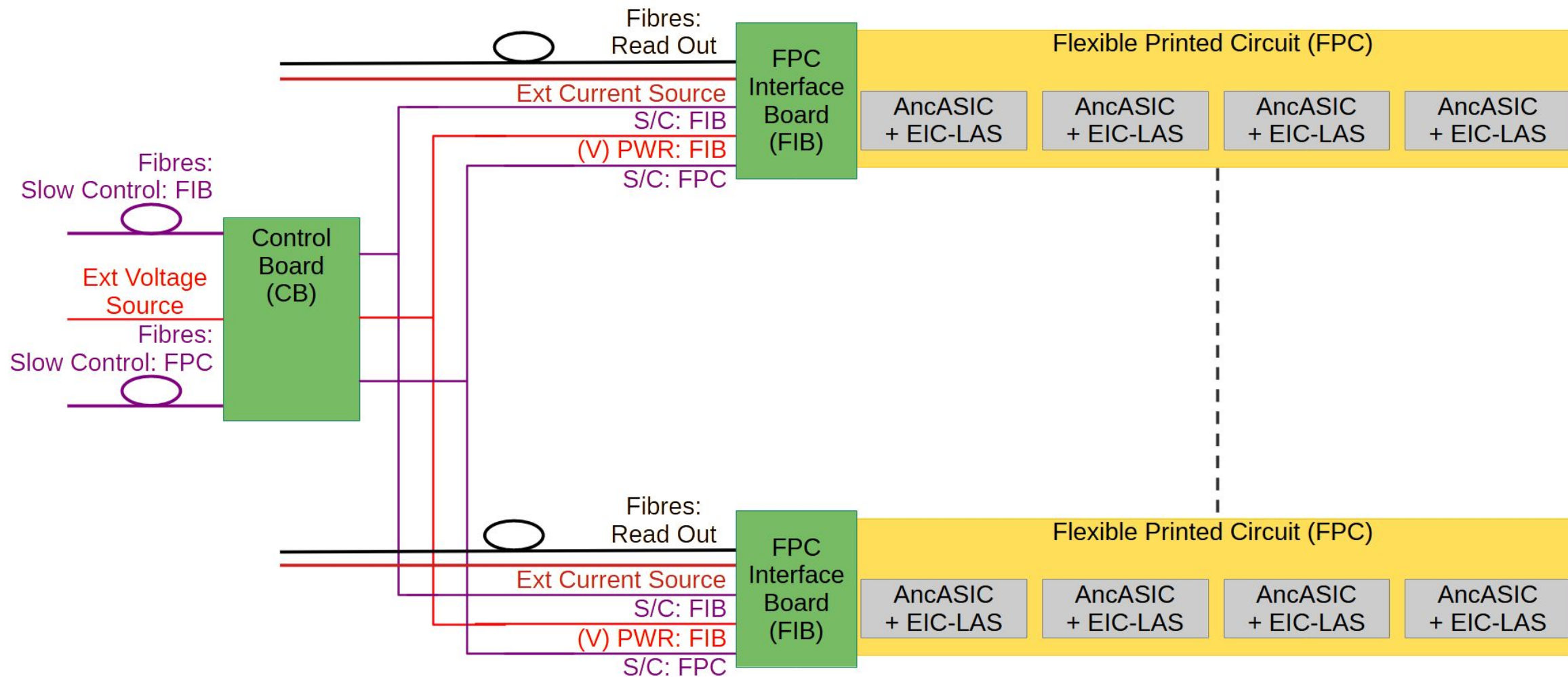


AncASIC Main Building Blocks

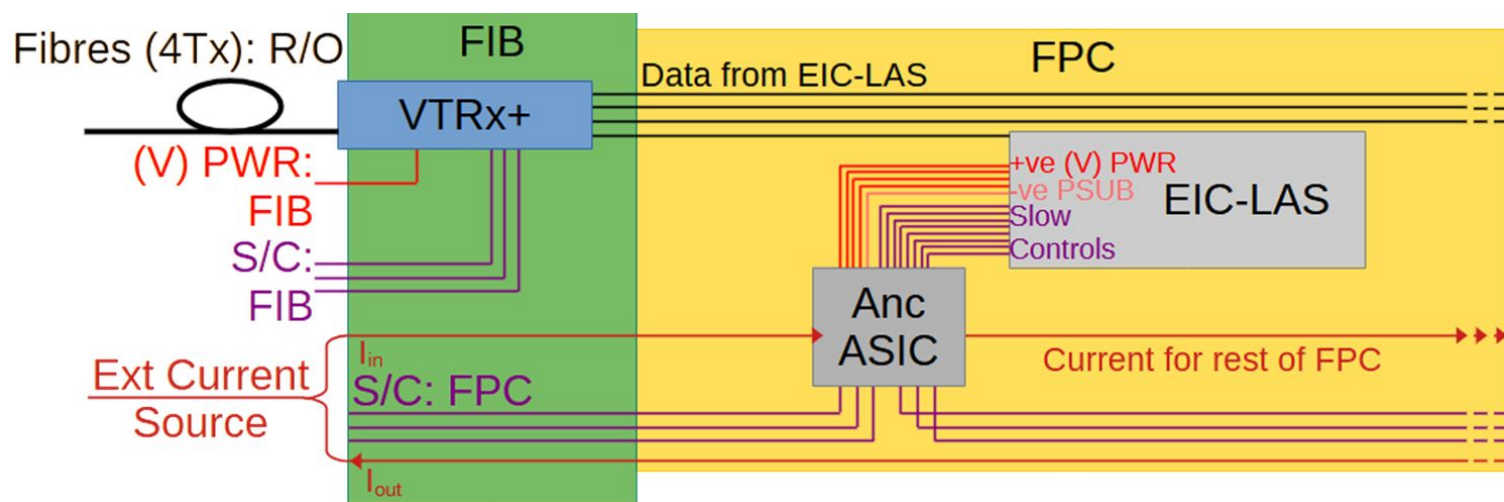
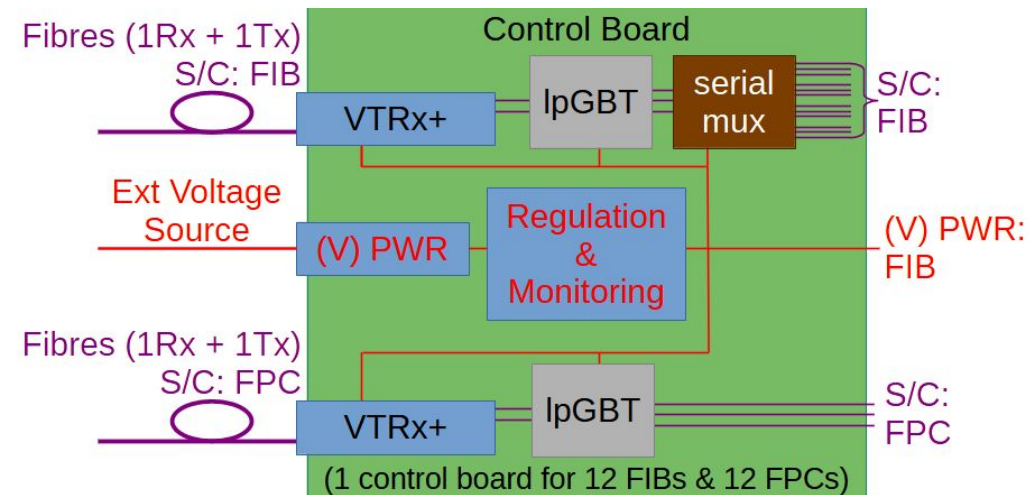
- **Neg. Bias Voltage Generator (NVBG):** frequency-controlled charge pumps
- **Shunt-LDO (SLDO):** serial power with DC current through multiple AncASICs
- **Slow Control (AncBrain):** Daisy-chained connection among multiple AncASICs to reduce the number of traces/cables



SVT OB/Disk Power/Readout Scheme

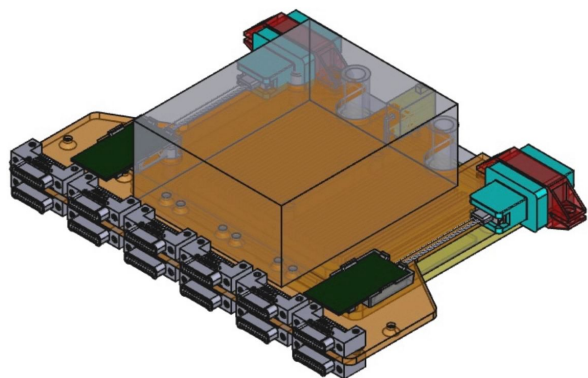


FCB and FIB for SVT OB/Disks



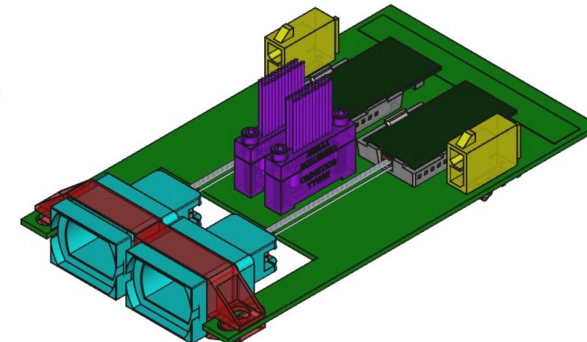
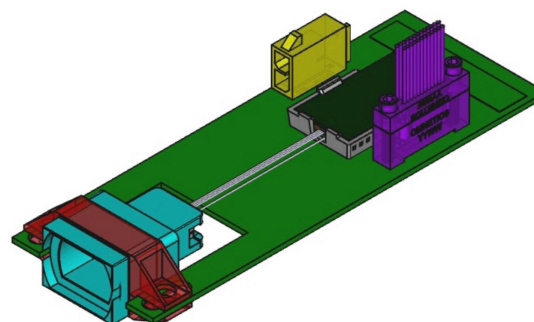
FPC Control Board

- Use the IpGBT e-links for the FPC S/C commands.
- Use the IpGBT I2C master connections for the FIB S/C commands.

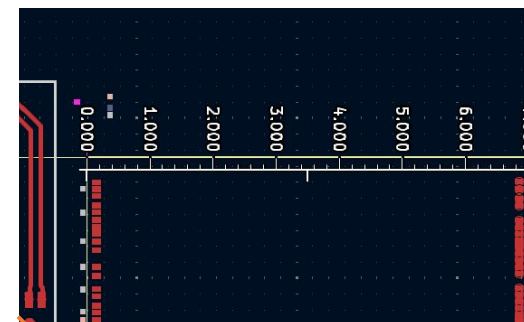
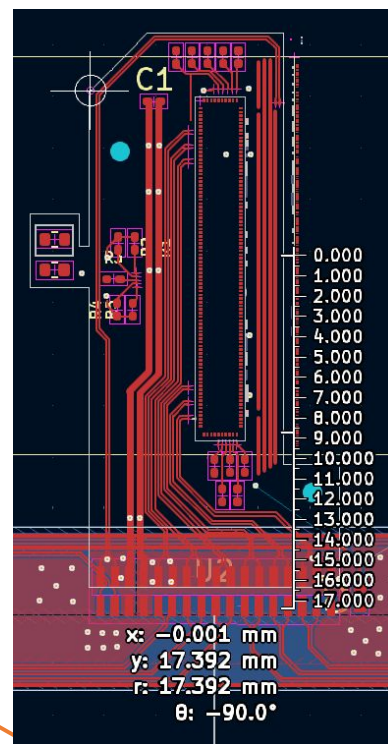
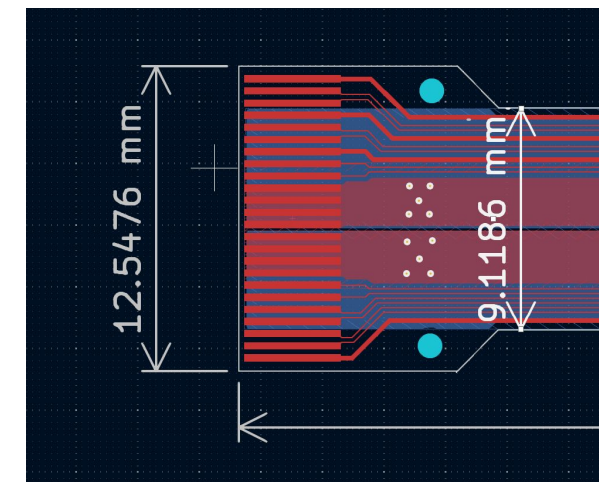


FPC Interface Board

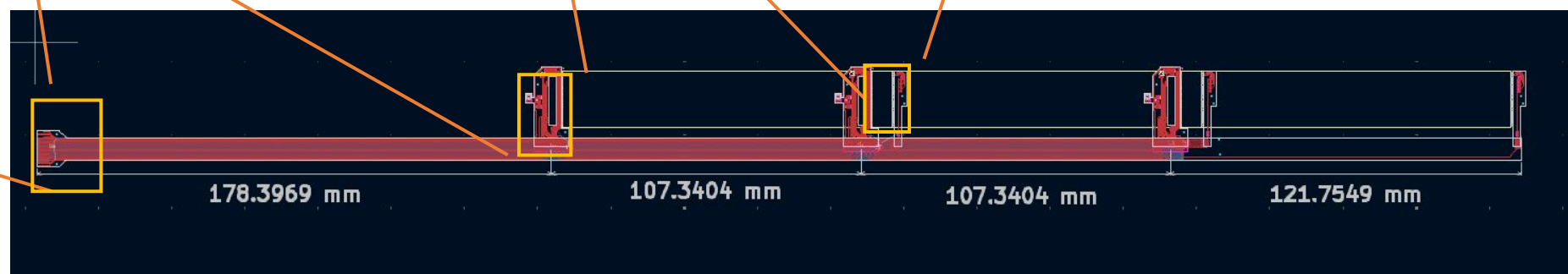
- FIB PWR and S/C for the VTRx+ (EIC-LAS data).
- FPC current supply and S/C for AncASIC to translate to 5 power domains (including NBVG) and slow control protocol for EIC-LAS.



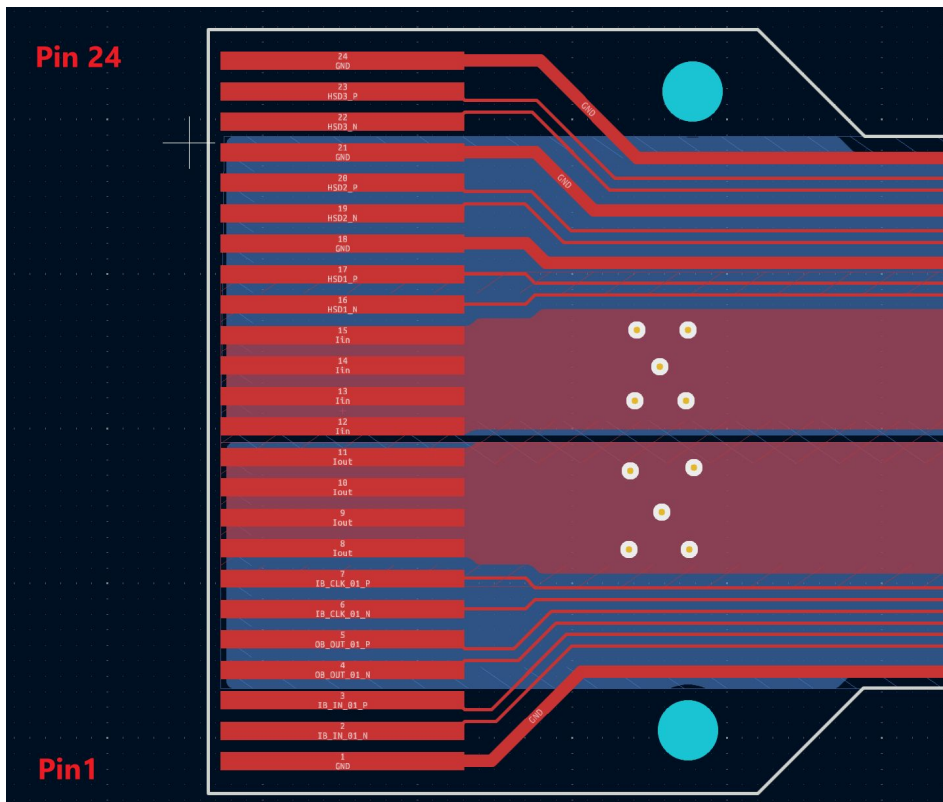
Main FPC - feature dimensions (JLCv1)



Connector end width	12.5476mm
Body width	9.1186mm
Total length	514.83mm
Distance between Center of sensor and Main FPC	17.392 mm
Overlap of RSU	1mm
Area	4747.6 mm ²
Metal Fill factor Top	0.45
Metal Fill factor Bot	0.68



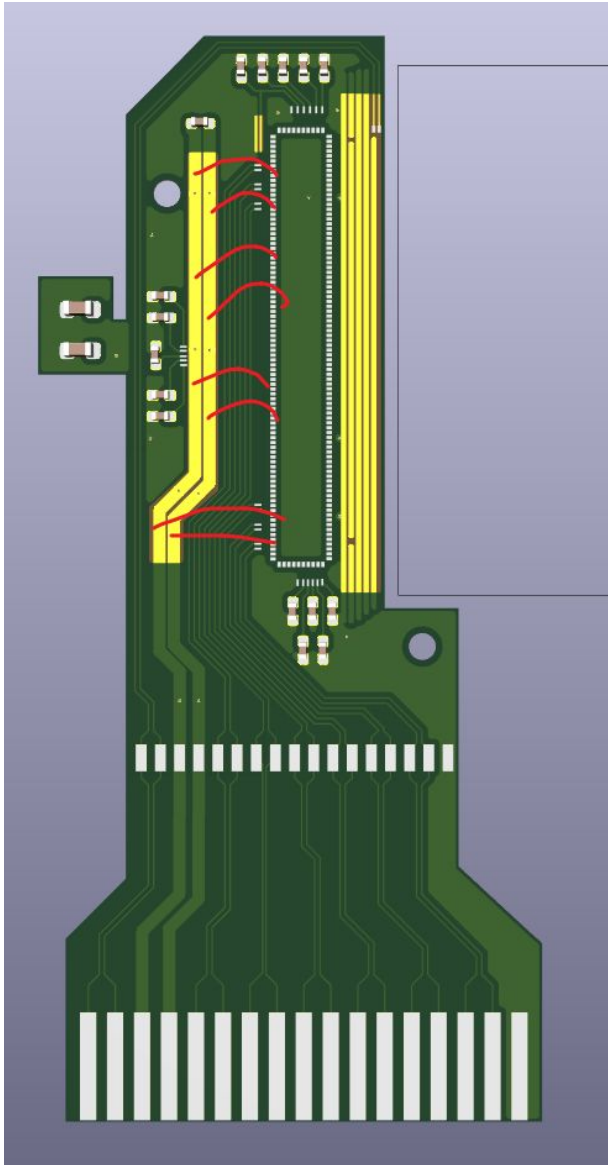
Main FPC - connector and nets (JLCv1)



Pin Number	Description
24,21,18,1	GND trace, width = 0.2 mm
23,22	High Speed Data, connect to Bridge FPC2, width/spacing = 3 mil, length = 387 mm.
20,19	High Speed Data, connect to Bridge FPC1, width/spacing = 3 mil, length = 272 mm.
17,16	High Speed Data, connect to Bridge FPC0, width/spacing = 3 mil, length = 160 mm.
12-15	Iin (See following pages for details)
8-11	Iout (See following pages for details)
7,6	SC_CLK, width/spacing = 3mil,length = 162mm
5,4	SC_OUT, width/spacing = 3mil, length =162 mm
3,2	SC_IN, width/spacing = 3mil, length = 164 mm

Note: All GND traces are not interconnected on the main FPC; therefore, common grounding must be established externally (e.g. FIB) if needed.

Bridge FPC power consumption – I_{in}/I_{out} (JLCv1)

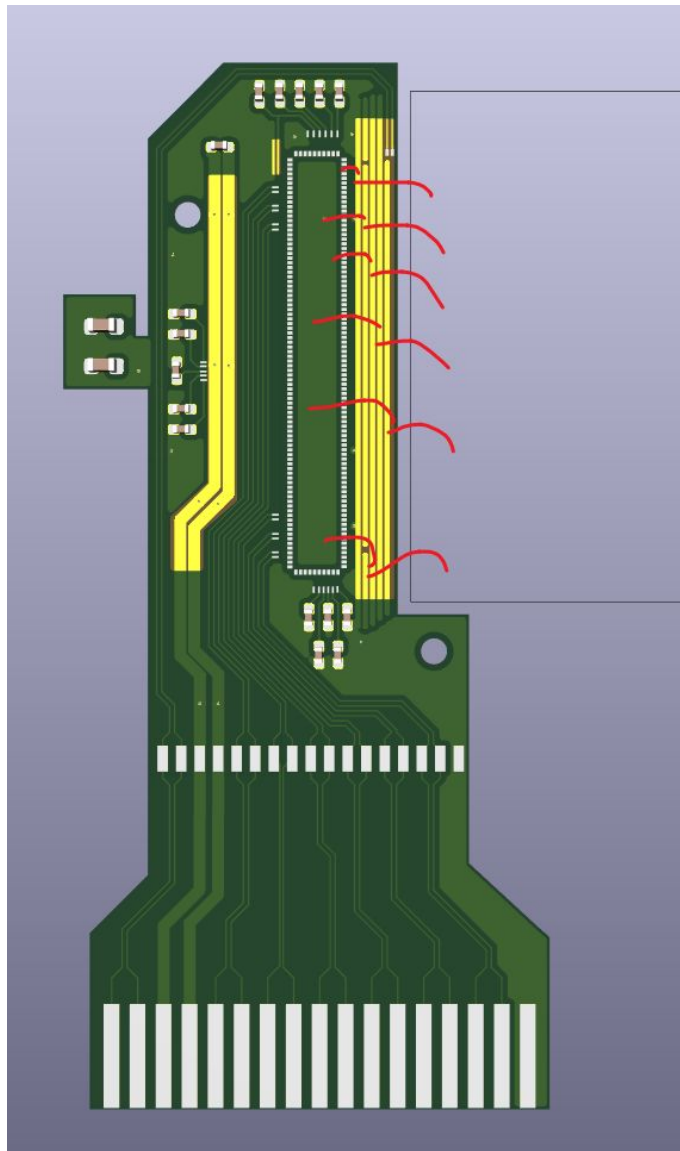


The resistance of I_{in}/I_{out} can be divided into two parts: Trace on FPC and bonding wire.

The estimated resistance and the parameters that used in the calculation is shown in the following:

Trace on FPC		Bonding wire	
ρ :Resistivity@20°C (ohm·m)	2.65E-8	ρ :Resistivity@20°C (ohm·m)	2.65E-8
H:Thickness (m)	1.50E-5	D:Diameter (m)	2.54E-5
W:Width on top (m)	0.0003084 (lin/lout)	L:Mean length (m)	0.0029(lin); 0.0023(lout)
Width on the bottom (m)	0.0022(lin); 0.0027(lout)		
L:Mean length (m)	0.017(lin/lout)	N:wire number	27(lin); 40 (lout)
Resistance (ohm)	0.0118 (lin) 0.0098(lout)	Resistance (ohm)	5.6e-3(lin);3e-3(lout)

Assume the current is 1.5 A, The power consumption is estimated as 68 mW. The main contribution is from the trace of I_{in}/I_{out} on FPC (~49 mW).



The power consumption of TXVDD/GSVDD/GAVDD/GDVDD can be divided into two parts: 1. From AncASIC to power bus; 2. From the power bus to the left edge of LAS (Power loss on the power bus is insignificant, as the current travels only a short distance on the it);

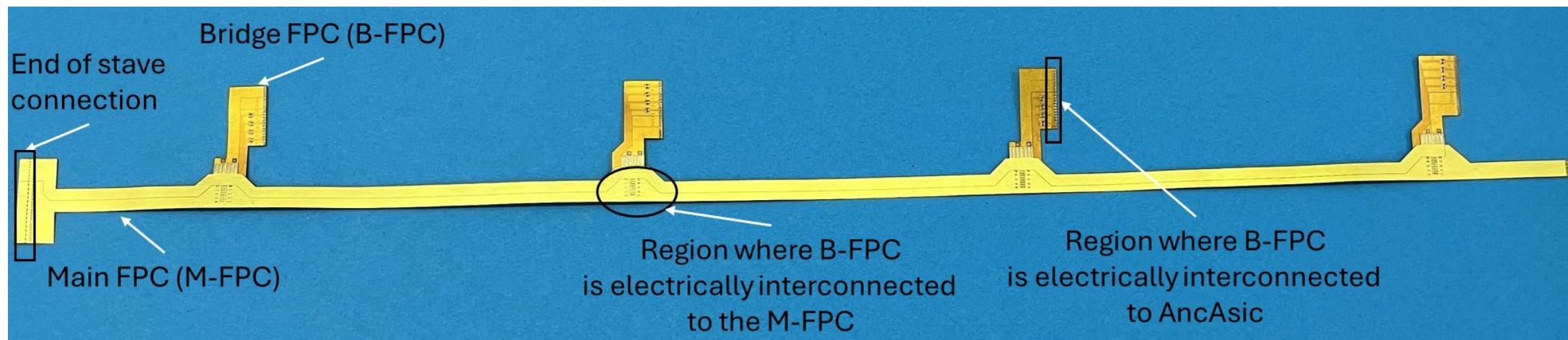
From AncASIC bonding to power bus		From power bus to left edge of LAS	
ρ : Resistivity@20°C(ohm·m)	2.65E-8	ρ : Resistivity@20°C (ohm·m)	2.65E-8
D:Diameter (m)	2.54E-5	D:Diameter (m)	2.54E-5
L(mm):	0.8(TXVDD); 1.1(GSVDD); 1.4(GAVDD); 1.7(GDVDD)	L1(mm):	1.9(TXVDD); 1.6(GSVDD); 1.3(GAVDD); 1(GDVDD)
Number of bonding wire:	3 (TXVDD); 6(GSVDD); 4(GAVDD); 15(GDVDD)	Number of bonding wire:	6 (TXVDD); 12(GSVDD); 8(GAVDD); 20(GDVDD)
Resistance:	1.4e-2(TXVDD);9.6e-3(GSVDD); 1.8e-2(GAVDD);5.9e-3(GDVDD)	Resistance:	1.7e-2(TXVDD);7.0e-3(GSVDD); 8.5e-3(GAVDD);2.6e-3(GDVDD)

Calculate the operating current for each power based on updated numbers form Chamonix:

The power consumption on power net is 6.3 mW

	Voltage(V)	Typ Power (mW)			Max Power (mW)		
		ESR	Cham	Cham-SC	ESR	Cham	Cham-SC
GAVDD	1.32	222	222	222	356	356	356
GDVDD	1.32	908	1052	349	1148	1280	560
GSVDD	1.32	52	38	38	78	55	55
TXVDD	1.2	240	71	66	360	100	91
Total (LAS)		1422	1382	675	1942	1791	1062

STFC-LTU FPC Prototypes

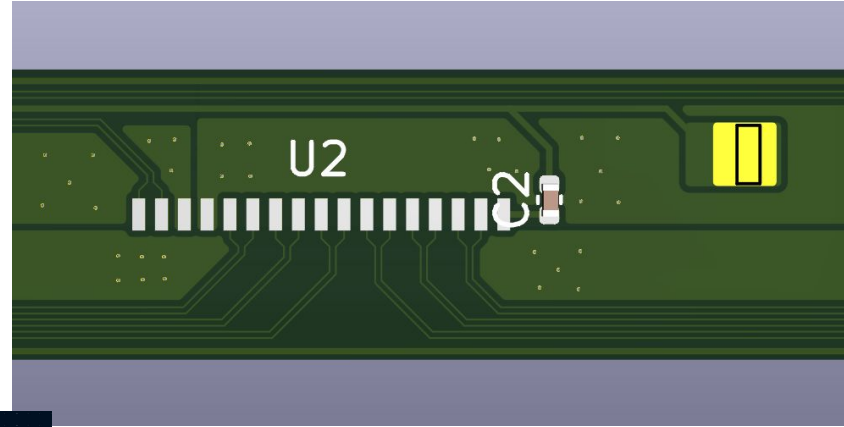


Cover layer (insulating)	Pi 12.5 (25)um	Kapton	Ni-SnBi (for soldering)
Glue ~5um			
Top Layer (signals)	Al 14um	FDI-A-24	
Pi 10um			
Glue ~5um			
Spacer	Pi 25um	Kapton	
Glue ~5um			
Bottom (GND)	Al 14um	FDI-A-24	
Pi 10um			

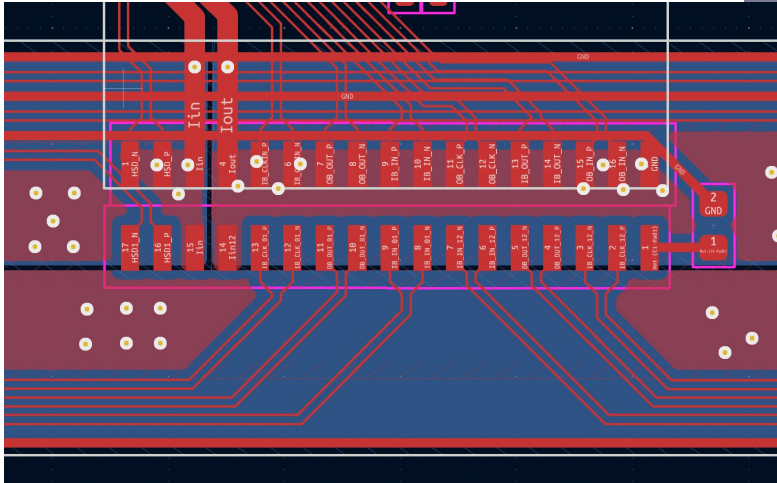
LTU FPC

Components	Thickness (um)	Material	X0(cm)	X0(%)
Metal layers	15 + 15*0.69	Aluminum	8.897	0.028
Dielectric	10+10+25+25	Polyimide	28.57	0.023
glue	15	TBC	39.07	0.004
Total				0.055

Connecting Bridge and Main FPCs (JLCv1)

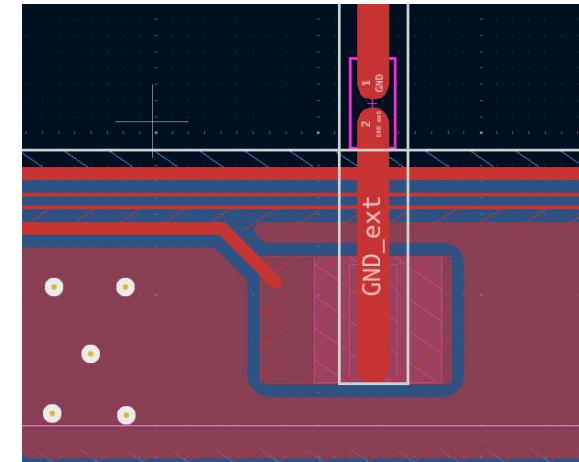


Left Bridge FPC:



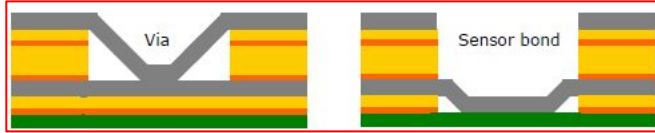
The left bridge FPC will be soldered to the main FPC by 17 pairs of pads. **Each pad has width 0.4mm, length 1mm, pitch 0.7mm.**

Right Bridge FPC:



The right bridge FPC will be soldered to the main FPC by 1 pair of pads.

spTAB vs wire-bonding on LTU FPCs



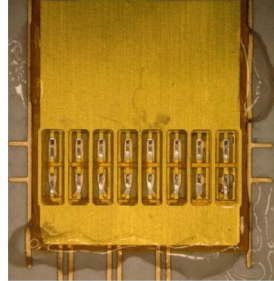
M-FPC prototype 2

- New FPC installed using an update jig from Oxford.
- Nylon stand-offs used as weights to aid alignment of FPC.
- UV-cure glue-dots used to hold FPC flat and aligned during bonding.
- Additional glue added to FPC edges post-bonding.

Prototype 1 trials reported in March

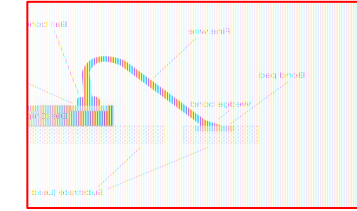


SVT WP3 – Elec Interfaces



Summary

- 2nd FPC prototype has been bonded.
- Bonded went well.
- No (obvious) damage seen from a visual inspection.
- Basic electrical continuity confirmed @ Birmingham
- Sent to Daresbury Lab for further testing.



Parameter matrix & 15 μ m overtravel

Parameter Matrix

Parameters	Based on PCB			Thinner Diffuser			Thinner Diffuser			Based on PCB			Thinner Diffuser			Thinner Diffuser		
	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev
22USW 22CN	20	11.18	0.89	17	7.9	1.18	17	9.88	1.83	19	10.73	1.77	19	11.11	2.24	15	11.65	0.49
26USW 22CN	20	11.46	0.18	17	6.83	1.76	18	10.83	1.4	20	10.45	1.32	20	11.78	0.43	20	12.12	0.34
26USW 25CN	19	11.28	0.99				20	8.53	1.81	19	11.04	0.87	20	11.1	0.79	20	11.96	0.47
26USW 25CN	20	11.21	0.62				20	9.74	2.15	19	11.03	0.25	20	11.96	0.34	20	11.96	0.79
26USW 25CN	20	11.33	0.35				12	6.61	1.84	20	11.04	0.88	20	11.11	1.09	20	11.77	1
30USW 25CN	20	11.04	0.8				17	7.95	2.04	20	11.06	0.69	20	11.87	0.53	20	11.43	1.41
30USW 30CN	16	10.49	0.82				17	5.89	2.1	20	11.03	0.49	20	11.87	0.68	20	10.99	1.38
32USW 30CN	20	10.90	0.65				13	5.66	1.95	20	10.8	0.82	20	12.07	0.58	20	12.16	0.75
32USW 30CN	20	10.66	0.77				4	5.68	1.32	20	9.45	1.2	20	11.18	1.29	20	11.04	1.89

15 μ m Overtravel

Parameters	Based on PCB			Thinner Diffuser			Based on PCB			Thinner Diffuser			Thinner Diffuser			Thinner Diffuser		
	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev	No of Wires	Mean	Std Dev
22USW 22CN	20	11.21	0.4				18	10.87	1.01	20	11.48	0.44	17	11.27	1.19	19	11.99	0.86
26USW 25CN	20	10.89	0.89	20	8.69	1.65	20	9.42	1.45	20	10.96	1.09	20	11.93	0.52	20	10.83	1.58
26USW 25CN	20	11.34	0.39	18	8.97	1.1	17	9.24	2.1	20	11.34	0.85	20	11.94	0.63	20	12.06	0.55
26USW 25CN	20	10.79	0.94	11	3.8	1.09	19	8.37	1.54	20	11.09	0.43	17	10.96	1.14	20	11.89	0.9
30USW 25CN	20	11.06	0.82				19	8.58	2.33	19	11.09	0.64				20	11.23	1.29
30USW 30CN	20	11.1	0.62				18	10.82	0.76							17	9.4	1.57
32USW 30CN	20	11.25	0.38				20	11.06	0.66							11	10.74	1.33

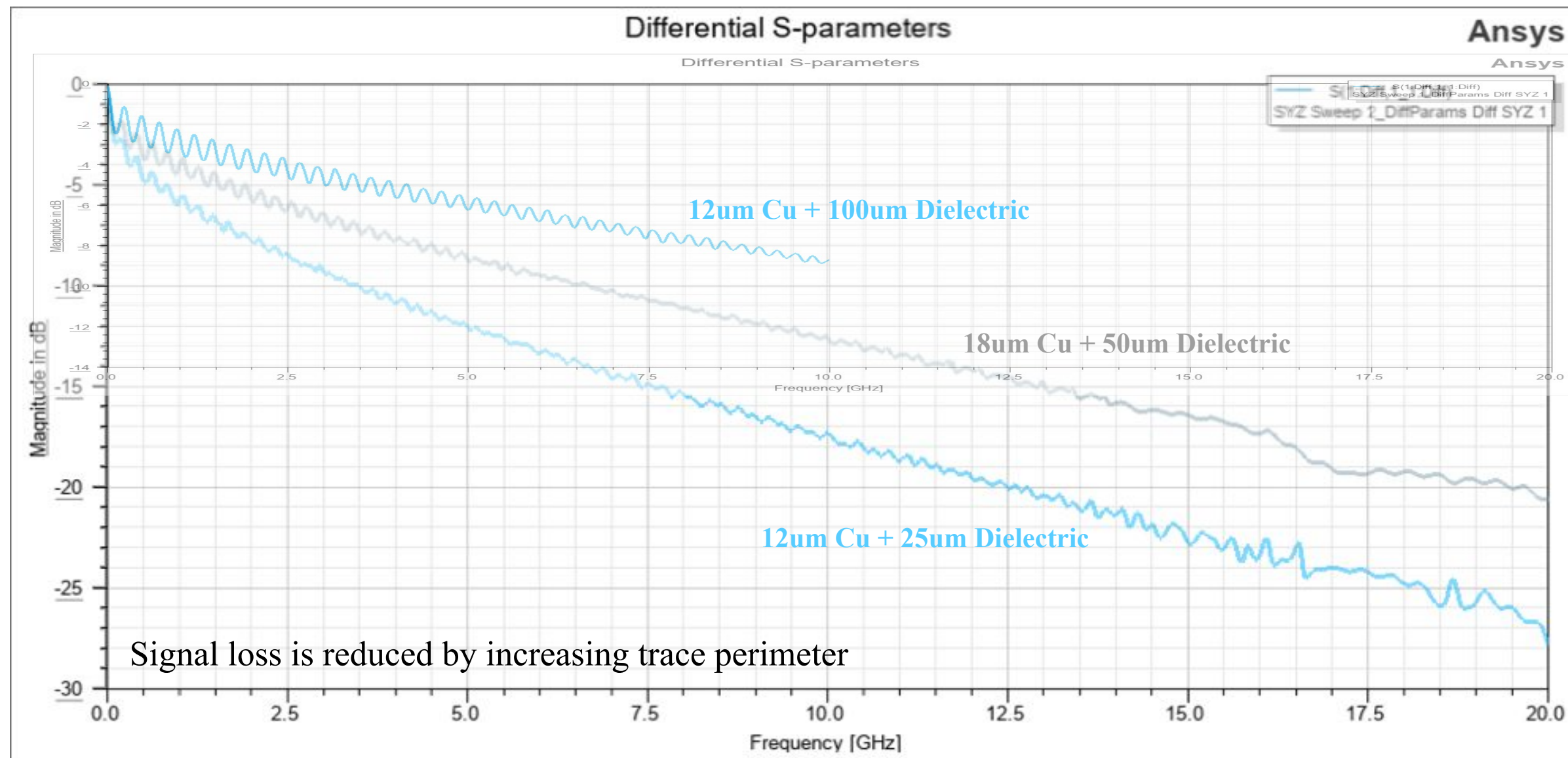
14/07/2025 J. Liu

Summary

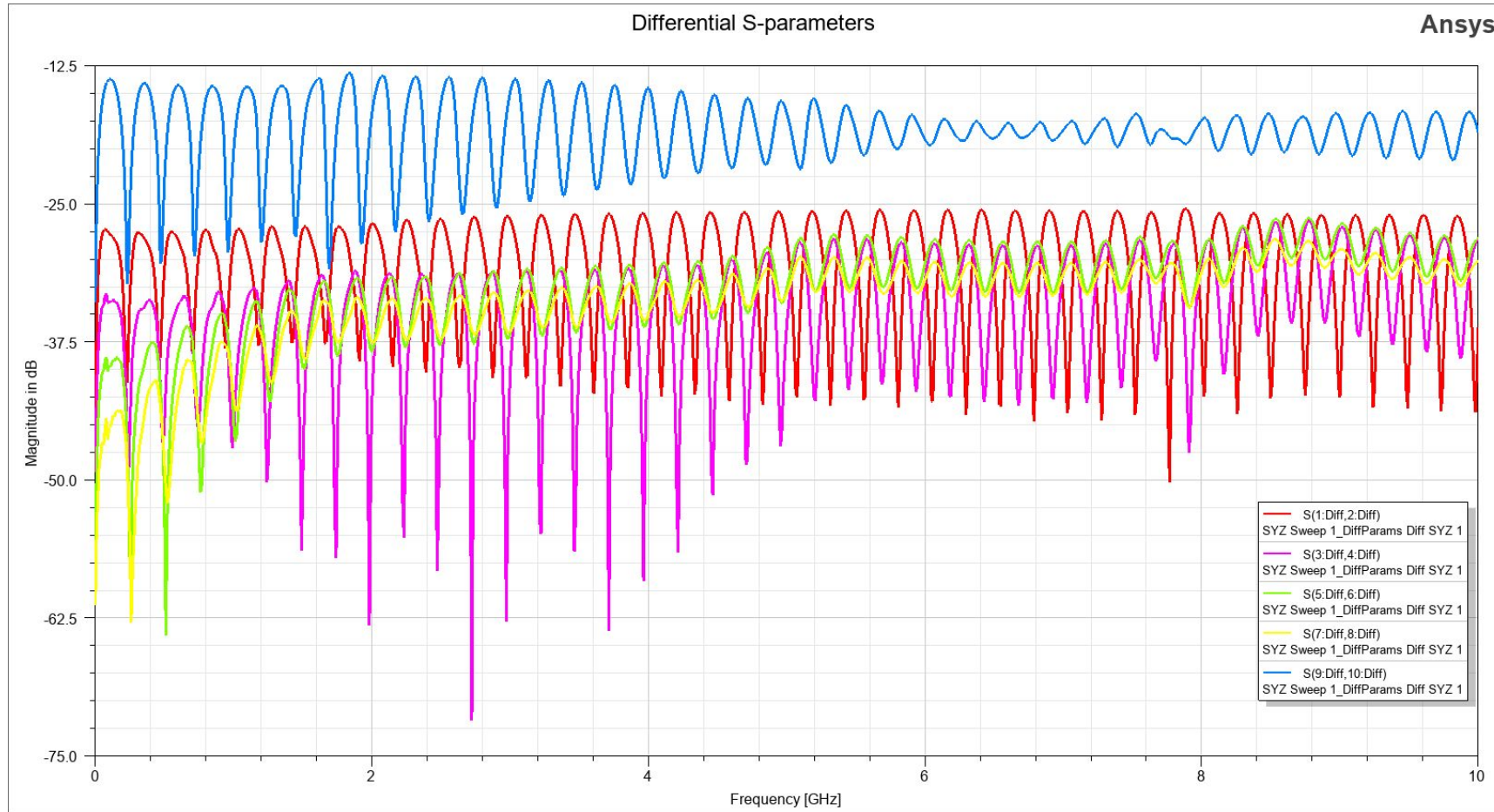
- Bonding quality was superior when foils were glued to a PCB, likely due to the added mechanical stability
- The thinner diffuser significantly improved vacuum-assisted bonding, though some stability challenges remain
- Multi-layer foils consistently offered easier and more reliable bonding, regardless of method
- The study demonstrated that acceptable mean strength and standard deviation values can be achieved
- Next steps:
 - Investigate further improvements for single-layer foils under vacuum. Any suggestions are welcome
 - Consider adjusting touchdown force or tail length
 - Plan comparative tests with alternative wire materials



S-parameters from Simulation



Cross talk for HSD



Diff1&2	W=190, S = 110
Diff3&4	W=190, S = 200
Diff5&6	W=190, S = 300
Diff7&8	W=190, S = 420
Diff9&10	W=190, S = 420+ GND Trace