

SVT DAQ & Slow Control

J. Schambach

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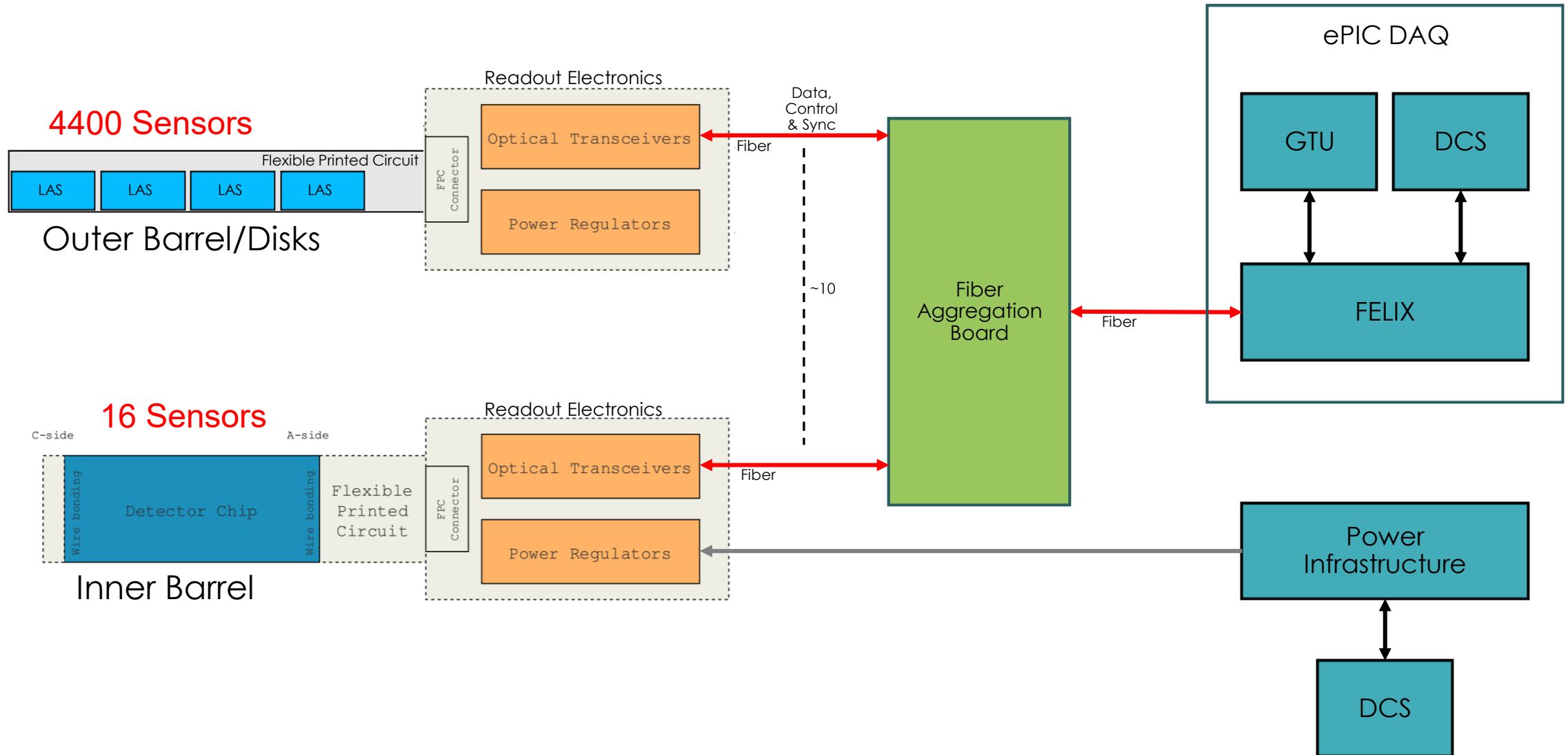
Previous comprehensive talk on DAQ & Slow Controls at the Oxford meeting in December 2025:

https://indico.bnl.gov/event/30334/sessions/8739/attachments/66878/115227/SVT_DAQ_DCS_20251218.pdf

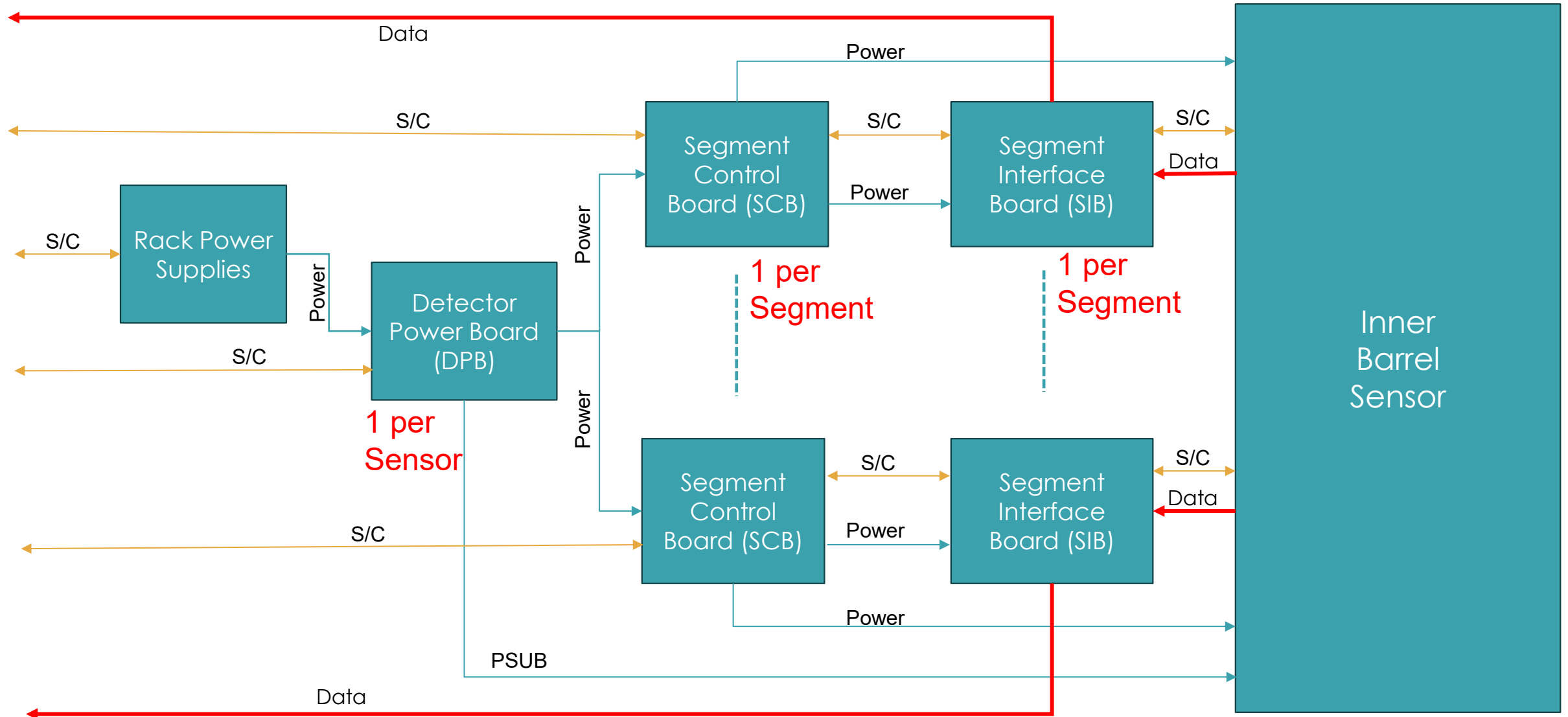
SVT Numbers

						10x275 GeV		
Barrel								
Layer Index	Area (mm^2)	# sensors	# pixels	# Data Fibers	# SC Fibers	Hit Rate/ms	Data Rate (Mbps)	Data Rate / Fiber (Mbps)
L0	58,811	4	119,688,192	96	6	1791732.00	218717.29	6075.48
L1	78,414	4	159,584,256	128	8	1095604.00	133740.72	2786.27
L2	196,035	8	398,960,640	320	20	600729.00	73331.18	611.09
L3	882,158	368	1,835,218,944	368	16	1645551.00	200872.92	545.85
L4	2,216,706	1120	4,654,540,800	1120	48	888591.00	108470.58	96.85
e-endcap								
Disk index								
ED0	176,710	96	398,960,640	96	8	538309.00	65711.55	684.50
ED1	536,815	334	1,388,050,560	334	16	976195.00	119164.43	356.78
ED2	553,632	334	1,388,050,560	334	16	940608.00	114820.31	343.77
ED3	552,835	334	1,388,050,560	334	16	618422.00	75490.97	226.02
ED4	551,127	334	1,388,050,560	334	16	97019.00	11843.14	35.46
h-endcap								
Disk index								
HD0	176,710	96	398,960,640	96	8	438216.00	53493.16	557.22
HD1	536,815	334	1,388,050,560	334	16	624534.00	76237.06	228.25
HD2	553,216	334	1,388,050,560	334	16	165565.00	20210.57	60.51
HD3	548,909	334	1,388,050,560	334	16	14334.00	1749.76	5.24
HD4	542,422	334	1,388,050,560	334	16	7064.00	862.30	2.58
TOTAL	8,161,315	4448	19,070,318,592	4896	242	1.0442E+10 hits/s	1244.8 Gbps	

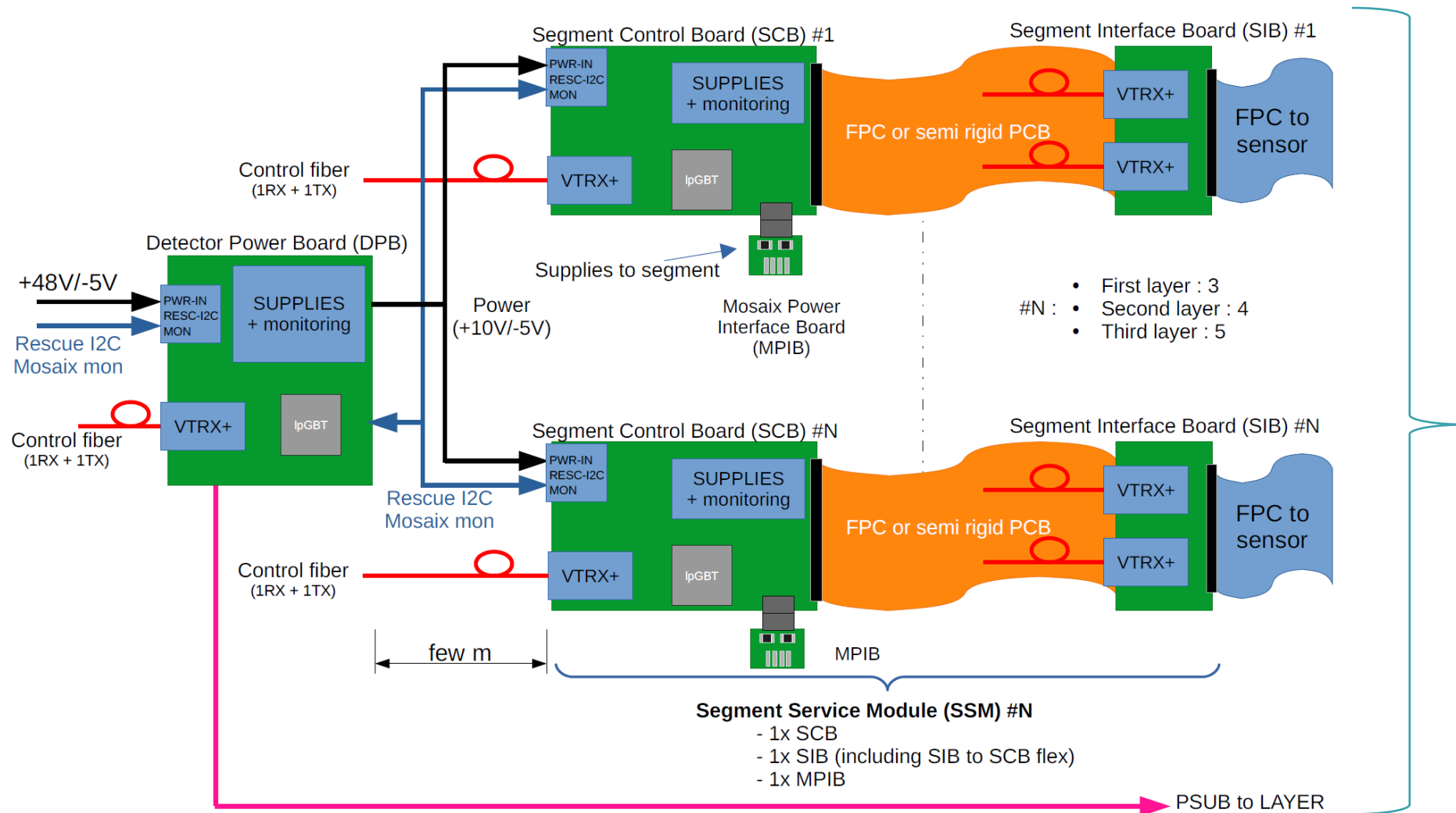
SVT Electronics – Simplified Overview



IB Readout, Power & Controls Scheme



IB Readout Architecture

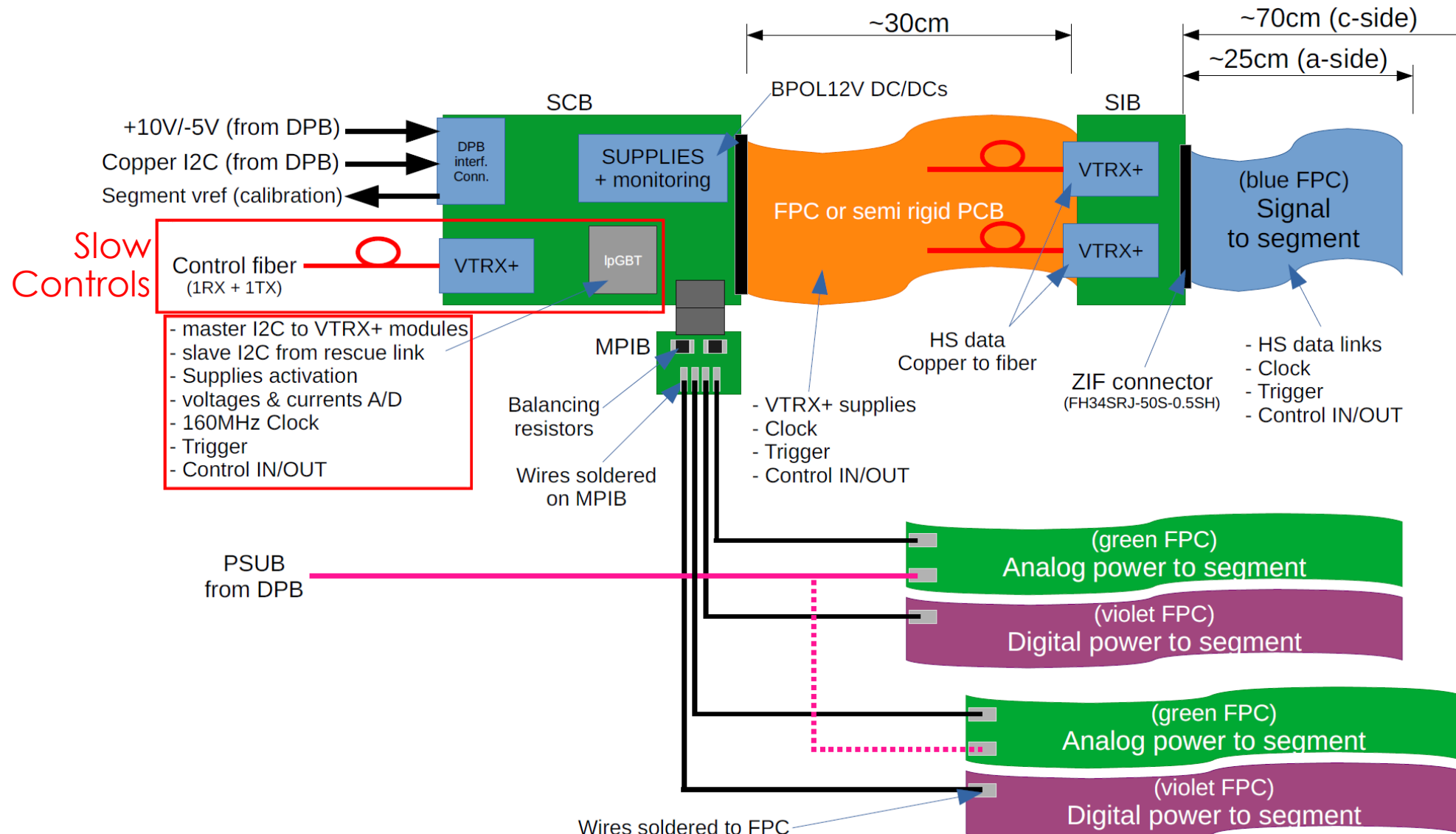


Detector Service Electronics

1 set per sensor

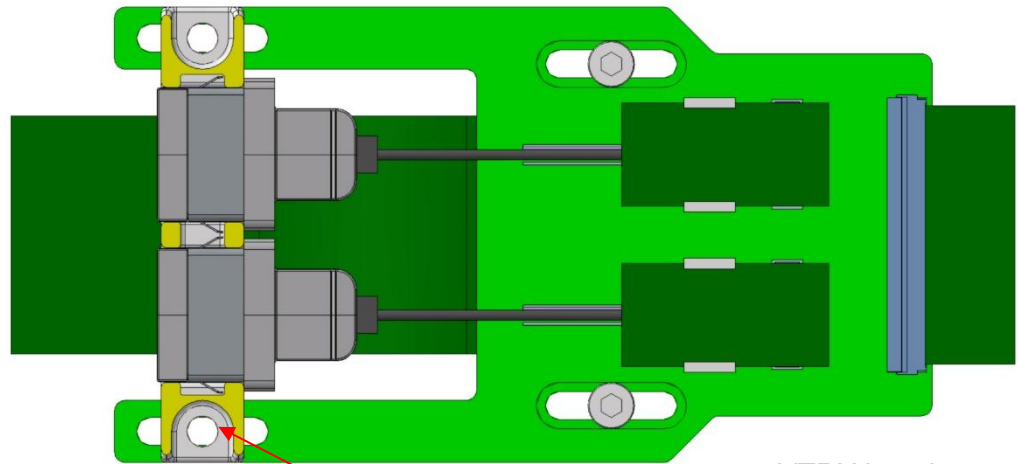
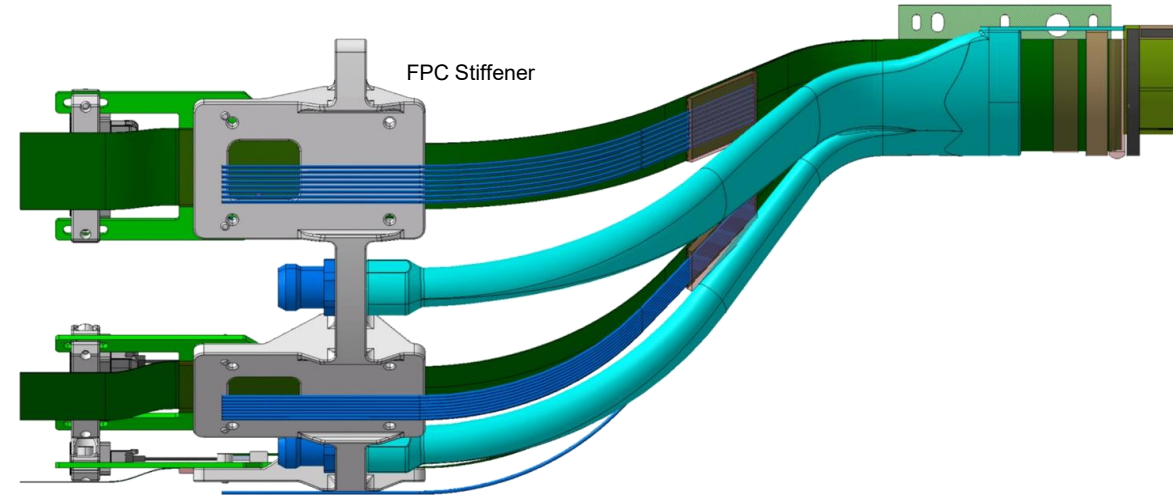
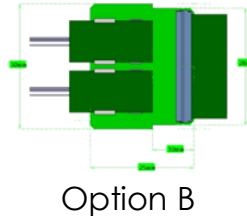
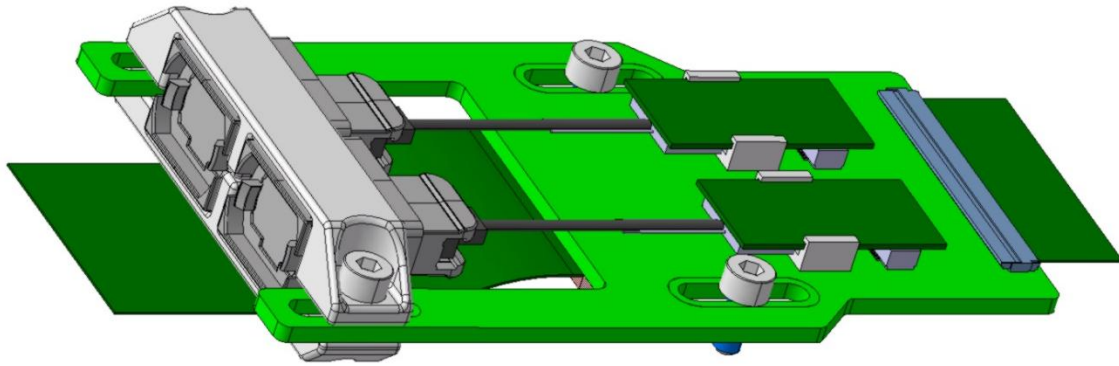
1 DPB
+
3 or 4 or 5 SSM

Segment Readout Architecture



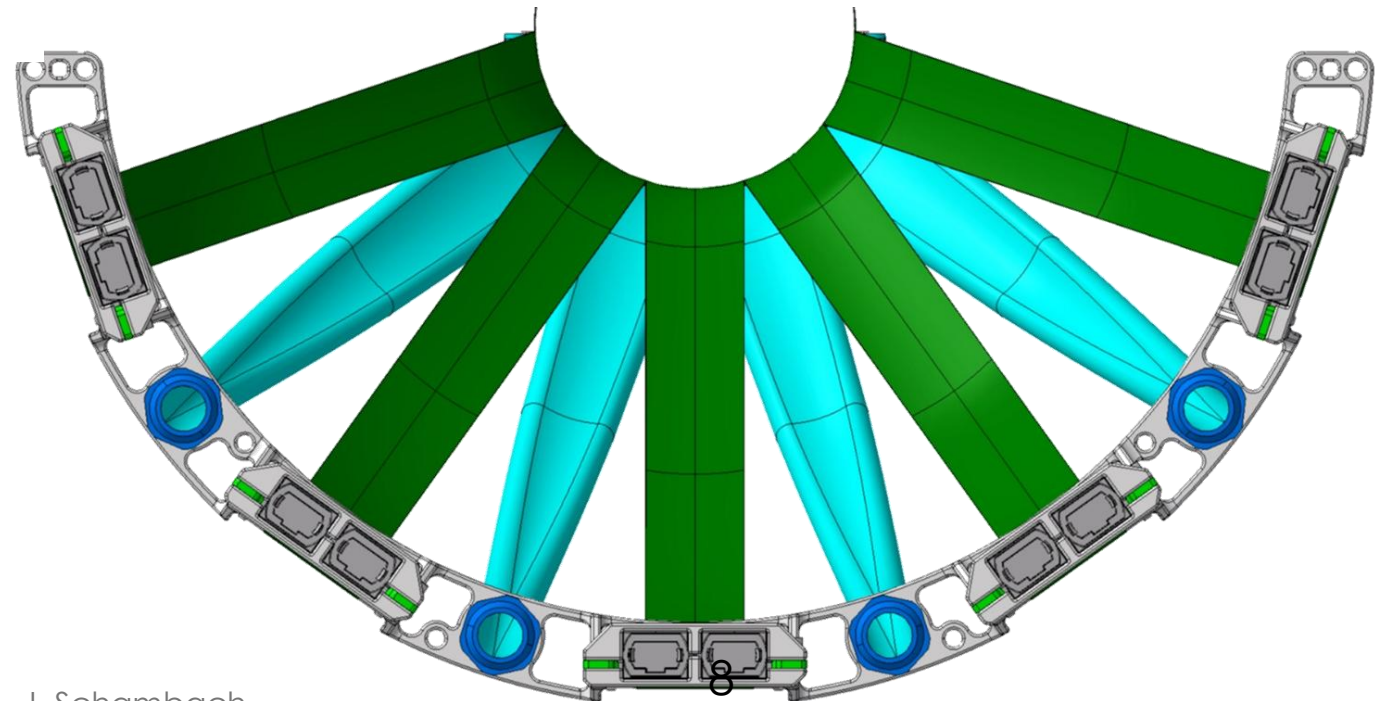
ITS3 SIB Design

Option A: Solution with large SIB boards

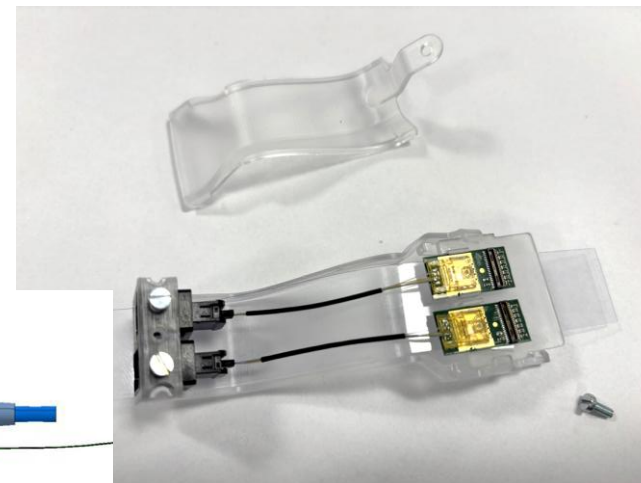
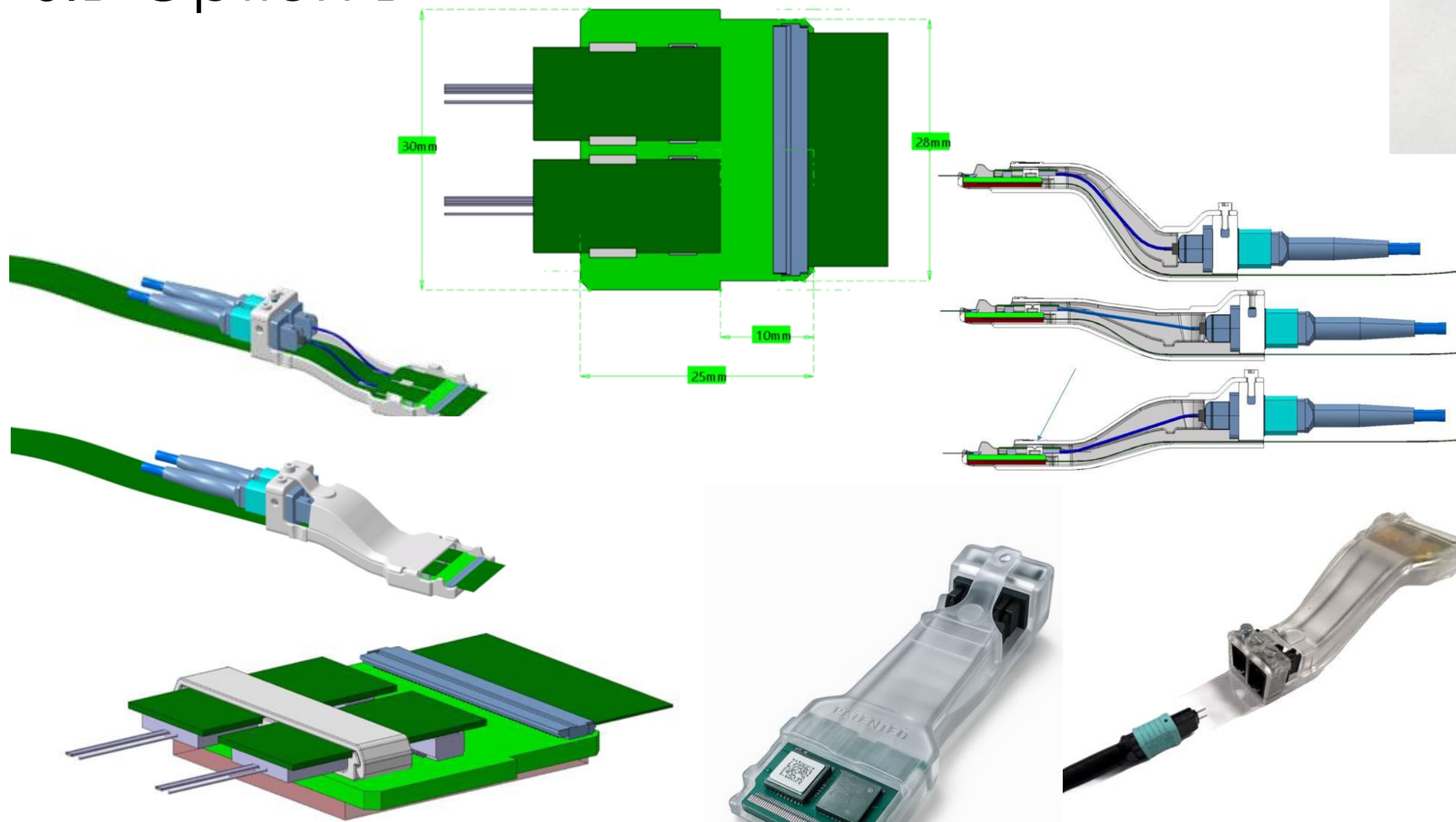


Adjustable

VTRX length 55mm
SIB length 79 mm



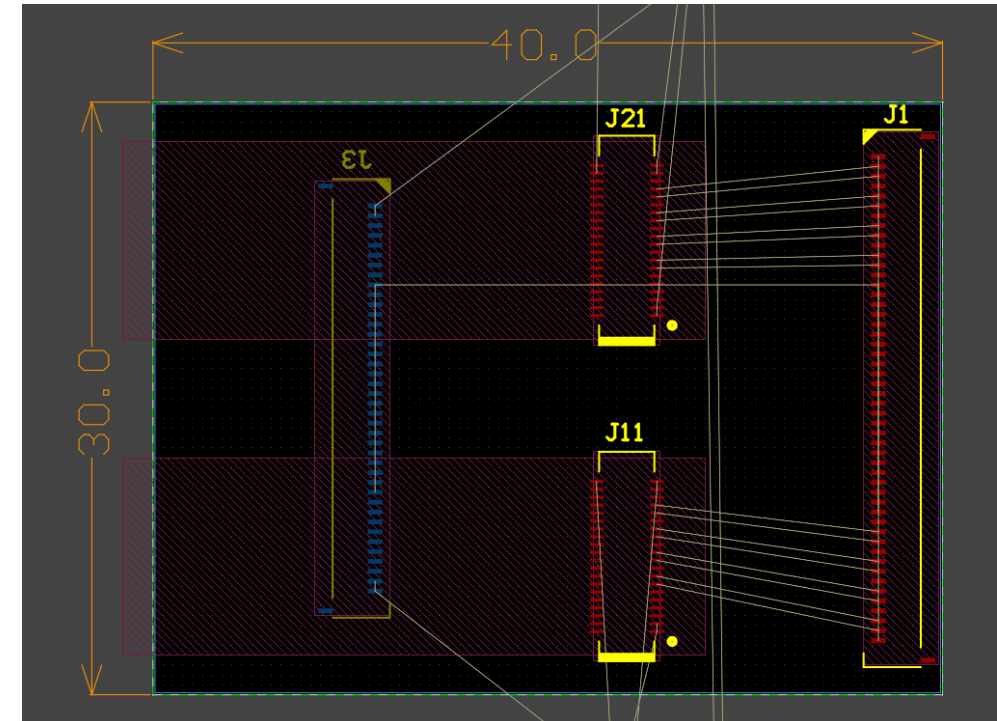
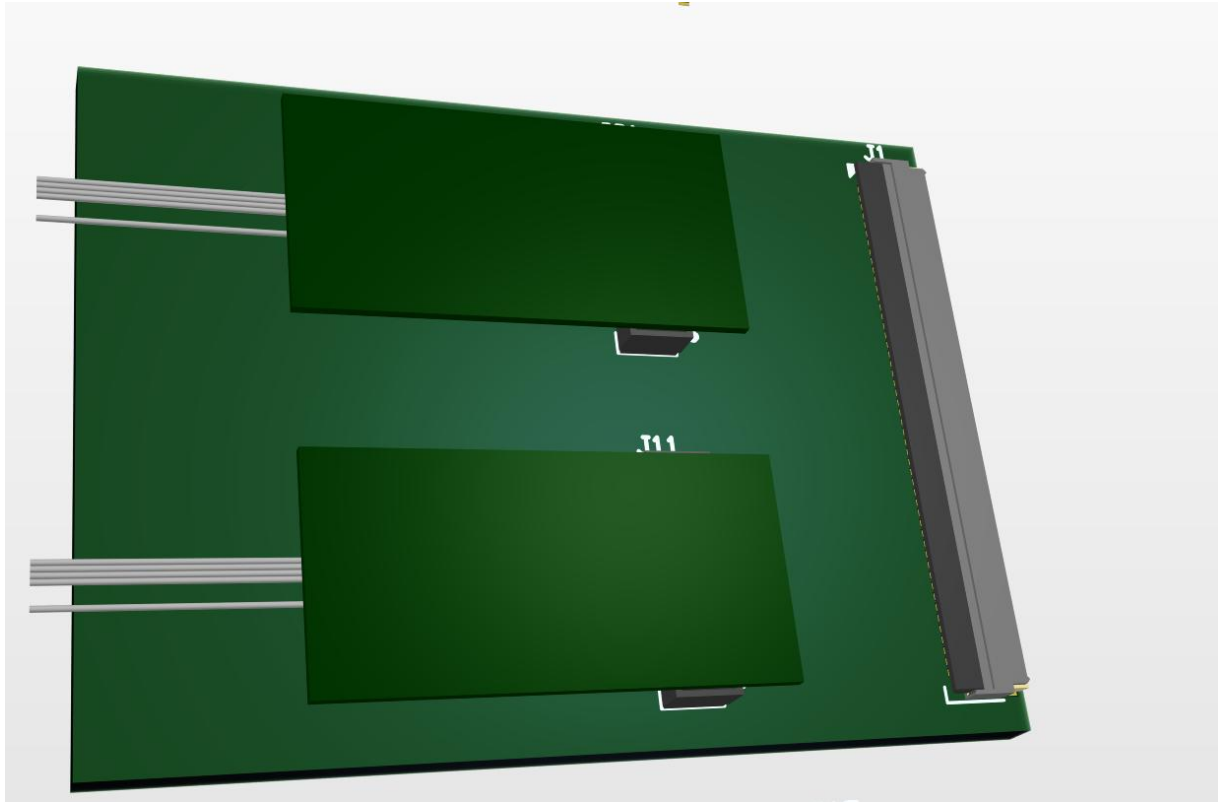
SIB Option B



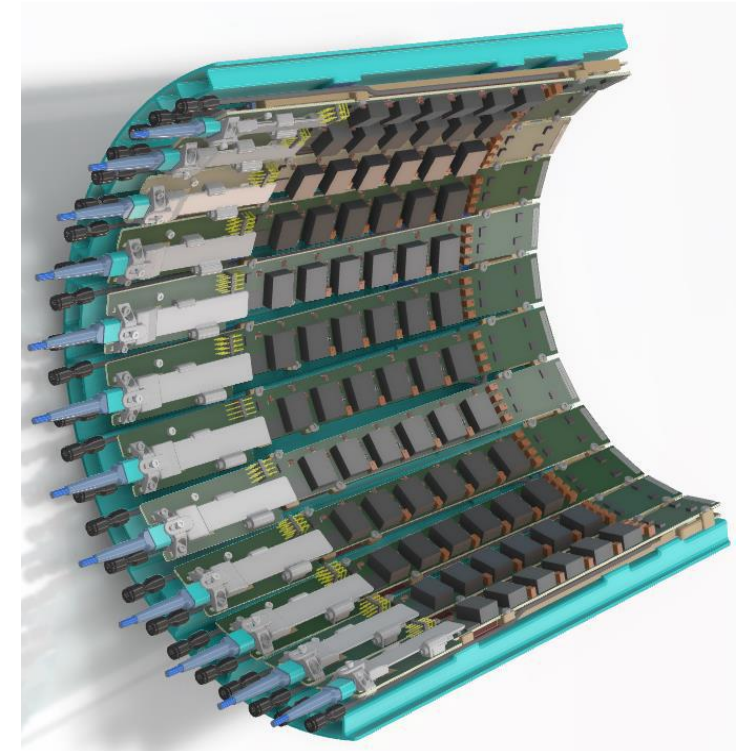
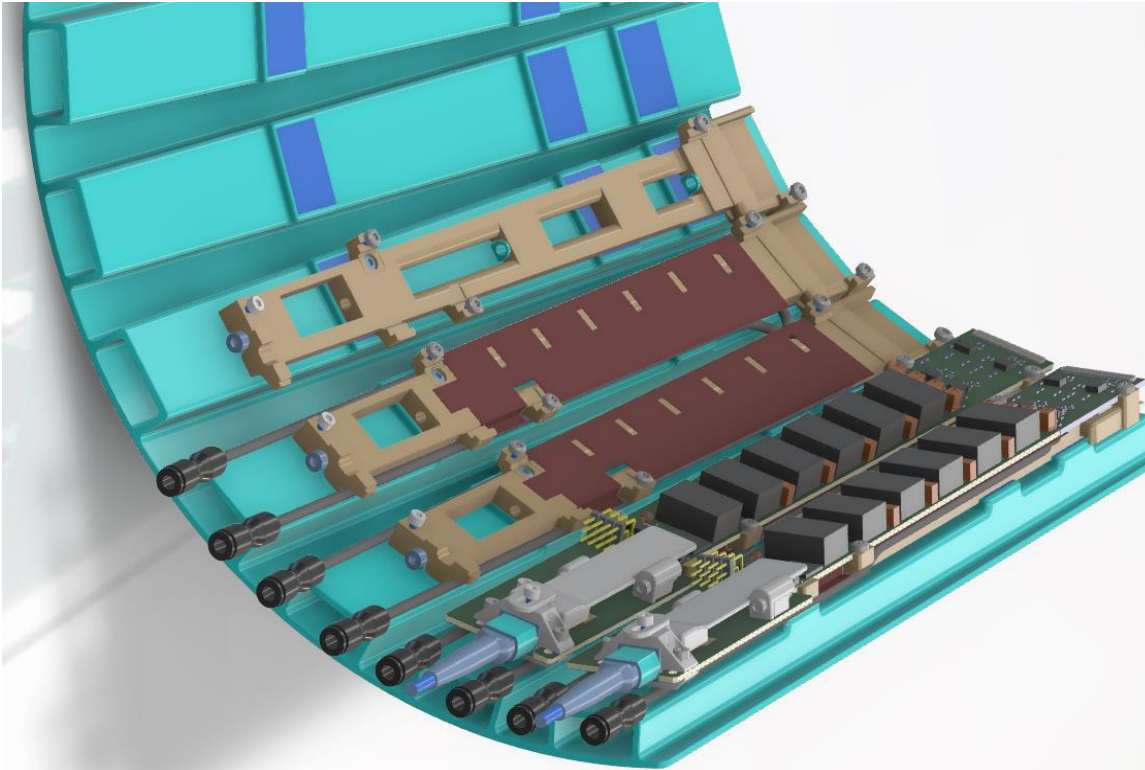
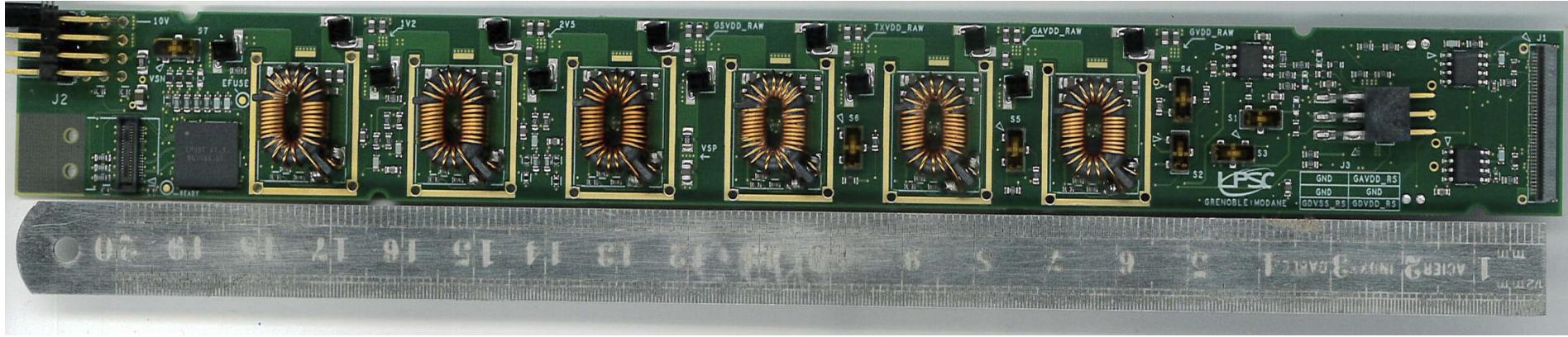
Small SIB ~30x25 mm²



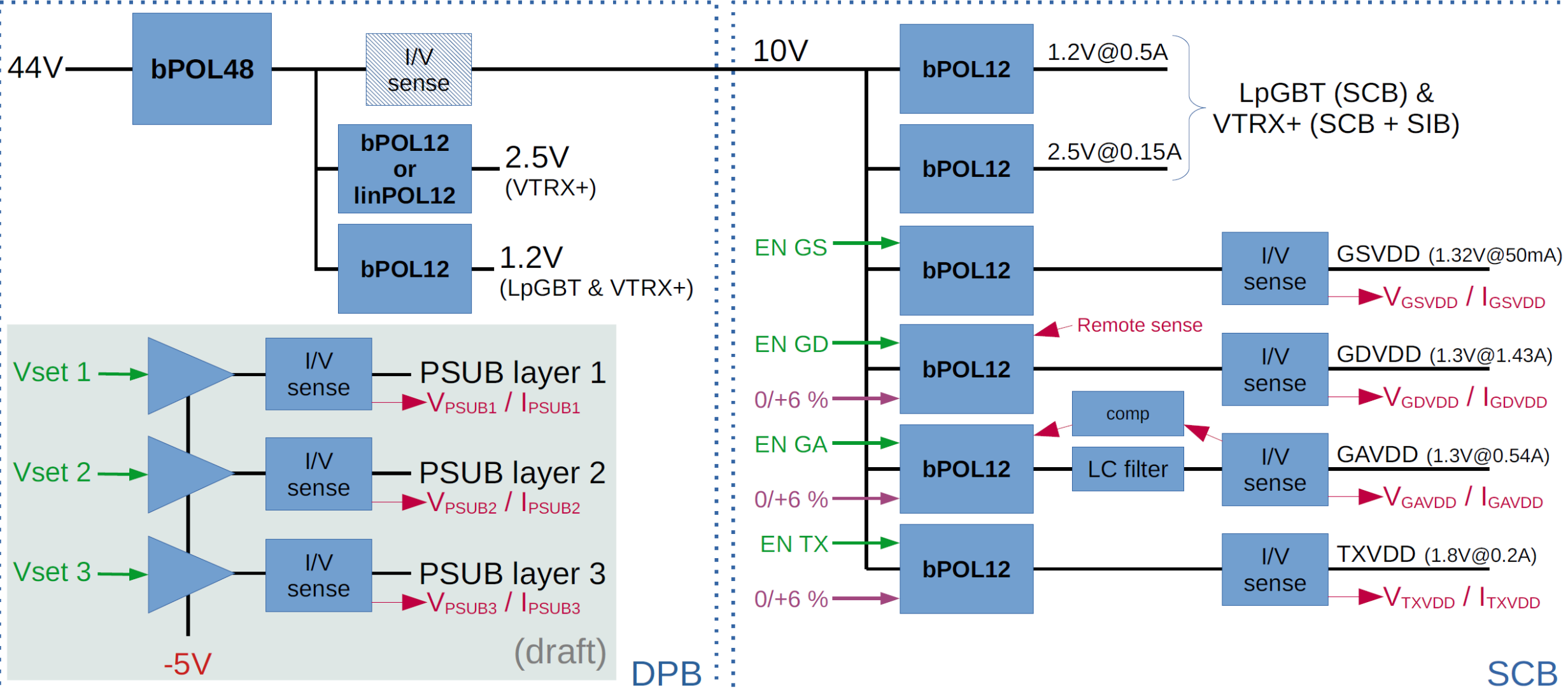
Very first attempts on SIB layouts for SVT



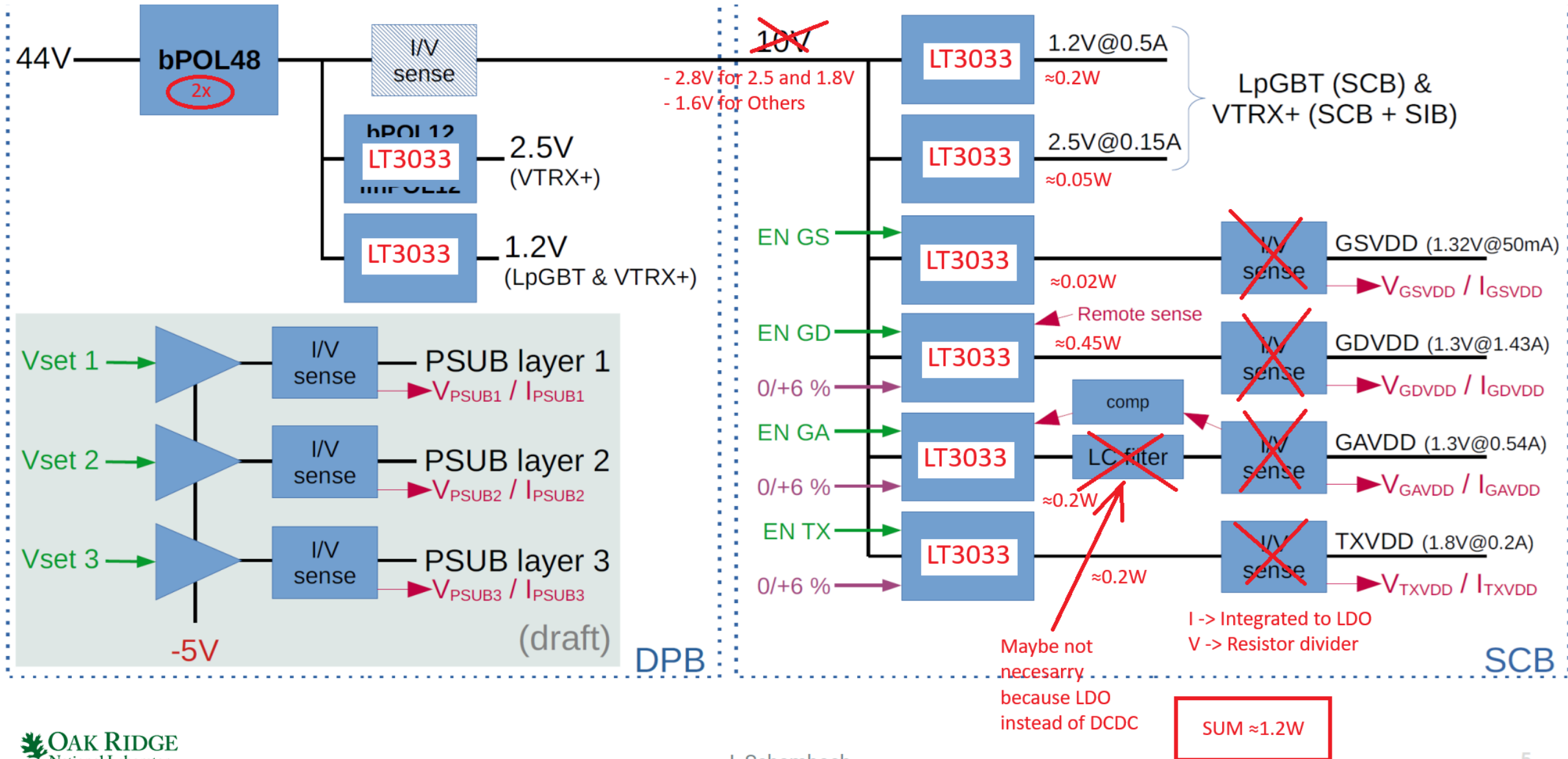
ITS3 SCB Design with bPOLs



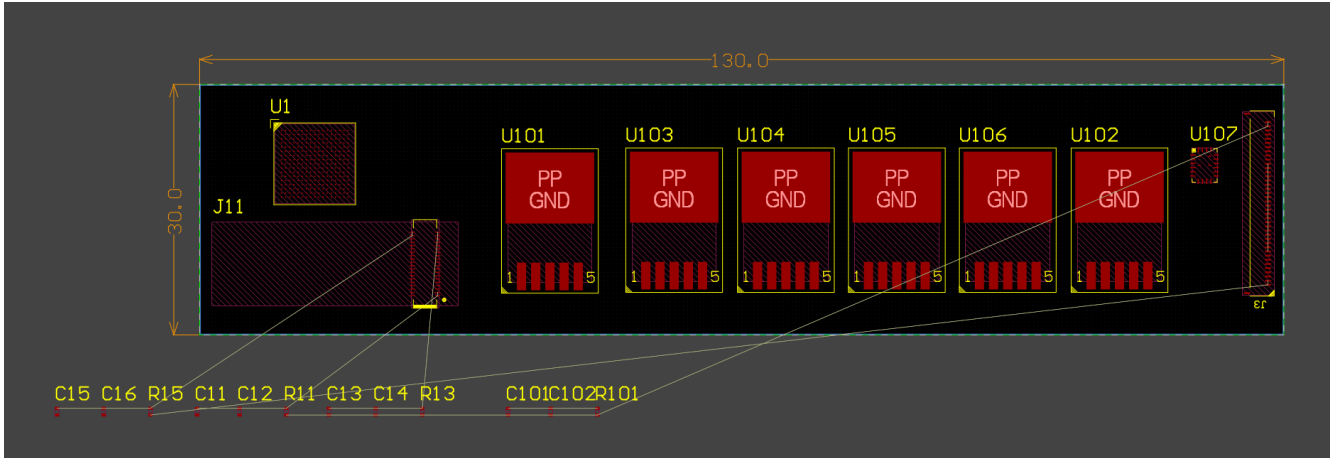
DPB – SCB Power Tree



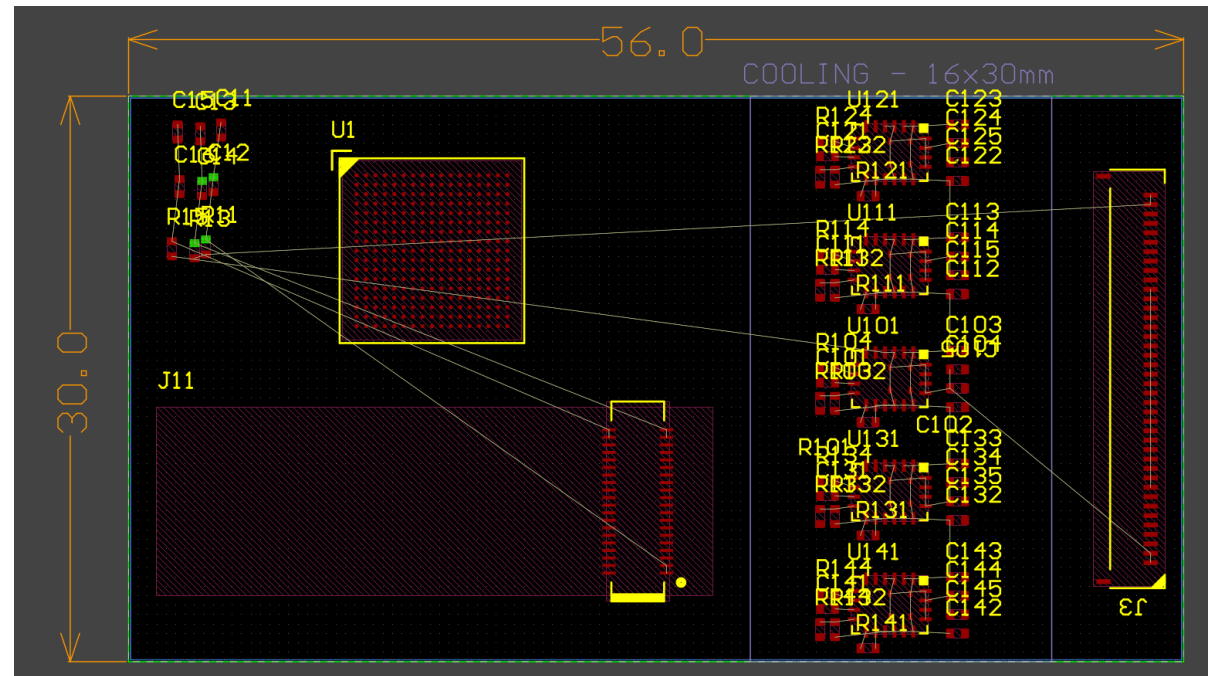
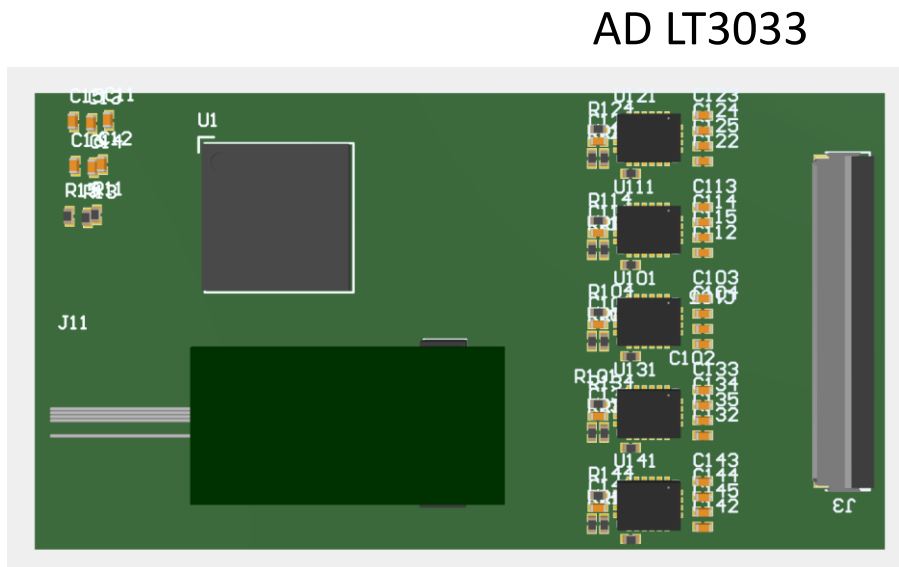
DPB SCB Power Tree with LDOs



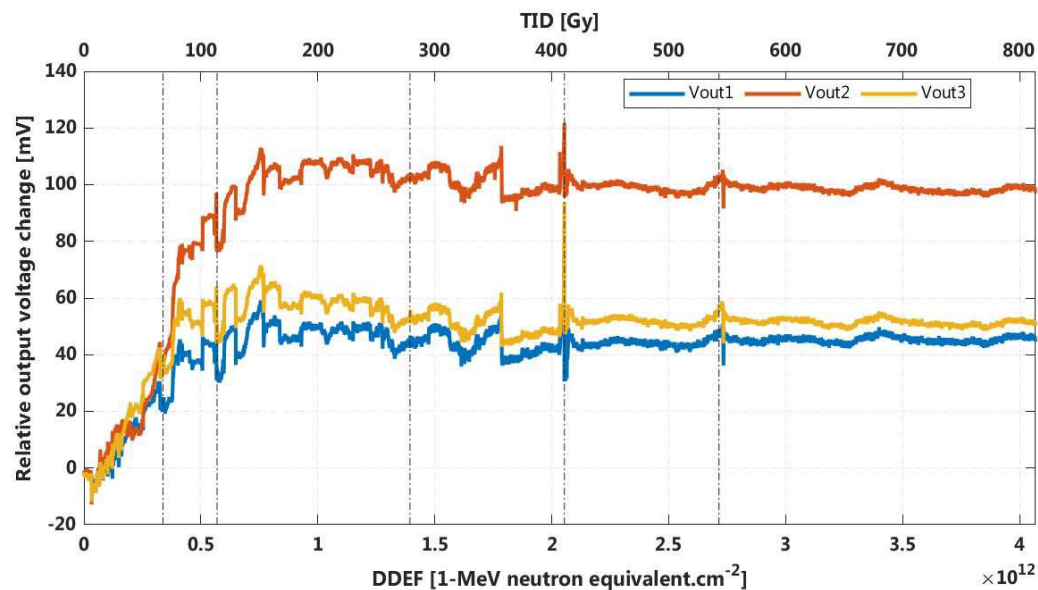
SCB with LDOs



TI TPS7A45xx



LT3033 CHARM Test 2022

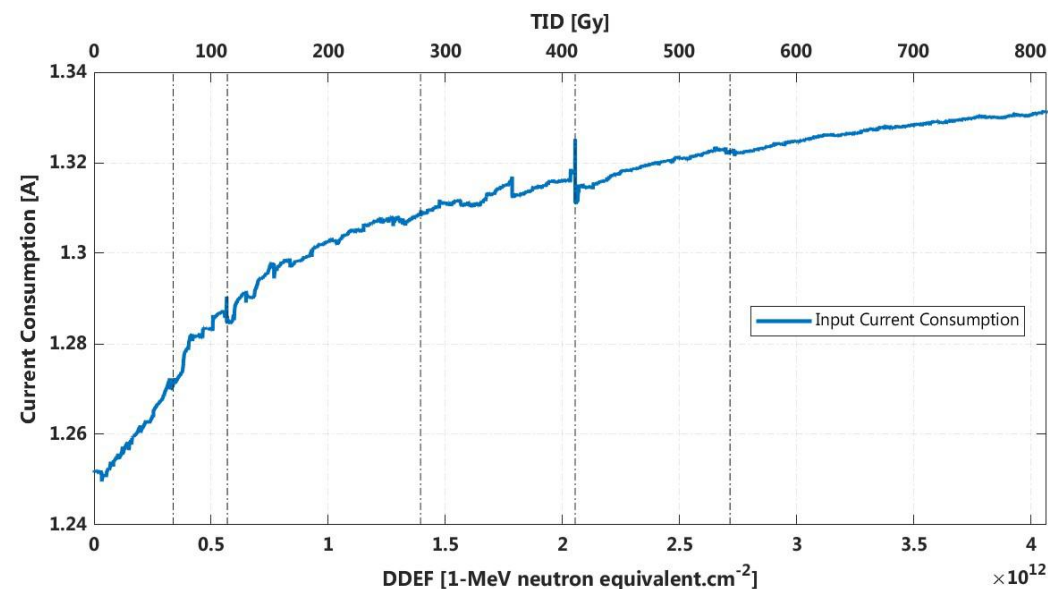


Voltage: max **100mV** change @ 5V

No failures on periodic power cycles
No SEL detected during this beam test:
SEL cross section < $4.39 \cdot 10^{-13} \text{ cm}^2$

TID = 814 Gy (81.4 kRad)
DDEF = 4.06×10^{12} 1-MeV neq cm⁻²

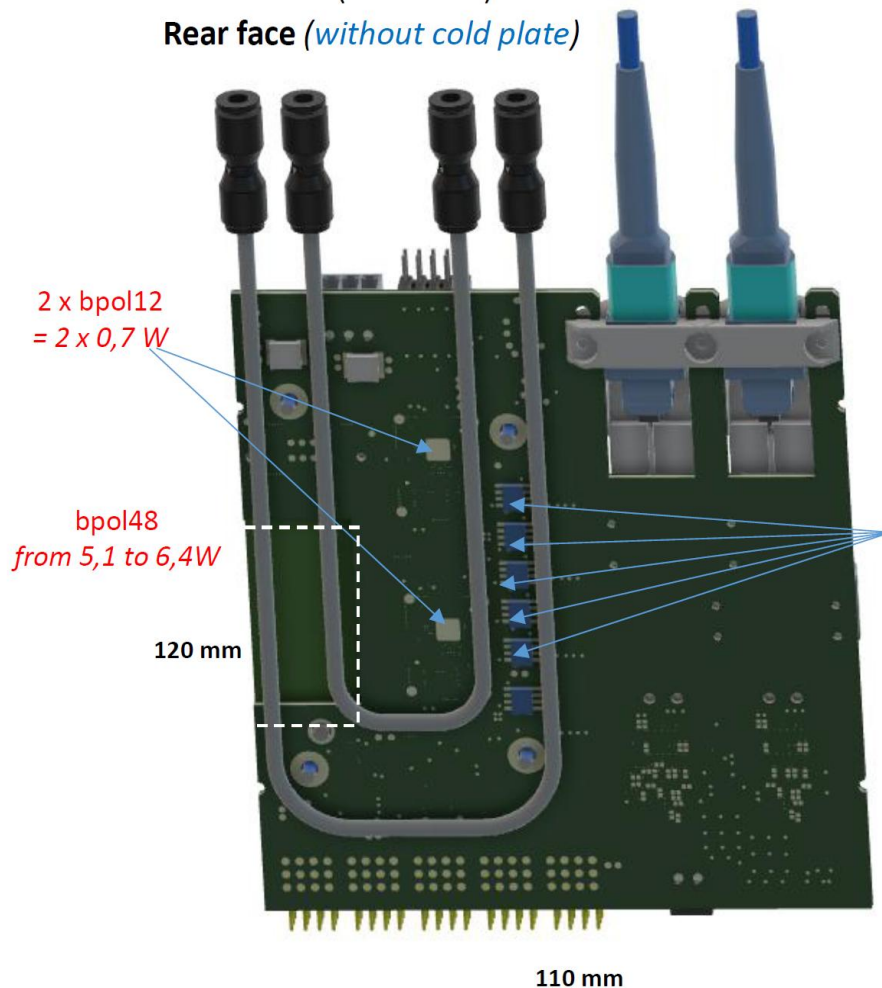
Current: max **25 mA** change



DPB integration - 2

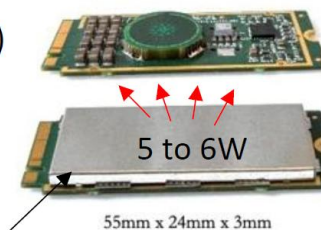
Dimensions (120 x 110)

Rear face (*without cold plate*)

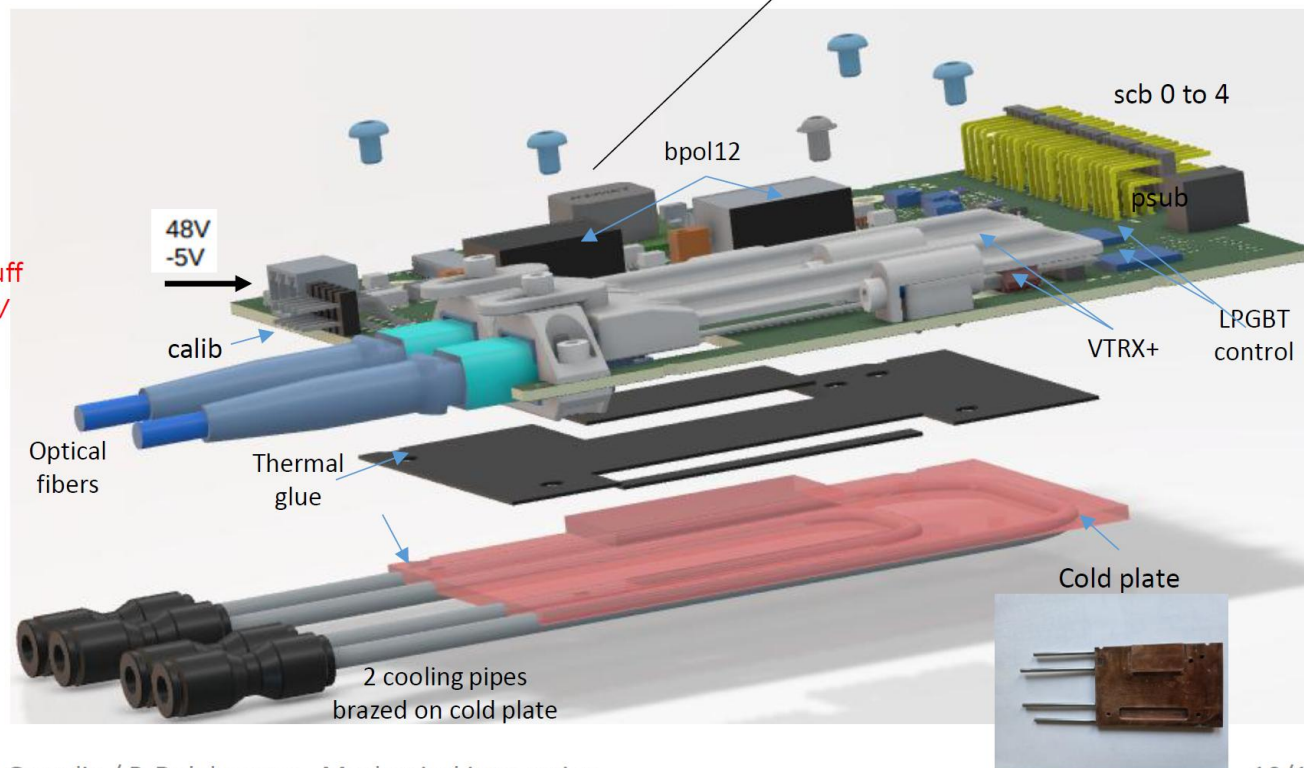


bPOL48V : cooling of the converter performed from the bottom of the PCB (Maximum temperature allowed : 50°C)

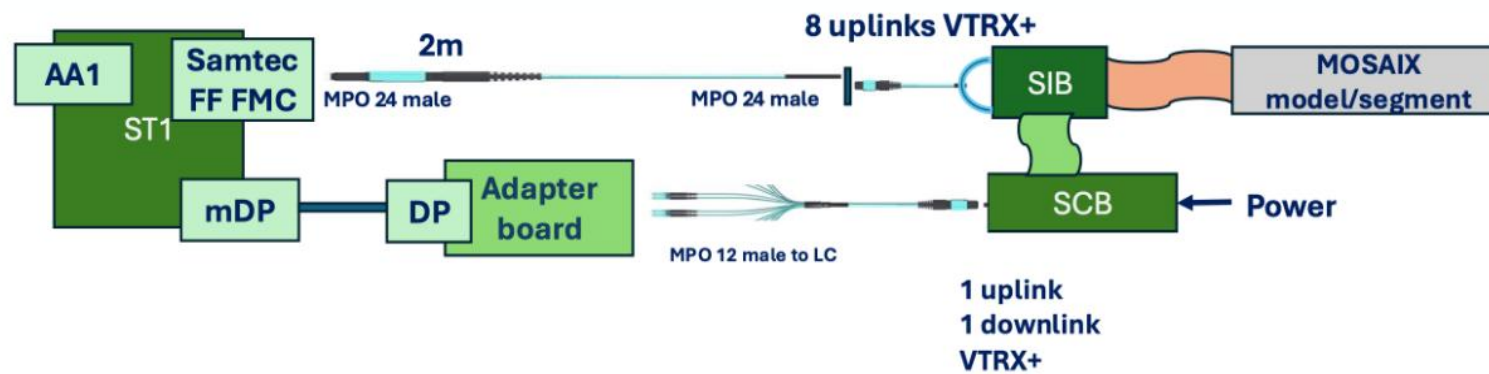
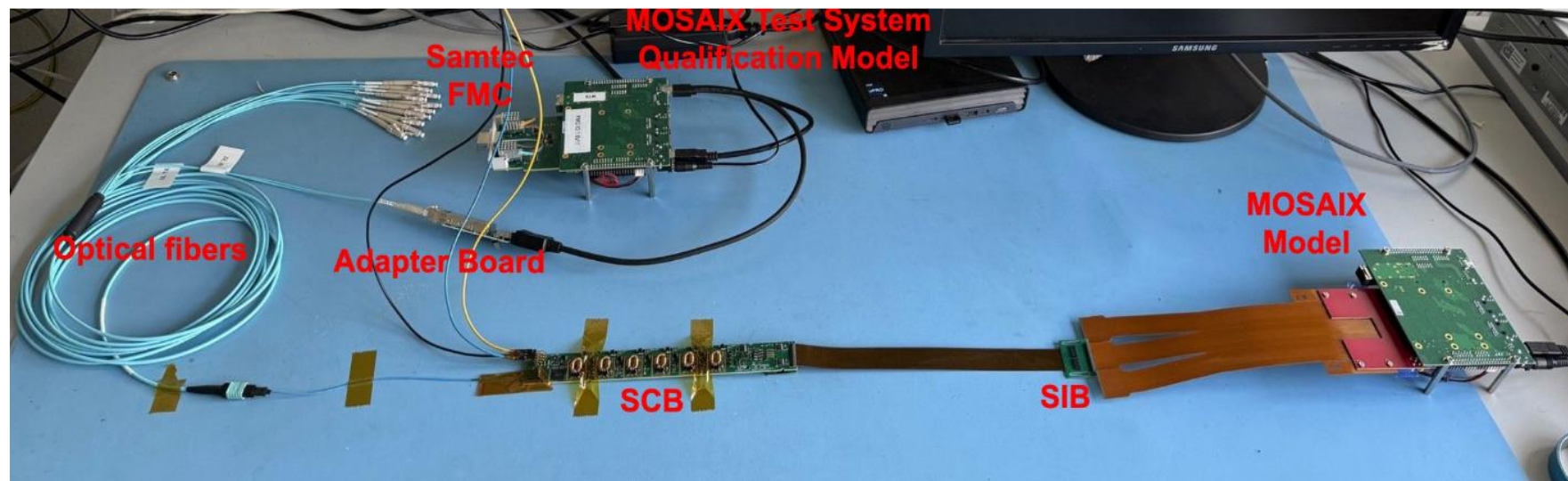
- Cooling plate temperature between 20°C and 30°C
- Temperature gradient between cooling lines inlet and outlet -> 15°C IN – OUT free
- Flow rate per circuit -> 3,3 l/h to 6,7 l/h



5 AOP buff
= 1,55W



Test Setup



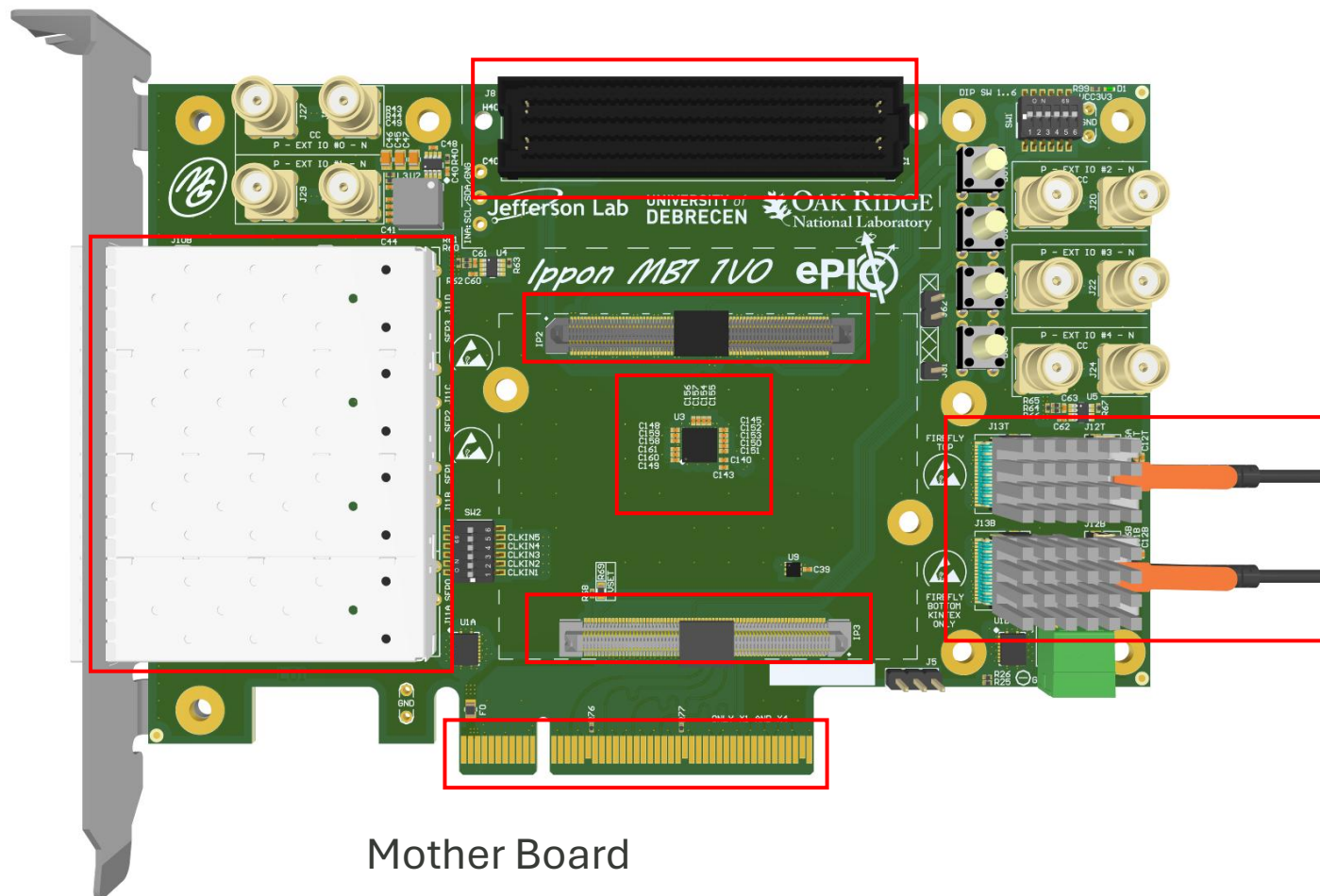
18



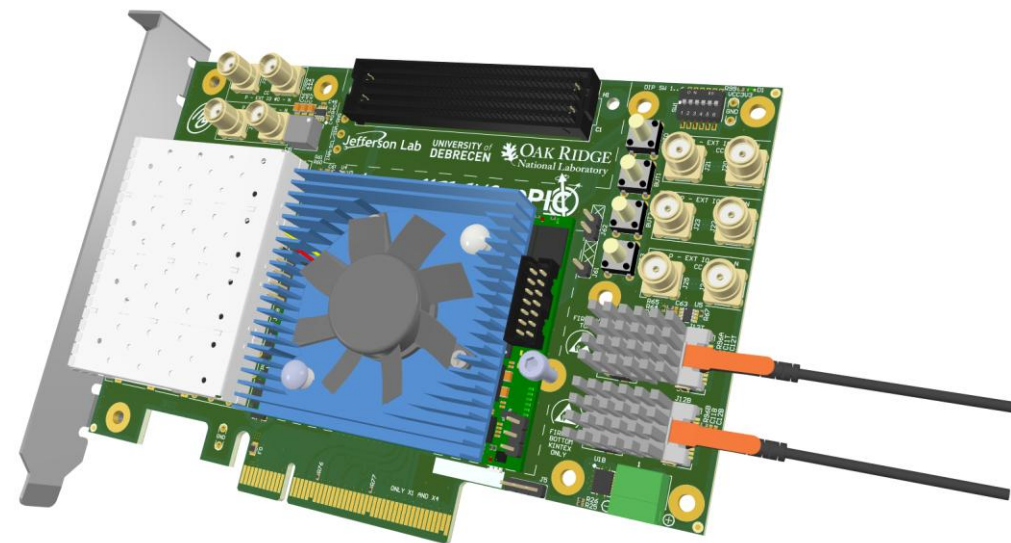
Multiple (~12) of these chains can be serviced by the provided **eLinks** (up and downlink) of just **one IpGBT**.

Generic RDO – “GRDO”

- GRDO design consists of two boards:
 - A relatively small Daughter Board (DB) containing FPGA
 - A motherboard(MB) customized for the application



Mother Board

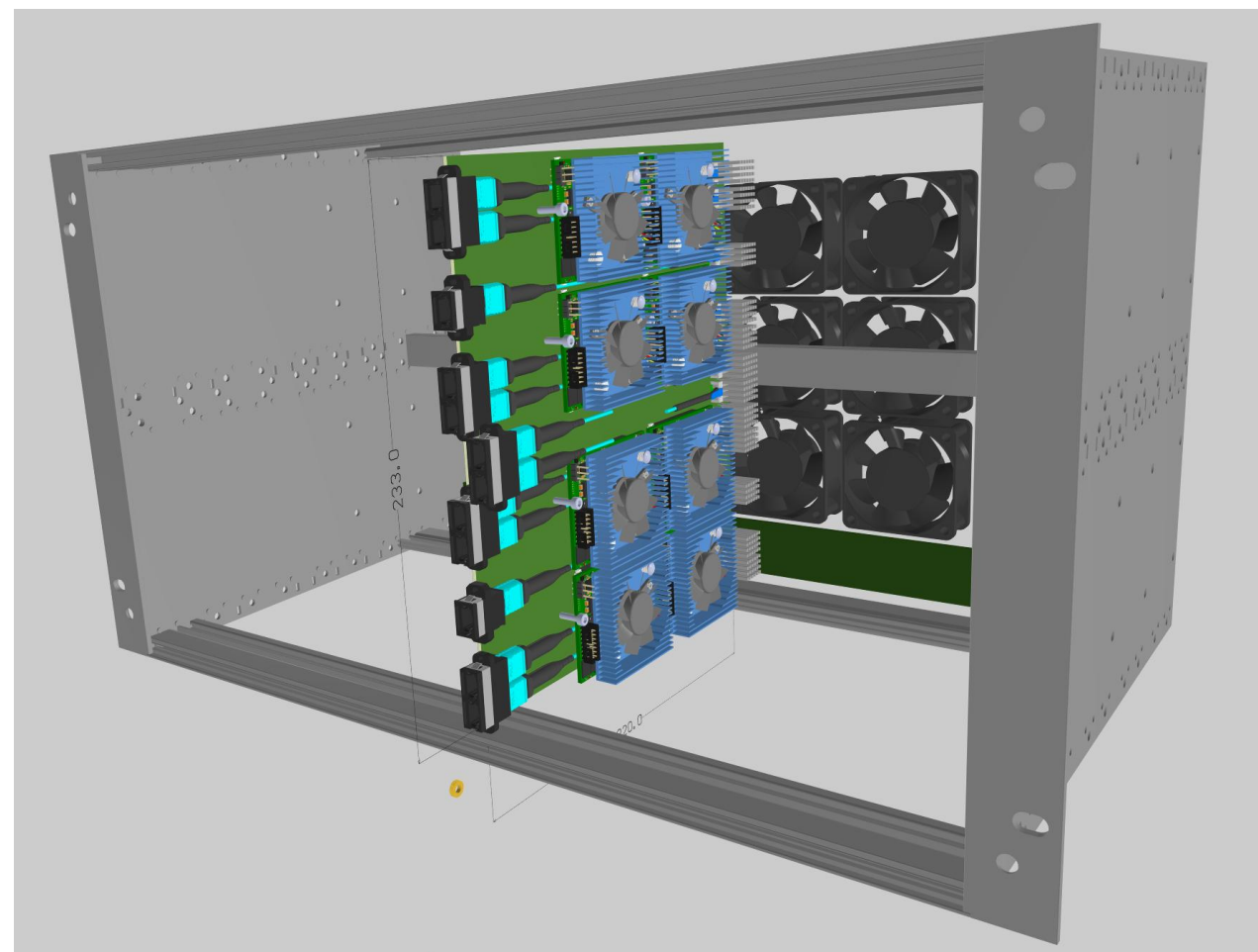
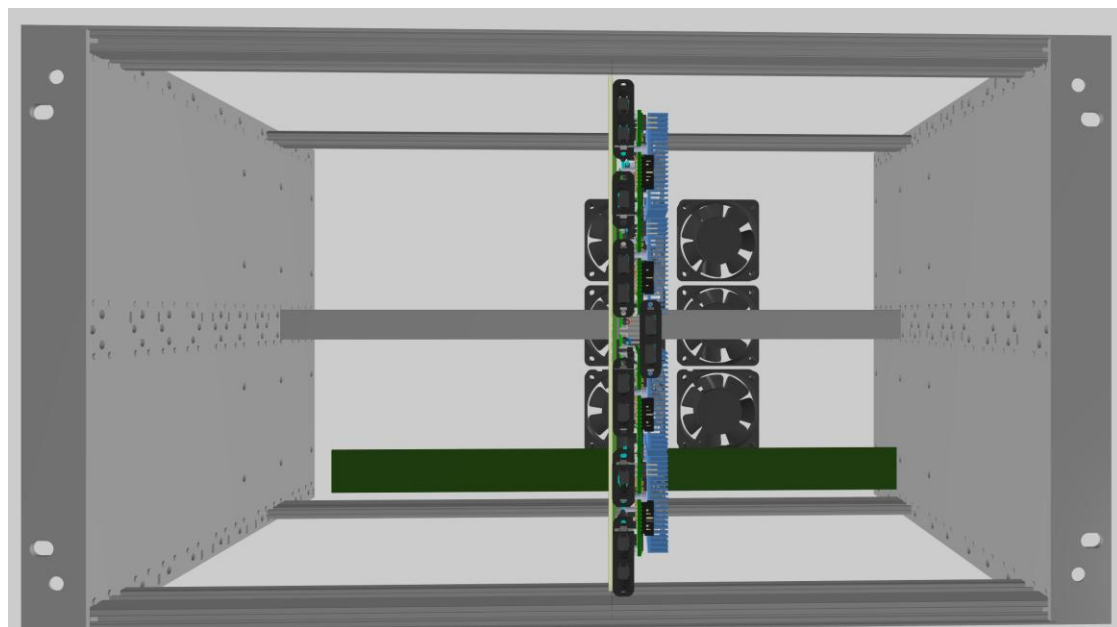


Daughter Board

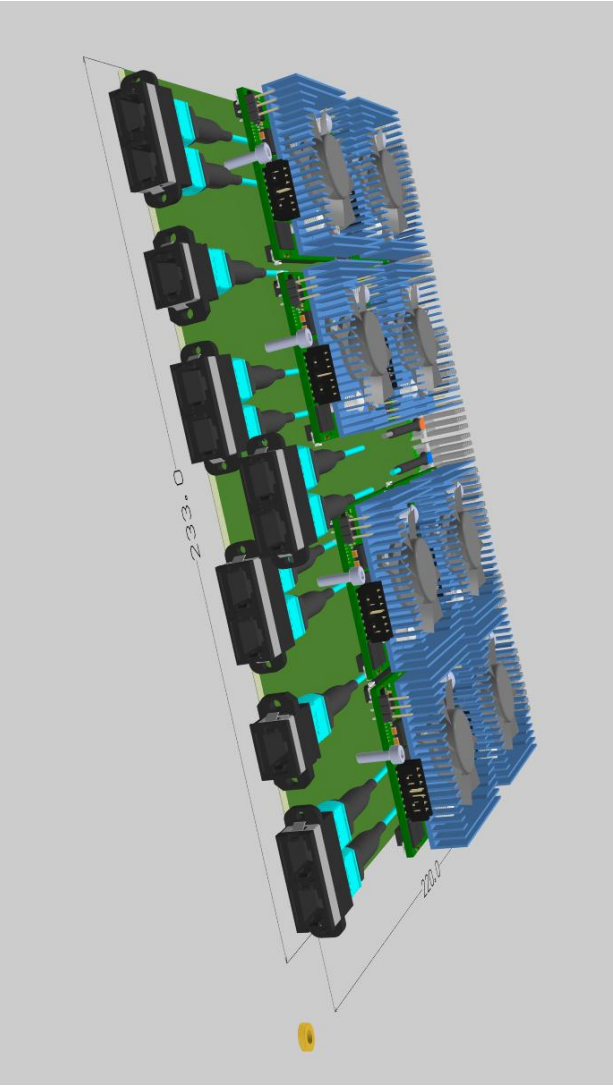
MB Components:

Expansion connectors - FPGA
Expansion connectors – FMC
SFP+
FIREFLY
PCIe x4

Suggested Concept of a rack mounted Fiber Aggregation Board



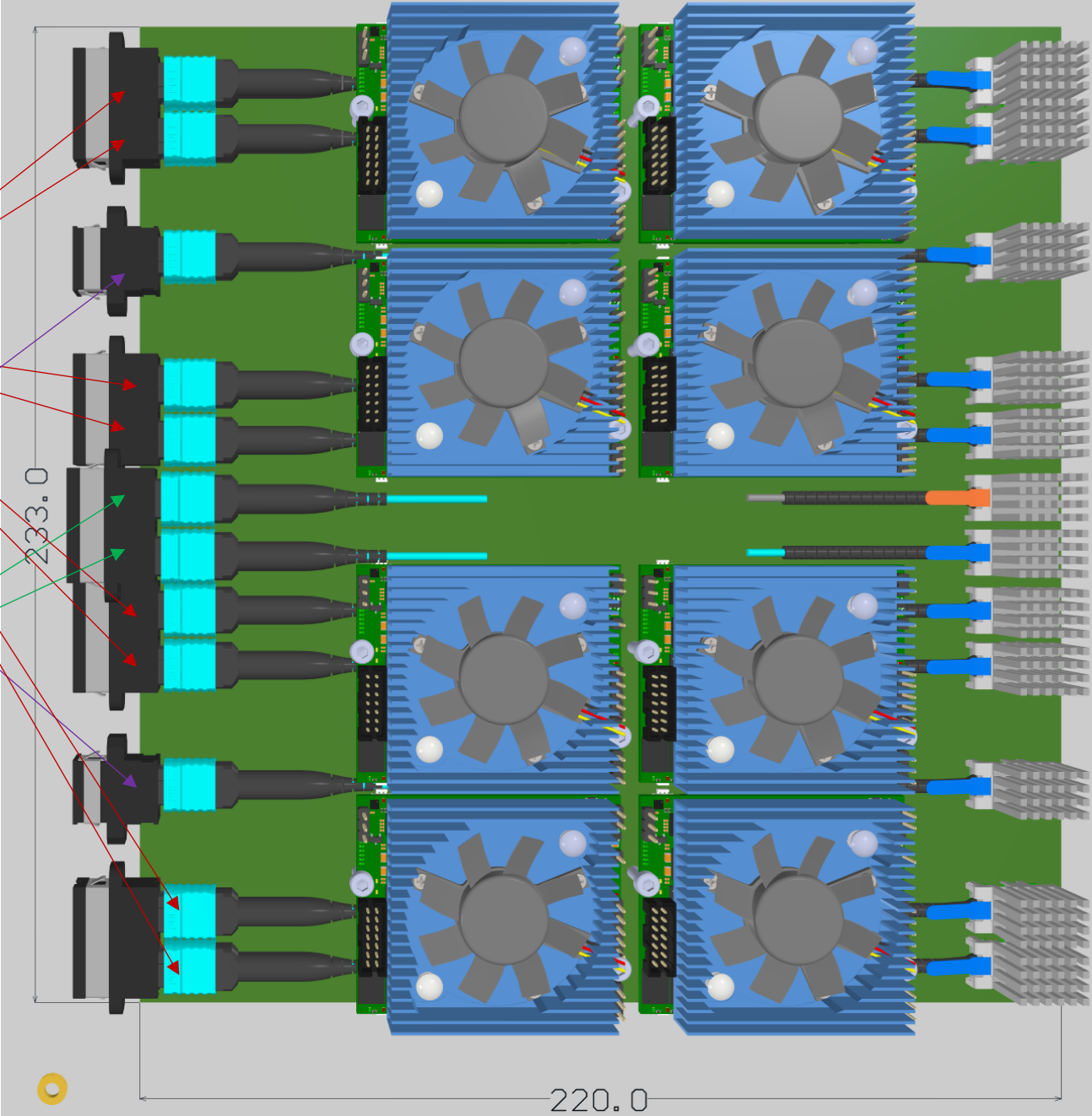
Fiber Aggregation Board



8x
12 RX Only Input (10G)
from detector patch panel
Each RDO has one FIREFLY
connector

2x
TO/FROM FELIX
FIREFLY 25G 4RX / 4TX
Each RDO has one 25G
RX/TX connector to FELIX

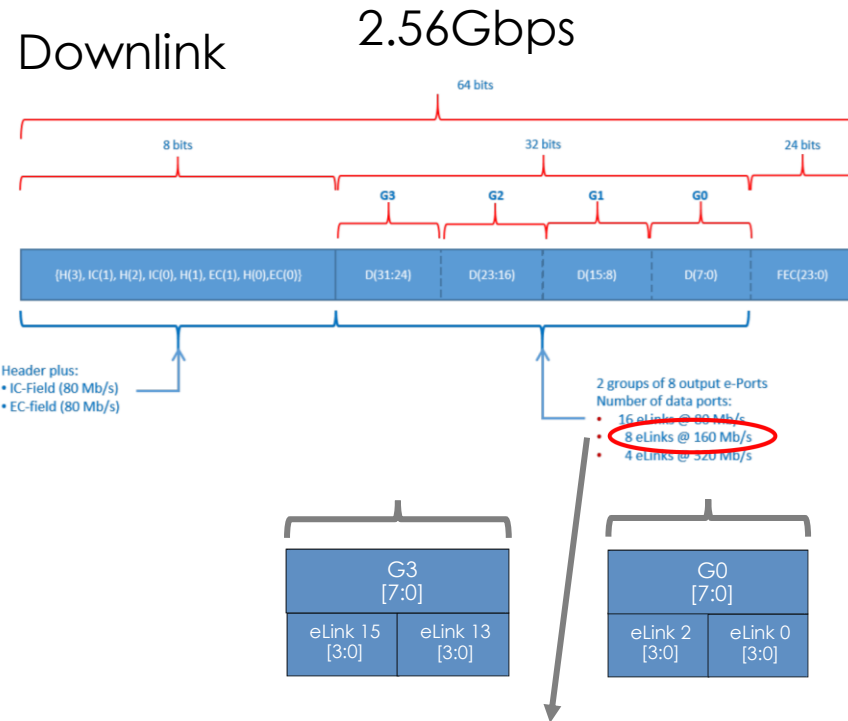
Each RDO has 1-1 TX/RX
lines to detector because
slow control...
1-1 TX/RX Output (10G) to
detector patch panel



Fiber Aggregator Board Firmware for Slow Control

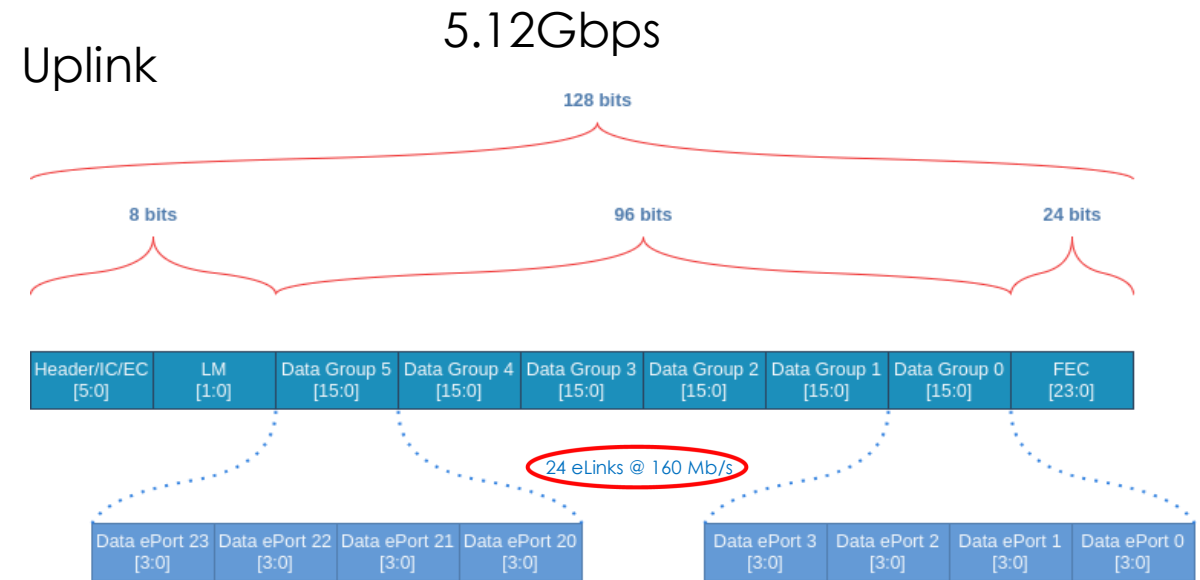
- Up to 20 IpGBT channels should be possible in one of the smaller US+ FPGAs based on resource usage in ATLAS FELIX firmware, a total of **~250** IpGBT links for SC are needed
- Use IpGBT firmware for SVT side, add firmware for Aurora protocol on FELIX side
- Aggregation Firmware (**uplink**):
 - Assemble IpGBT frames into 40bit SC words for each tile depending on data rate (LAS vs MOSAIX)
 - Only keep “data” tile words
 - Drop other SC words or handle locally (errors, dropped frames, empty frames, status, ...)
 - Add geometric word to identify Segment and mux into TX channel towards FELIX
 - Add summary status for locally handled conditions
- Slow Controls Firmware (**downlink**):
 - Separate downlink data into individual IpGBT channels and interpret (pass-through or handle locally)
 - Add sync signal to delimit readout frames for IB
 - Add commands for readout frame generation on AncASIC for OB and disks
 - (others?)

IpGBT eLink Routing



Shadowing eLinks enabled for OB & Disks

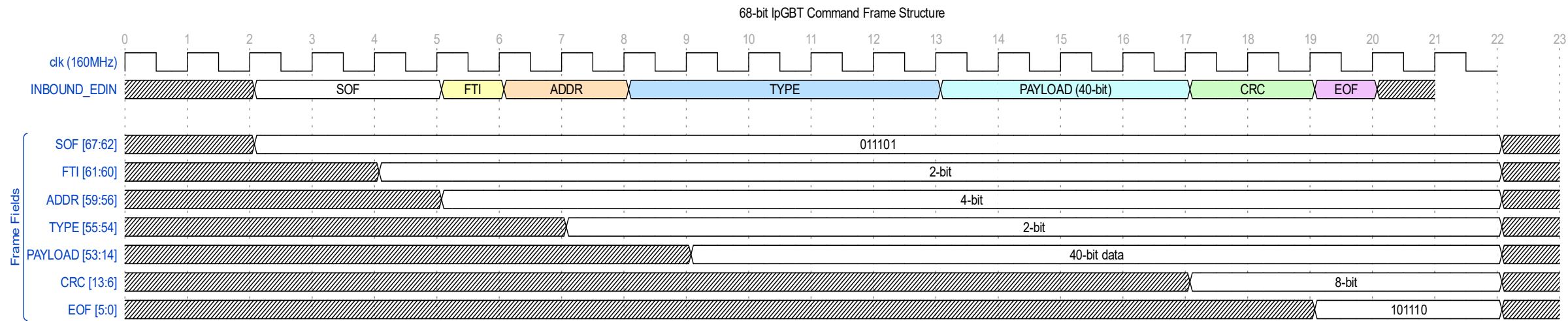
DataRate[1:0]	DataIn[7:0]	DataOut			
		e-Link[3]	E-Link[2]	E-Link[1]	E-Link[0]
2'b10 (x4) 160Mbps	{chn2[7:4],chn0[3:0]}	-	DataIn[7:4]	-	DataIn[3:0]
2'b10 (x4) 160Mbps	{chn2[7:4],chn0[3:0]}	DataIn[7:4]	DataIn[7:4]	DataIn[3:0]	DataIn[3:0]



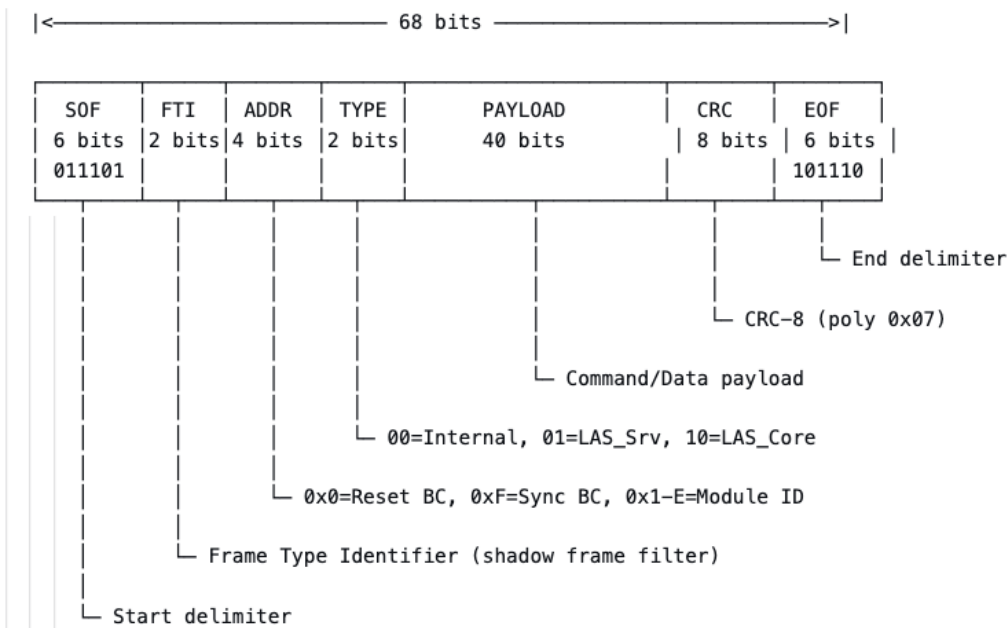
Inner Barrel:
 40 bits * 2 transitions * 16 (bit-stuffing) / 4 bits per frame =
320 frames to reconstruct a 40bit SC word

Outer Barrel & Disks:
 17 frames to reconstruct a 68bit AncBrain word

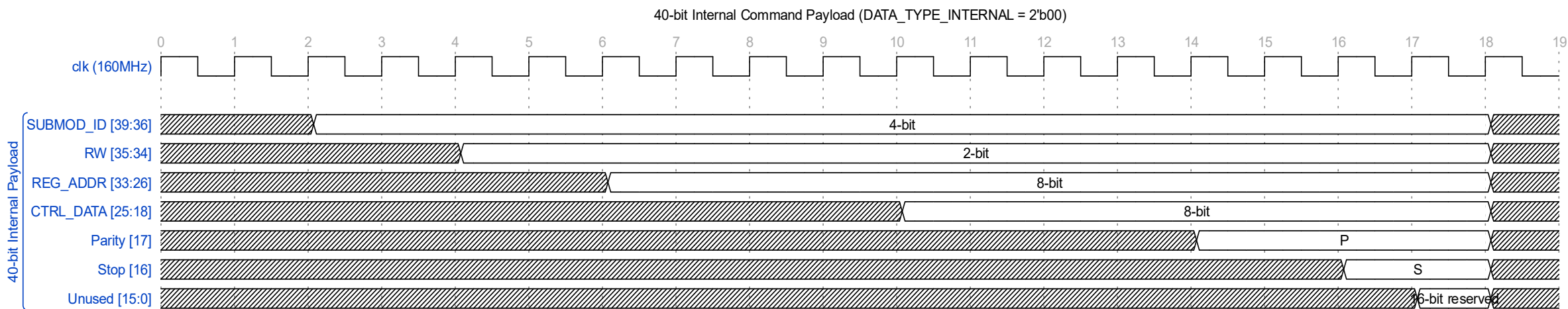
68 – bit AncBrain frame; IpGBT transparent to transmitted data and its format



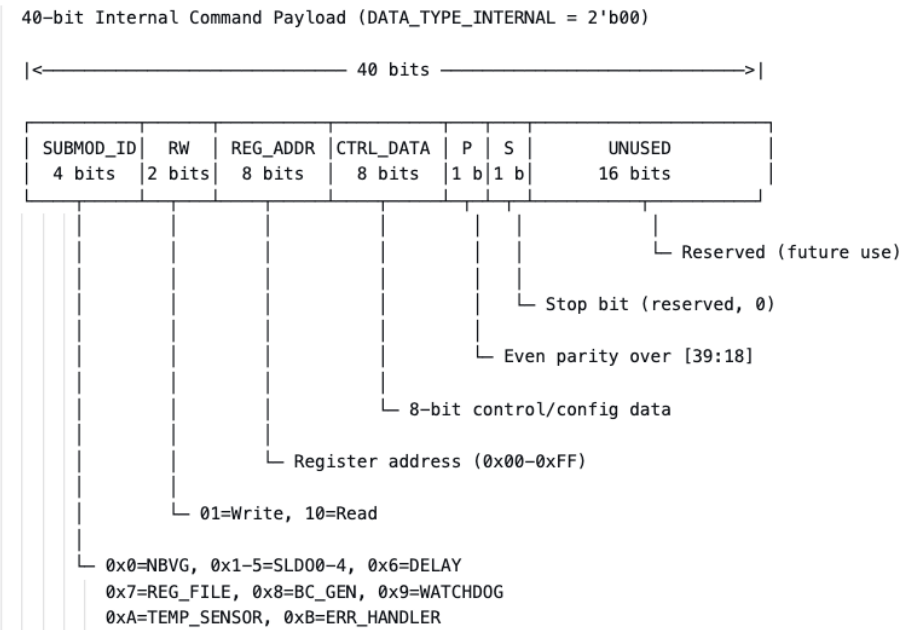
Total: 68 bits | SOF=6'b011101, EOF=6'b101110 | FTI=2-bit Frame Type ID | CRC-8 poly=0x07 (over bits [59:14])



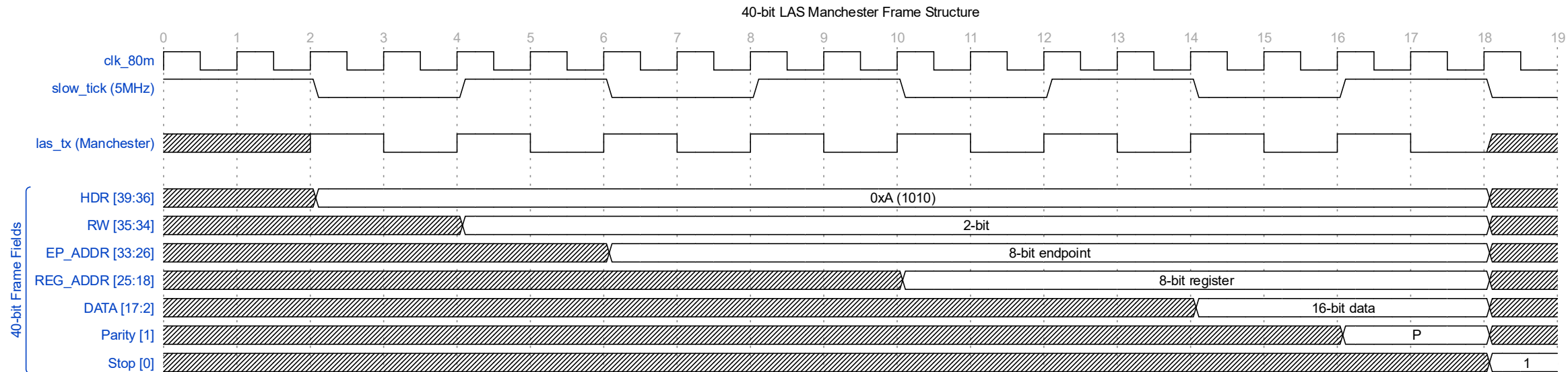
40 – bit AncBrain internal payload format



Parity: even parity over bits [39:18] | RW: 01=Write, 10=Read



40 – bit MOSAIX interface payload format



Manchester encoded @ 5Mbps effective | Half-bit: 50-125ns | Full-bit: 150-225ns

40-bit LAS Payload (DATA_TYPE_LAS_SRV = 2'b01 / DATA_TYPE_LAS_CORE = 2'b10)

|<----- 40 bits ----->|

HDR	OPCODE	EP_ADDR	REG_ADDR	REG_DATA	P	STOP
4 bits	2 bits	8 bits	8 bits	16 bits	1 b	1 b
1010					1	1

Stop bit (always 1)

Even parity over [35:2]

16-bit register data

Register address (0x00-0xFF)

Endpoint address (0x00-0xFF)

00=Write (posted), 01=Write (non-posted), 10=Read

Sync header (4'hA = 1010)

Manchester encoded @ 5Mbps effective | Half-bit: 50-125ns | Full-bit: 150-225ns

Summary of all calibration and monitoring scans for ITS2

(from the ALICE ITS Calibration Paper: arXiv:2510.27592v1)

Scan	Objective	Frequency	Description
Digital/Analog	Calibration	~1/year	Tagging of problematic pixels and pixel columns
VCASN	Calibration	~1/year	Course tuning of pixel thresholds
ITHR	Calibration	~1/year	Fine tuning of pixel thresholds
Short Threshold	Monitoring	~1/day	Measurement and monitoring of pixel thresholds
Full Threshold	Monitoring	~1/year	Measurement of thresholds used as reference
VRESETD	Monitoring	~1/year	Monitoring of VRESETD working point
Pulse Shape	Monitoring	~1/year	Probing of the pixel analog signal shape
Noise	Calibration	~1/year	Detection of noisy pixels

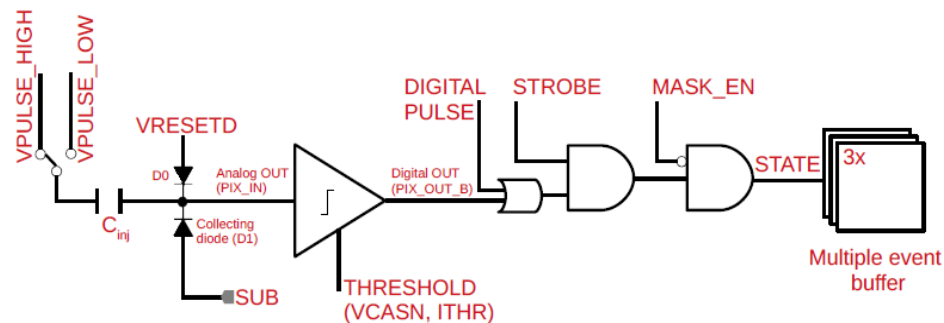


Figure 2: Simplified schematic view of the ALPIDE pixel cell.

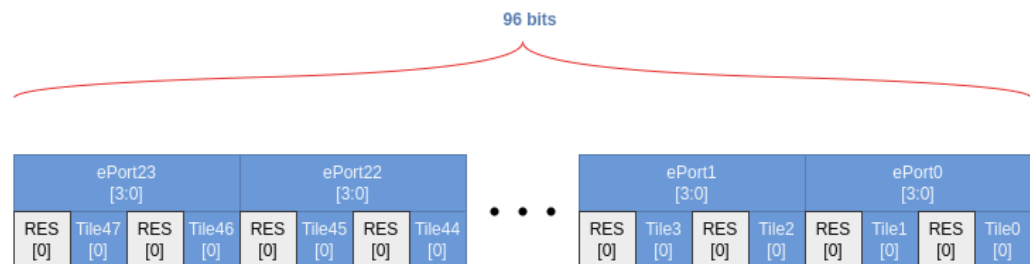
The **MOSAIX** pixel cell is conceptually very similar to the (ITS2) **ALPIDE** pixel cell, so I am showing here the calibration scans used for ALPIDE as an example of similar scans necessary for MOSAIX.

All DACs controlling the various pixel circuitries are **global** to a pixel matrix, no individual pixel control is possible (other than the mask)

LEC Data Routing

5 Gbps / 40 MHz

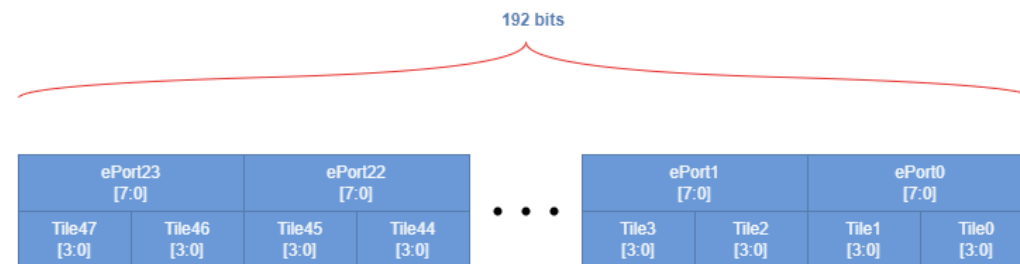
LAS



16 frames to reconstruct tile word

10 Gbps / 160 MHz

MOSAIX



4 frames to reconstruct tile word

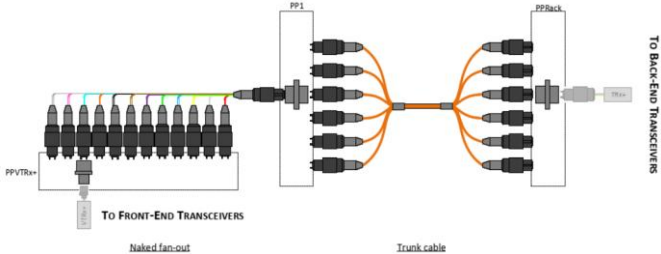
1 row threshold scan:

- 1 tile header
- 1 region header
- 38 data
- 1 region header
- 38 data
- 1 region header
- 40 data
- 1 region header
- 40 data
- 1 tile trailer

162 words x 16 frames
x 25ns = 64.8 μ s
For 1 row to transfer to
aggregator board

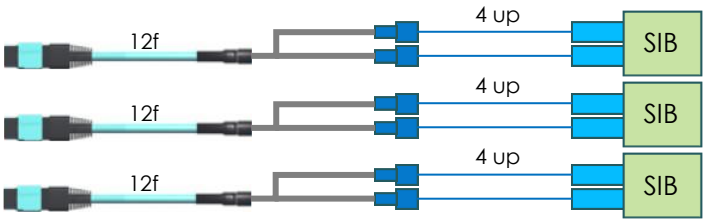
162 (16bit) words

Inner Barrel Fiber Fanout Plans



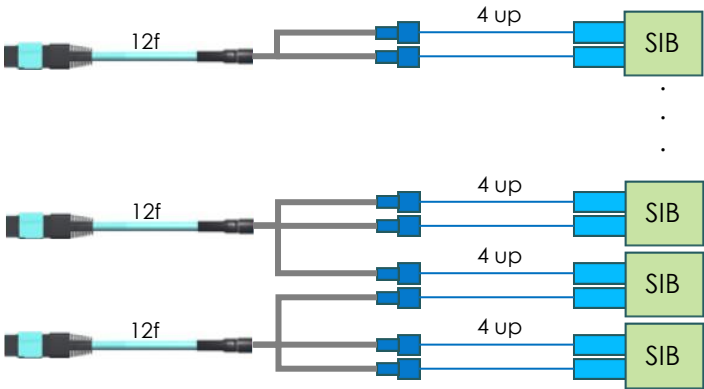
Complete Fiber Run

Variant A



L0: 12 fiber bundles (8f used)
L1: 16 fiber bundles (8f used)
L2: 40 fiber bundles (8f used)

Variant B

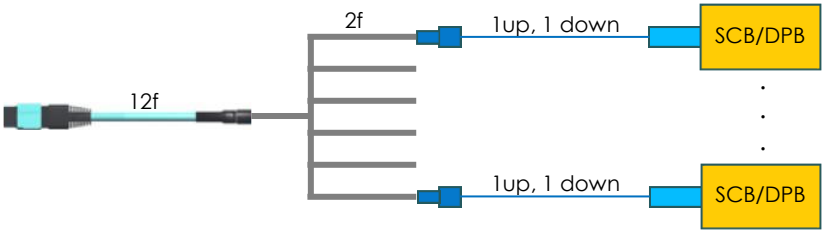


(L1 and L2)

L0: 8 fiber bundles (12f used)
L1: 10 fiber bundles (12f used) + 1 fiber bundle (8 used)
L2: 26 fiber bundles (12f used) + 1 fiber bundle (8 used)

L0: 12 SIB + 12 SCB + 4 DPB
L1: 16 SIB + 16 SCB + 4 DPB
L2: 40 SIB + 40 SCB + 8 DPB

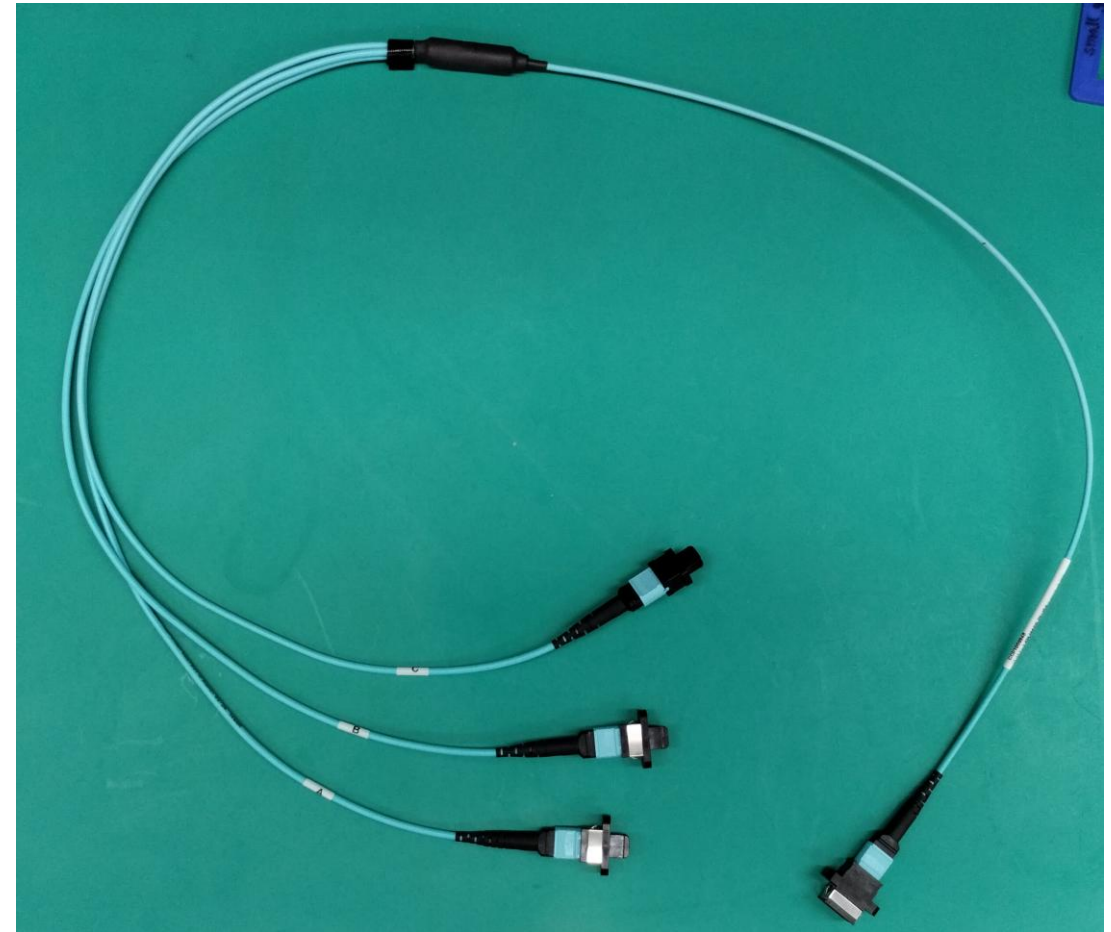
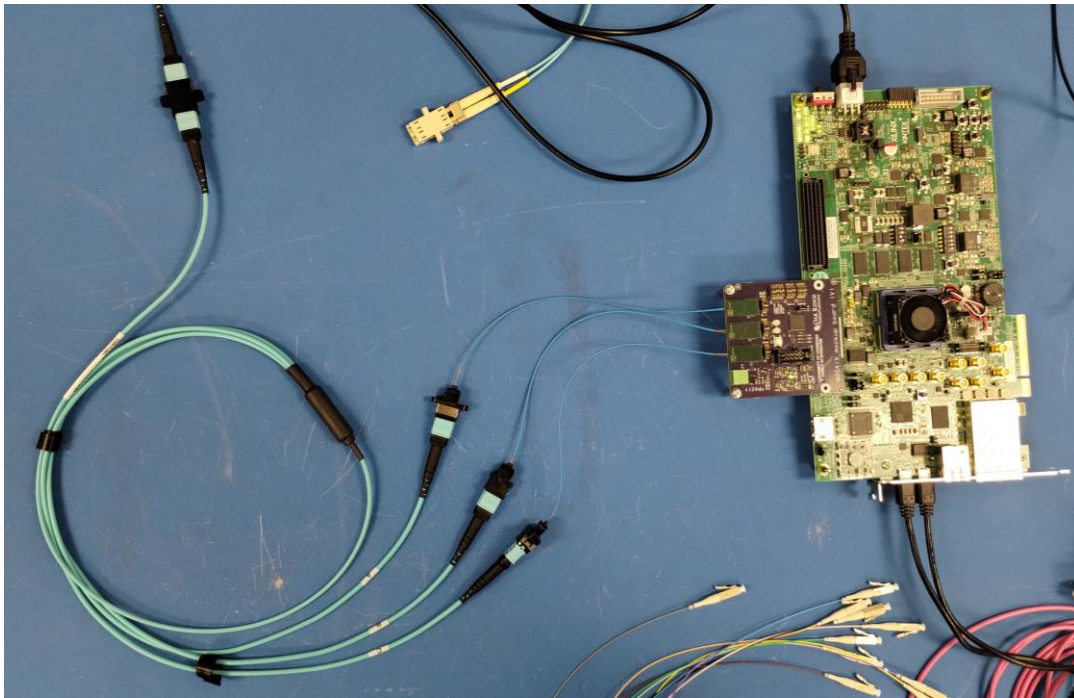
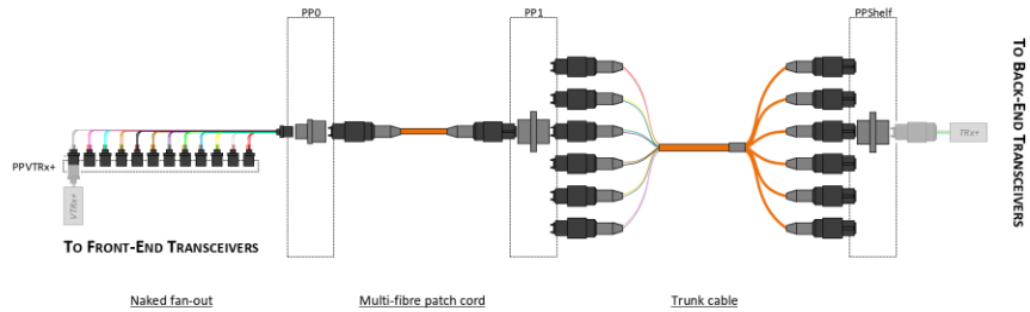
Variant A: 81 fanout fibers
 Variant B: 63 fanout fibers



SCBs
L0: 2 fiber bundles (12f used)
L1: 3 fiber bundles (8f used)
L2: 8 fiber bundles (10f used)

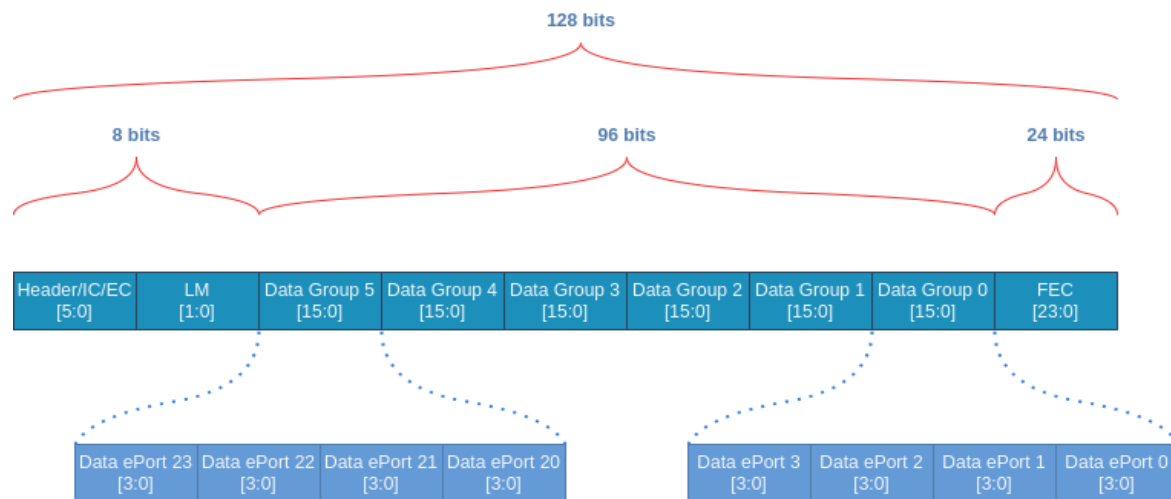
DPBs:
 4 fiber bundles (8f used)

Fiber Distribution Ideas

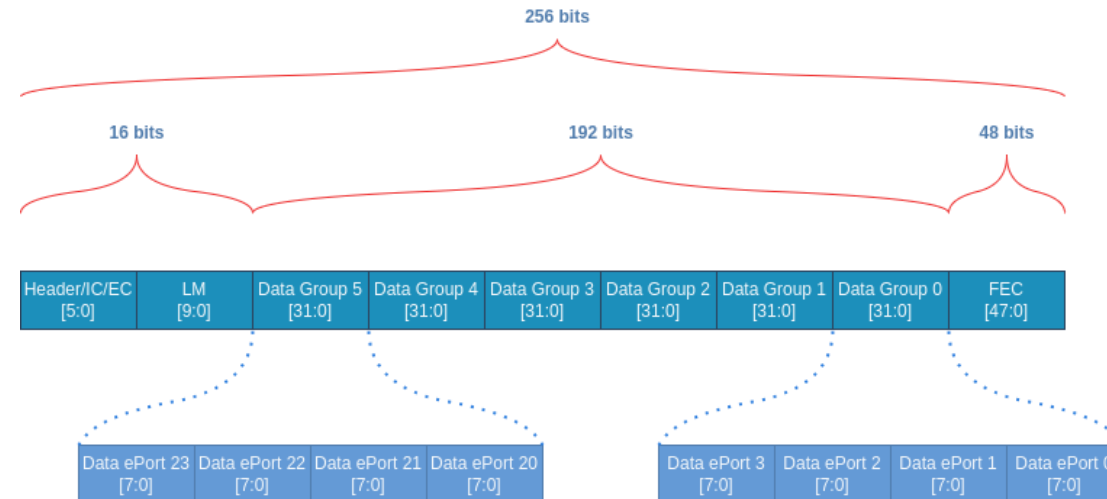


IpGBT ePort Routing

5.12Gbps



10.24Gbps



MOSAIX uplink						
Uplink bandwidth (Gbps)	5.12			10.24		
FEC Coding	FEC12			FEC12		
Tile bandwidth (Mbps)	40	80	160	40	80	160
Tiles per uplink ¹	48	48	24	48	48	48
Bits per tile	1	2	4	1	2	4
Tiles per ePort	2	2	1	2	2	2
Bits per ePort	4	4	4	8	8	8
Used bits per ePort	2	4	4	2	4	8
Bandwidth efficiency	50%	100%	100%	25%	50%	100%

1. To simplify routing scheme, 48 tiles are connected in instances where there are bandwidth enough to support a higher number of tiles.

READOUT PROTOCOL																
Word type	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDLE	1	1	0	0	0	1	0	1	IDLE config [7:0]							
LOCK	1	1	0	0	1	0	1	0	IDLE config [7:0]							
READOUT_STATUS_1	1	0	0	1	1	1	0	0	Integration Window Counter [15:8]							
READOUT_STATUS_2	1	1	1	1	IWC Checksum [3:0]				Integration Window Counter [7:0]							
TILE_HEADER	1	0	1	0	0	0	0	0	Unit Slice [4:0]				Tile [1:0]		T/B	
REGION_HEADER	1	0	1	0	1	1	Region Address [1:0]		Integration Window Counter [7:0]							
DATA	0	Pixel Address Row [8:0]									Pixel Address Column [5:0]					
TILE_TRAILER	1	0	1	1	TRU Status Flags [3:0]				Packet Checksum [7:0]							
EMPTY_INTEGRATION_WINDOW	1	1	1	0	TRU Status Flags [3:0]				Integration Window Counter [7:0]							
DROPPED_INTEGRATION_WINDOW	1	1	0	1	TRU Status Flags [3:0]				Integration Window Counter [7:0]							
RECOVERY	1	0	0	1	0	0	1	1	'0							
RESERVED	1	0	0	0	RESERVED											

Bit Counts

1 tile noise pixel:

- 1 tile header
- 1 region header
- 1 data
- 1 tile trailer

4 words

-> **64 bits per pixel**

1 tile hit (3 pixels):

- 1 tile header
- 1 region header
- 3 data
- 1 tile trailer

6 words

-> **96 bits**

-> **32 bits per pixel**

1 hit (3 pixels) per region:

- 1 tile header
- 1 region header
- 3 data
- 1 region header
- 3 data
- 1 region header
- 3 data
- 1 tile trailer

18 words

-> **288 bits**

-> **24 bits per pixel**

2 hits (3 pixels) in 1 region:

- 1 tile header
- 1 region header
- 6 data
- 1 tile trailer

9 words

-> **144 bits**

-> **24 bits per pixel**

4 hits (3 pixels each) in 1 region:

- 1 tile header
- 1 region header
- 12 data
- 1 tile trailer

15 words

-> **240 bits**

-> **20 bits per pixel**

1 tile hit (2 pixels):

- 1 tile header
- 1 region header
- 2 data
- 1 tile trailer

5 words

-> **80 bits**

-> **40 bits per pixel**

1 row threshold scan:

- 1 tile header
- 1 region header
- 38 data
- 1 region header
- 38 data
- 1 region header
- 40 data
- 1 region header
- 40 data
- 1 tile trailer

162 words

-> **2,592 bits**