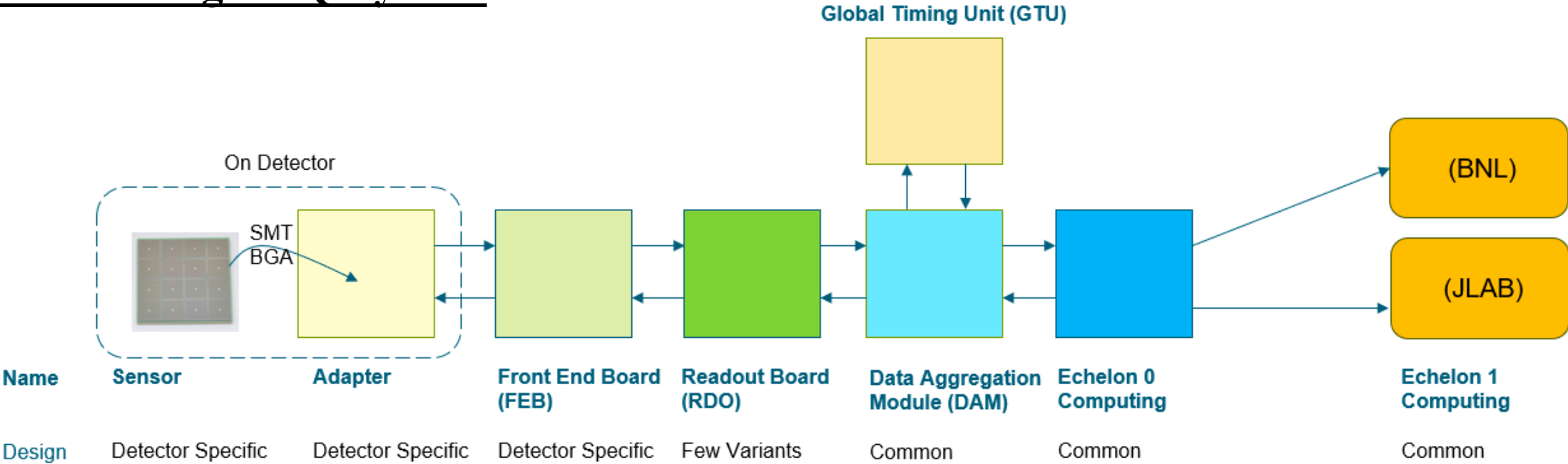


Test Setups and Chain Test Planning

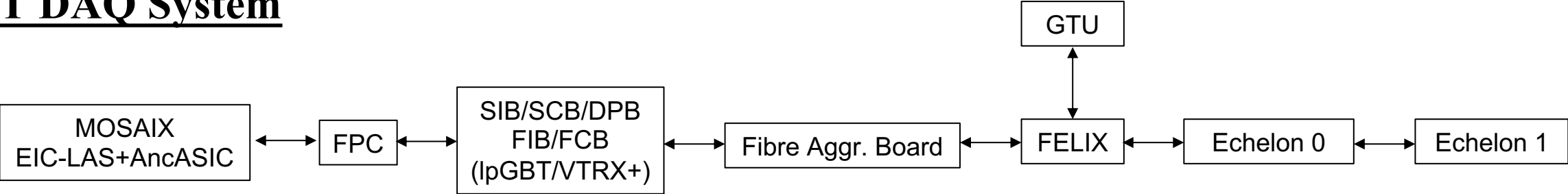
Zhenyu Ye

Lawrence Berkeley National Laboratory

ePIC Streaming DAQ System

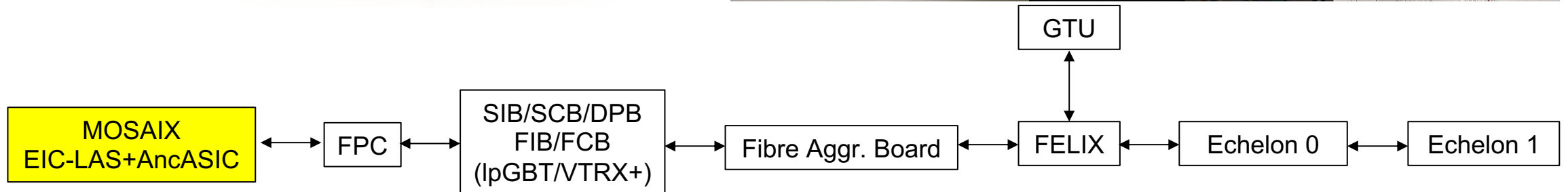
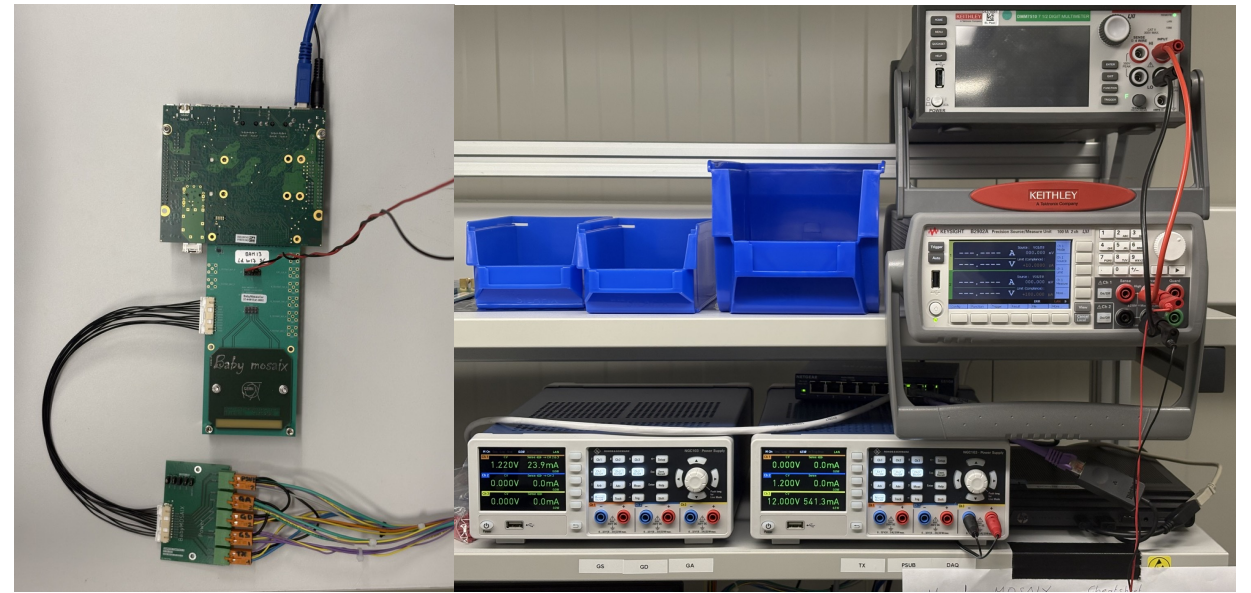
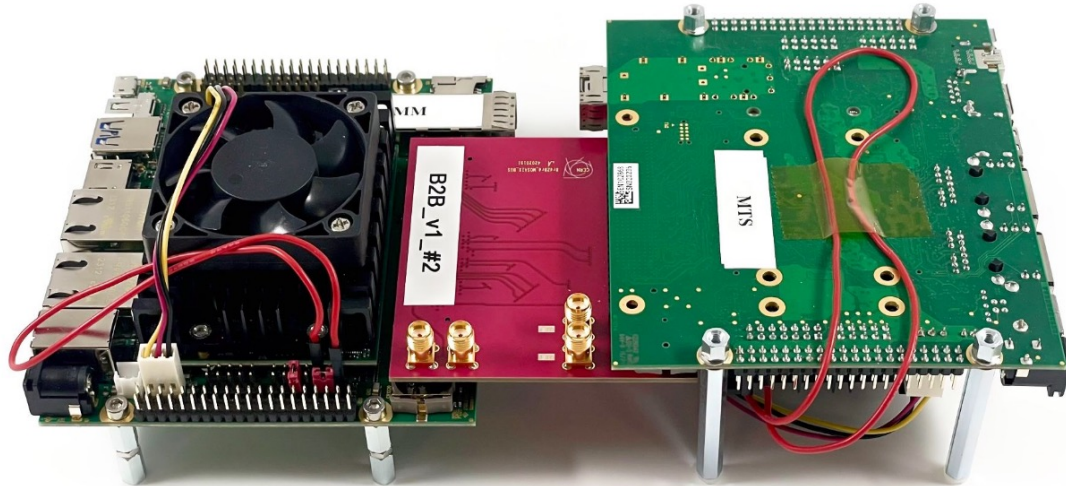


SVT DAQ System



MOSAIX

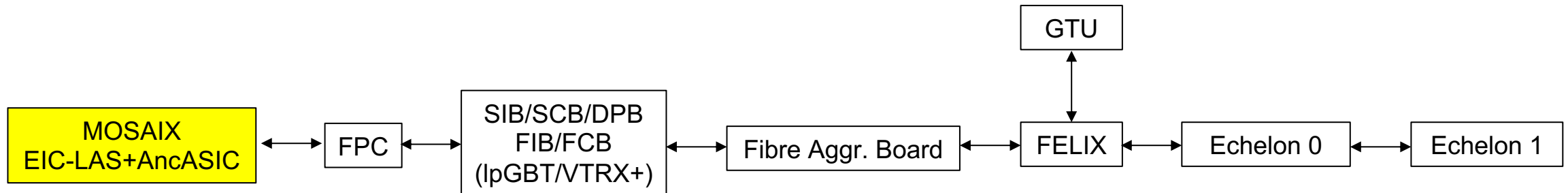
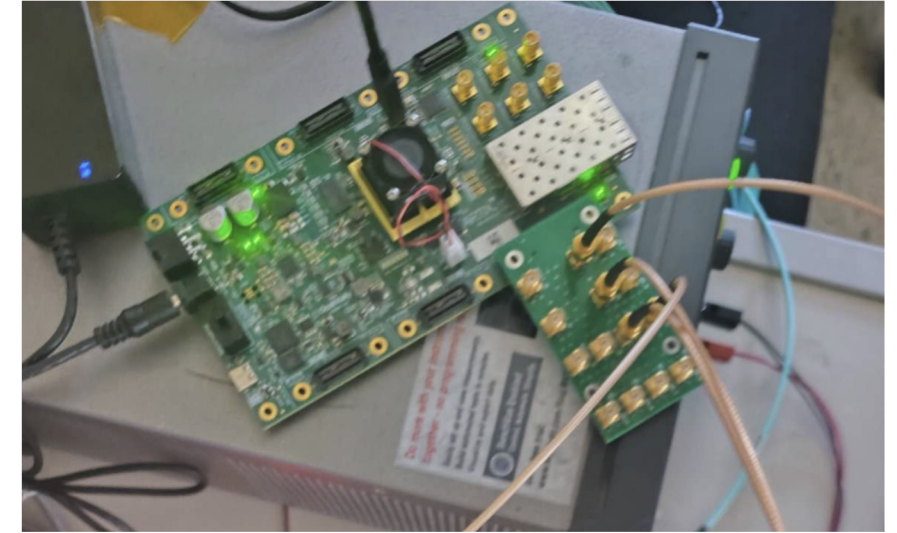
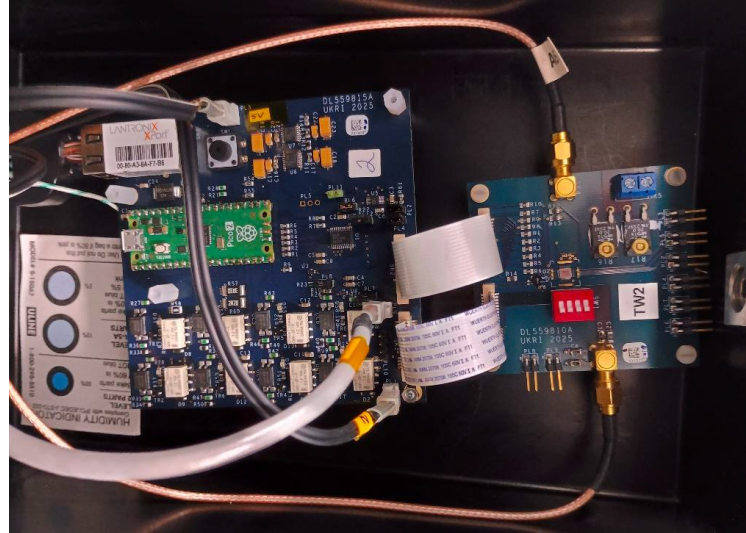
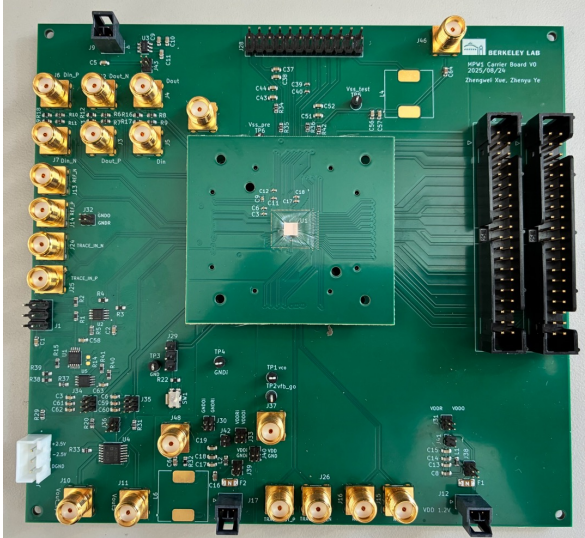
- ER2 FPGA emulator + test system available at a few SVT institutions which are also on ALICE-ITS3, a few months of lead time if placing an order now
- ER2 babyMOSAIX available at a few SVT institutions which are also on ALICE-ITS3, will become available for SVT institutions, after SVT wafers diced and mounted onto carriers at LBL in [2026Q4, 2027Q1]



AncASIC

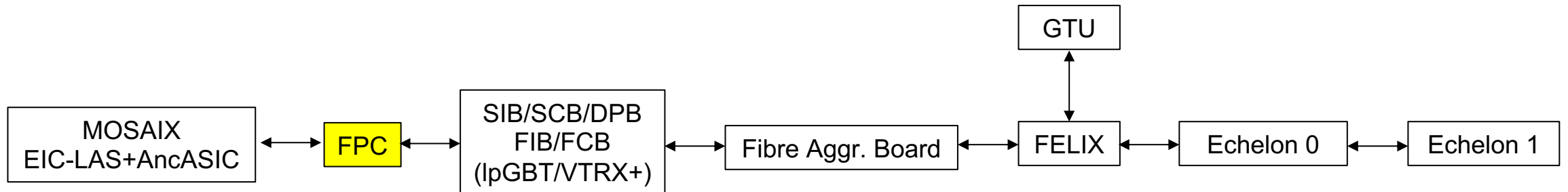
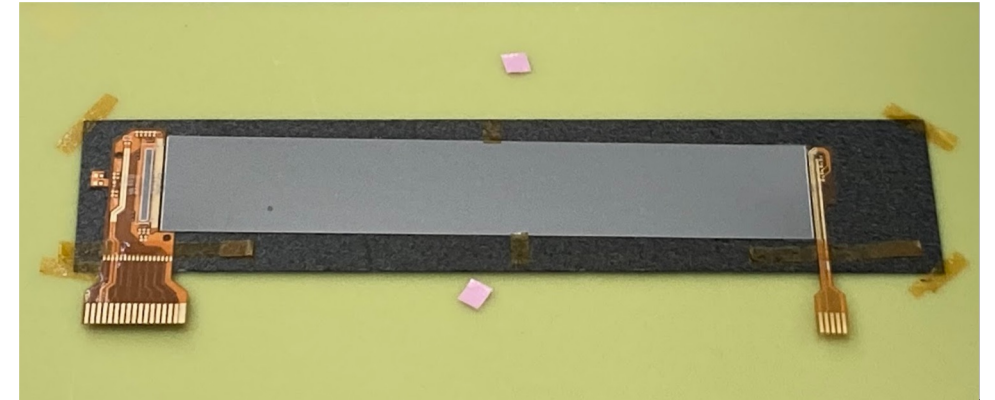
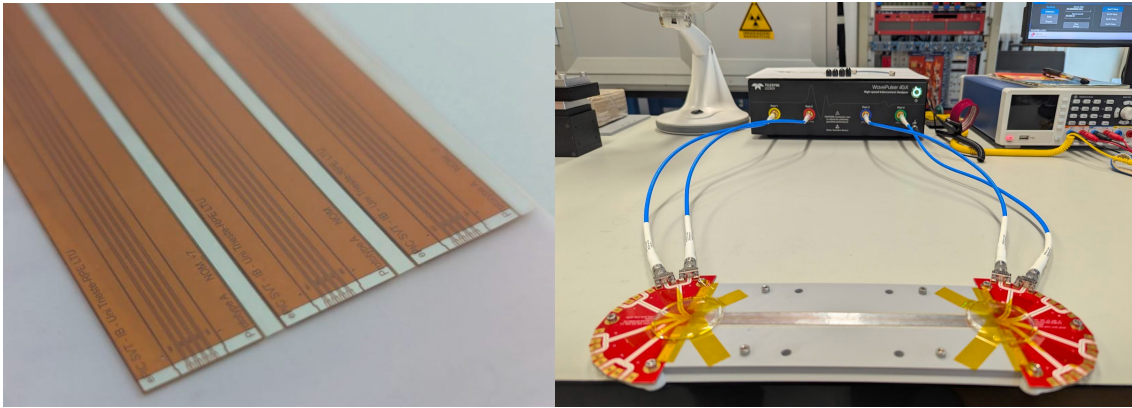
- MPW1: NVBG available at BNL/LBL
- MPW2: SLDO available at UK/LBL/Trieste
- MPW3: AncBrain FPGA emulator available at LBL

AncBrain, SLDOs and NVBG on Si available in [2027Q1]



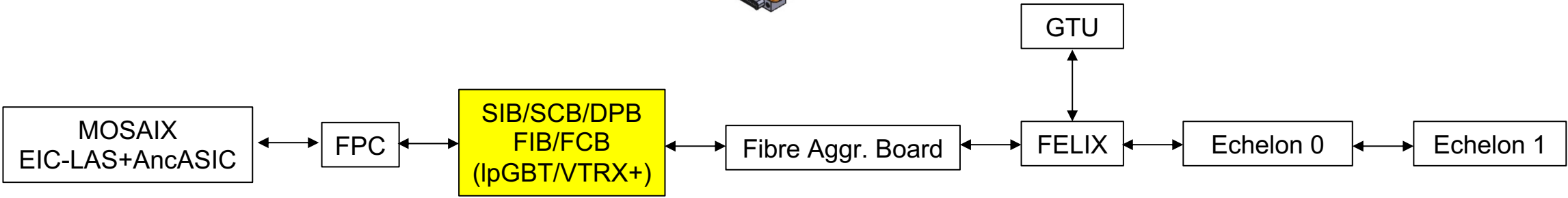
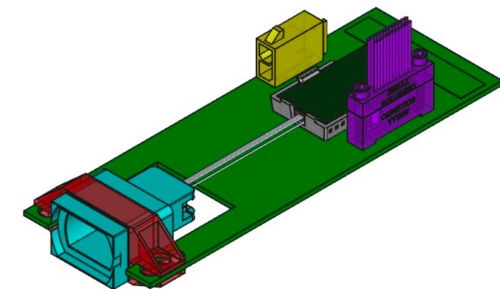
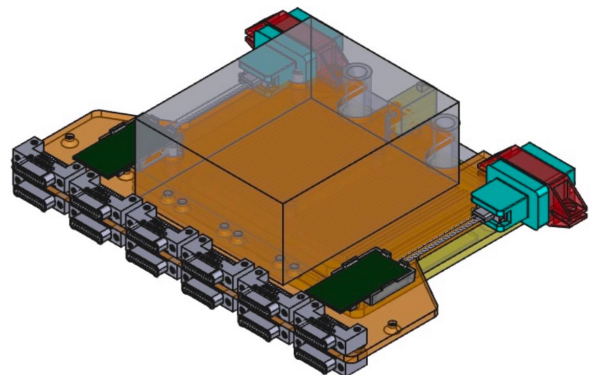
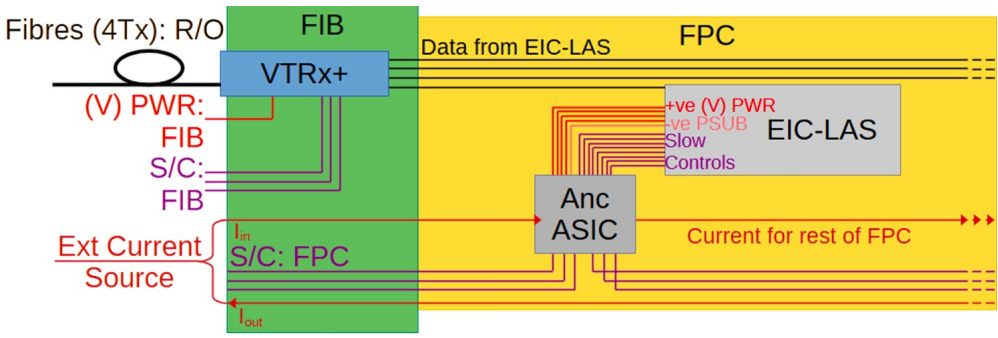
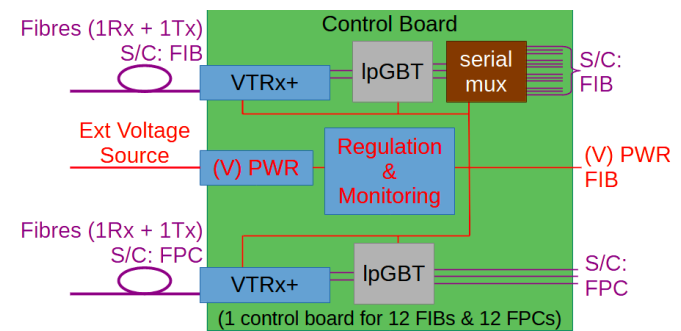
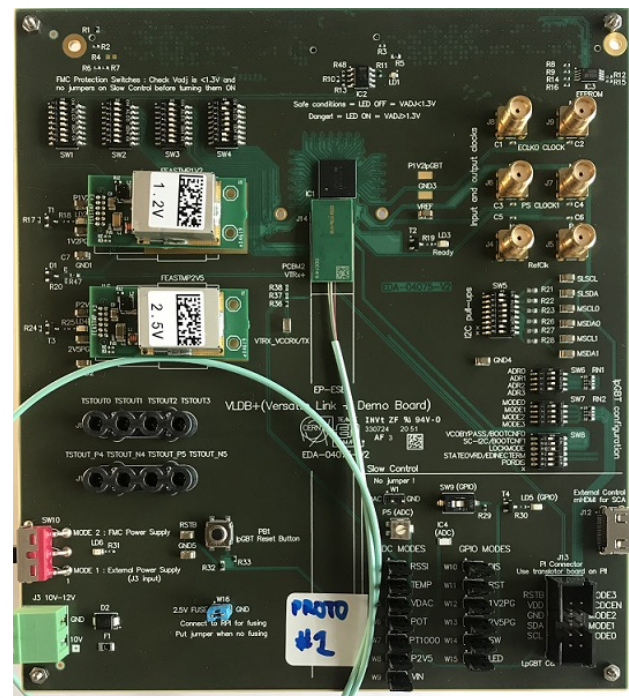
Flexible Printed Circuits

- Prototype FPCs available at INFN/LBL/UK
- First electrically functional FPC prototypes anticipated in [2027Q1, 2027Q2] (TBC)



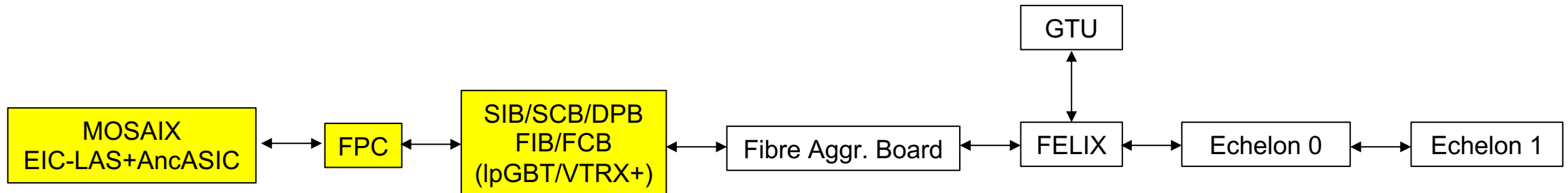
RDOs

- VLDB+ (lpGBT/VTRx+ CERN evaluation board) available through CERN
- First version of SVT FCB/FIB anticipated in [2027Q1, 2027Q2] (TBC)



babyMOSAIX+AncASIC+FPCs+RDOs

- Work can start now with MOSAIX and AncBrain FPGA emulators, and VLDB+
- We should aim at chain tests with ER2 sensor, AncASIC, FPCs, FIB/FCB in [2027Q2]

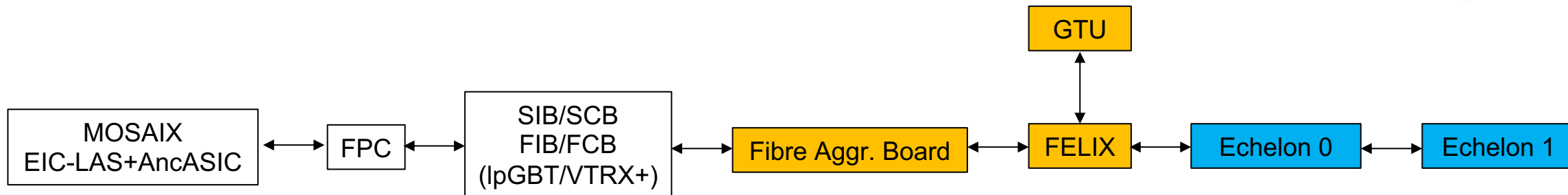
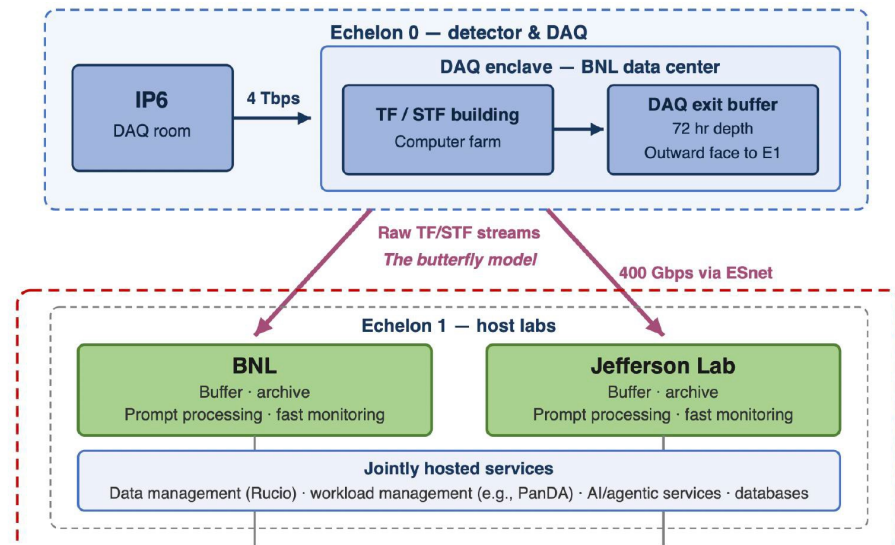
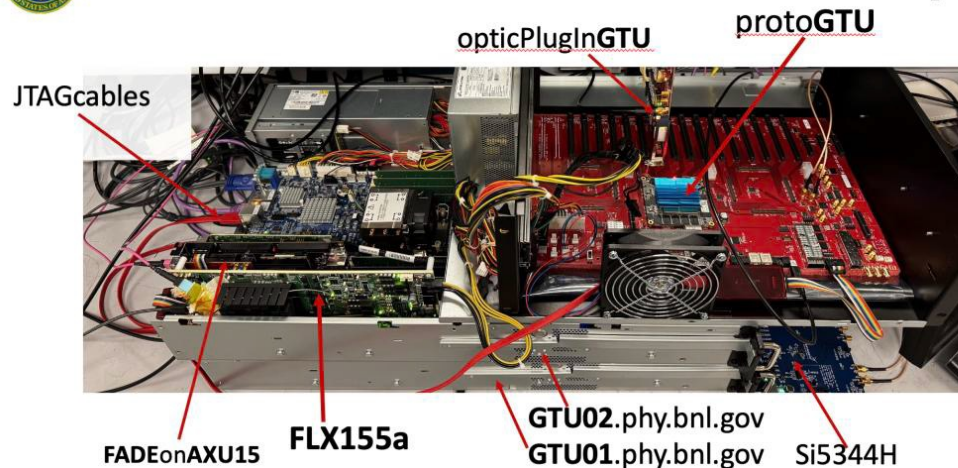


Fibre Aggr. Board, FELIX, GTU, Echelon 0/1

- Fibre Aggr. Board available in [2027Q1]
- FELIX (earlier version used by sPHENIX) available at BNL/ORNL/LANL/LBL/..., can be replaced by commercial FPGA evaluation kits for initial tests
- rcDAQ (sPHENIX), NestDAQ (Japan), CODA/JANA2/ERSAP (Jlab) for Echelon 0/1



3. The ePIC DAQ setup - at BNL (510_1-231)

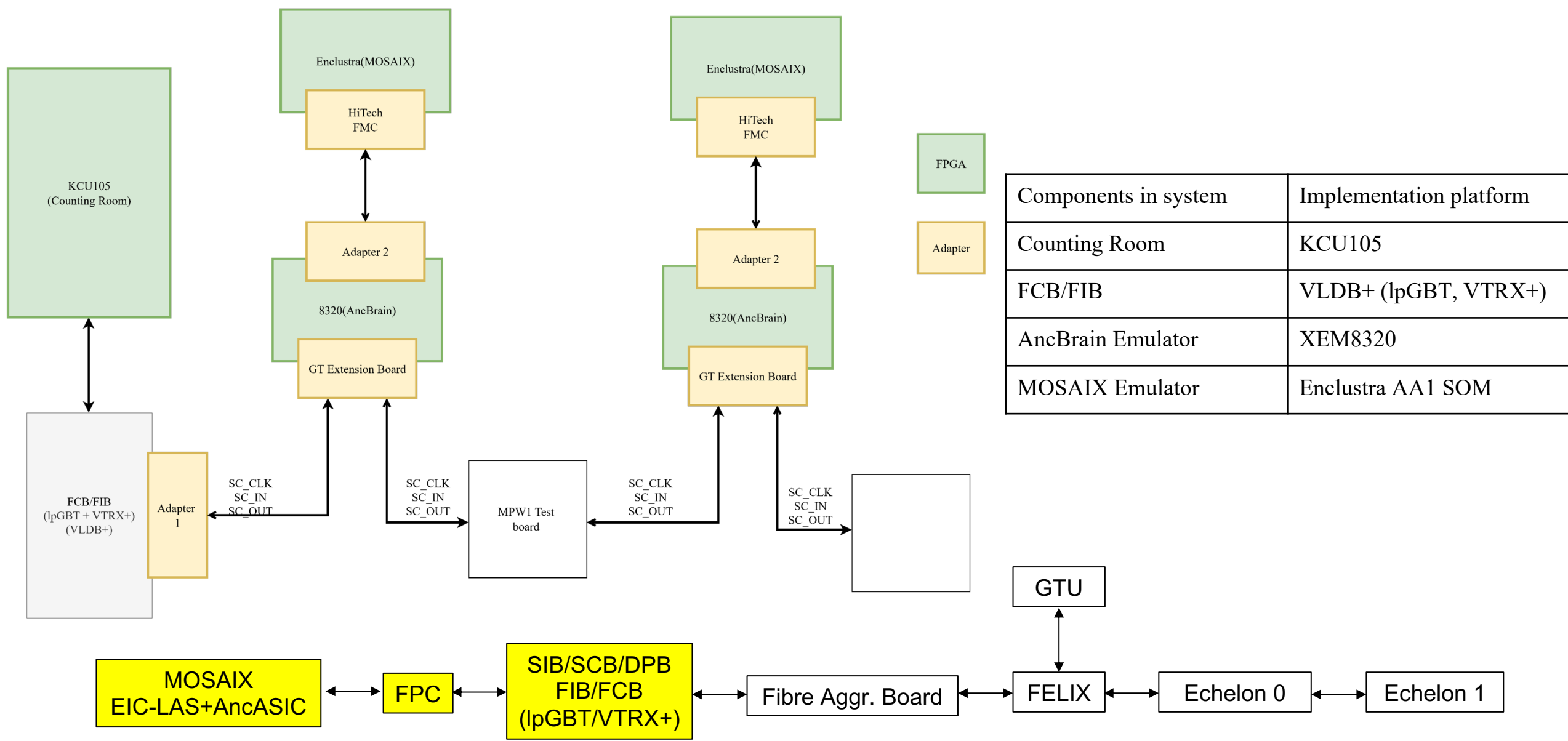




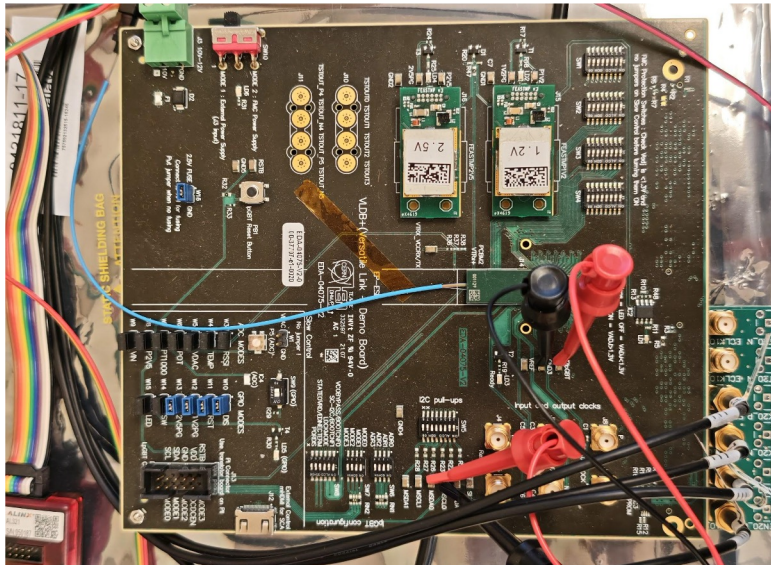
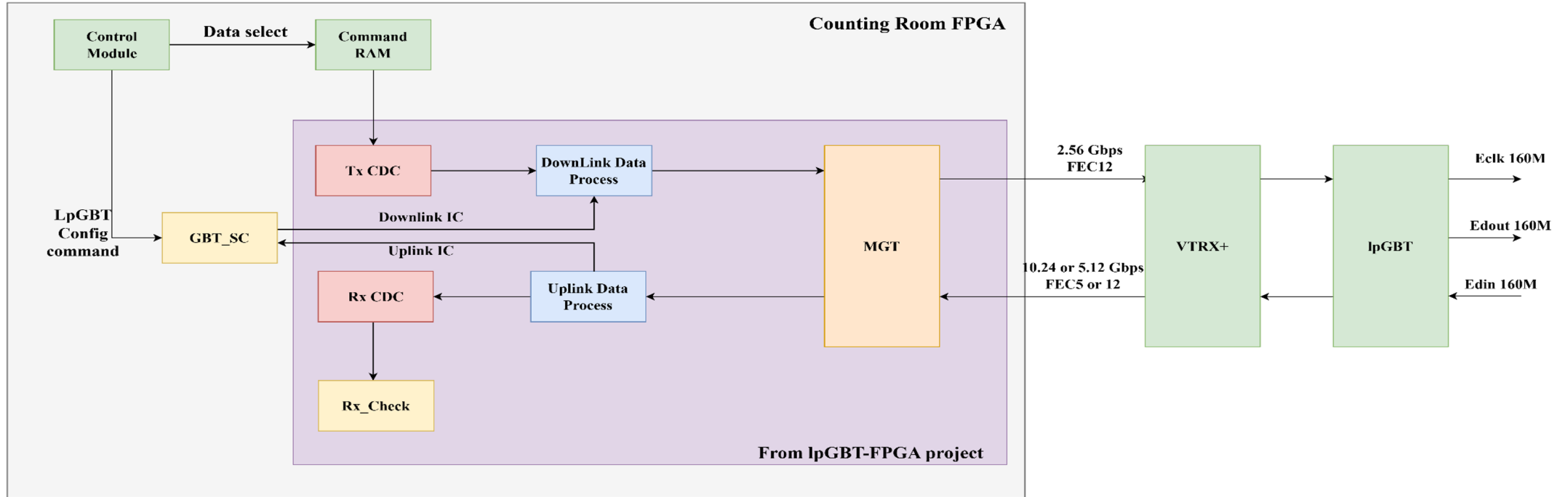
Work towards Chain Tests at LBL

Contributions from Yu Hu, Zhengwei Xue

Hardware Mockup Platform

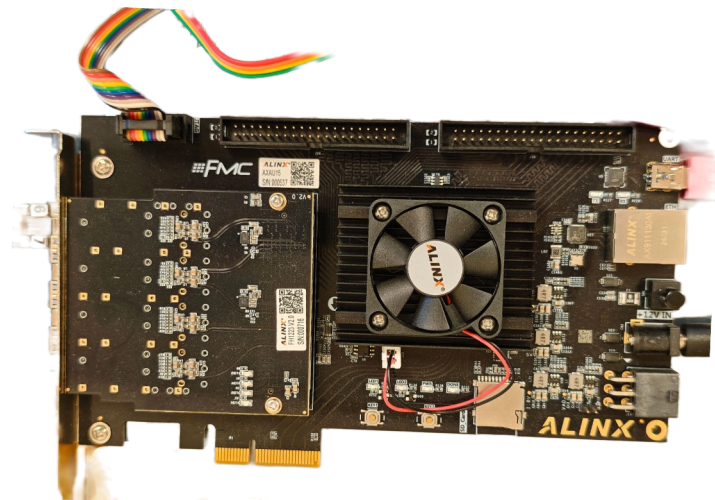


Counting room FPGA + lpGBT + VTRX+

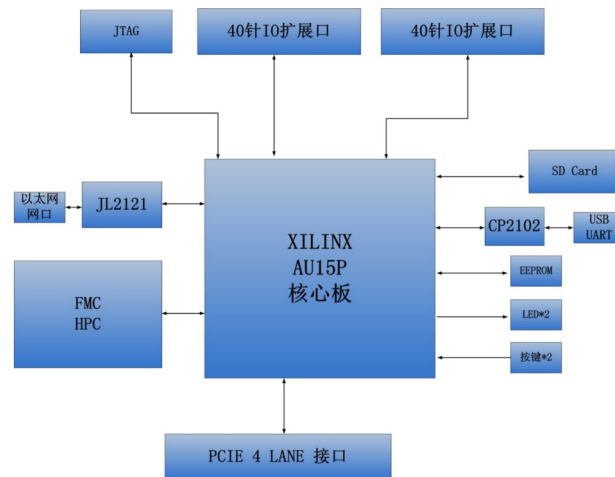


This project integrates key functionalities from lpGBT-FPGA and GBT-SC.

Using ETROC2 (CMS ETL) As a Testbed



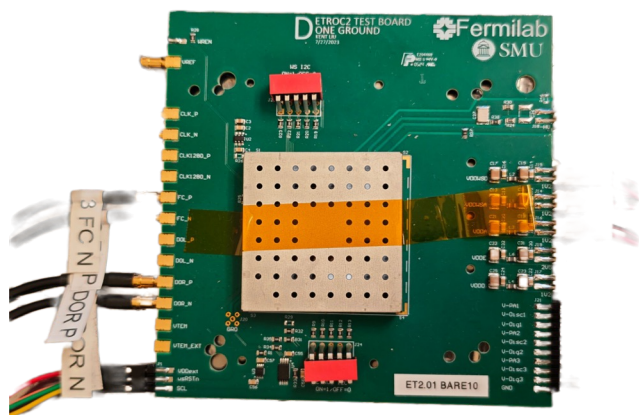
ARTIX UltraScale+ FPGA - AXAU15



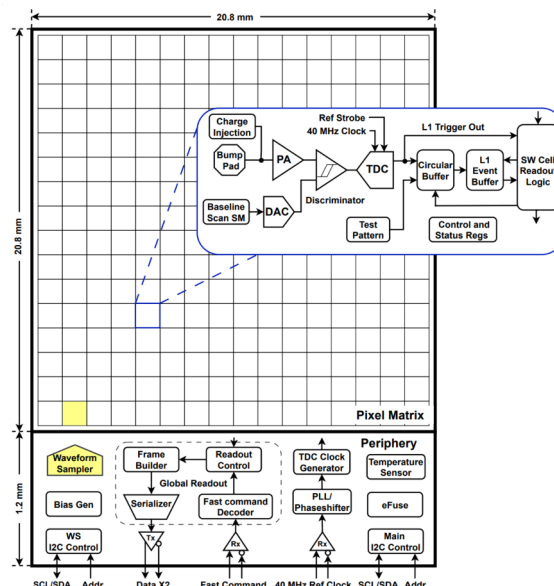
Core board schematics

- 200 MHz system master clock, 156.25 MHz ref clock to GTH
- 10/100/1000M ethernet RJ-45, USB Uart, PCIE x4, FMC HPC (4* SPF Module), JTAG,...

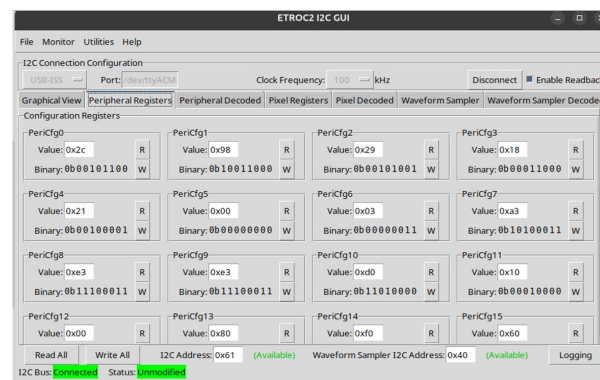
ETL ReadOut Chip (ETROC)



16x16 pixel matrix to pair with a 16x16 Low Gain Avalanche Diodes (LGAD)



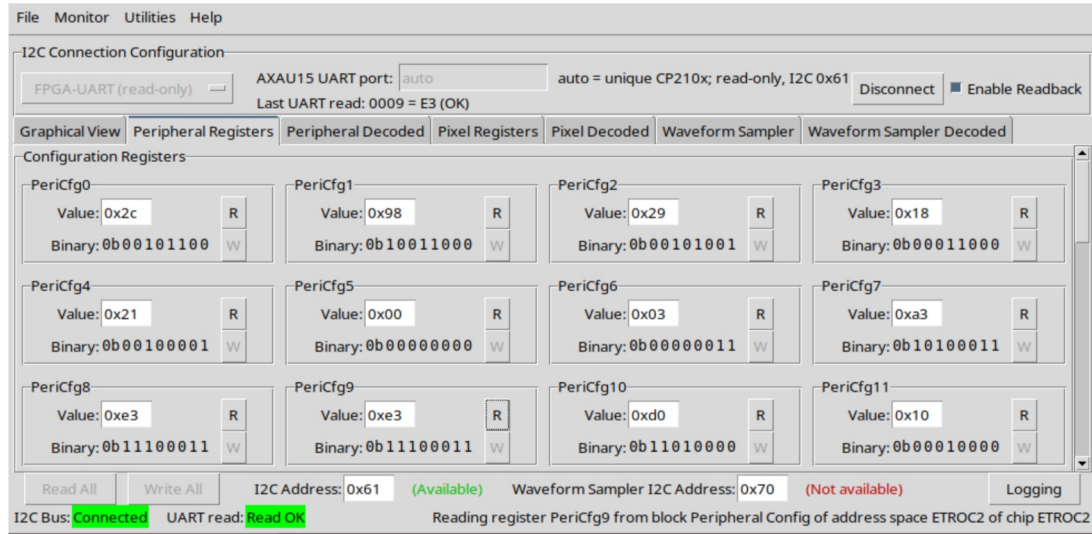
Block diagram of the ETROC2 chip



- Developed GUI package can be used to do SC through i2c
- A good starting point as reference for our SC flow



Control Room + IpGBT/VTRx+ ETROC2



✓ ETROC2 register R/W GUI

```
lbl268a@lbl268a-K30AD-M31AD-M51AD:~/VLDB/20261006-AXAU15-ETROC-DAQ-QINJ-v9$ python3 uart_control.py sta
rtup
status before: D1U0A0
init: I1
ECLK10: 0x21 (40 MHz)
ETROC softBoot pulsed (PeriCf0 0x00 -> 0x02 -> 0x00)
PeriSta0..5 = 2A 0B 00 83 0C 00
PS_Late      0
AFCcalCap    21
AFCBusy      0
fcAlignFinalState 0
controllerState 11
fcAlignStatus 0
fcBitAlignError 0
invalidFCCount 3203
pllUnlockCount 0
PS_Late samples 00110110
after 2 s: pllUnlockCount +0, invalidFCCount +3211, AFCcalCap 21->21, AFCBusy 0, controllerState 11
Assessment: PLL LOCKED (state 11, AFC idle, no new unlocks, stable AFCcalCap); invalidFCCount increasin
g (expected while no fast commands are sent)
```

✓ Initialize and configure IpGBT and ETROC

```
lbl268a@lbl268a-K30AD-M31AD-M51AD:~/VLDB/20261006-AXAU15-ETROC-DAQ-QINJ-v9$ python3 uart_control.py qin
j --delay 504 --repeat 3
saved 4096 words to captures/20261006_192954_qinj0.bin
word 115 3C5C054C5E HEADER L1counter=21 type=00 BCID=3166
word 116 8EE8B0E8A8 DATA EA=0 col=7 row=7 TOA=278 TOT=58 CAL=168
word 117 0000000183 TRAILER chipID=0x000000 status=0 hits=1 CRC=0x83
saved 4096 words to captures/20261006_192954_qinj1.bin
word 115 3C5C058AAF HEADER L1counter=22 type=00 BCID=2735
word 116 8EE8A8E8A9 DATA EA=0 col=7 row=7 TOA=277 TOT=58 CAL=169
word 117 0000000113 TRAILER chipID=0x000000 status=0 hits=1 CRC=0x13
saved 4096 words to captures/20261006_192954_qinj2.bin
word 116 3C5C05CA43 HEADER L1counter=23 type=00 BCID=2627
word 117 8EE8B0E8A8 DATA EA=0 col=7 row=7 TOA=278 TOT=58 CAL=168
word 118 0000000147 TRAILER chipID=0x000000 status=0 hits=1 CRC=0x47
QInj delay 504 BX, 3 injection(s): header 3, data 3, trailer 3
```

✓ Charge injection and receive data from ETROC

AncBrain FPGA Emulator

AncBrain emulator developed on XEM8320, with RTL from BNL AncBrain project.

- ✓ Internal Register Read/Write Test
- ✓ Broadcast Signal Generation Test
- ✓ Error Injection and Handling Tests
- To-do: tests with MOSAIX emulator.

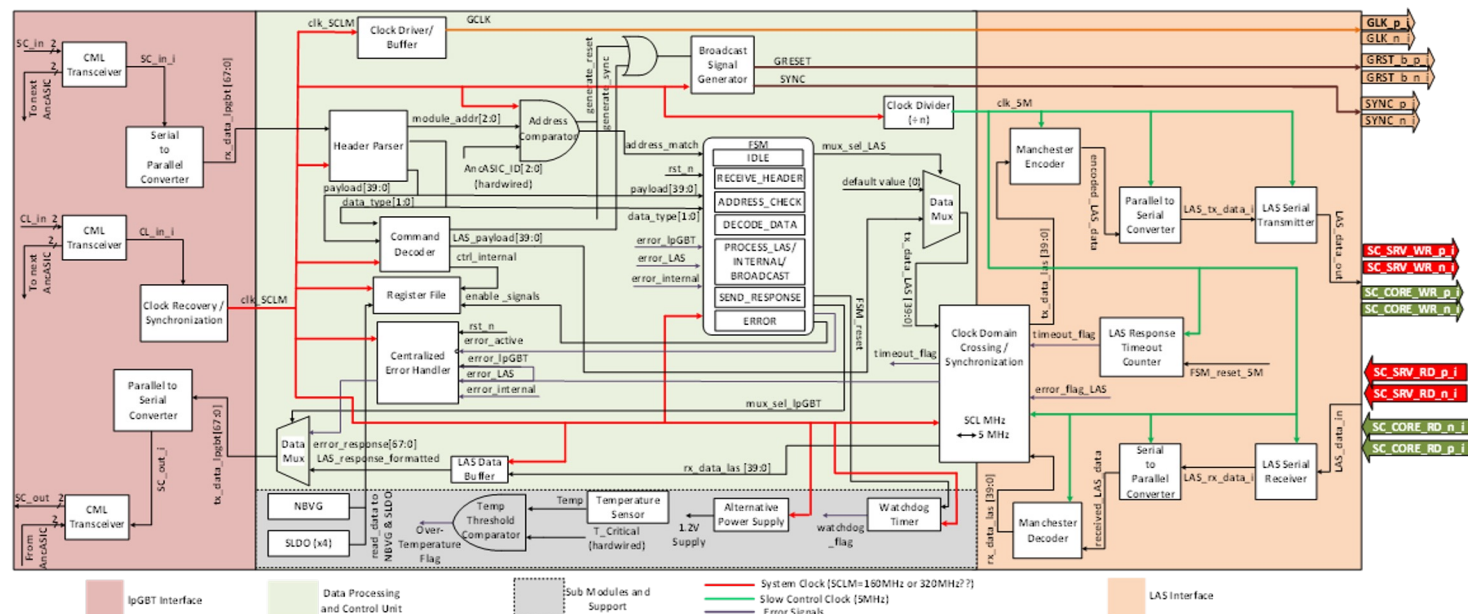


KCU105



VLDB+

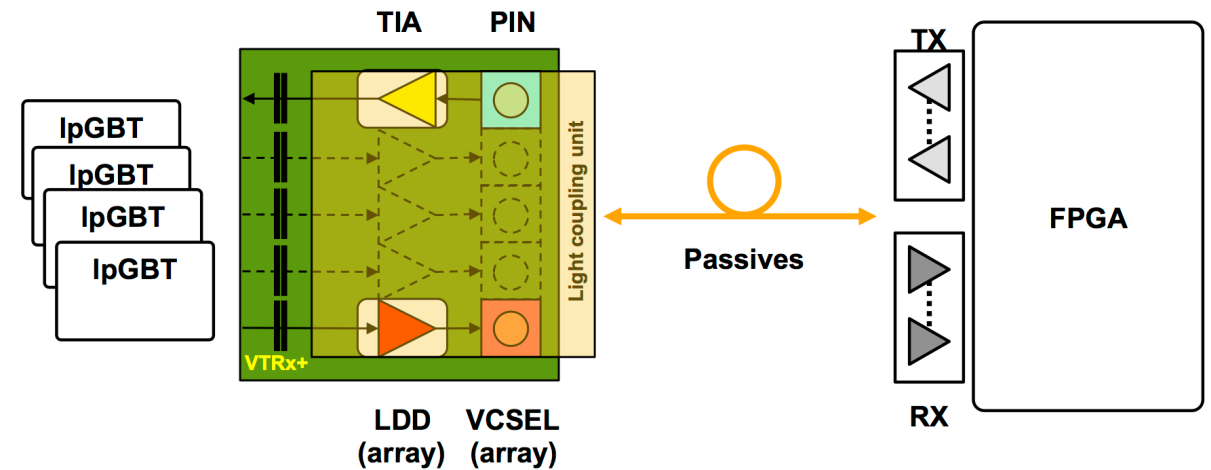
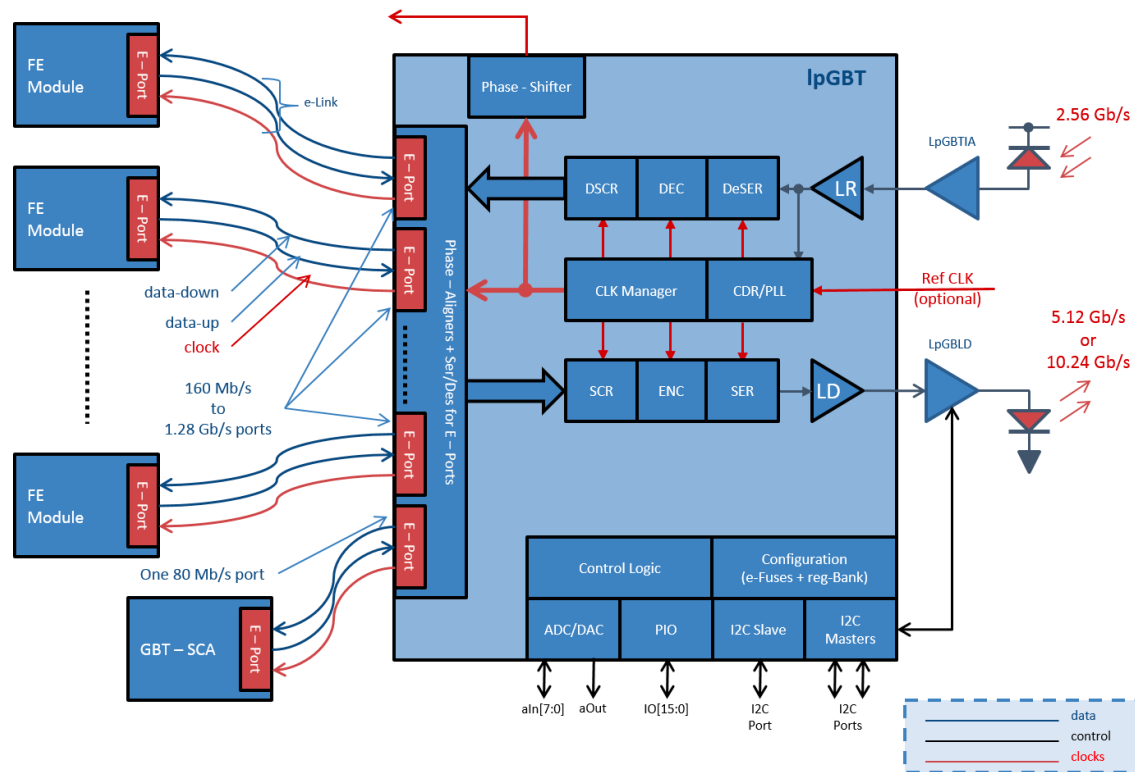
XEM8320



Summary and Outlook

- Used ETROC2 as a testbed to establish a general framework for slow control and readout via lpGBT and VTRx+
 - VTRx+ optical downlink/uplink established using FPGA GTH and lpGBT
 - lpGBT initialized from the FPGA; register R/W verified through VIO
 - ETROC2 register R/W via lpGBT I²C
 - ETROC2 clock supplied by lpGBT ECLK10 (40 MHz); PLL lock verified
 - ETROC2 readout verified: fillers, event frames, and charge-injection data read through the uplink
- Moving towards MOSAIX/EIC-LAS+AncASIC
 - AncBrain emulator developed on FPGA based on RTL of AncASIC MPW3 submission.
 - We should aim at chain tests using babyMOSAIX, AncASIC, FPCs, FCB/FIB in [2027Q2]

IpGBT and VTRx+



Low Power Giga Bit Transceiver (IpGBT)

for high-speed bi-directional links

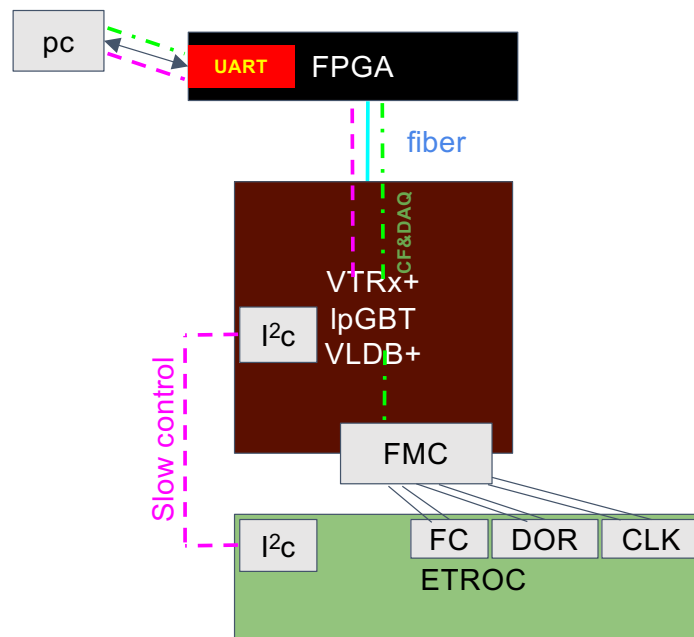
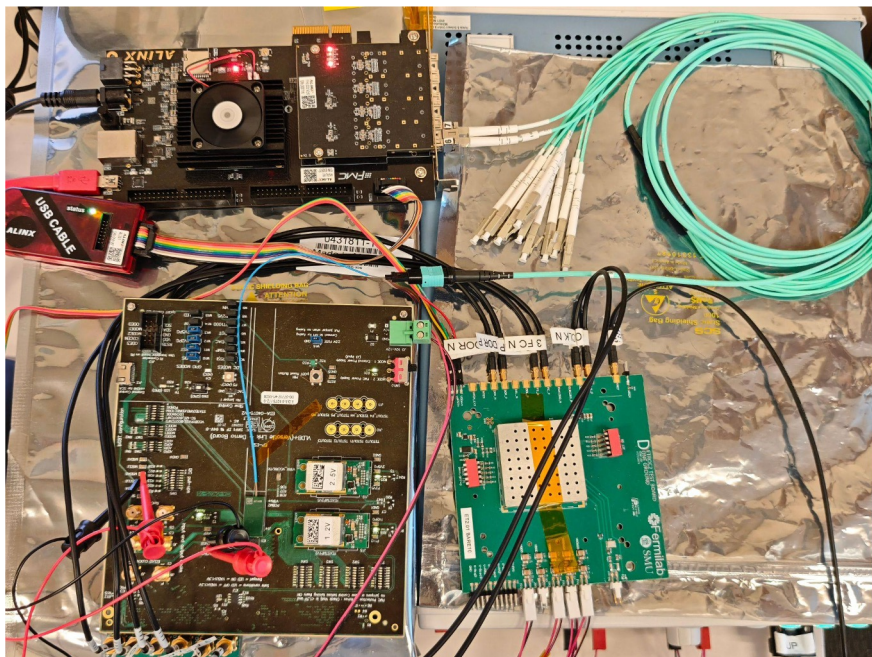
- 2.56 Gb/s links in the direction from the counting room to detectors (downlink)
- 5.12 or 10.24 Gb/s in the direction from detectors to the counting room (uplink)

Versatile Link+ Transceiver (VTRx+)

for optoelectronic conversions

- 4Tx up to 10.24 Gb/s
- 1 Rx up to 2.5 Gb/s

FPGA + VLDB + ETROC Control Path



Clocks and sync

- Master clock: FPGA oscillator → MGT → 2.56 Gb/s downlink
- IpGBT: recovers 40 MHz from the downlink → whole system synchronous
- ETROC2 clock: IpGBT ECLK10 (40 MHz) → ETROC PLL → TDC and 320 Mb/s links
- FC: FPGA → 1 byte / 25 ns → EDOUT10 → IDLE (0xF0)/Command
- Data: ETROC → EDIN10 → 5.12 Gb/s uplink → FPGA recovered clock
- Timing: FPGA counts BX → charge injection → L1A after exactly 504 BX ($12.5 \mu s + 3BX$)

UART protocol

- Link: PC → USB-UART (2 Mbaud) → FPGA; text commands → 1-line reply
- Registers R/W, Control, setup automatic L1A after each charge injection, Readout, Decoding (PC)

Streaming:

- Fast-command link & Data link (FPGA → ETROC) is always streaming
- The readout itself is running “trigger model” - leave only when L1A arrives
- Capture: FPGA hold 4096-word ($\sim 8 \times 504 BX$, 102 us), then read over UART

Physical: VLDB+ FMC J2 → extension board → SMA cables → ETROC2 test board

Control path: PC → USB-UART (2 Mbaud) → AXAU15 FPGA (AU15P) → optical fibre → VLDB+ IpGBT

Downlink (2.56 Gb/s, IpGBT-FPGA core):

- IpGBT IC channel → IpGBT registers (configuration)
- IpGBT I2C master → ETROC2 slow control (registers, pixel config)
- FC byte, 8 bits per 25 ns → IpGBT eTx group 1 → EDOUT10 → ETROC2 FC (320 Mb/s)
- ECLK10 (40 MHz) → ETROC2 reference clock

Uplink (5.12 Gb/s, FEC5):

- ETROC2 data out (320 Mb/s) → IpGBT eRx EDIN10 → fiber → FPGA
- FPGA records raw frames into block RAM → UART dump → Python decoder

Verified AncBrain Simulation Test Cases

The simulation testbench was set up to specifically validate the interaction between the **AncBrain module** and a **loopback module**, with the lpGBT interface inputs being driven by a shift register to generate controlled command patterns.

- **Internal Register Read/Write Test:**

- Ensures configuration and check registers are accessible.

- **Broadcast Signal Generation Test:**

- Verifies the correct generation and timing of broadcast signals.

- **Error Injection and Handling Tests:**

- Validated the design's robustness against various induced errors, including:
 - CRC Errors
 - Parity Errors
 - Missing EOF or SOF
 - Address Errors

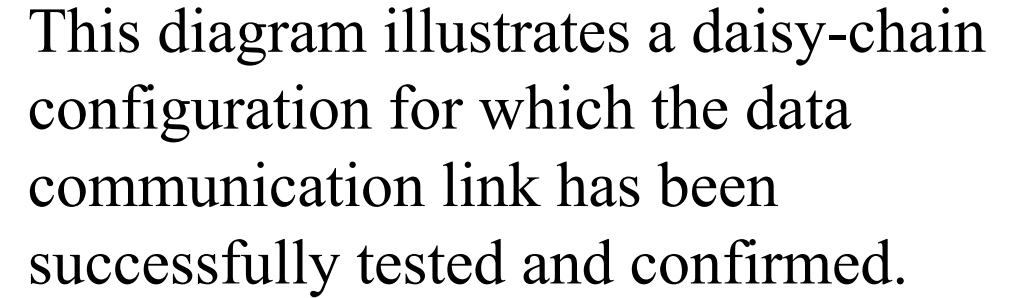
- **Interface Verification with the LAS Emulator:**

- Verified the firmware's response processing logic by utilizing a loopback module that intentionally delays the returned data.

To-do:

Perform simulations with the integrated MOSAIX emulator module.

Complete and expand the Error Injection test suite.



Similar to the CML (Current-Mode Logic) Transceiver in the AncBrain, the FPGA's on-chip GTY transceivers also operate based on the CML standard, which could provide a hardware-level approximation for testing key aspects of the signal standard, such as DC vs. AC coupling.