

SiPM info.

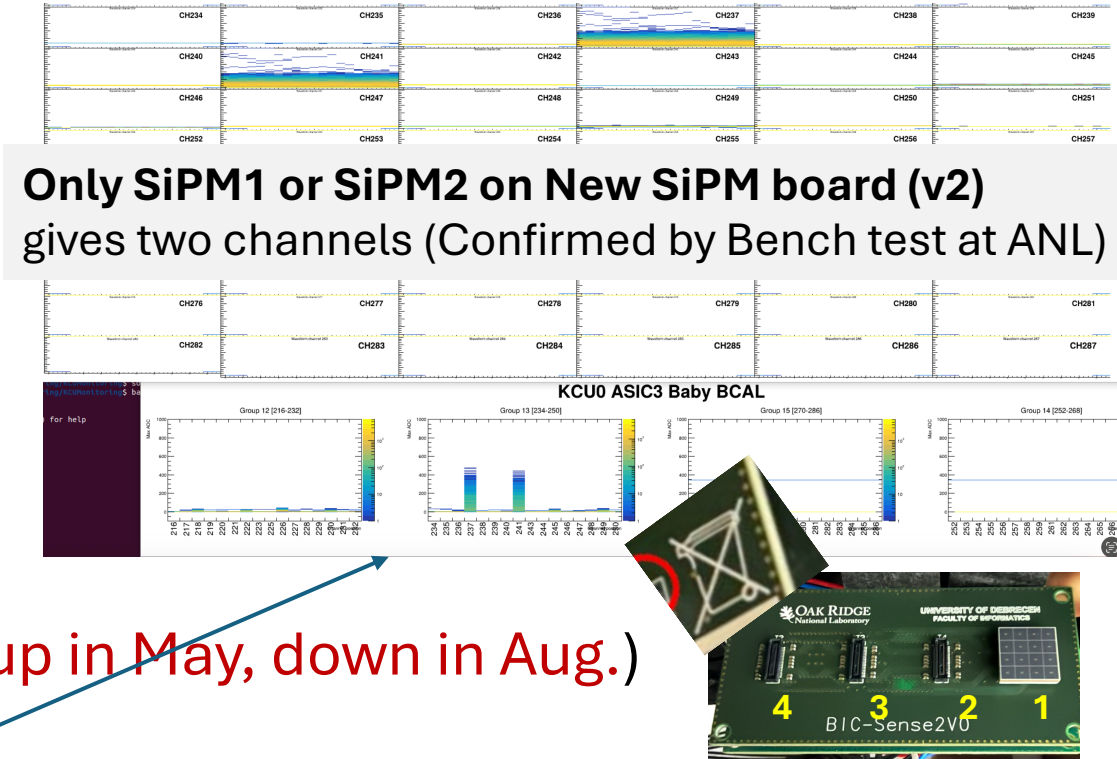
2026/9/29

Bobae Kim

*Updates 10/8; Correct SiPM3,SiPM4 → SiPM1, SiPM2

Contents

- Running periods:
 - May run
 - August run with dummy SFIL
 - August run with all active SFILs
- Items to verify:
 - SiPM board orientation (Always trash cans **up in May, down in Aug.**)
 - SiPM array - ASIC channel mapping
 - Observed **Not a one-to-one response** on summing boards (only New SiPM board (V2))
- Issue
 - **May** : The mapping of **SiPM1** and **2** to the ASIC channel (from **v2 New SiPM board**) ranges needs to be confirmed by a bench test.
 - On-going; using individual channels, then, matching group number
 - **Aug. : Two SiPMs (SiPM1 and SiPM2) are mixed** on the **new SiPM board (V2)**.
 - Done

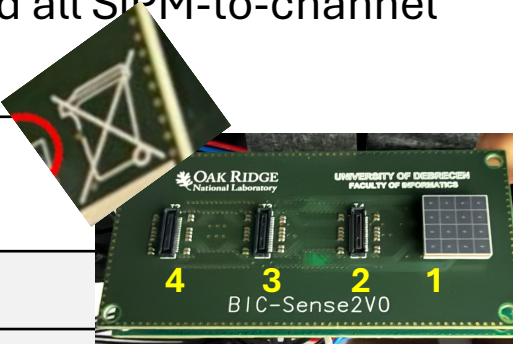


May TB: old/new SiPM boards

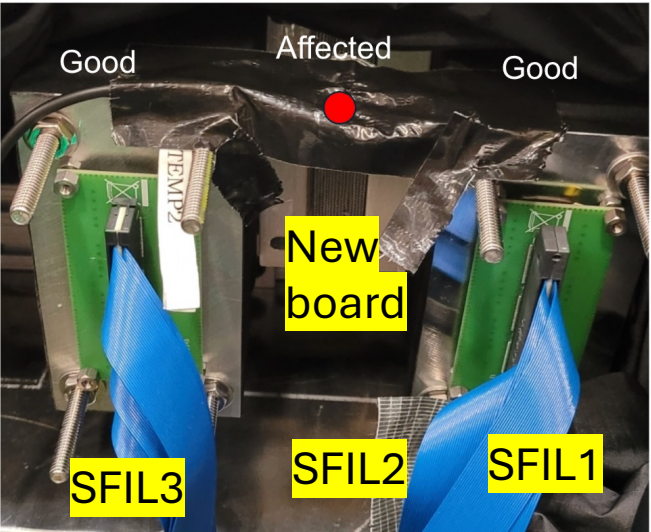
- On May 13, KCU1 SFIL 2 was moved from ASIC A2 to ASIC A3, while the KCU0 configuration and all SiPM-to-channel assignments remained unchanged.

North SiPM board	SFIL	South SiPM board
1	1	2
2	2	2
1	3	1

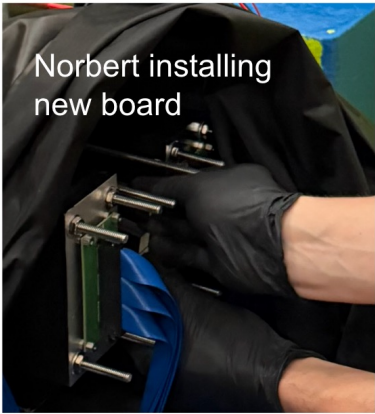
North KCU1	SFIL	South KCU0
A0	1	A0
A2 → A3	2	A2
A1	3	A1



HGCROC Mapping - ASIC 1 (North)

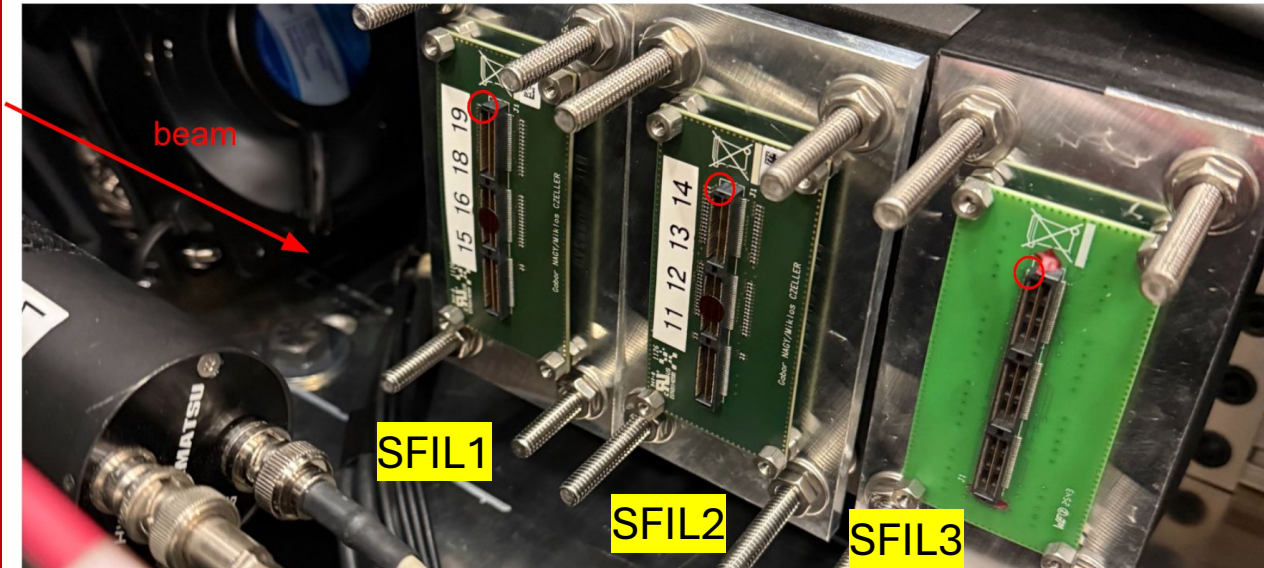


It looks like new SIPM boards have swapped traces for last two groups



Top - Bottom (ASIC 0 - SOUTH)

Same orientation. Group 0 on the bottom!

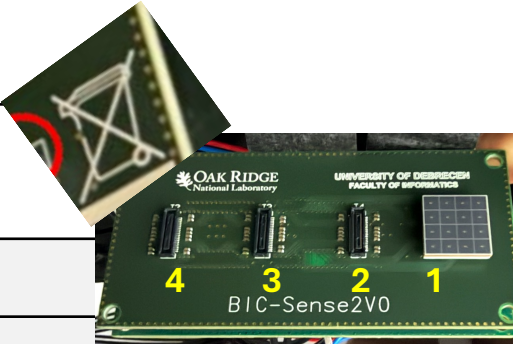


May TB: old/new SiPM boards

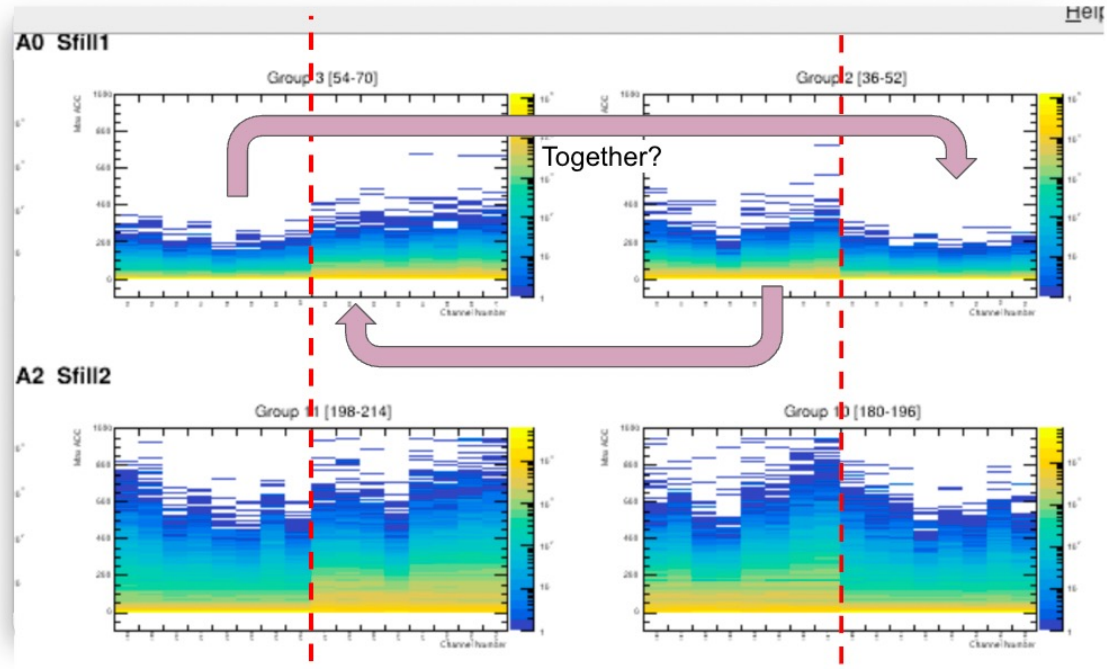
*Note: Group 0 is bottom! = **SiPM1**

North SiPM board	SFIL	South SiPM board
1	1	2
2	2	2
1	3	1

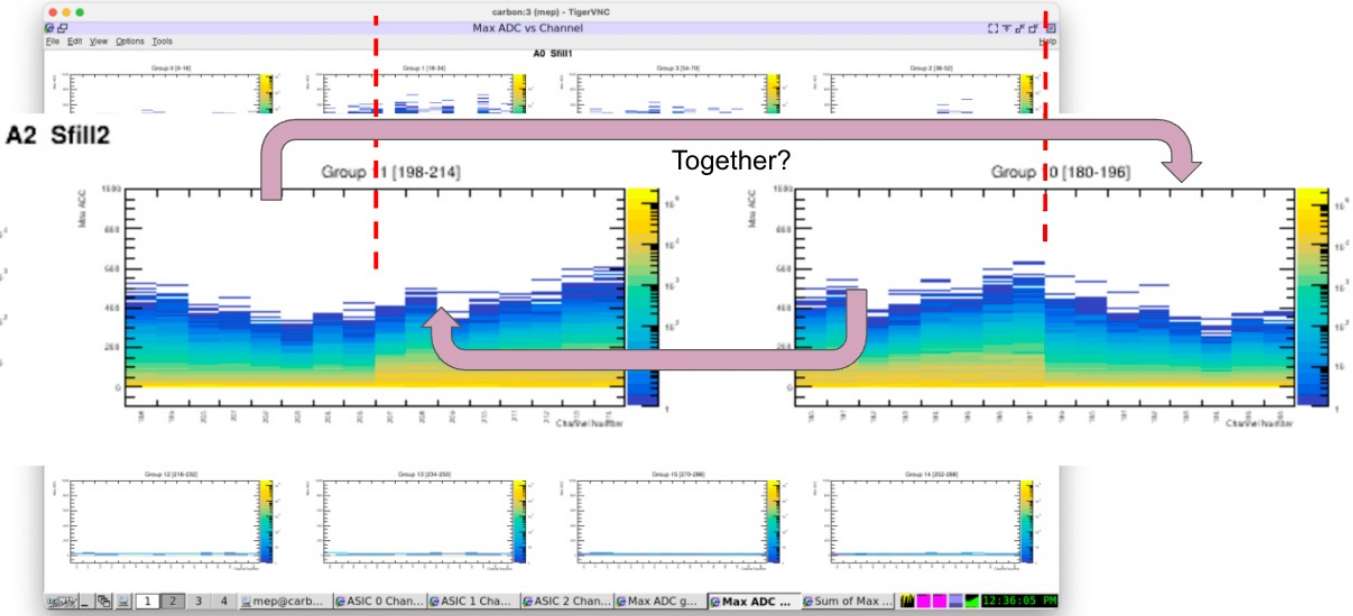
North KCU1	SFIL	South KCU0
A0	1	A0
A2 → A3	2	A2
A1	3	A1



HGCROC Mapping - ASIC 0 (South)



HGCROC Mapping - ASIC 1 (North)

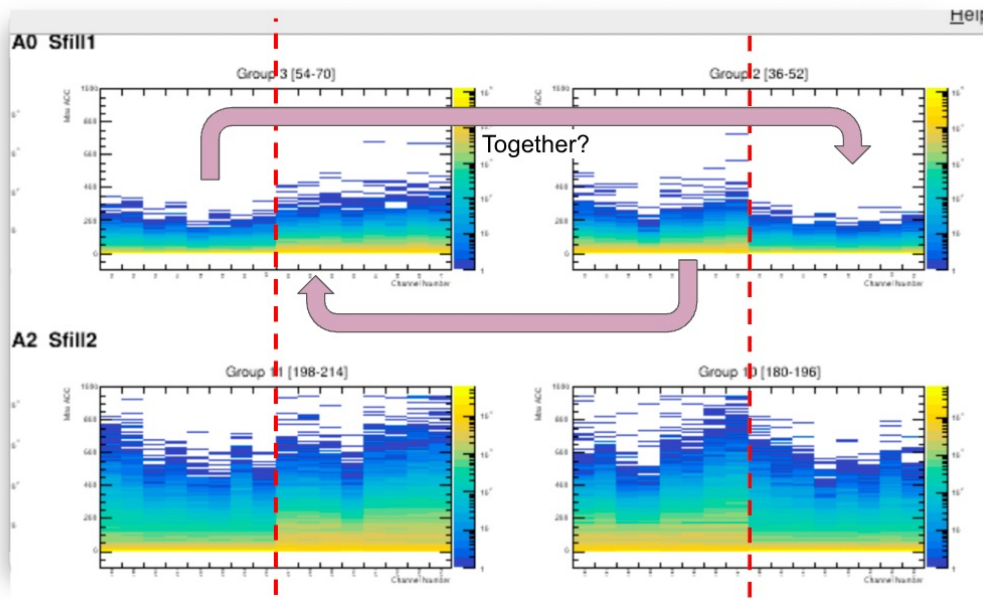


May TB: before/after 5/13

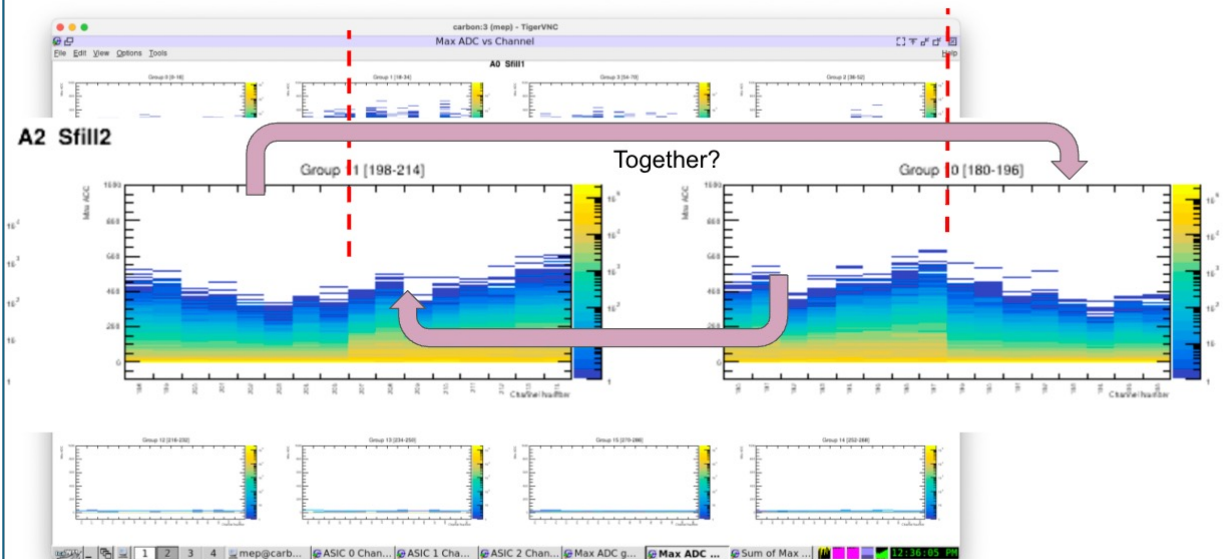
- On May 13, KCU1 SFIL 2 was moved from ASIC A2 to ASIC A3, while the KCU0 configuration and all SiPM-to-channel assignments remained unchanged.

Side	SFIL	KCU	Before May 13	After May 13	Change
South	SFIL1	KCU0	A0	A0	No change
South	SFIL2	KCU0	A2	A2	No change
South	SFIL3	KCU0	A1	A1	No change
North	SFIL1	KCU1	A0	A0	No change
North	SFIL2	KCU1	A2	A3	A2 → A3; Move channels 144-214 into 216-286
North	SFIL3	KCU1	A1	A1	No change

HGCROC Mapping - ASIC 0 (South)

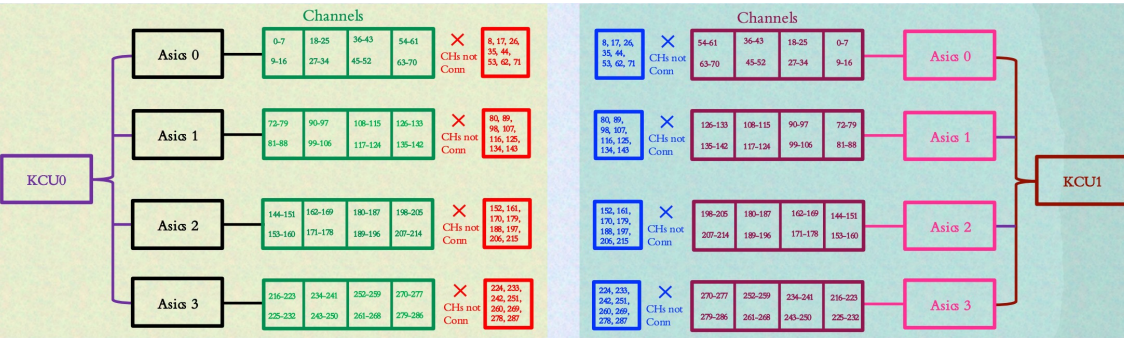


HGCROC Mapping - ASIC 1 (North)



May TB: Mapping info.

SFIL	Side	KCU	SiPM Array	ASIC	Channel ranges	Note
SFIL 1	South	KCU0	SiPM 1	A0	0–7, 9–16	
			SiPM 2	A0	18–25, 27–34	
			SiPM 3	A0	45–52, 54–61	Note the swap
			SiPM 4	A0	36–43, 63–70	Note the swap
SFIL 2			SiPM 1	A2	144–151, 153–160	
			SiPM 2	A2	162–169, 171–178	
			SiPM 3	A2	180–187, 207–214	Note the swap
			SiPM 4	A2	189–196, 198–205	Note the swap
SFIL 3			SiPM 1	A1	72–79, 81–88	
			SiPM 2	A1	90–97, 99–106	
			SiPM 3	A1	126–133, 135–142	
			SiPM 4	A1	108–115, 117–124	



SFIL	Side	KCU	SiPM Array	ASIC	Channel ranges	Note
SFIL 1	North	KCU1	SiPM 1	A0	0–7, 9–16	
			SiPM 2	A0	18–25, 27–34	
			SiPM 3	A0	54–61, 63–70	Note the swap;
			SiPM 4	A0	36–43, 45–52	Note the swap;
SFIL 2			SiPM 1	A2 → A3	144–151, 153–160 → 216–223, 225–232	Changed to A3 on 05/13
			SiPM 2	A2 → A3	162–169, 171–178 → 234–241, 243–250	Changed to A3 on 05/13
			SiPM 3	A2 → A3	180–187, 207–214 → 252–259, 279–286	Note the swap; changed to A3 on 05/13
			SiPM 4	A2 → A3	189–196, 198–205 → 261–268, 270–277	Note the swap; changed to A3 on 05/13
SFIL 3			SiPM 1	A1	72–79, 81–88	
			SiPM 2	A1	90–97, 99–106	
			SiPM 3	A1	126–133, 135–142	
			SiPM 4	A1	108–115, 117–124	

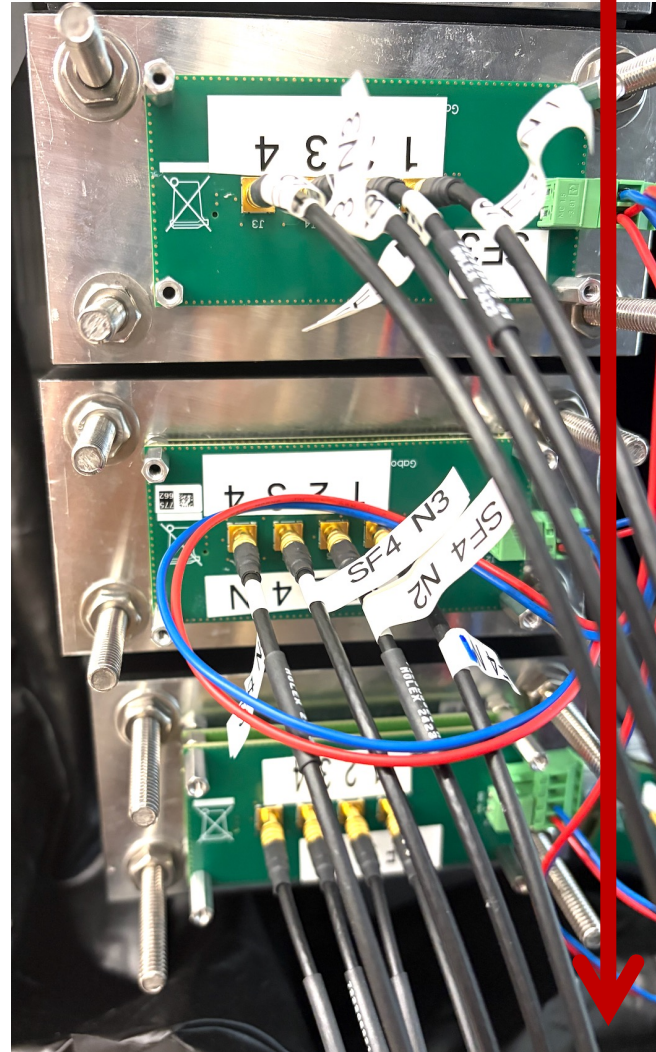
Aug. TB setup: old/new SiPM boards

Beam
direction

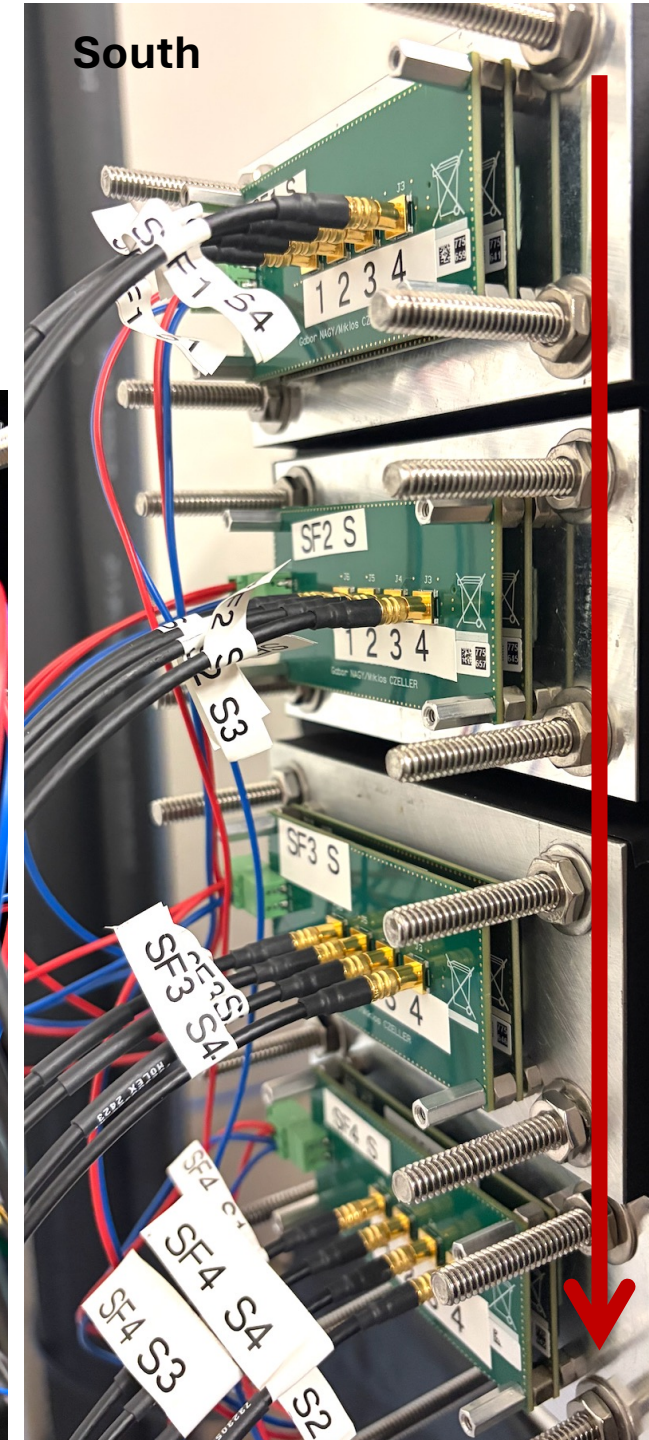
North SiPM board	SFIL	South SiPM board
1 (old)	1	2
2 (new)	2	2
2	3	2
2	4	2
1	5	1

* All trash cans on both sipm and summing boards, facing **downward** with respect to the beam direction.

North



South



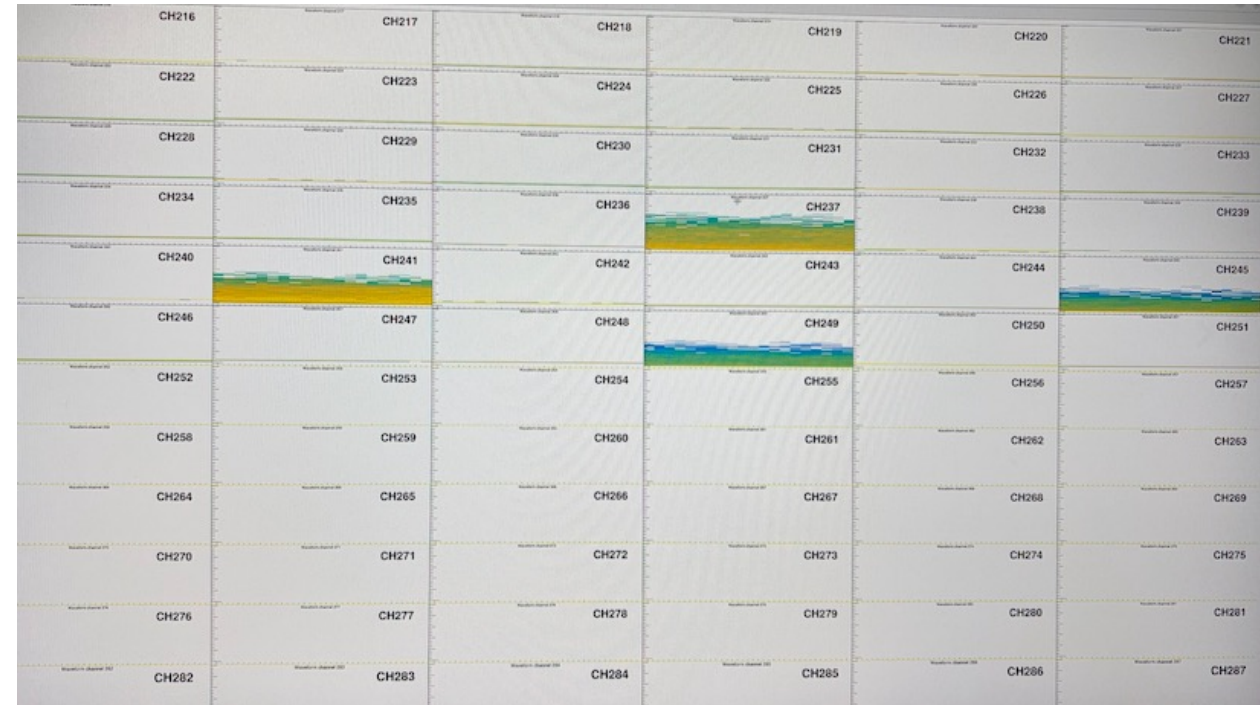
Aug. TB setup: **old**/new SiPM boards + summing board Check

- Used North SFIL1 (v1 sipm board; Old) and SFIL2 (v2 sipm board; new)
- The old SiPM board showed a one-to-one response for all four channels.
- The new SiPM board showed a one-to-one response only for SiPM1 and SiPM2.
- When SiPM1 or SiPM2 was illuminated with the LED, both **Ch241 and 237 responded**.

Example. One-to-one response

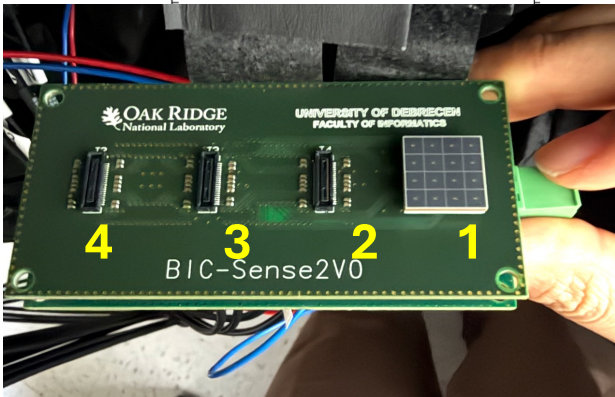
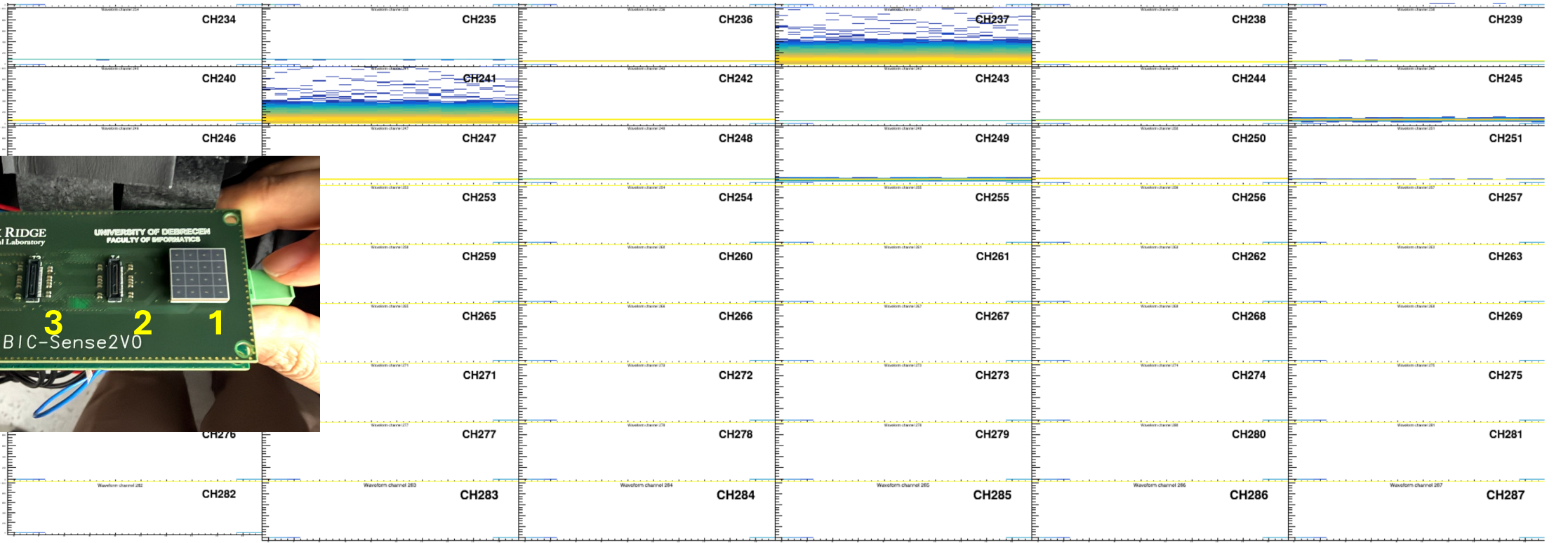


Example. $\frac{1}{2}(\text{SiPM1} + \text{SiPM2})$ response @ New sipm boards

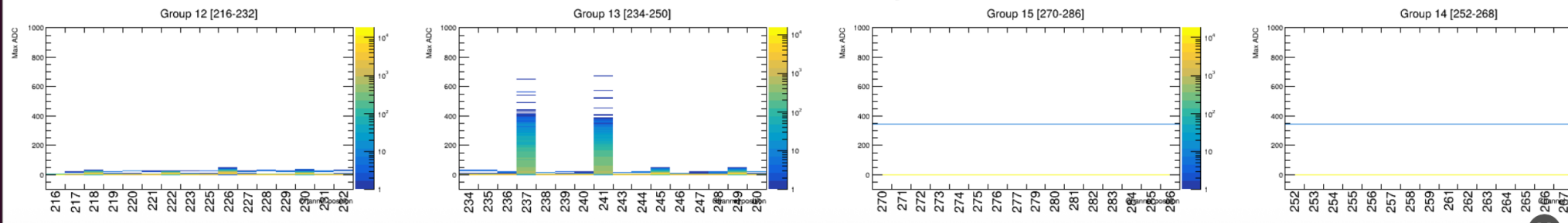


Aug. TB setup: old/new SiPM boards + summing board Check

- Used SFIL2 North (new SiPM board)
- Remove SiPM 2,3,4 & Connect only **SiPM1**

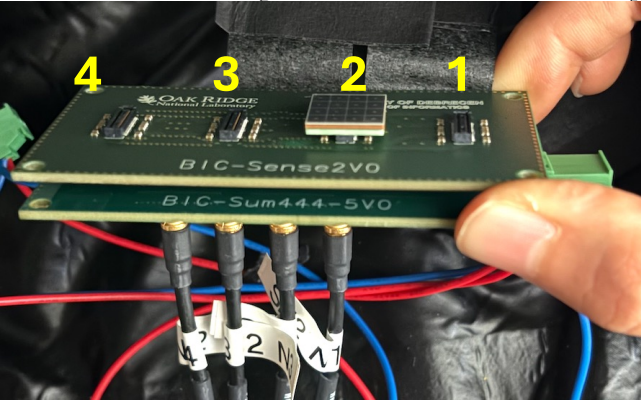
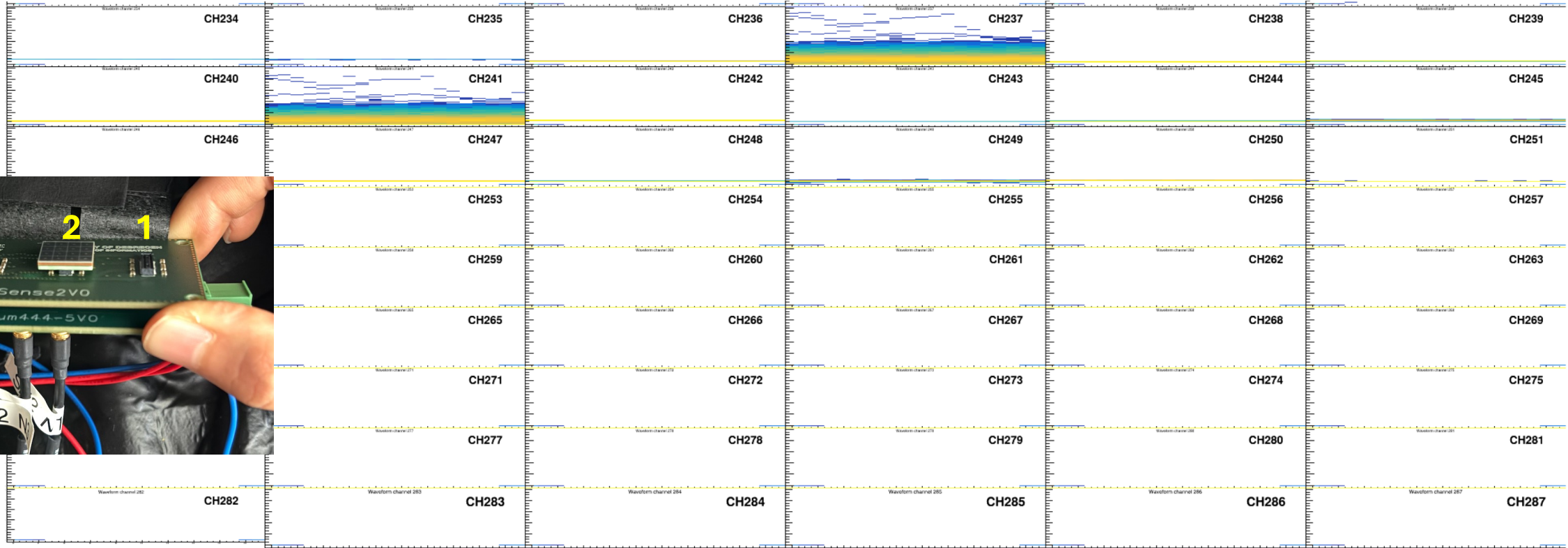


KCU0 ASIC3 Baby BCAL



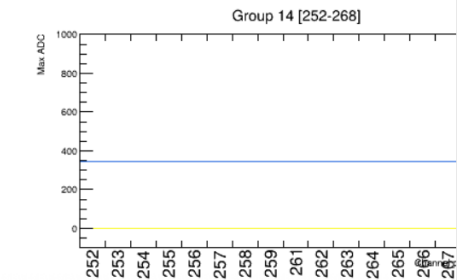
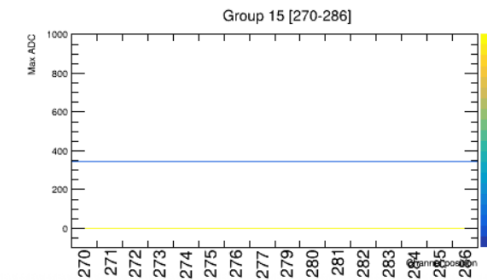
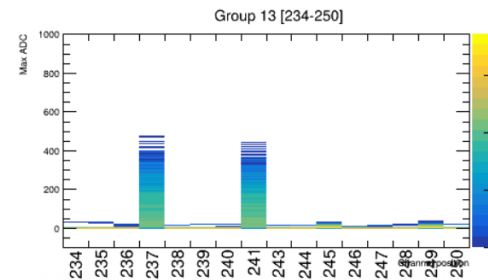
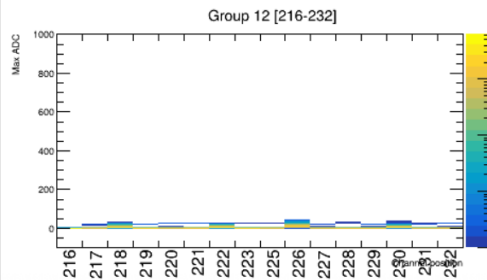
Aug. TB setup: old/new SiPM boards + summing board Check

- Used SFIL2 North (new SiPM board)
- Remove SiPM 1,3,4 & Connect only **SiPM2**



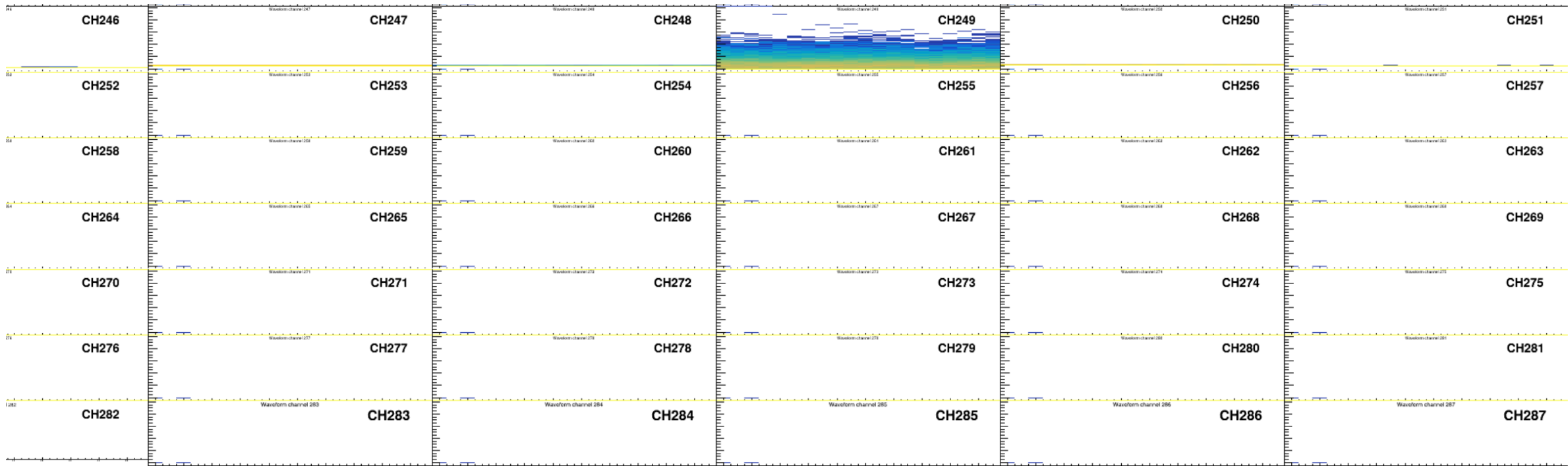
KCU0 ASIC3 Baby BCAL

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ing/KCUMonitoring\$ ba
for help

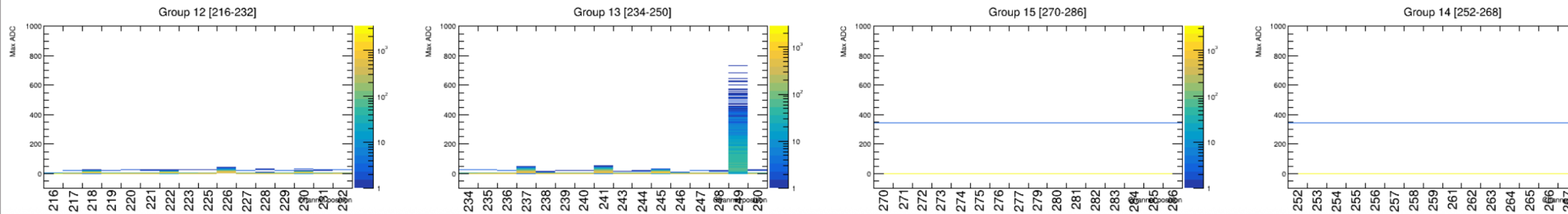


Aug. TB setup: old/new SiPM boards + summing board Check

- Used SFIL2 North (new SiPM board)
- Remove SiPM 1,2,3 & Connect only **SiPM4**

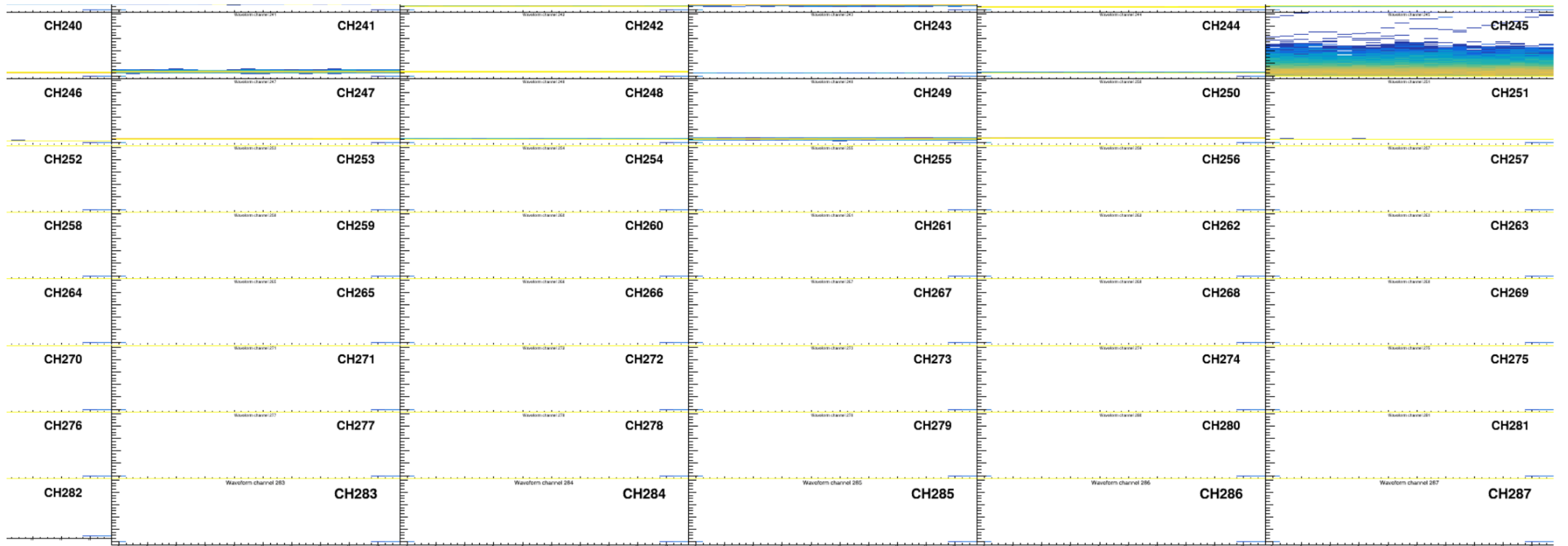


KCU0 ASIC3 Baby BCAL

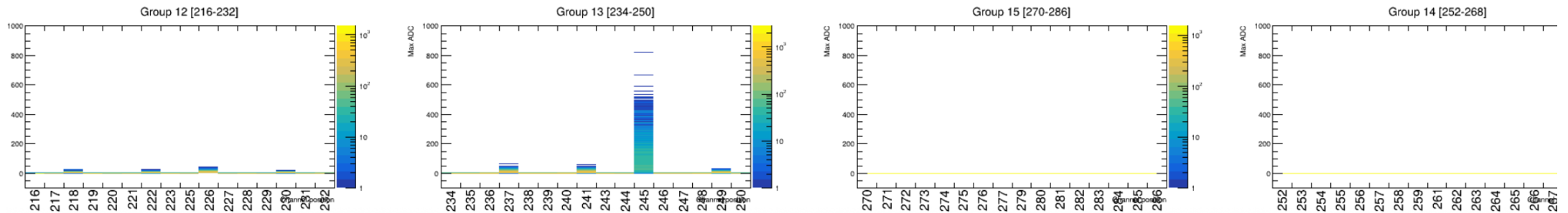


Aug. TB setup: old/new SiPM boards + summing board Check

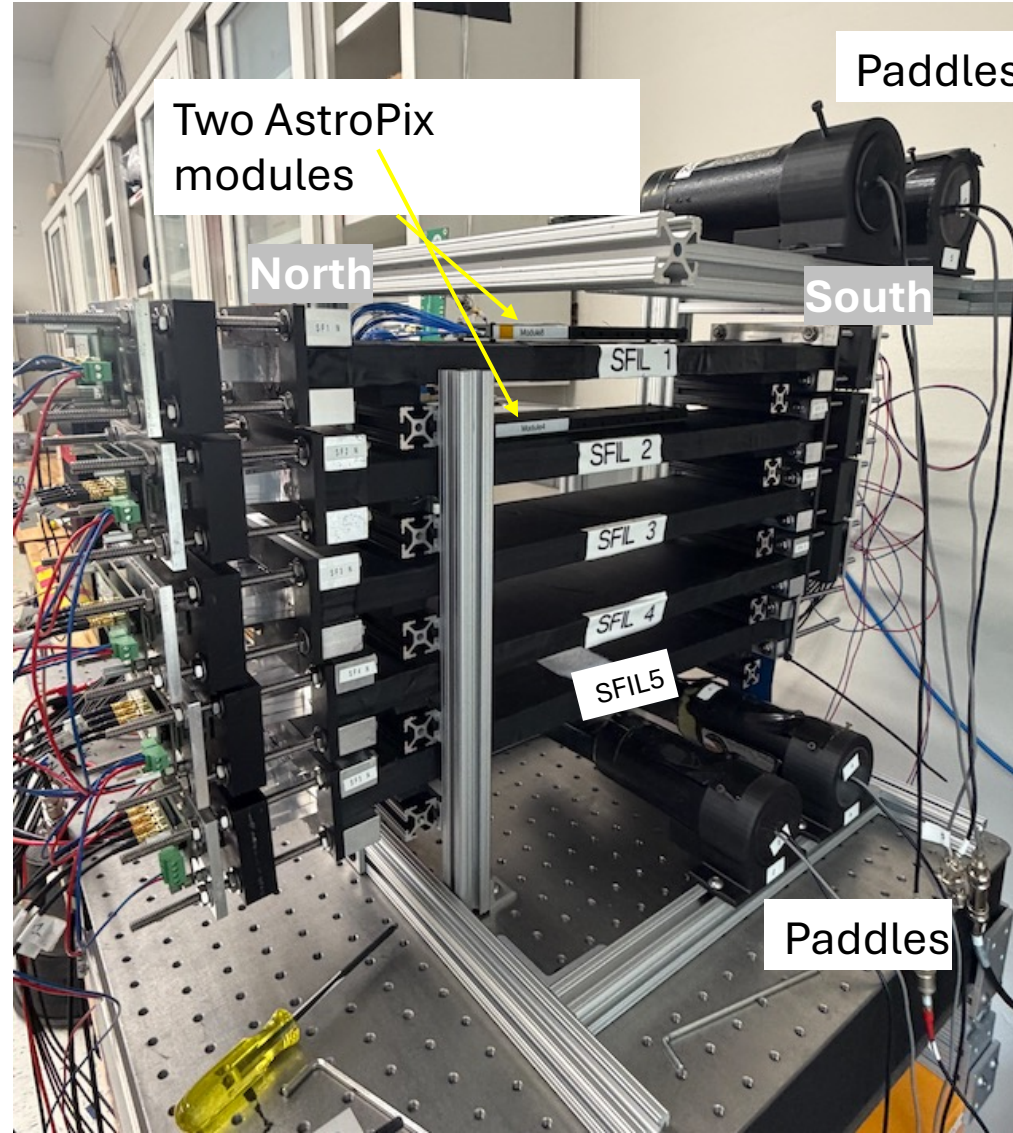
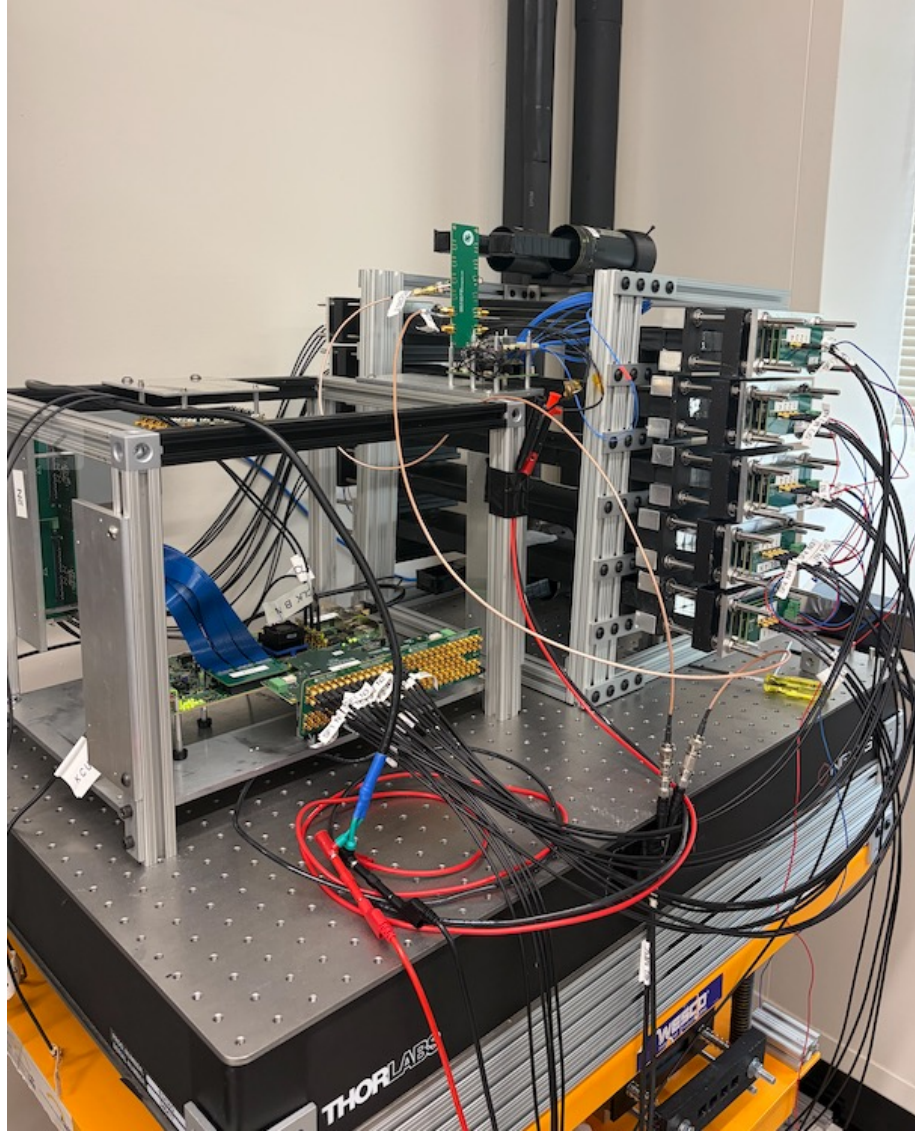
- Used SFIL2 North (new SiPM board)
- Remove SiPM 1,2,4 & Connect only **SiPM3**



KCU0 ASIC3 Baby BCAL



Aug. TB setup: same setting at ANL



Aug. TB: KCU0/1 Change Summary

KCU0 Change Summary

- **Aug. 5–9:** A2 was assigned to Baby BCAL North, and A3 was assigned to SFIL North.
- **Aug. 10:** The A2 and A3 functions were exchanged:
 - A2 → SFIL North
 - A3 → Baby BCAL North
- **Aug. 13:** The A2/A3 HGCROC board was replaced with the spare previously used in KCU1.
- **Aug. 14:** SFIL5 North was included in the mapping documented under KCU0 A2.

KCU1 Change Summary

- **Aug. 5:** A0 was assigned to SFIL5 South dummy, and A1 was assigned to SFIL5 North dummy. Only part of the SFIL5 South channels were operational.
- **Aug. 7–8:** The HGCROC board was replaced with a spare because approximately half of its channels were not working.
- **Aug. 8–9:** The board was moved from slots A1–A2 to A2–A3 without an intended functional change.
- **Aug. 10:** A2 was assigned to SFIL5 South, and A3 was assigned to SFIL5 North, with approximately half of the channels operational.
- **Aug. 13:** The original KCU0 board was installed in KCU1 A0/A1 for SFIL5 North but did not work properly.
- **Aug. 14:** Only SFIL5 South remained documented under KCU1 A2.

Aug. TB: KCU0/1 summary

Date	KCU0 Config	KCU1 Config	Note
After Aug 5	A0: Passive SFIL1,2,3,4 South A1: Paddles A2: Baby BCAL North A3: Active SFIL1,2,3,4 North	A0: SFIL5 South dummy indiv. A1: SFIL5 North dummy indiv.	Initial configuration. Only part of the SFIL5 South channels were operational.
After Aug 8	A0: Passive SFIL1,2,3,4 South A1: Paddles A2: Baby BCAL North A3: Active/Active-modified/Passive SFIL1,2,3,4 North	A0: SFIL5 South dummy indiv. A1: SFIL5 North dummy indiv.	The KCU1 HGCROC board was replaced with a spare because approximately half of its channels were not working.
After Aug 9	A0: Passive SFIL1,2,3,4 South + Passive SFIL3,4 North A1: Paddles A2: Baby BCAL North A3: Active/Active-modified SFIL 1,2 North	A2: Single-SiPM board, no LGs/cookies A3: Single-SiPM board, with LGs/cookies	The KCU1 HGCROC board was moved from slots A1–A2 to A2–A3. The documentation states that no functional change was made.
After Aug 10	A0: Passive SFIL1,2,3,4 South A1: Paddles A3: Baby BCAL North A2: SFIL1,2,3,4 North	A2: SFIL5 South indiv. A3: SFIL5 North indiv., half working	The setup was rebuilt. On KCU0, the Baby BCAL North and SFIL North assignments were exchanged between A2 and A3.
After Aug 13	A0: Passive SFIL1,2,3,4 South A1: Paddles A3: Baby BCAL North A2: SFIL1,2,3,4 North + SFIL5 North individual	A2: SFIL5 South indiv., unchanged A0: SFIL5 North, not working well	The KCU0 A2/A3 HGCROC board was replaced with the spare previously used in KCU1. The original KCU0 board was moved to KCU1 A0/A1 but did not operate properly.
After Aug 14, 9:55 PM CT	A0: Passive SFIL1,2,3,4 South + SFIL5 South individual A1: Paddles A3: Baby BCAL North A2: SFIL1,2,3,4,5 North	A2: SFIL5 South individual?	The SFIL5 North mapping was documented under KCU0 A2. Only SFIL5 South remained documented under KCU1.

Aug. TB: 8/13 and 8/14 (add SFIL5)

SFIL position	ASIC0: Passive SFIL1,2,3,4 South	ASIC0 channel	ASIC2: SFIL North	ASIC2 channel	SFIL position	SFIL North Edge board	ASIC2 channel
SFIL 1-1	J1	2	J1	146	SFIL 1 1N	J1	146
SFIL 1-2	J2	6	J2	150	SFIL 1 2N	J2	150
SFIL 1-3	J3	10	J3	154	SFIL 1 3N	J3	154
SFIL 1-4	J4	14	J4	158	SFIL 1 4	J4	158
SFIL 2-1	J5	21	J5	165	SFIL 2 1	J5	165
SFIL 2-2	J6	25	J6	169	SFIL 2 2	J6	169
SFIL 2-3	J7	29	J7	173	SFIL 2 3	J7	173
SFIL 2-4	J8	33	J8	177	SFIL 2 4	J8	177
SFIL 3-1	J9	63	J9	207	SFIL 3 1	J9	207
SFIL 3-2	J10	59	J10	203	SFIL 3 2	J10	203
SFIL 3-3	J11	52	J11	196	SFIL 3 3	J11	196
SFIL 3-4	J12	48	J12	192	SFIL 3 4	J12	192
SFIL 4-1	J63	43	J63	187	SFIL 4 1	J63	187
SFIL 4-2	J64	37	J13	186	SFIL 4 2	J13	186
SFIL 4-3	J15	0	J15	144	SFIL 4 3	J15	144
SFIL 4-4	J16	4	J16	148	SFIL 4 4	J16	148
					SFIL 5 1	J17	153
					SFIL 5 2	J18	156
					SFIL 5 3	J19	163
					SFIL 5 4	J20	167

Aug. TB: Edge board channel info.

Sorted by Edge Board Ch...																				
Edge Board	#	ASIC 0	#	ASIC 1	ASIC 2	ASIC 3	Edge Board	#	ASIC 0	#	ASIC 1	ASIC 2	ASIC 3	Edge Board	#	ASIC 0	#	ASIC 1	ASIC 2	ASIC 3
J01		2		74	146	218	J23		65		137	209	281	J45		60		132	204	276
J02		6		78	150	222	J24		61		133	205	277	J46		54		126	198	270
J03		10		82	154	226	J25		50		122	194	266	J47		49		121	193	265
J04		14		86	158	230	J26		46		118	190	262	J48		45		117	189	261
J05		21		93	165	237	J27		40		112	184	256	J49		41		113	185	257
J06		25		97	169	241	J28		36		108	180	252	J50		39		111	183	255
J07		29		101	173	245	J29		16		88	160	232	J51		3		75	147	219
J08		33		105	177	249	J30		18		90	162	234	J52		7		79	151	223
J09		63		135	207	279	J31		32		104	176	248	J53		13		85	157	229
J10		59		131	203	275	J32		34		106	178	250	J54		20		92	164	236
J11		52		124	196	268	J33		67		139	211	283	J55		24		96	168	240
J12		48		120	192	264	J34		69		141	213	285	J56		30		102	174	246
J13		42		114	186	258	J35		55		127	199	271	J57		68		140	212	284
J14		38		110	182	254	J36		57		129	201	273	J58		64		136	208	280
J15		0		72	144	216	J37		1		73	145	217	J59		58		130	202	274
J16		4		76	148	220	J38		5		77	149	221	J60		56		128	200	272
J17		9		81	153	225	J39		11		83	155	227	J61		51		123	195	267
J18		12		84	156	228	J40		15		87	159	231	J62		47		119	191	263
J19		19		91	163	235	J41		22		94	166	238	J63		43		115	187	259
J20		23		95	167	239	J42		28		100	172	244	J64		37		109	181	253
J21		27		99	171	243	J43		70		142	214	286							
J22		31		103	175	247	J44		66		138	210	282							

Activities

ROOT

17:19:07

Running for 0:03:16

Run: 3316

Events: 3593 (18.9 Hz)

Logging Enabled

Close

End

beam

calib

cosmics

junk

KCU0

CH186

CH187

CH192

CH193

CH198

CH199

FPGA 0

ASIC 0

ASIC 1

ASIC 2

ASIC 3

-- Top Register --

Top

-- Global Analog Registers --

Global_Analog_1

Global_Analog_0

-- Reference Voltage Registers

Reference_Voltage_1

Reference_Voltage_0

-- Master TDC Registers --

Master_TDC_1

Master_TDC_0

-- Digital Half Registers --

Digital_Half_1

Digital_Half_0

-- Channel Wise Registers --

CM_2

CM_3

Channel_36

Channel_37

Channel_38

Channel_39

Channel_40

Channel_41

CH186

CH187

CH192

CH193

CH198

CH199

Waveform 10

CH186

Waveform channel 198

CH198

File

Edit

View

Options

Tools

Help

Max ADC vs Channel

KCU0 ASIC0 Passive South

Group 0 [0-16]

Group 1 [18-34]

Group 3 [54-70]

Group 2 [36-52]

KCU0 ASIC2 Passive North

Group 8 [144-160]

Group 9 [162-178]

Group 11 [198-214]

Group 10 [180-196]

KCU0 ASIC1 Paddles

Group 4 [72-88]

Group 5 [90-106]

Group 7 [126-142]

Group 6 [108-124]

KCU0 ASIC3 Baby BCAL

Group 12 [216-232]

Group 13 [234-250]

Group 15 [270-286]

Group 14 [252-268]

AstroPix Imaging Layer R&D Milestones

- AstroPix Multilayer/Multichip demonstration
- First beam-test operation of the 9-chip AstroPix prototype module ([AstroLinx mock-up](#))
- Integration between H2GCROC (Calorimeter readout) and A-STEP board (AstroPix readout) using external common clock

AstroPix v3



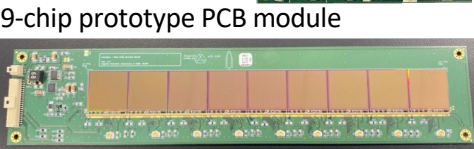
Single chip



Quad-chip



Three-layer of quad-chips



9-chip prototype PCB module

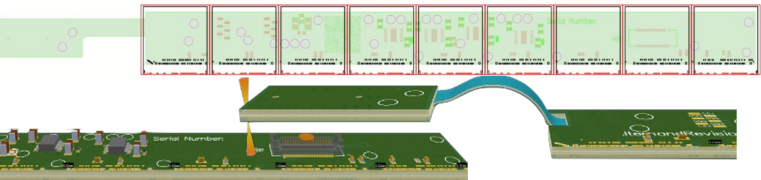
9-chip module with AstroLinx

AstroPix v4



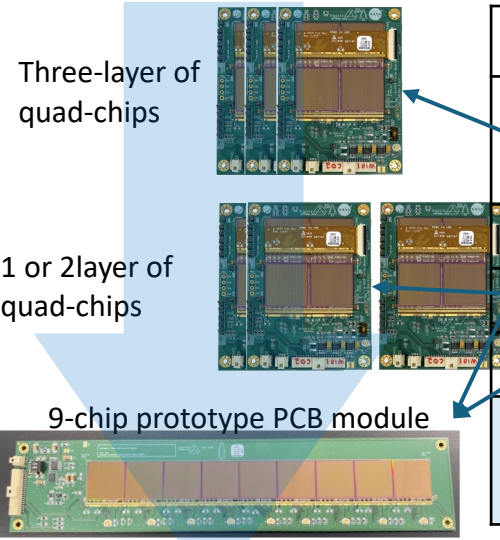
AstroPix v5: Chip delivery is expected in [end of Oct.](#) after the fabrication process.
+ ETC (Final AstroPix readout system, designed and developed by NASA)

Configuration of AstroPix v4	AstroPix readout	#.Chip	Status
Single chip	GECCO board	1	✅ bench/beam tests (KEK, Dec.2025)
Configuration of AstroPix v3	AstroPix readout	#.Chip	Status
Single chip	GECCO board	1	✅ bench/beam tests (FNAL, Jun.2024) (arXiv:2602.06084)
Three-layer of single-chips	Three GECCO boards + customized DAQ	1x3	✅ beam tests (CERN & KEK, 2025 summer) by Korean collaborators (arXiv:2605.07681)
Quad-chip	A-STEP FPGA board	2x2	✅ bench/beam tests (KEK, Dec.2025)
Three-layer of quad-chips	A-STEP FPGA board	3x(2x2)	✅ bench/beam tests (KEK, Dec.2025)
9-chip prototype PCB module	A-STEP FPGA board	1x9	✅ bench test/beam tests (KEK, May.2026 & Jlab Aug.2026 & CERN Set.2026)



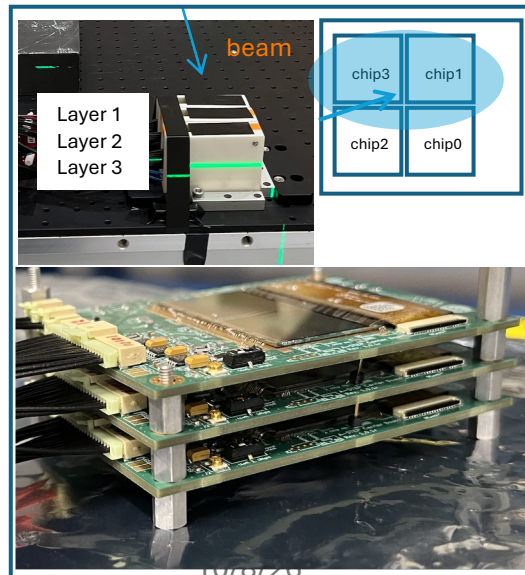
AstroLinx (module board) v3 testing will begin after fabrication is complete.

AstroPix Setup for TB

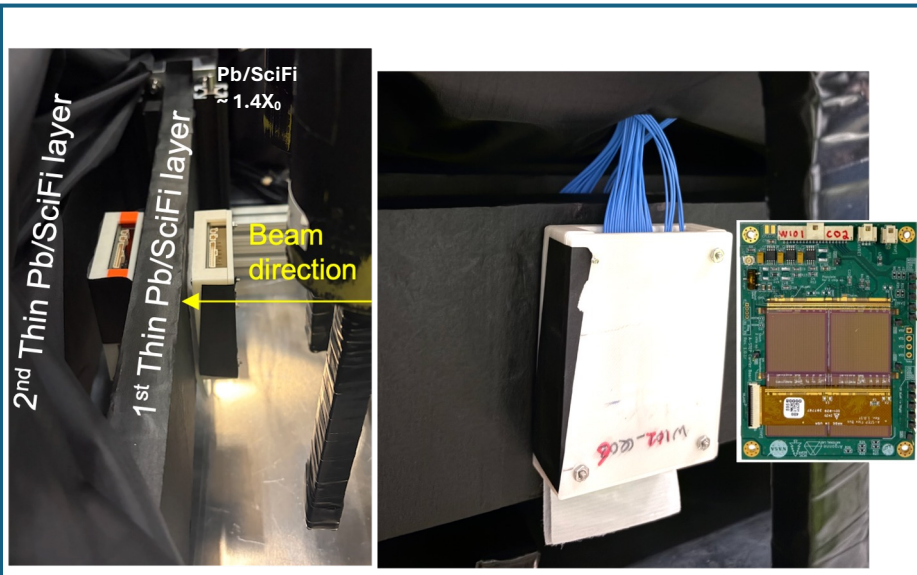


Date and Site	AstroPix Setup
Dec. 2025, KEK	AstroPix v4 single chip + GECCO
	Three quad chips + ASTEP
May. 2026, KEK	9-chip module + ASTEP
May. 2026, Hall D	Two quad chips + ASTEP
Aug. 2026, Hall D	9-chip module + ASTEP
End of Oct, 2026	Available v5 chip
	v3 AstroLinx

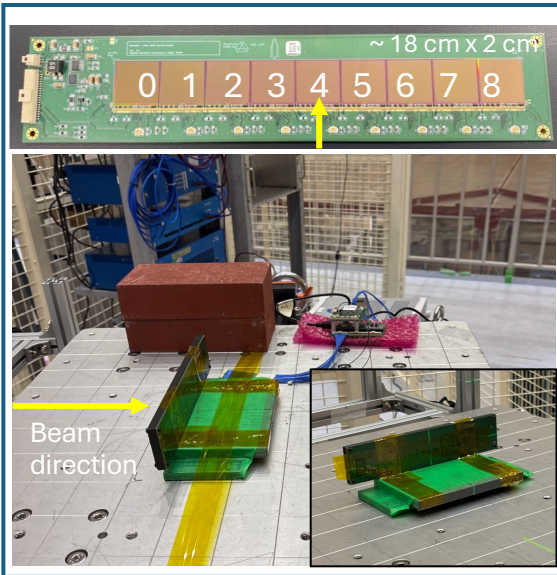
Dec. 2025, KEK



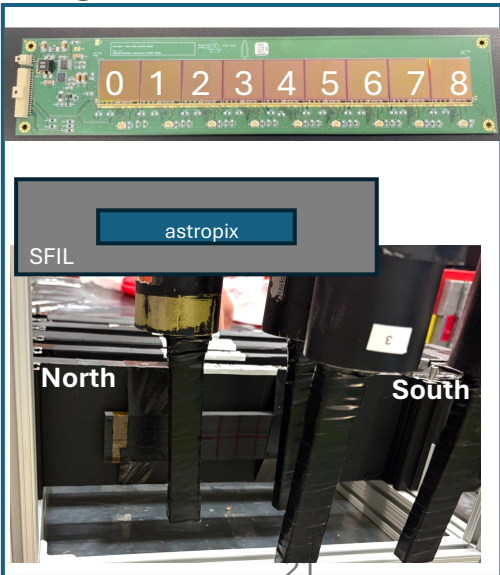
May. 2026, Hall D



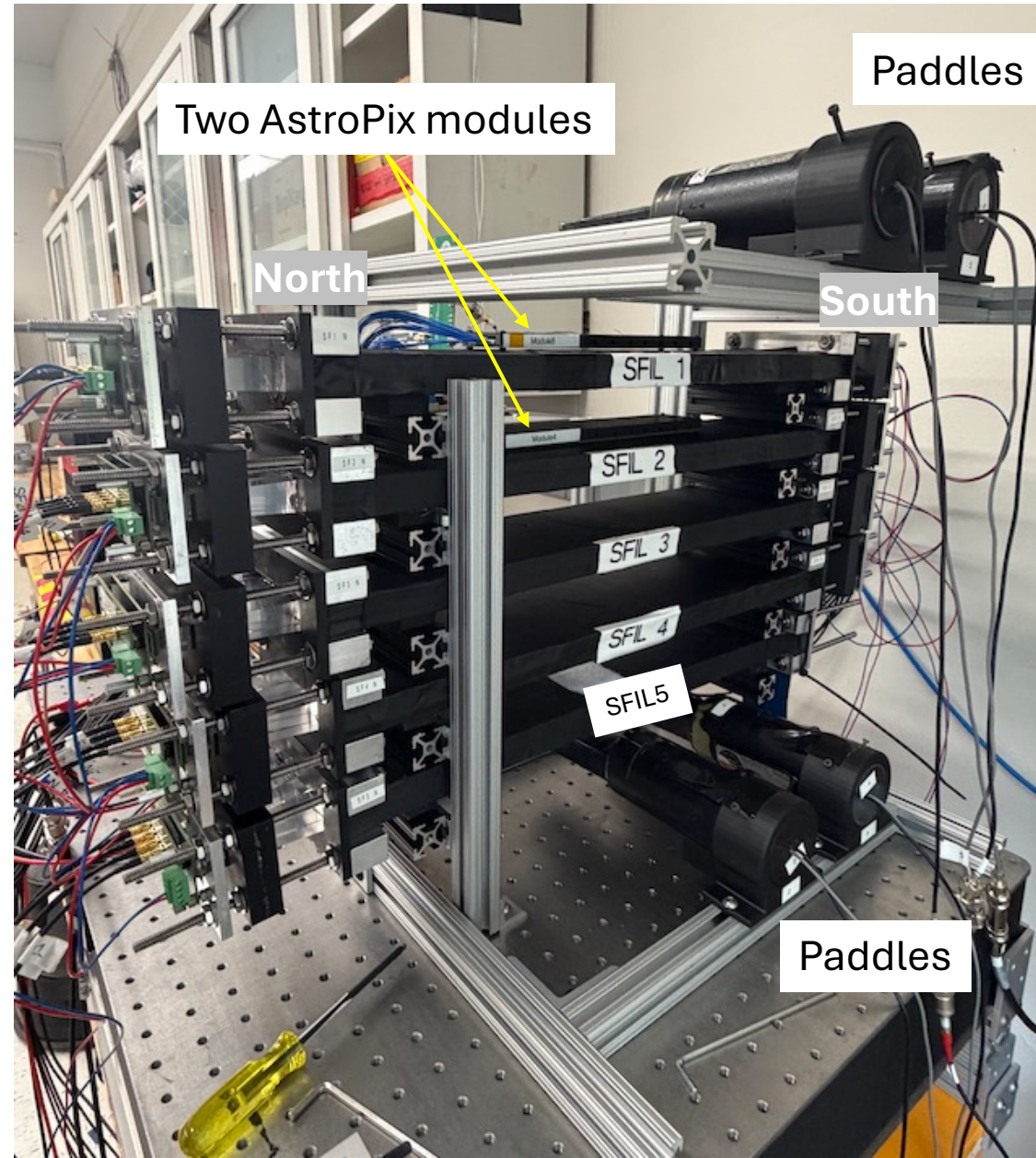
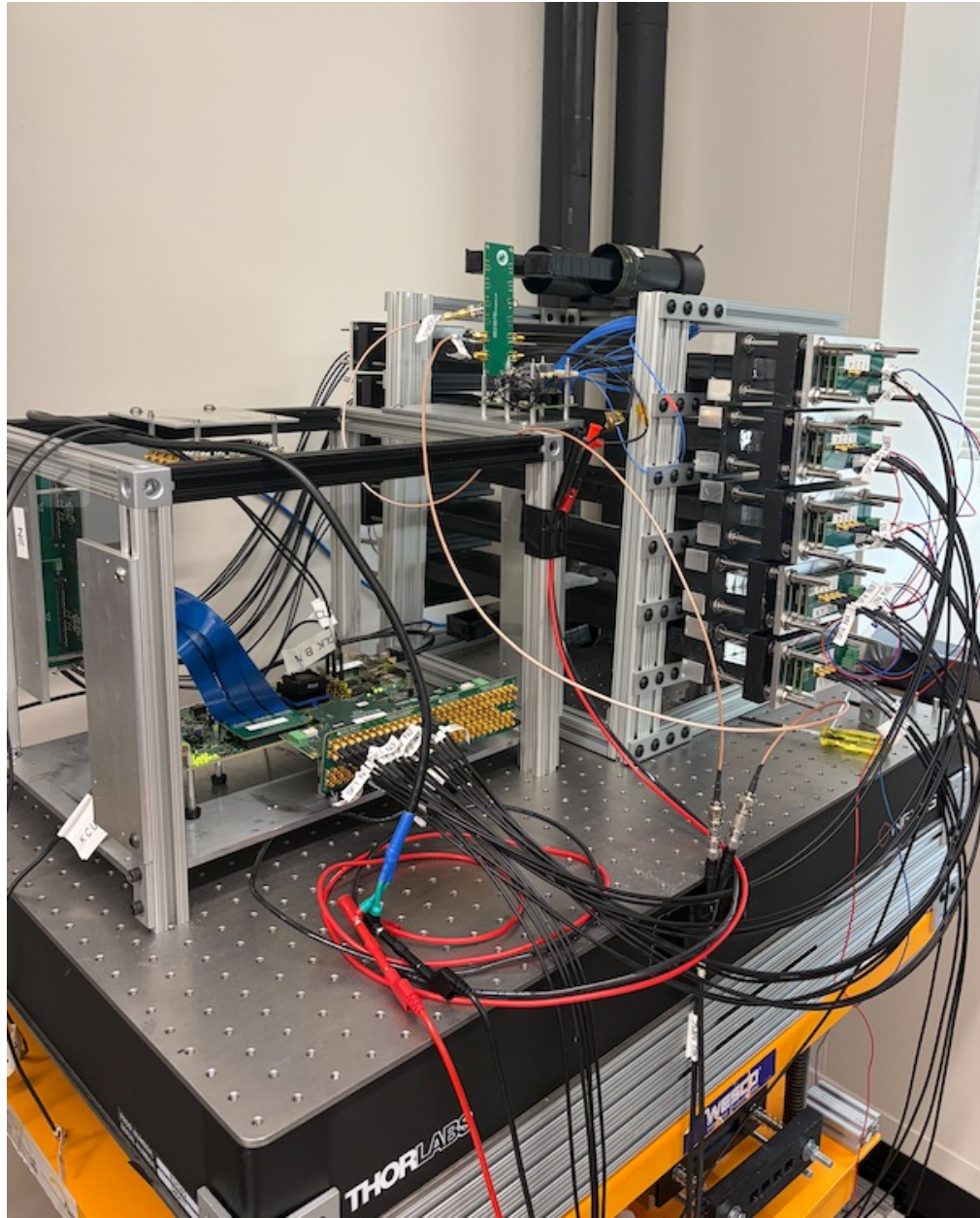
May. 2026, KEK



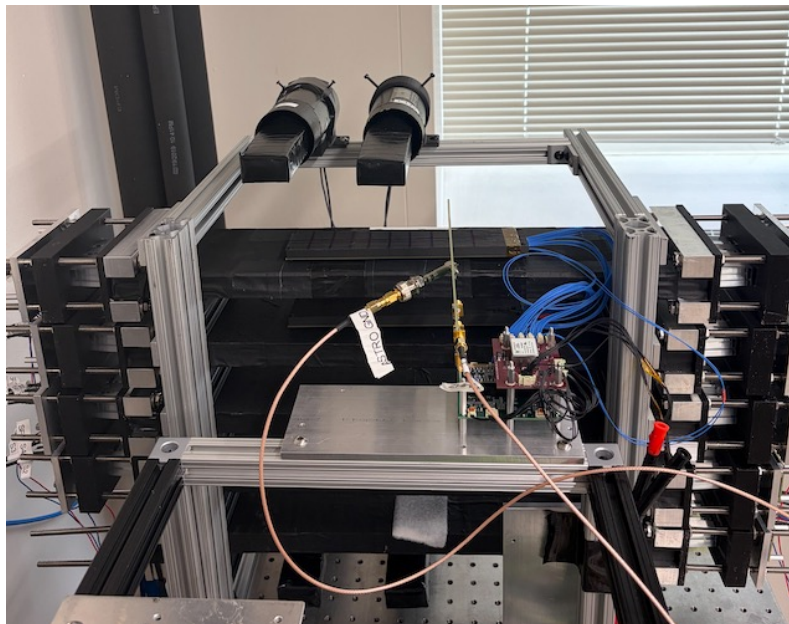
Aug. 2026, Hall D



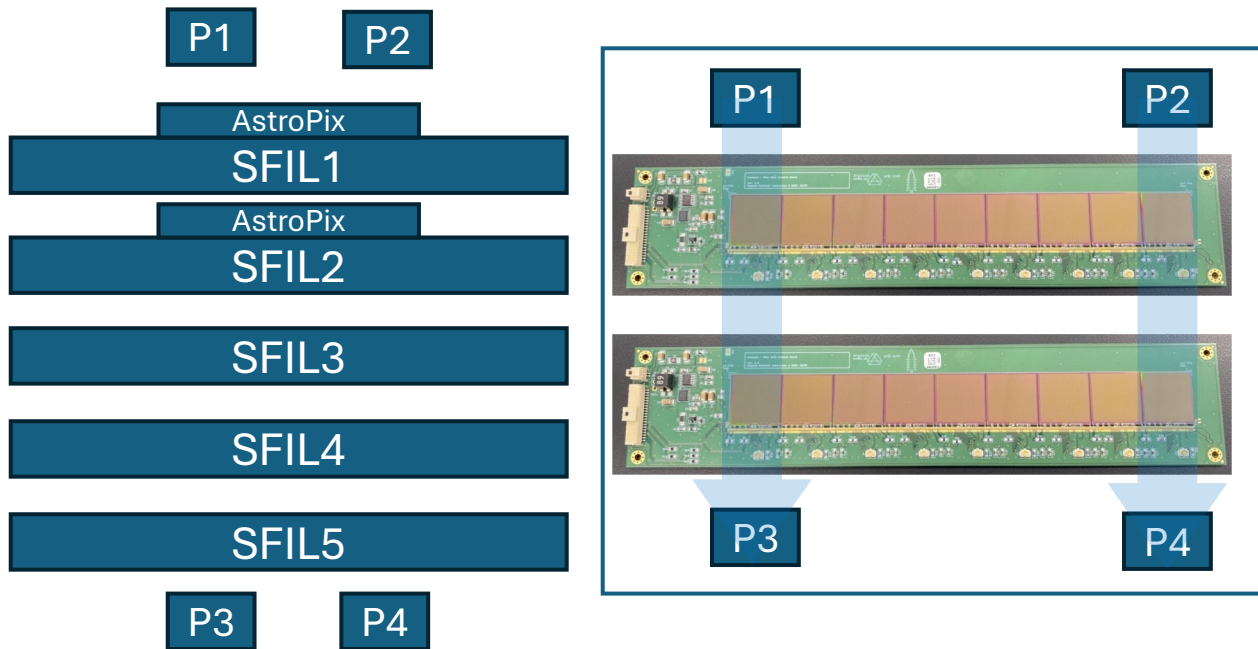
Cosmic Setup at ANL



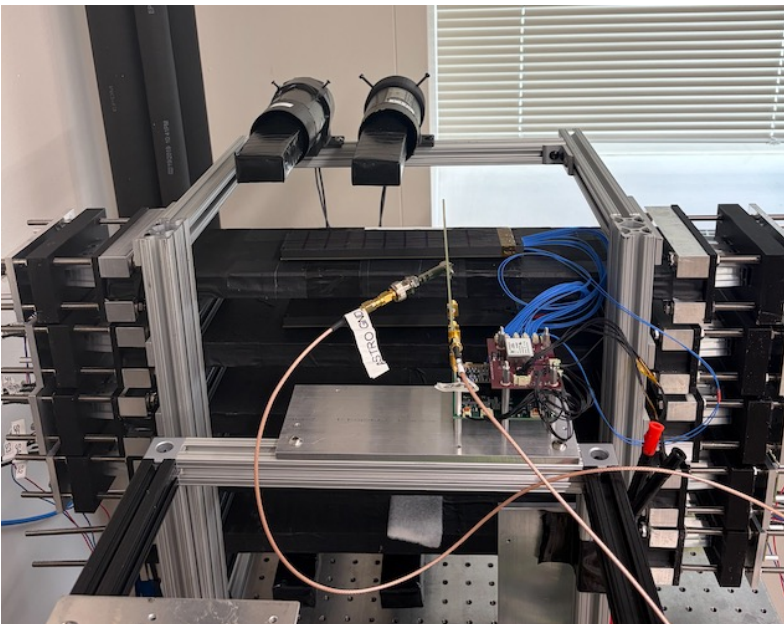
Cosmic Test Goals at ANL



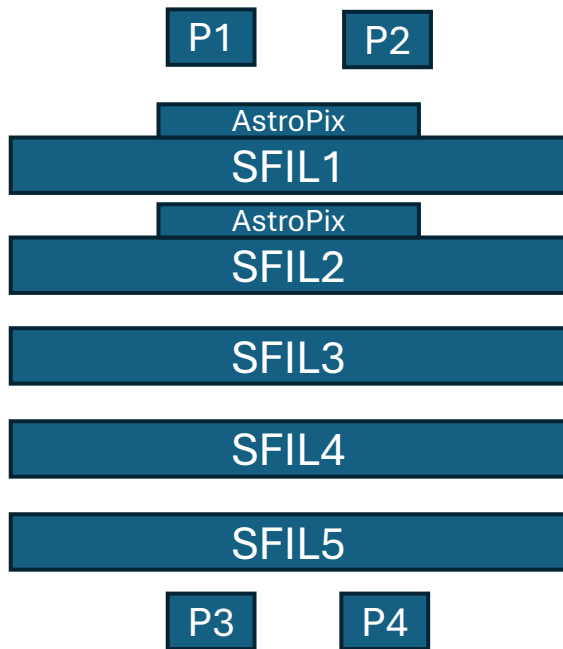
- Same setup as Hall D TB (except 2nd astropix and paddles)
- Mapping information (SiPM-H2GCROC)
 - Summing boards/individuals
- Cosmic data taking for SFIL's calibration
- Characterize the **chip-dependent readout latency** in the 9-chip daisy chain using cosmic-ray data.
 - Use the H2GCROC FPGA timestamp as the timing reference and correct the beam-test data accordingly.
- Synchronize AstroPix with SFIL using cosmic-ray data



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Setup at B102	
✓	SFIL position
✓	all cable connection (N/C SFIL5 south)
	AstroPix position (not fixed yet)
	4 Paddles: prefer placing paddles at the position of AstroPix chip0 and chip 9; need to scan at other chip positions?
	how to cover SFIL with a black sheet; each SFIL's LG or ?
1	KCU operation
	Upload bit file then check normal operation
	10Gbps; pedestal, TOA, TOT calibration code; same config. File used in the beam test in hall d
	Korean team used 1Gbps. Need to check different calibration codes between 1 and 10 Gbps
2	For mapping information of SFIL (~next Tue.TB analysis meeting)
	Use an LED driver to couple an LED directly to the SiPM or light guide / light leakage ;
	SiPM old/new boards; individual, summing boards
	old/new board patterns;
	if possible, summing boards and then individuals
3	KCU+AstroPix operation
	Challenge
	v3 provides half hit information for each col/row, with different FPGAtimestamp.
	Need to set a strategy for synch. , no need for v4

Synchronization (meeting w.SH 9/21/2026)

	v3 chip (single/quad/9chip)
	col/row matching efficiency
	Data loss due to high particle intensity; Broken data packet
	9 chip prototype; position-dependence data loss
	chip-to-chip response variation vs data transmission
	1.Peripheral, chip-level
	2.daisy-chain, module-level
	To obtain realistic shower imaging
	sustain high beam rate at chip-level
	reduce signal processing time; ToT~us-level so far, fine clock
	Synchronization
	notice-h2gcroc sync.
	notice-AstroPix, RCDAQ 사용
	notice TCB (provide global timestamp); FPGA TS 125 MHz
	> convert real-time, Find 1st event then check reletive different FPGA TS
	At experiment, providing global timestamp from bunch crossing, continuous streaming readout

May Run log (1)

From run 1325	First run with KCU1 SFIL2 swapped from ASIC2 to ASIC3. Also, CAEN M0 is back
From run 1333	Paddles 3,4,5 REMOVED from trigger, only triggering on paddle 6 now.
From run 1340	KCU Mapping changed. North SFIL2 is now in KCU1 Asic3
From run 1419	First attempt at CAEN speedup, new RCDAQ version from Martin
From run 1720	Finished working on light leak and periodic noise. Light leak solved, periodic noise on SFIL1 and 3 of KCU1 solved. KCU0 has huge periodic noise in SFIL3 :(
From run 1741	Finished working on light leak and periodic noise. Light leak solved, periodic noise on SFIL1 and 3 of KCU1 solved. KCU0 has huge periodic noise in SFIL3 :(
From run 1939	Start of runs with internal clock on HGCROC only
From run 1940	New dynamic range for all HGCROC ASICs, should be 2x more response for the same charge
From run 2028	I restarted the runs, now it is half of the response from the default ones for the begining. It is much larger dynamic range, MIP is maybe within the noise levels. DYNAMIC RANGE CHANGE
From run 2148	SiPM parameters not logged due to carbon reboot. First run running with external clock
From run 2184	AstroPix stalled. stop the run. let me check standalone; included only first AstroPix quadchip

May Run log (2)

[illegible]

Aug. Run log (1)

From run 2735	Newest autologged run in BIC test beam v2. No HGCROC due to missing trigger cable. Astropix is 9 chip PCB, CAEN is only trigger paddles.
From run 2781	RUN WITH COUNTERBIAS
From run 2782 ~ 2803	Cherenkov run (dummy)
Run 2804	Stop the run for H2GCROC calibration (ASIC0 KCU0 for passive)
From run 2805 ~ 2822	Cherenkov run (dummy)
From run 2915	START of beam with 5 active SFILs and all Passive Summing boards (but SFIL 5)
From run 2916 ~ 2924	SFIL5 (KCU1) for Cherenkov comparison on the same setting as during the dummy run
From run 2925	gain on SFIL5 (KCU1 ASIC 2 and 3) changed (decreased) starting in this run - Important for comparison with Cherenkov
From run 2953 ~ 2954	Used for trying to recover the KCU0 ASIC2
From run 2956 ~ 3011	FULL South Side of setup present SFIL 5 North 50% SFILs 1-4 North only 5 channels total

Aug. Run log (2)

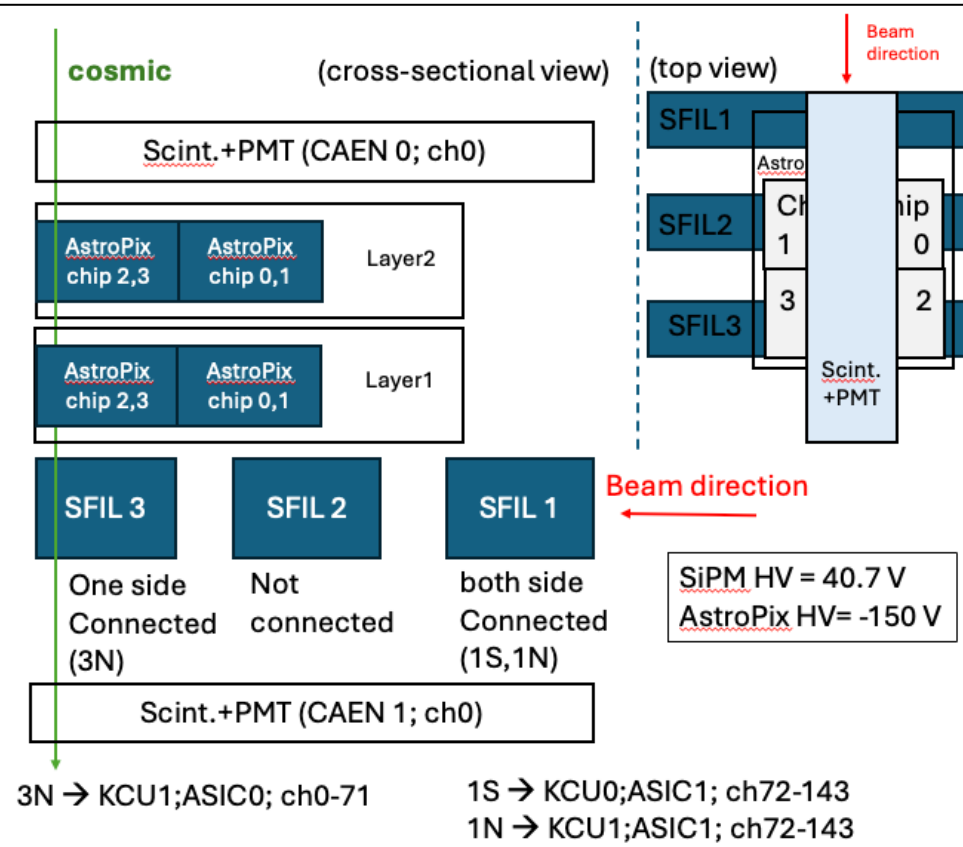
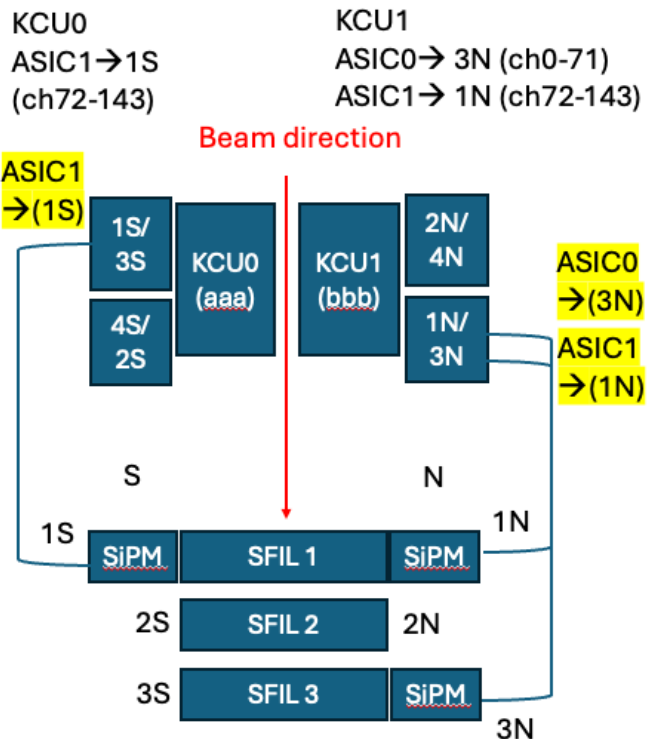
[illegible]

May setup

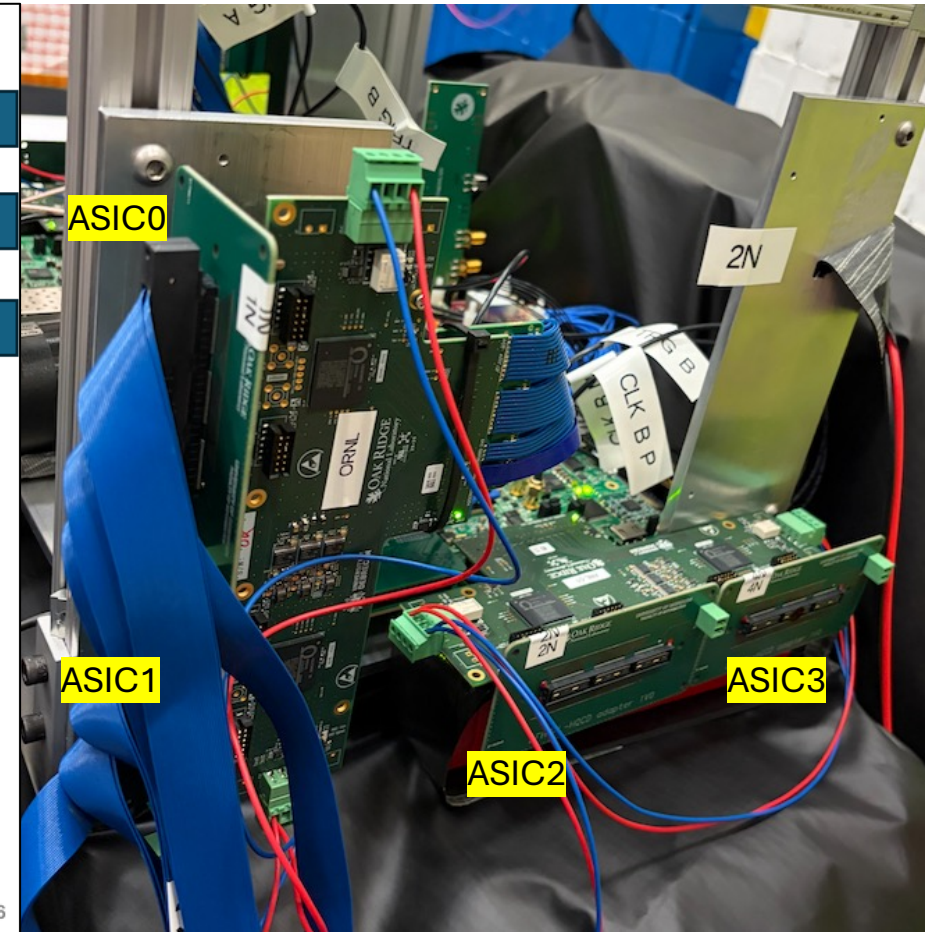
H2GCROC mapping (16 channel; individual readout)

- KCU; ASIC0 = ch0~71
- KCU; ASIC1 = ch72~143

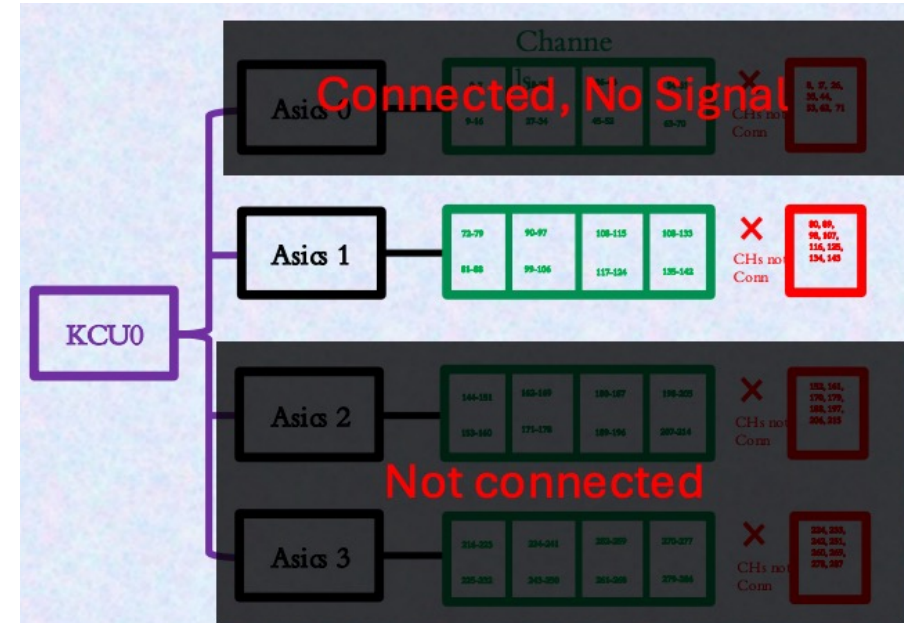
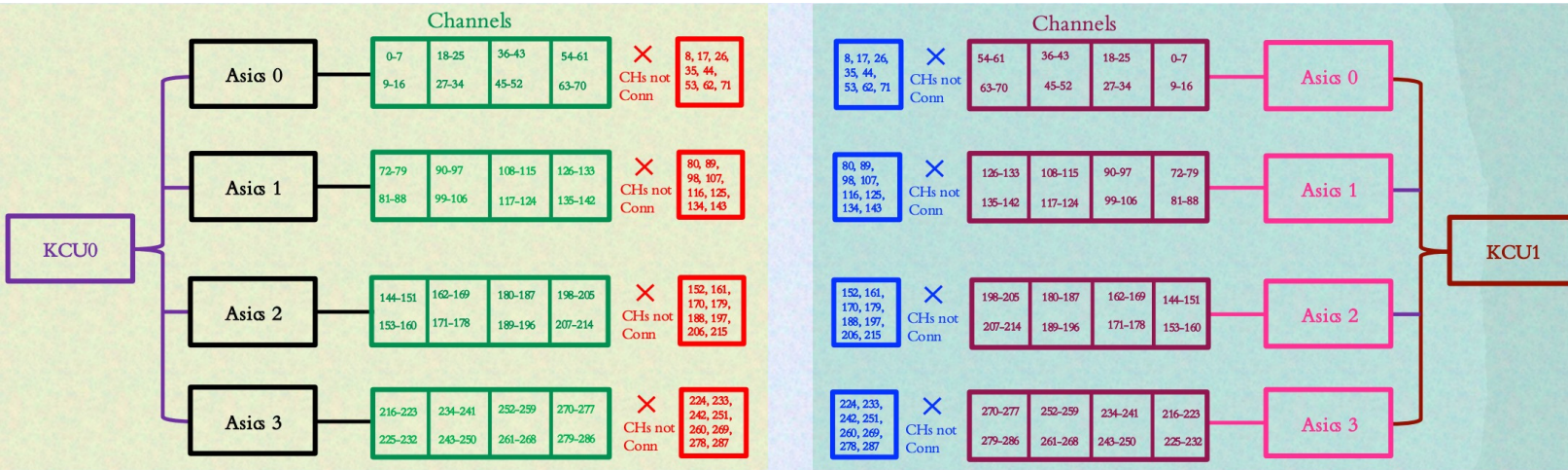
Current Setup (1)



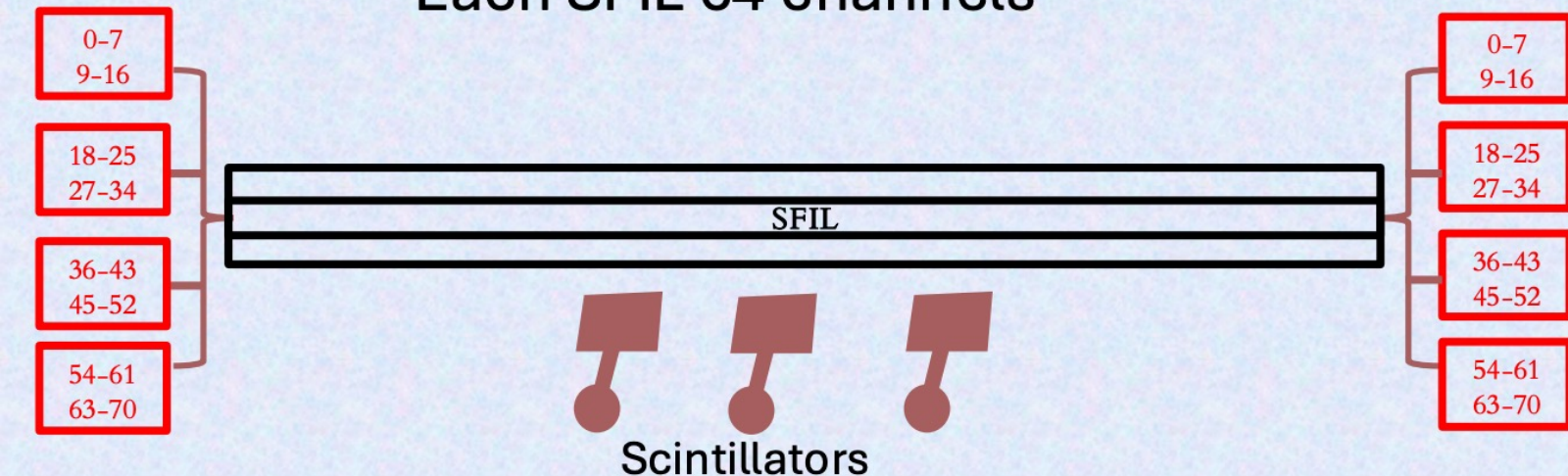
* Readout of individual channels in a 16-channel SiPM array



From Olaiya's slide (http://localhost:13666/ePIC_BIC/542)



4 lightguides in each SFILS
Each lightguide 16 channels
Each SFIL 64 channels



All samples analyzed up until now have 0-71 pedestal (connected but no signal) channels, 72 -143 (connected with signal) channels, and others were not connected.

May setup

H2GCROC mapping (16 channel; individual readout)

- KCU; ASIC0 = ch0~71
- KCU; ASIC1 = ch72~143

