FCFD status

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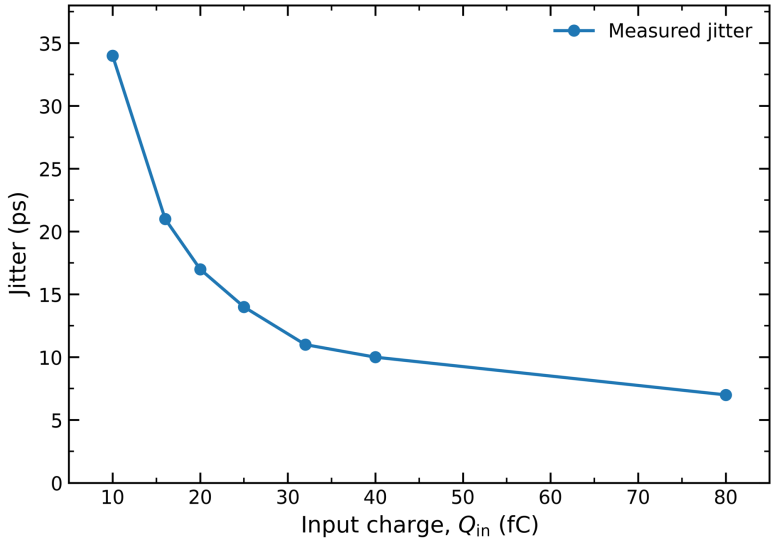
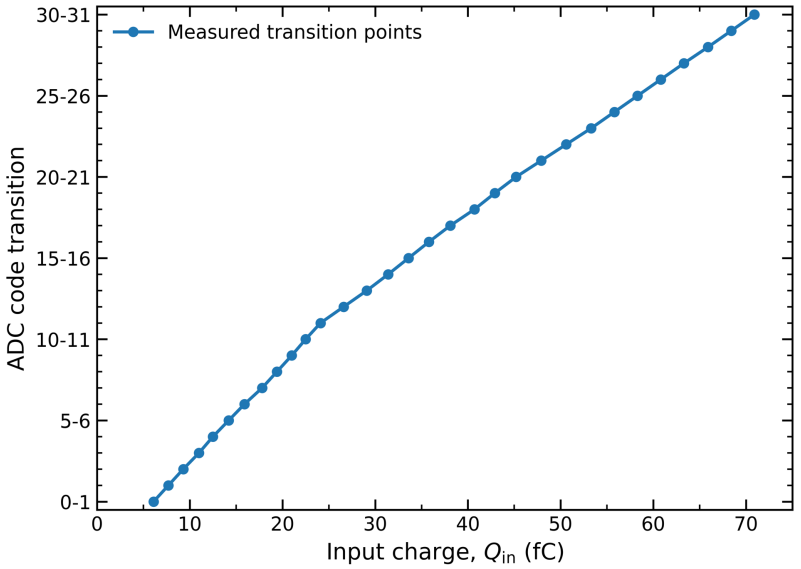
FCFD1.2 analog testing status

- Several efforts on testing the analog and digital sections ongoing
- Analog frontend test results
  - Measured jitter with charge injection is consistent with expectation and with the FCFD1.2 results
  - ADC is a piecewise polynomial, with variable bin size in the dynamic range covered of the chip
  - Noise of the amplitude measurement is 0.93 fC, consistent with expectation
  - Currently performing more detailed measurements to study the stability and uniformity across different channels and various chips





FCFD1.2 digital testing status

- I2C communications and configurations tested and validated
  - All registers can be read and written with 100% accuracy
- The clock divider:
  - Generates the main 40 MHz timing signals clk40 and tick40_ce from the 320 MHz reference clock (clk320).
  - It also generates a dedicated 40 MHz clock (clk40_i2c) for the I2C block.
  - In addition, the module produces the bunch-crossing counter bx_cnt, which is used by the readout logic

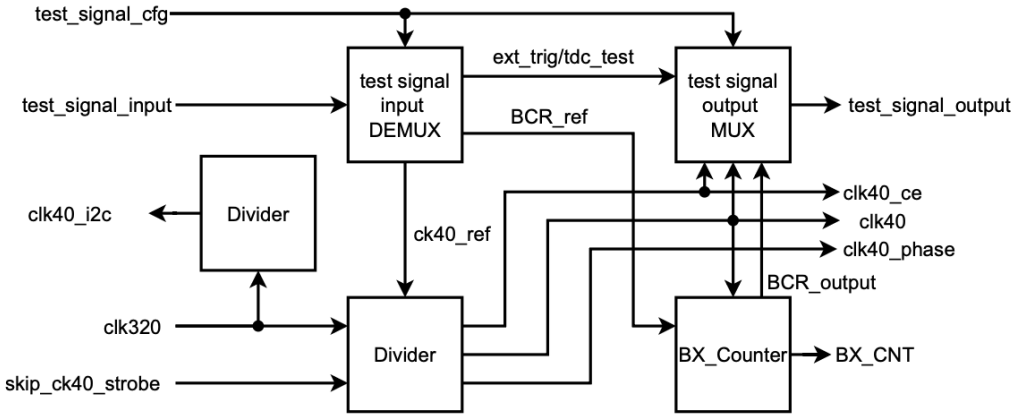
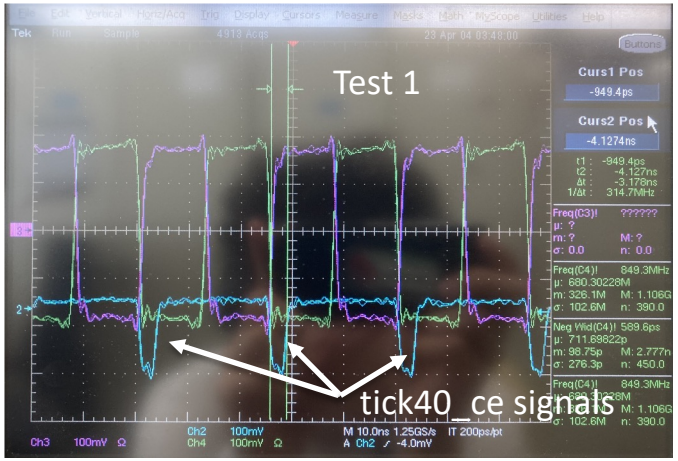


Figure 1: Clock divider block diagram

Clock divider tests

Clock-divider logic works in every configuration

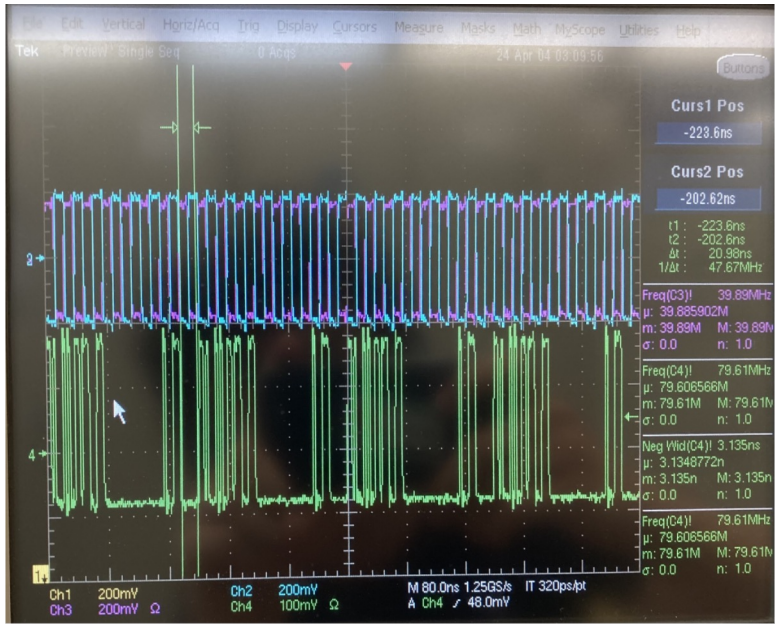
- **Test 1**: Verify the 40 MHz clock-enable strobe
  - One clk320 cycle (3.125 ns) wide, corresponding to a 12.5% duty cycle
- **Test 2**: Verify clk40 and phase adjustment against reference



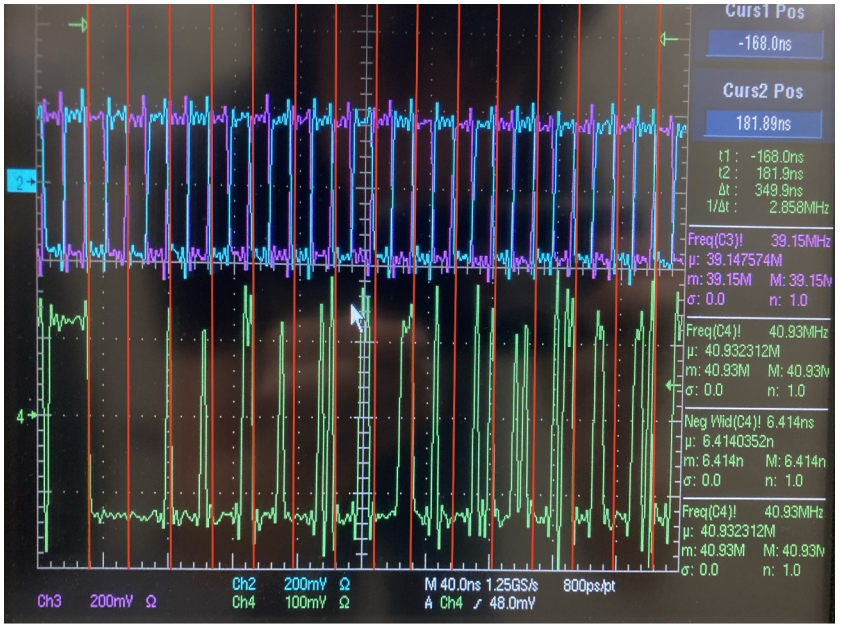
  - Correct 40 MHz output; phase-adjustment logic operates with the intended 3.125 ns resolution, eight phase steps span one complete 40 MHz clock period.
- **Test 3**: Verify the BCR output and 512-cycle repetition.
  - External BCR pulses were correctly detected and routed to bcr_output, demonstrating proper bunch-crossing counter reset/alignment.
- **Test 4**: Used for external triggering
  - Replicates exactly the test input signal on the test output signal

Serial link validation

- Verify the selectable data sources feeding the FCFD serial transmitter
  - Fast readout can be configured to transmit test patterns in place of normal data.
  - Patterns are an 8-bit counter, a fixed pattern 0x5C, and a PRBS7 sequence
    - **Validated the pattern generator, framing, and serializer.**



Test 1



Test 2

Fermilab

Summary

- Active period of testing on several fronts!
- Analog frontend performance consistent with expectations
- I2C communication and configurations validated
- Clock divider logic validated
- Serial link performance validated
- Next moving on to the TDC performance measurements
  - First version of the firmware being currently commissioned
  - Second version of the testing board designed and submitted to add some of the features for testing