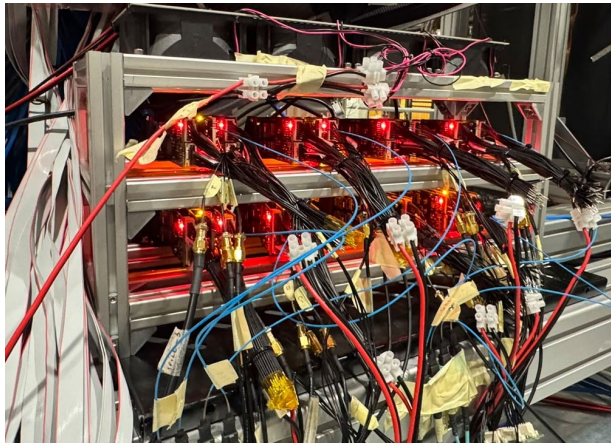
eRD109 update: dRICH RDO

Davide Falchieri (INFN Bologna) for the RDO team:
Pietro Antonioli, Sandro Geminiani, Matilda Panza,
Luigi Rignanese, Giovanni Torromeo

ePIC DAQ meeting
03 September 2026

Hardware inventory

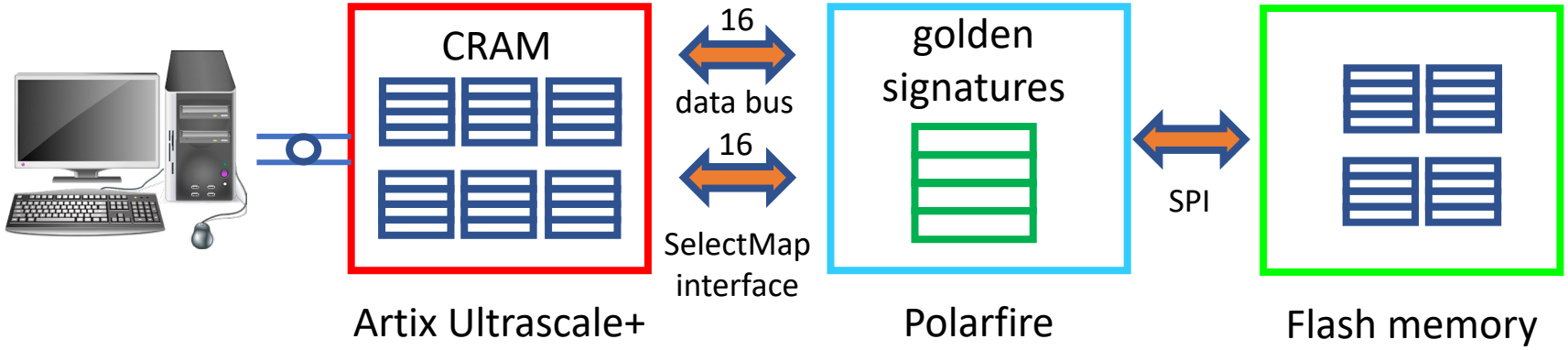
- We currently have **8 RDOs v1.0** boards:
  - they have been used at a test beam at CERN in June 2026
  - 6 are in use with the SiPM prototype
  - 1 is used for optical link characterization
  - 1 is used to test the scrubbing

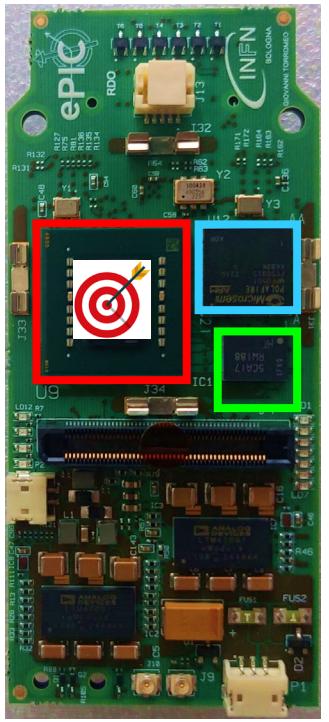


- Plans:
  - we are beginning to design RDO v1.1:
    - bug fixes
    - small changes
    - replacement of microcontroller (ATtiny416 → SAMD21)
  - we are going to produce a new batch of **5 RDOs v1.1** from the same company as v1.0 (Artel)
  - probably we will also order another batch of **3 RDOs v1.1** from another company (SCEN) to check the capabilities of the manufacturer

Next deadline: irradiation test (October 2026)

- We will have a second irradiation test with protons in Trento (Centro di ProtonTerapia) after the one of 28 March 2026:
    - this time the goal is to irradiate the Artix Ultrascale+ FPGA while the Polarfire FPGA performs a **blind scrubbing**





blind scrubbing:

- the Polarfire reads a frame from the FLASH and writes it on the Artix US+ CRAM, one frame after the other in an infinite loop

Sandro Geminiani

SAMD21 software design

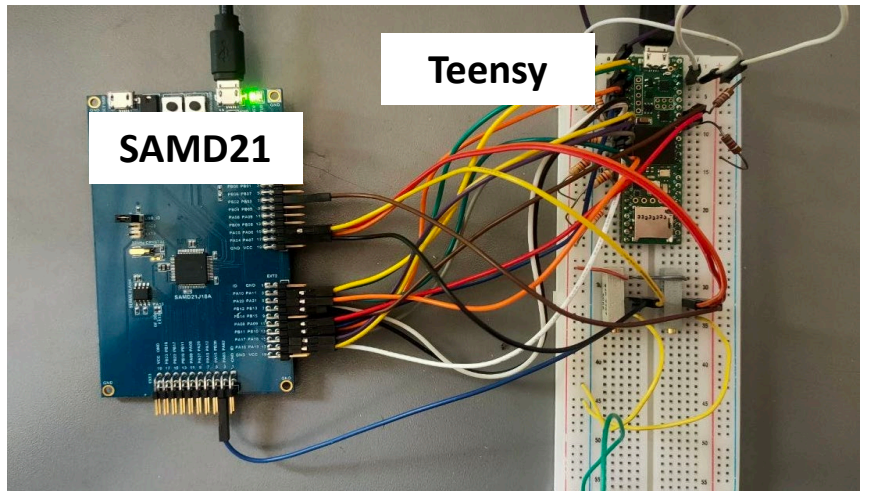
RDO – uC migration from ATtiny416 to SAMD21

Luigi Rignanese

New functionalities:

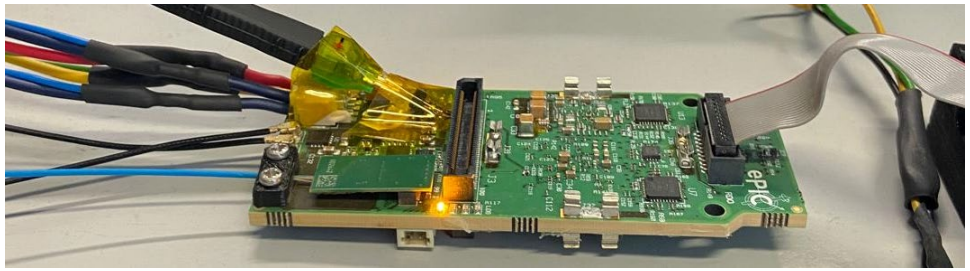
- input and output voltages monitored
- all the monitored values are saved in case of any fail and can be accessed by the FPGA at the next startup
- implemented the possibilities to modify the current limits from outside by “bumping” one of the input voltages (1.4 V) [to be tested]
- LDO fails and FPGA emulator implemented on a Teensy 4.1 [fails injection, registers polling]

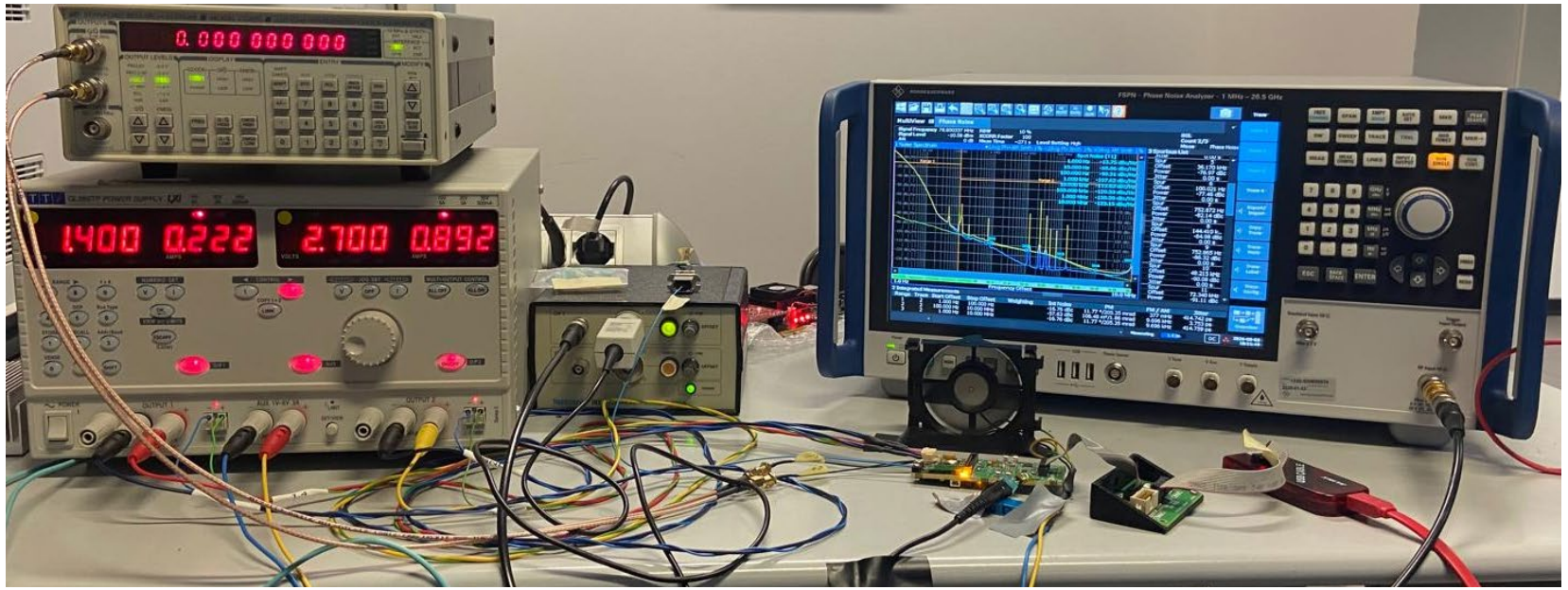
```
-> State: RUN  FW:0xA  profile:NOM  fault:1  retry:0  HBage:9
-> selftest PG:0x0  last knock:0  last cmd I2C:0x0
-> IMON L1..H3  live: 126/126/126/155/155/155   snap: 125/126/128/155/153/155
-> VMON L1..H3  live: 255/255/255/255/255/255   snap: 255/255/255/255/255/255
-> VINL/VINH/T  live: 255/255/255  snap: 255/255/255
-> Last fault: L1 0.85V
```



RDO – Fade- Alinx setup

- data transmission on the high-speed link between RDO -Alinx-Fade with Aurora protocol 64B/66B:
  - **10 Gbps uplink**
  - **2.5 Gbps downlink**



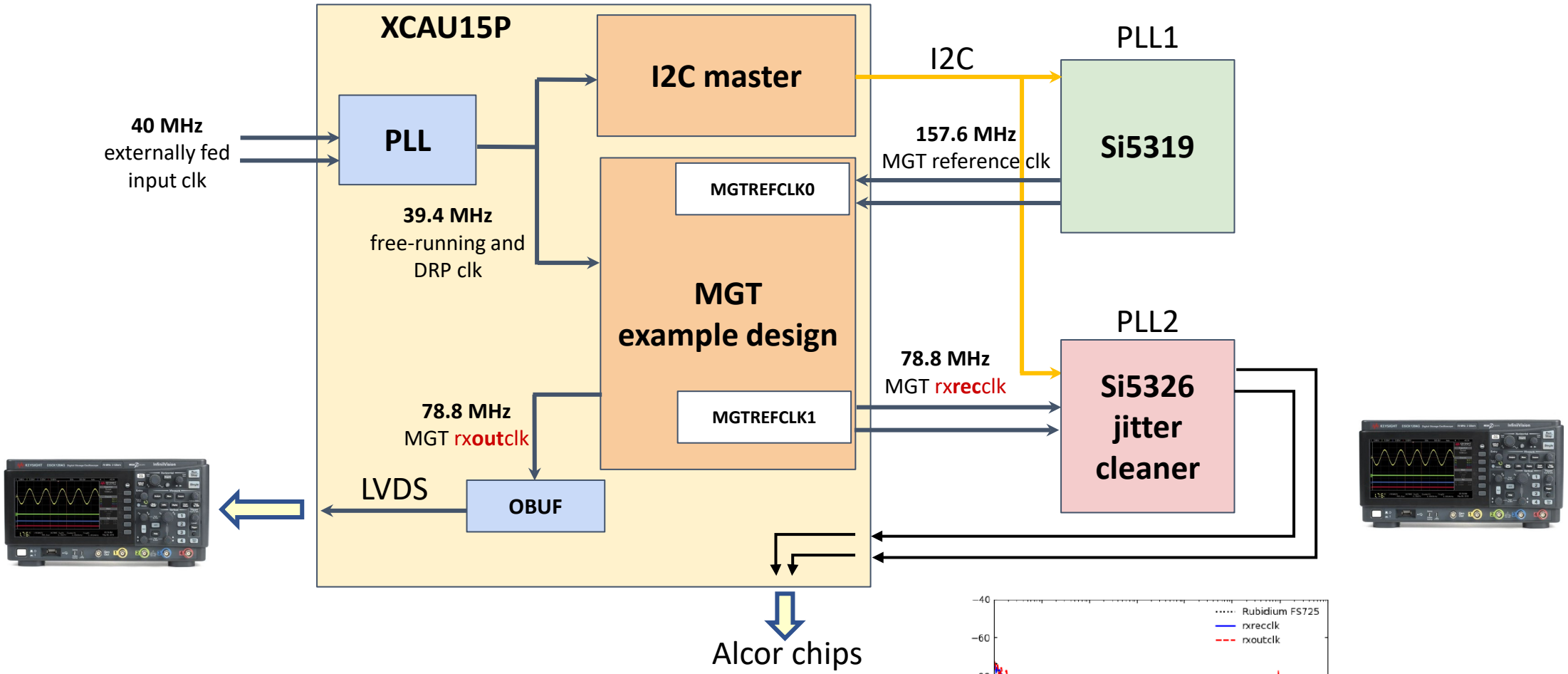


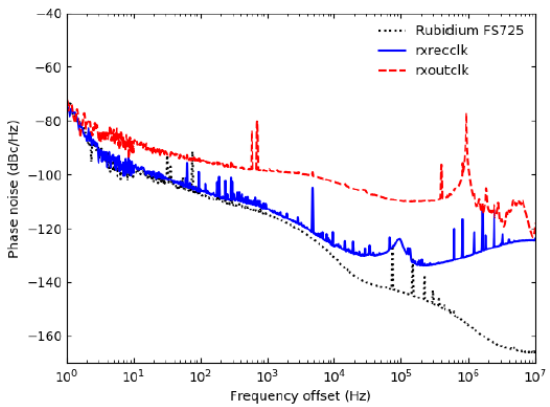
Sandro G.

Matilda P.

Giovanni T.

RDO – Alinx setup: clocks



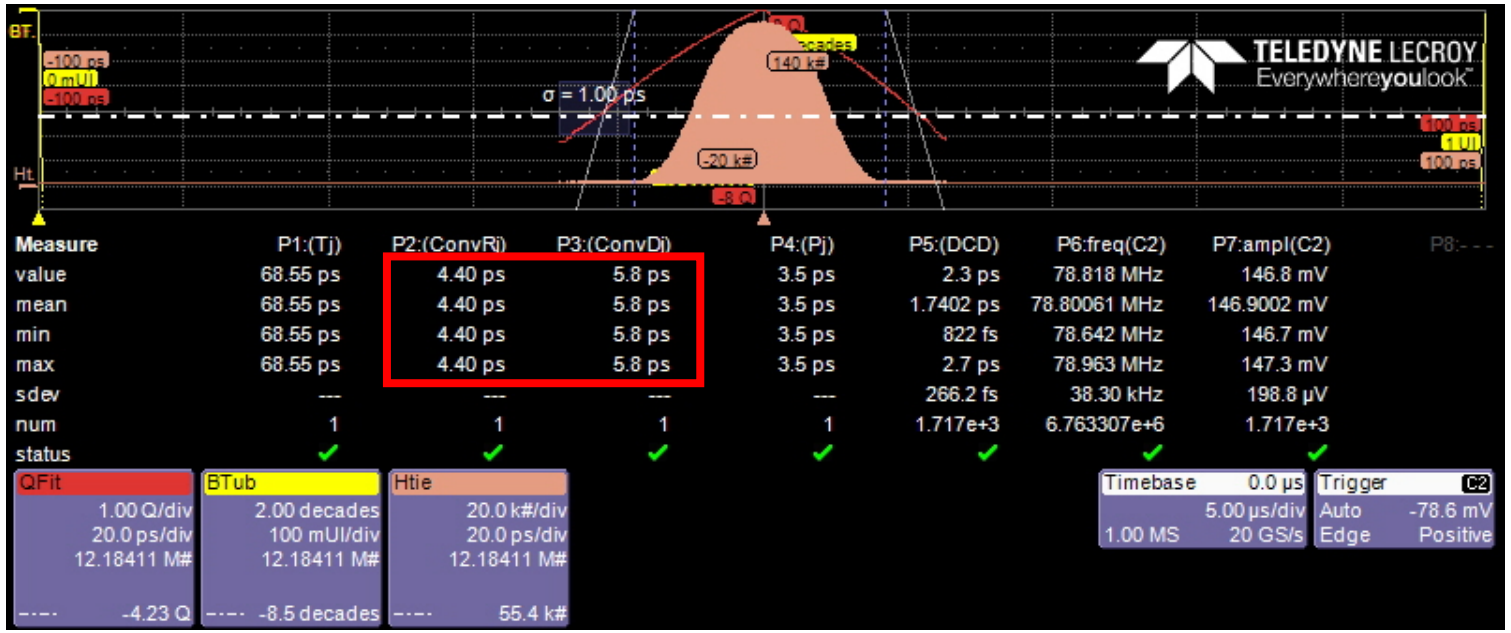


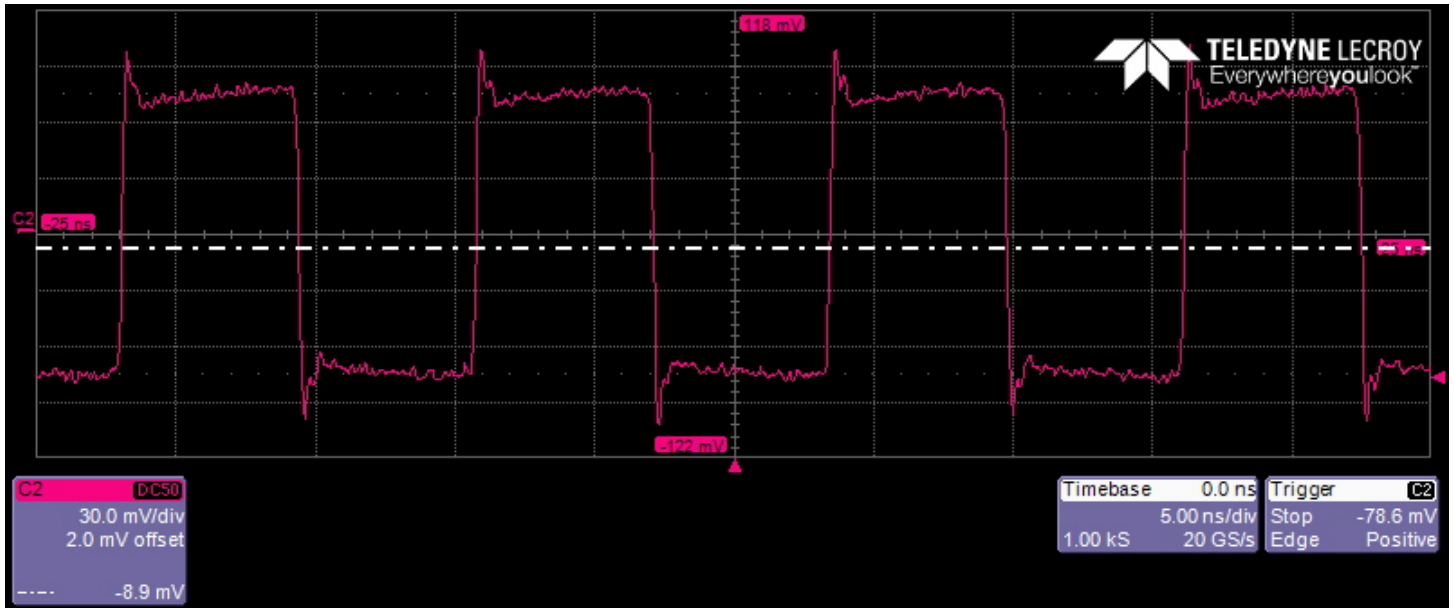
https://ieeexplore.ieee.org/document/8967127

Achieving Picosecond-Level Phase Stability in Timing Distribution Systems With Xilinx Ultrascale Transceivers

RDO – Alinx setup: clocks

rxrecclk @ 78.8 MHz
FPGA output

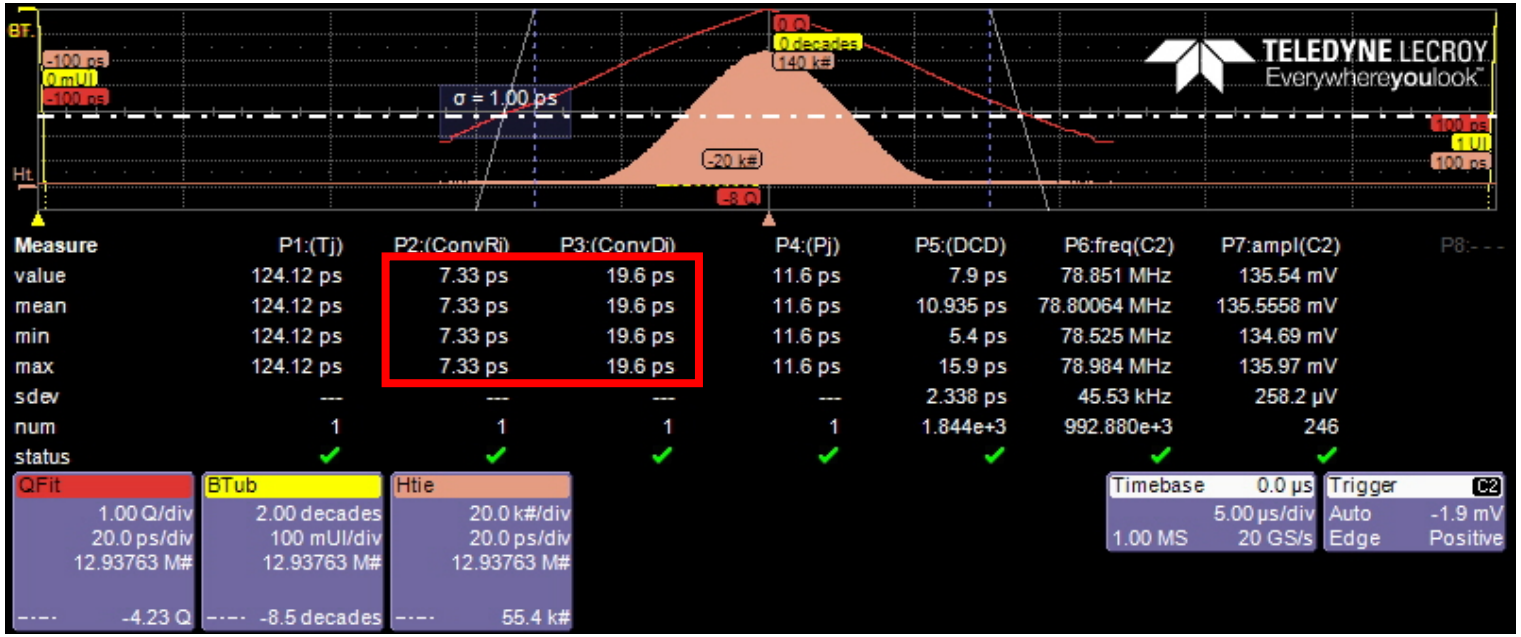


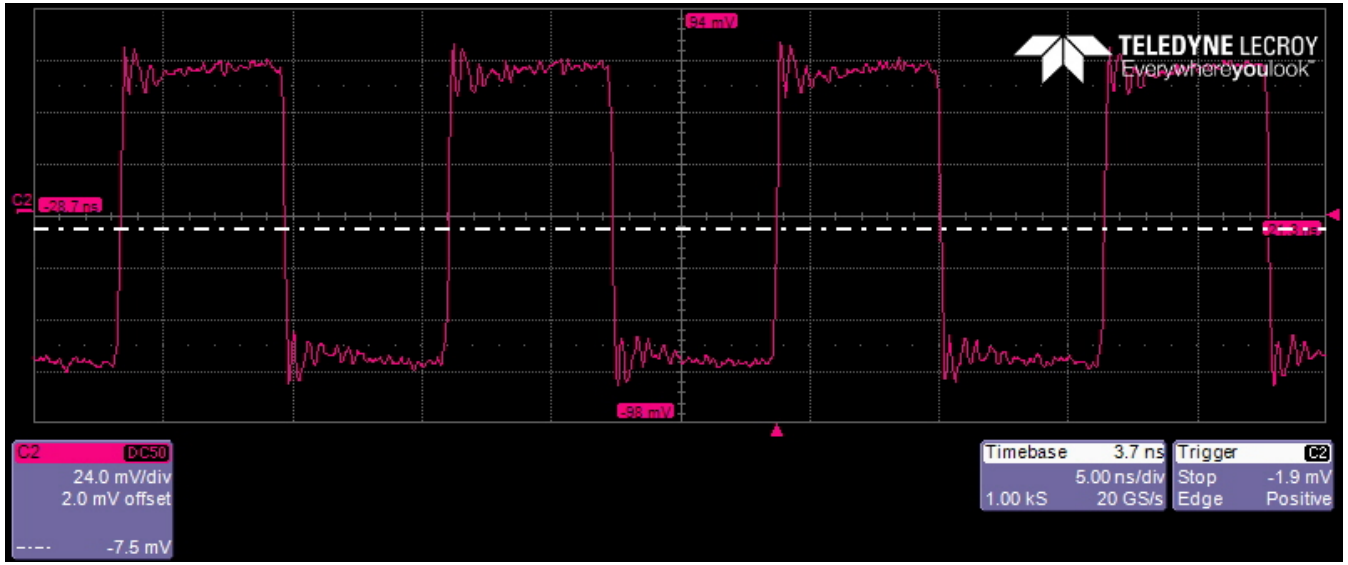


RDO – Alinx setup: clocks

rxrecclk @ 78.8 MHz
FPGA output

rxoutclk @ 78.8 MHz
FPGA output





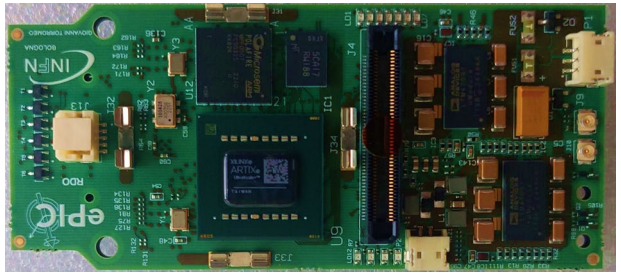
rxoutclk @ 78.8 MHz
FPGA output

Next steps

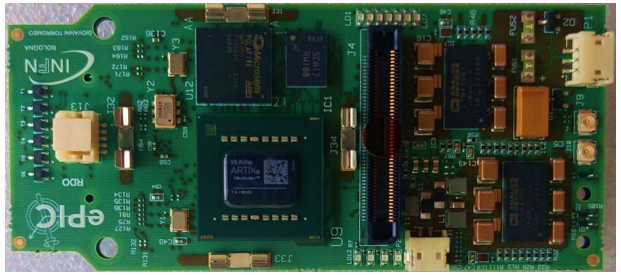
- repeat the same measurements on the clock coming out from the Si5326 jitter cleaner

- repeat all these measurements with al least 2 RDOs connected to one Alinx-FADE device (we need a QSFP for this)

rxrecclk1
rxoutclk1



rxrecclk2
rxoutclk2



Backup slides