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Status report of the eRD109 project on SALSA chip development

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EPIC DAQ/electronics WG meeting

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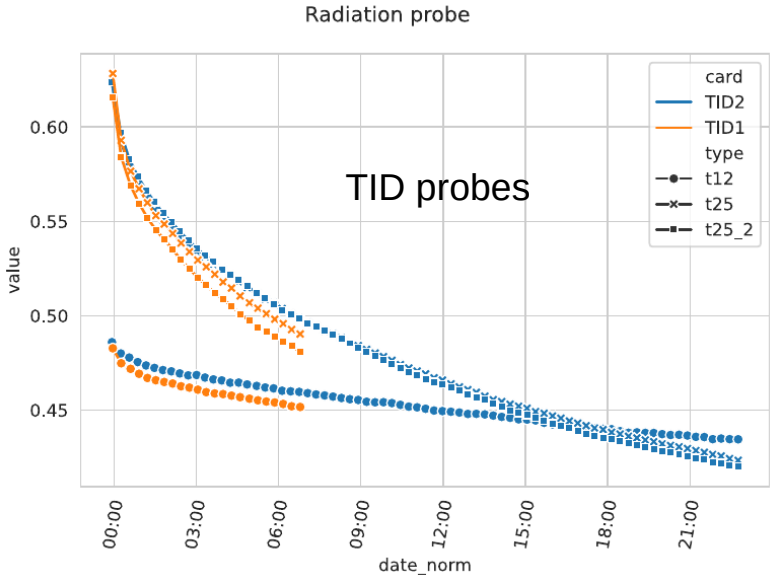
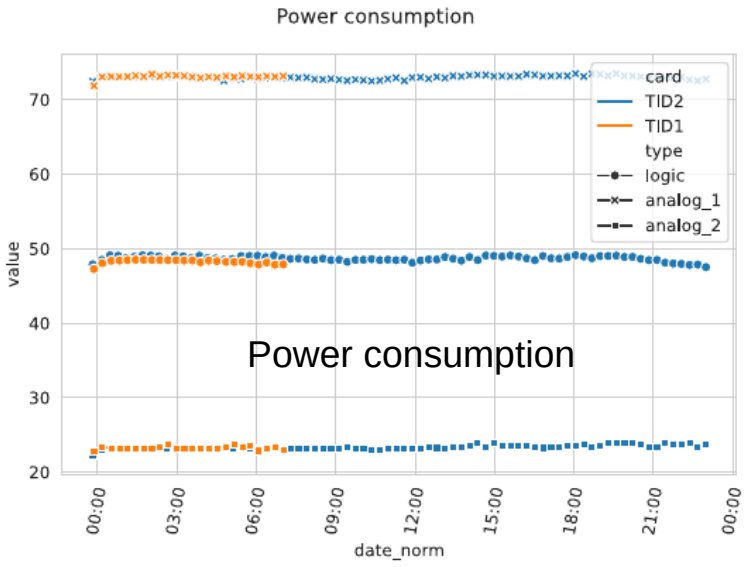
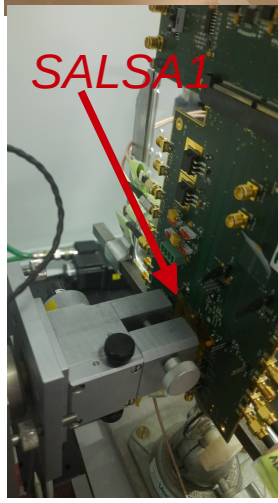
SALSA1 TID TESTS

SALSA1 prototype radiation tests

- Radiation tests done end of June at 40 keV X-ray generator in SOLEIL facility near Saclay
- Dose roughly estimated based on commercial probes, around 300-400 krad/h
- 2 chips irradiated: Chip1 during 7h (2.1-2.8 Mrad), Chip2 during 22h (6.6-6.8 Mrad)



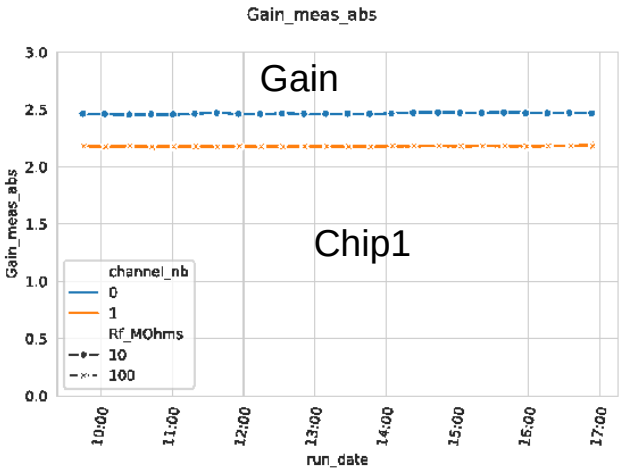


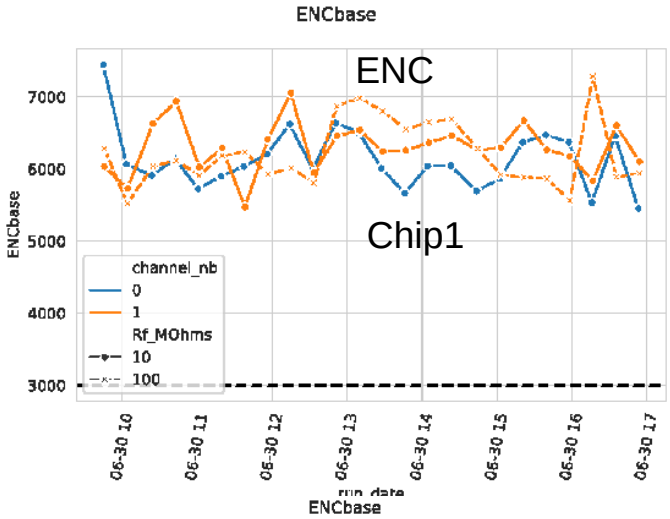


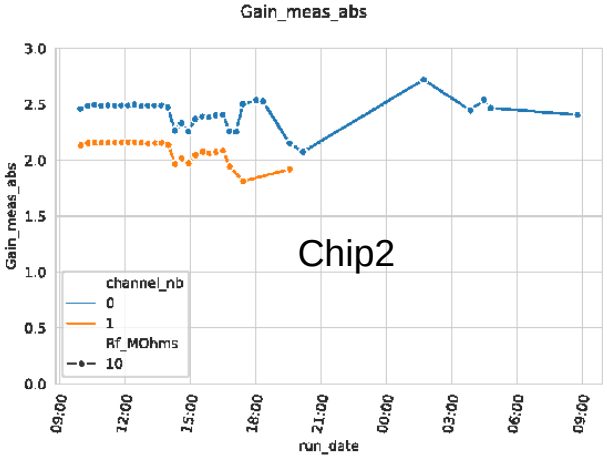
SALSA1 TID TESTS

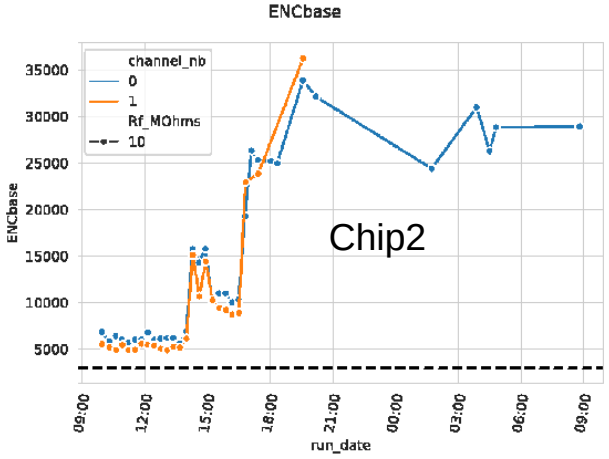
Gain and noise measurements

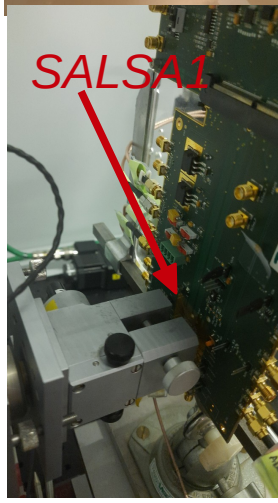
- Stable gain and ENC for both chips during first 7 hours
- Large increase of noise for Chip2 after 7h. Measurements done later at Saclay ok
- Not understood, may be due to external noise source during off-hour data taking







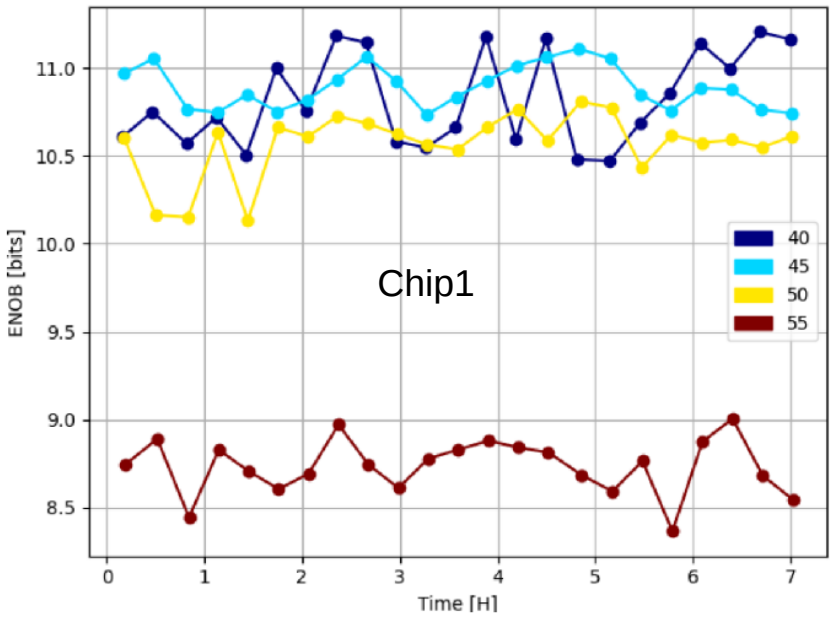


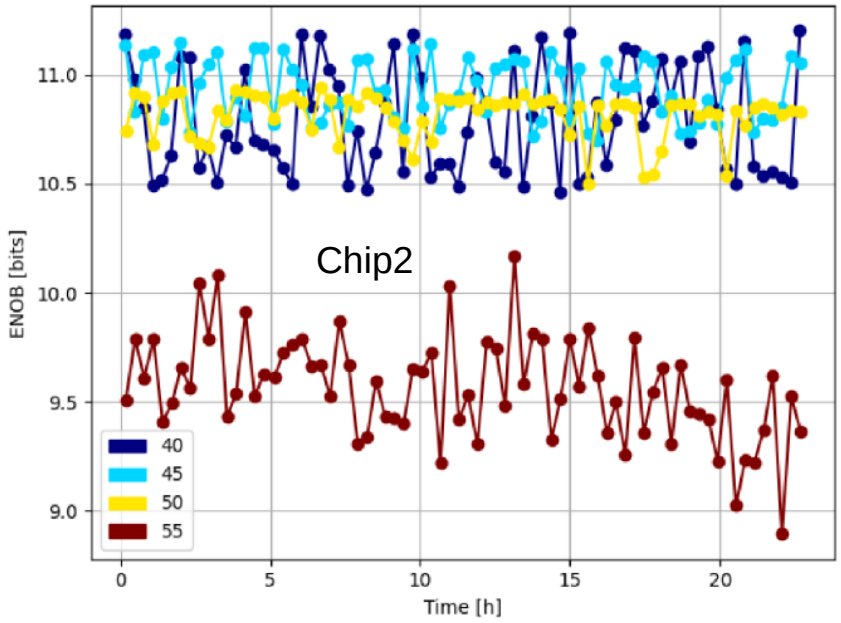


SALSA1 TID TESTS

ADC measurements

- Stable ENOB (effective number of bits) up to 50 MS/s
- Slight degradation of ENOB above 50 MS/s after ~15h (4.5-6 Mrad)





CURRENT STATUS: SALSA2

SALSA2 development status

- Floor plan (whole chip excepted front-end)
  - Adaptation to copper pillars + ring pads ongoing, open questions on I/O pillars and pads positioning
  - Most pillars dedicated to ground and power, defining a grid to distribute power to digital blocks, used as constraint by the layout synthesizer
  - BGA package company ok with 150µm pitch copper pillars with adapted interposer integrated in package, time estimated for packaging process ~5 months
- Front-end:
  - Changes done on layout to adapt to copper pillars + pad ring, part of pillars/pads still to be connected to ground or power. DRC and LVS validations ok, but doubts remaining about the validity of the DRC rules. Design sent to CERN to let them verify on their side our design (layout, pillars, rules), no answer yet.
  - Post-layout simulations to be redone, as lot of changes made compared to bump version
- DSP
  - Work ongoing on synthesis, with improvements on power lines and memory positioning, to improve surface and power consumption estimations
  - Verification of data processing within DSP blocks ongoing. Done for pedestal and baseline correction, ongoing for zero-suppression and common mode noise suppression, to be done for digital filter and packetizer. Integration into digital block ongoing
  - Tests ongoing with FPGA, integration of DSP in main UVM workspace ongoing
- I/O and control core
  - Most modules done and integrated, ready for verification; Initialization state machine validated; Main controller (including fast command decoder) done, integration ongoing; Slow-control to be integrated; Packet generator ongoing. To do: validation of fast command interface with DSP
  - First test synthesis done, layout smaller than foreseen surface → ok
  - UVM: all agents done excepted data injection to I/O core; To do: fast command interface between DSP and control core models, alignment of DSP parameters. Complex test scenarios to be written

PROJECT MILESTONES AND NEXT STEPS

Timeline

- SALSA2 chip submission foreseen November 2026 or beginning of 2027, depending on the consequences of bump issue not fully known
- Tests from Spring or Summer 2027
- Distribution to users expected from end Summer 2027

eRD109 FY24 project milestones

- SALSA2 specifications → July 2024
- SALSA2 submission → November 2026 or beginning 2027
- Beginning of SALSA2 tests → Spring or Summer 2027

eRD109 FY25 project milestones

- SALSA3 design specifications → aiming Q4 2026 (after SALSA2 submission)
- SALSA3 submission → Spring 2028
- Performance evaluation → 2nd semester 2028

Very next steps

- SALSA1 tests → further analysis ?
- PRISMEv1 chip → TID tests delayed
- SALSA2 development → in progress