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# Disk FPC Updates

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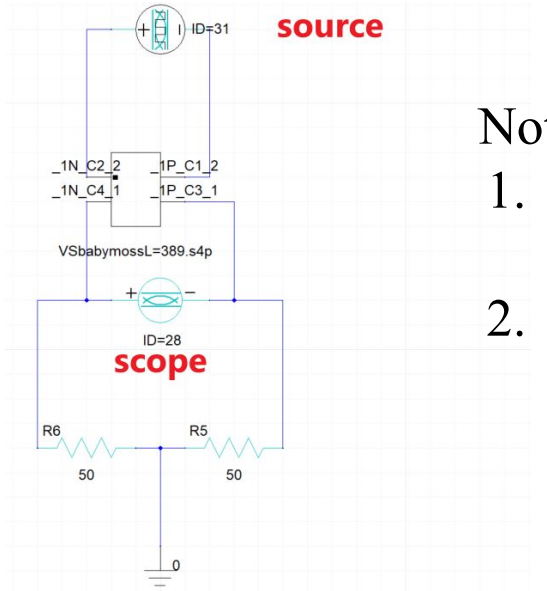
# Ansys Simulation from Stefano Caregari @MIT

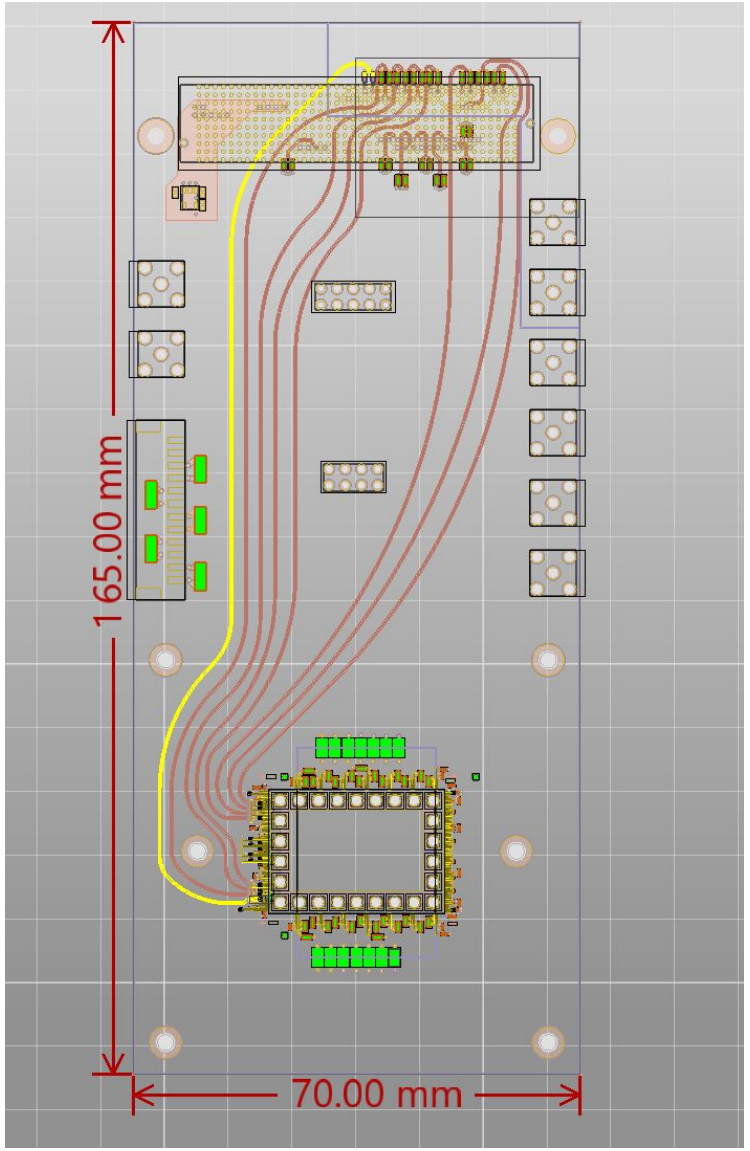
Eye simulation steps:

- PCB models imported in Ansys SIwave
- S parameters .s4p models extracted for each PCB element - HFSS 3D tool is used to model vias regions
- S parameters models are connected in series and simulated as a circuit in Ansys Electronics Desktop
- Long transient simulated .csv are fed to the same SW that processes .csv from the oscilloscope for comparison

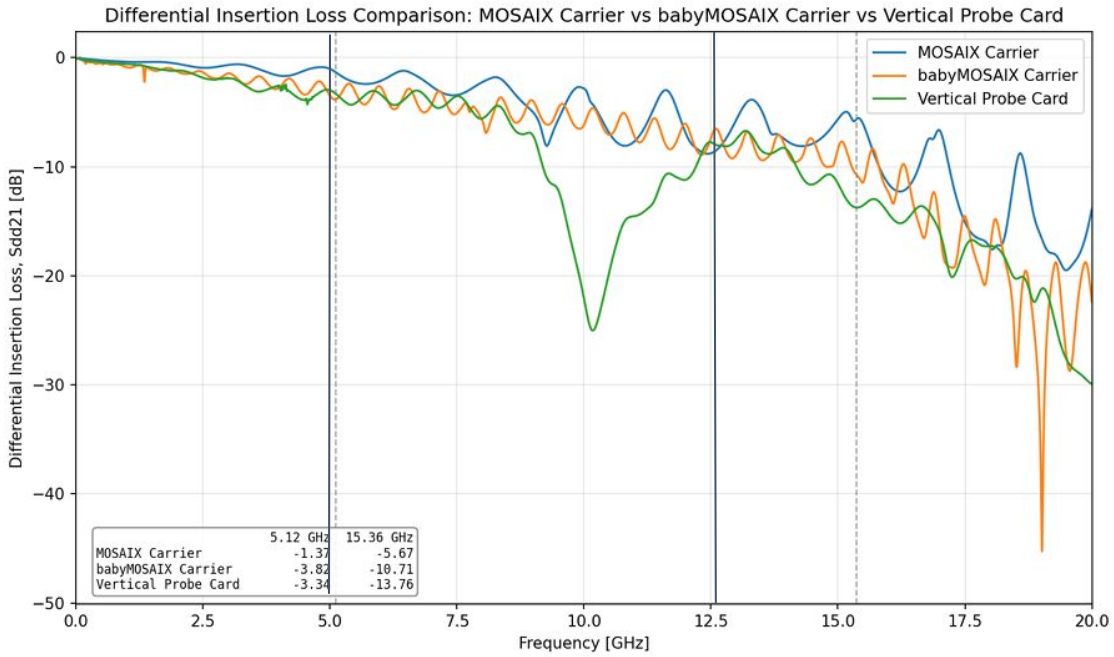



Note:

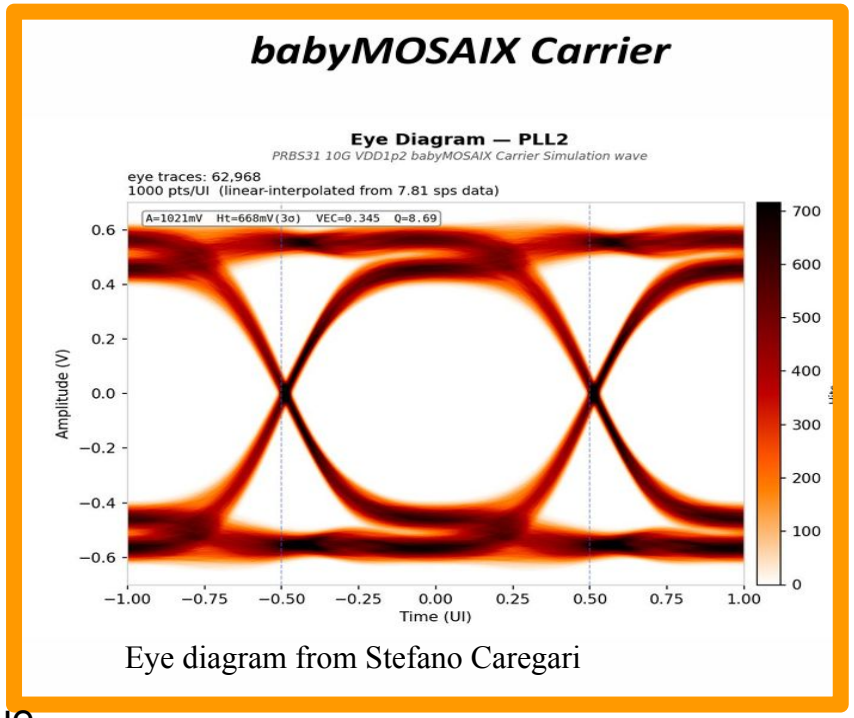
1. The length of the HSD trace on the BAM carrier is 158 mm;
2. HFSS 3D tool significantly increases the computation time, I skipped it for now.



# Cross-checking S-parameter and Eye Diagram

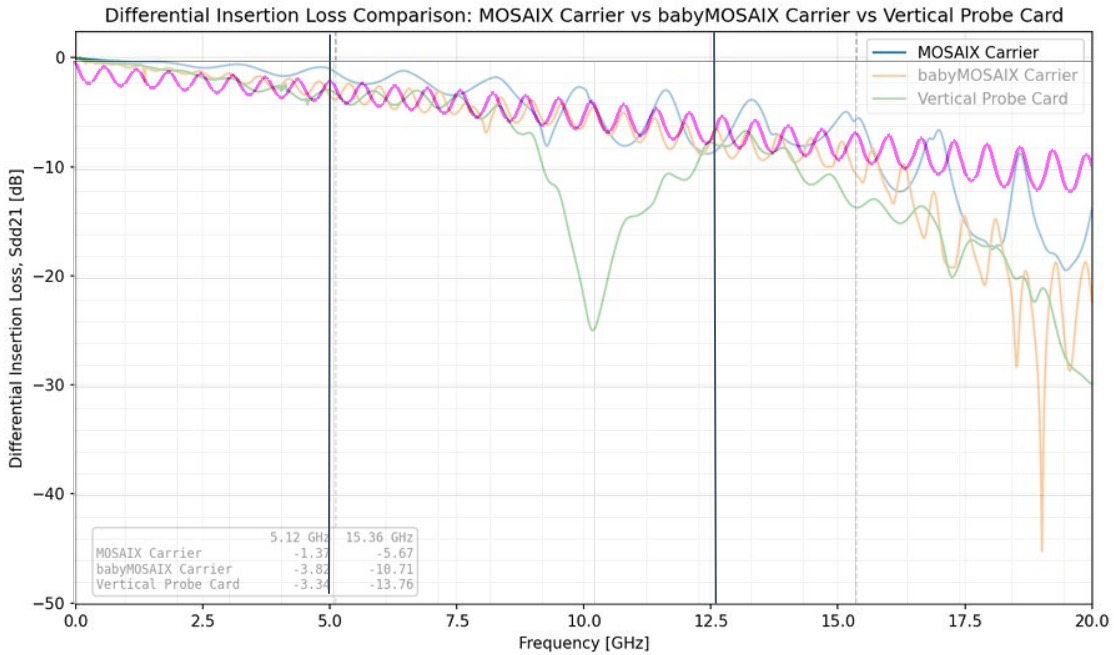


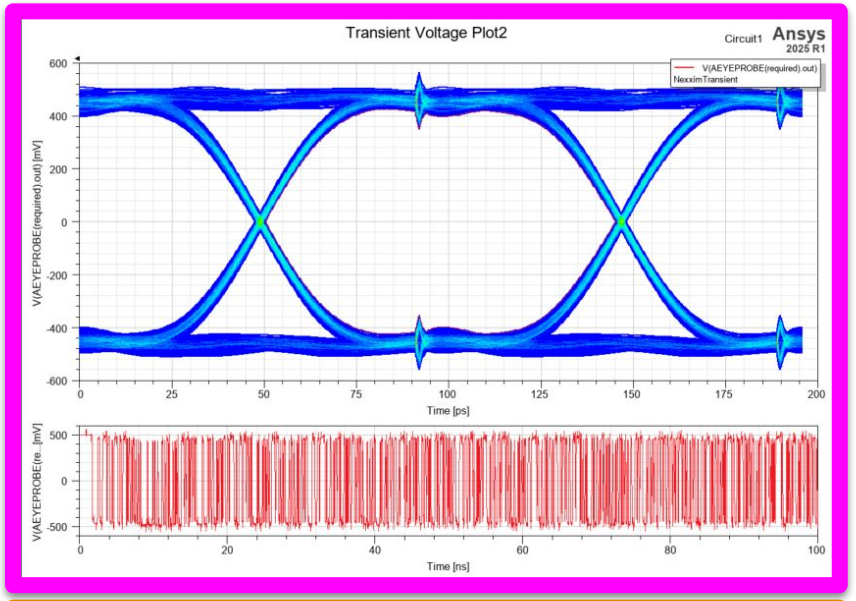

Orange: Stefano Caregari's result

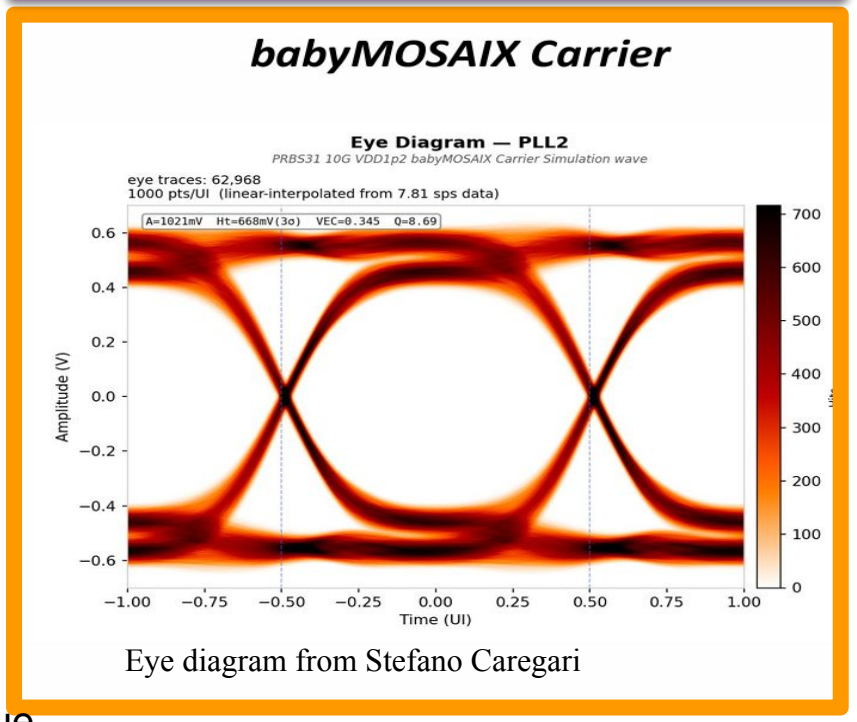



Eye diagram from Stefano Caregari

# Cross-checking S-parameter and Eye Diagram



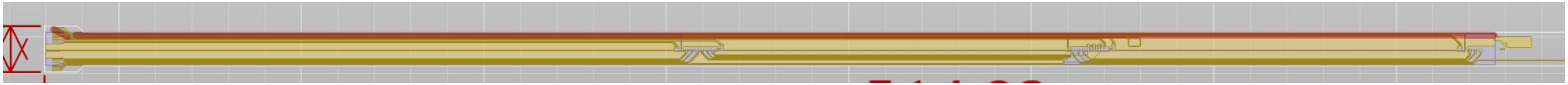



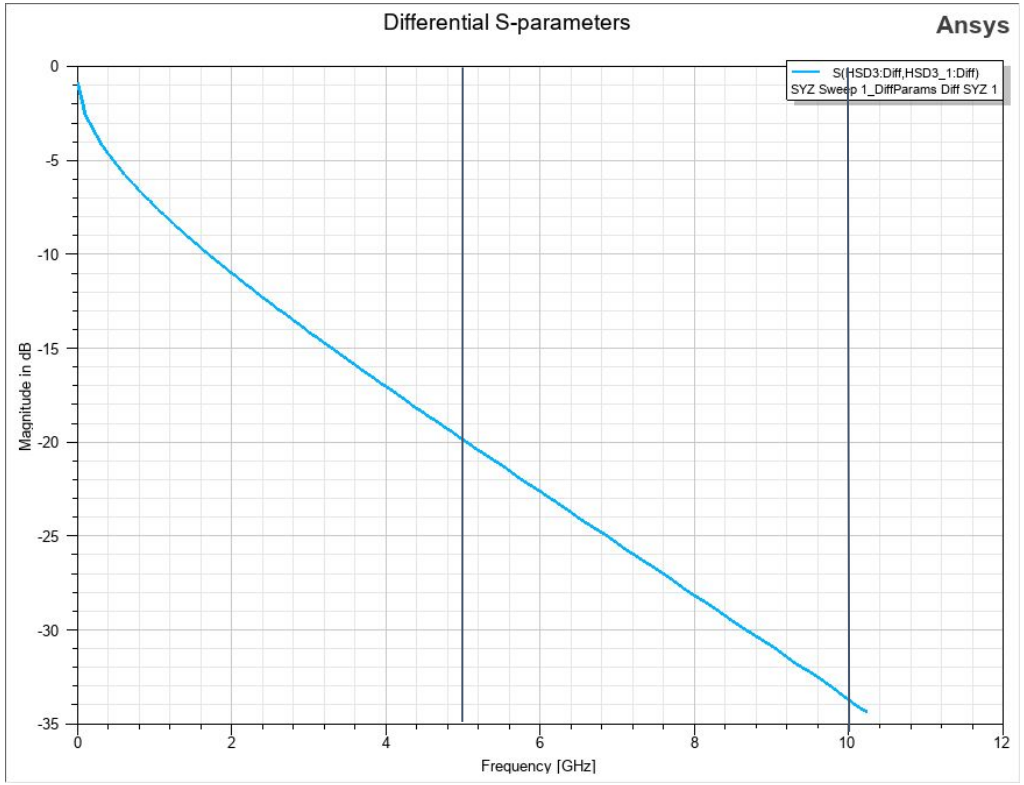

Eye diagram from Stefano Caregari

Orange: Stefano Caregari's result

Purple: My result

# S-parameter for JLC_V1 FPC



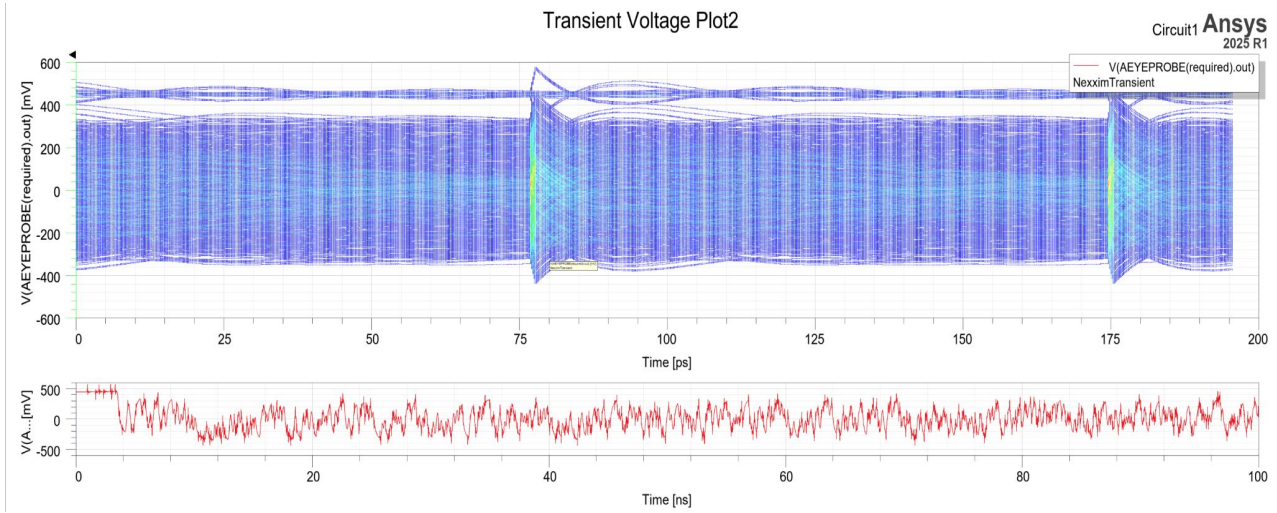



Maximum length for HSD trace is 389mm (red area).
Width = 55 um, Spacing = 140 um, Thickness = 12 um.

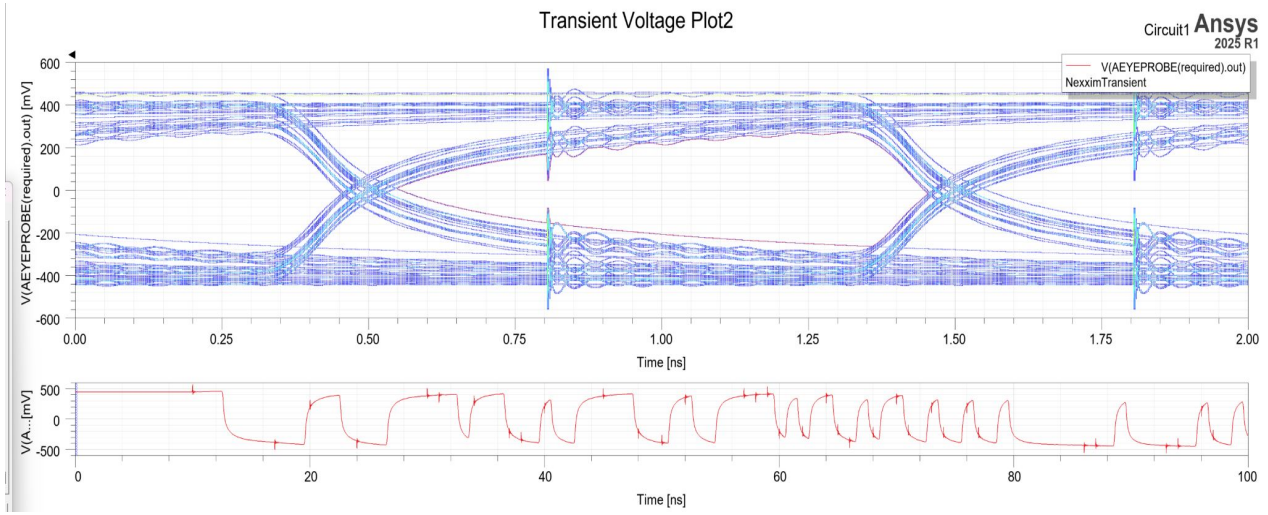
The cross-sectional area of the HSD traces in babyMOSAIX carrier is around **8 times** larger than it in JLC_V1 FPC, while the perimeter is ~**3 times** that in JLC_V1 FPC. When considering high-frequency signal loss scenarios, perimeter is a more convincing metric.

Significant signal transmission lost, eye diagram is unacceptable @10.24Gbps (see next slide).

# Eye diagram For JLC_V1 FPC



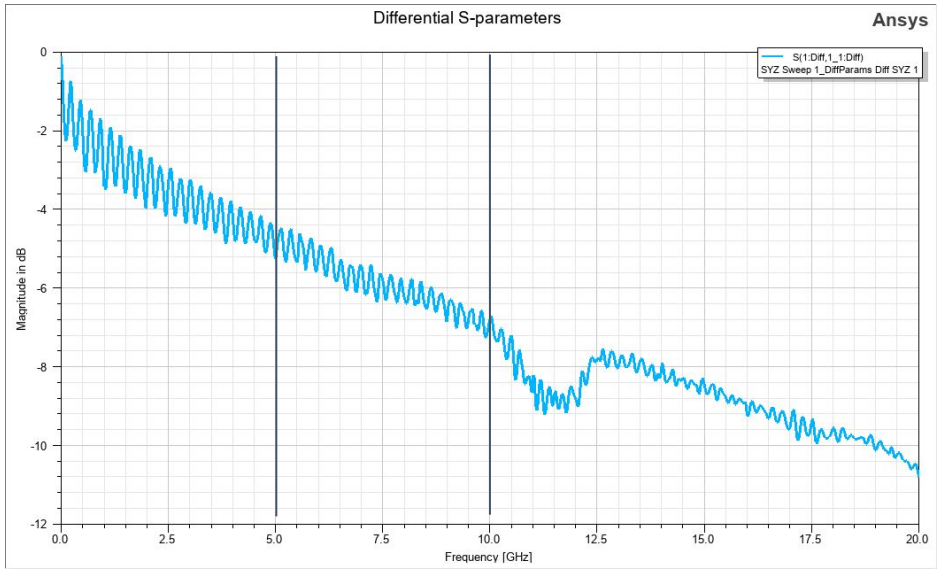

HSD @10.24 Gbps



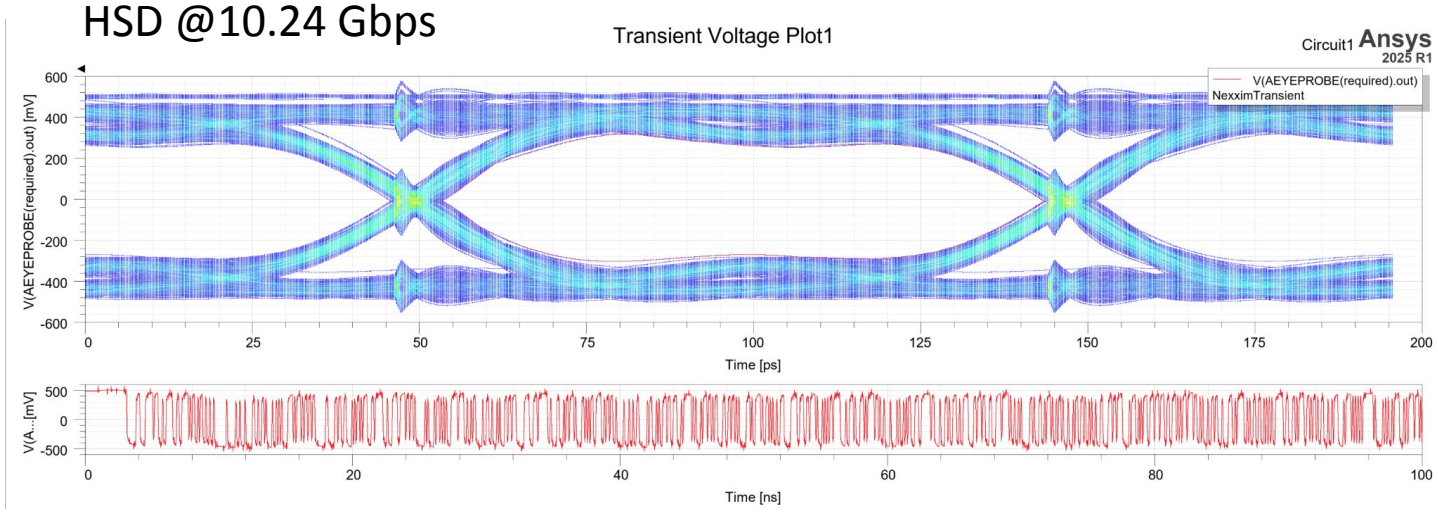

HSD @1 Gbps

Note：Certain structures on the FPC (the FPC connector interface and the corners of the traces) also contribute to signal loss.

# Increasing HSD trace thickness/width




HSD @10.24 Gbps




Original: Width = 55 um, Spacing = 140 um, Thickness = 12 um.
New: Width = 150um, Spacing = 160 um, Thickness = 35 um.

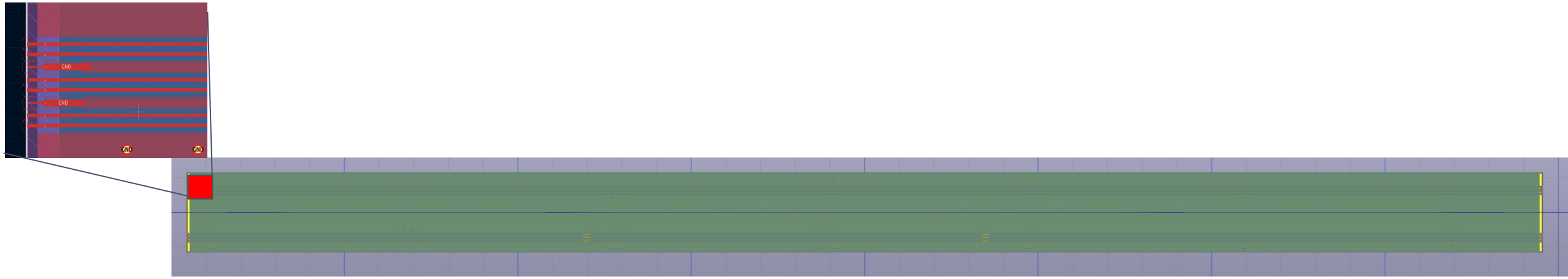
Note: The impedance of the new trace is controlled to 100 ohm, by increasing the thickness of dielectric to 116 um.

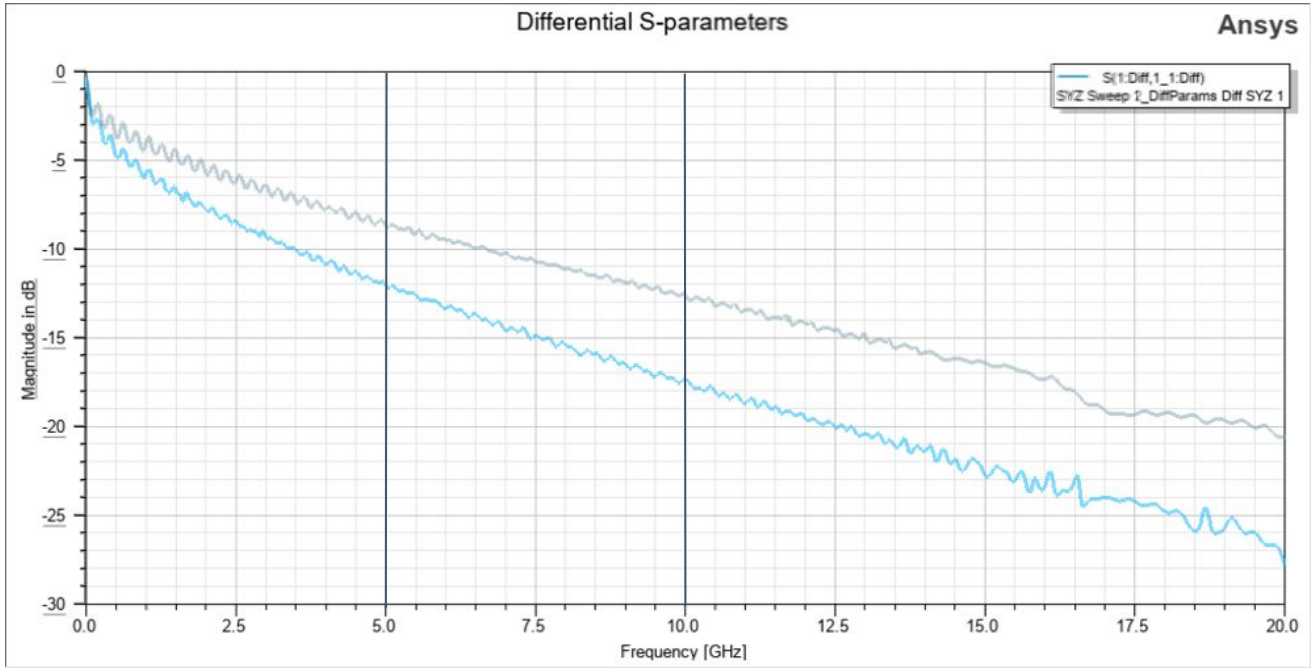
# Available cross section for JLC FPC

| | Thickness(um) | |
|---|---|---|
| Cover layer | 27.5 | 50 |
| Copper | 12 | 18 |
| Dielectric | 25 | 50 |
| Copper | 12 | 18 |
| Cover layer | 27.5 | 50 |
| **Total thickness** | 104 | 185 |
| suggested trace width | 55 | 93 |
| suggested trace spacing | 140 | 152 |
| perimeter | 134 | 222 |

**JLC has suggested width/space for the cross section with 104um & 185um total thickness.**

# FPC with simple traces in JLC's available stackup

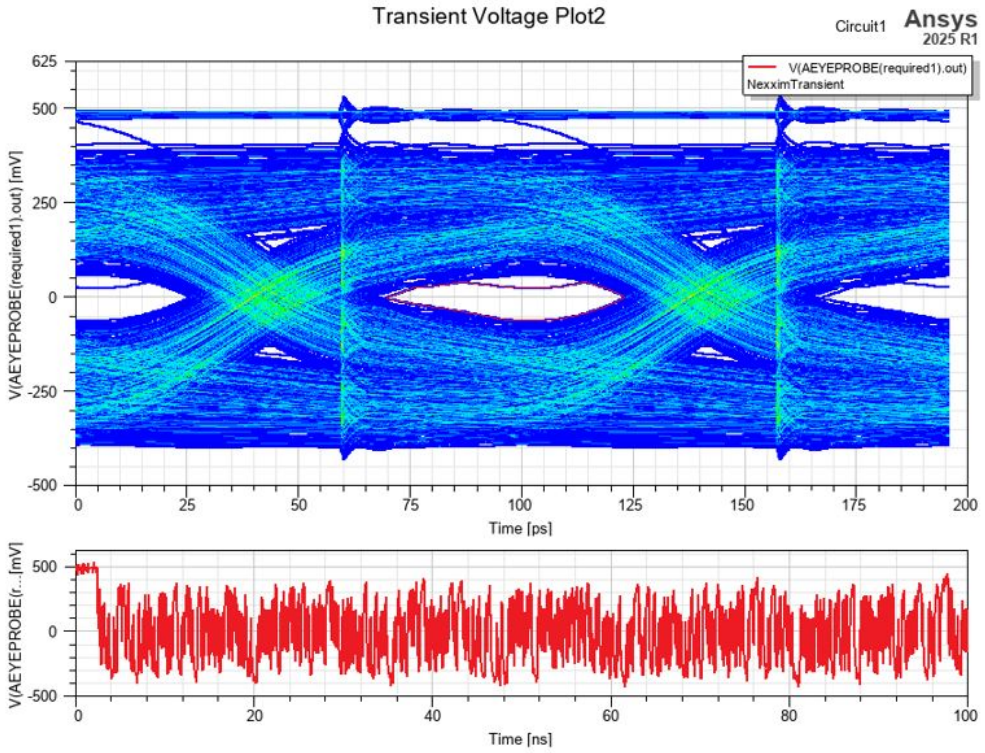




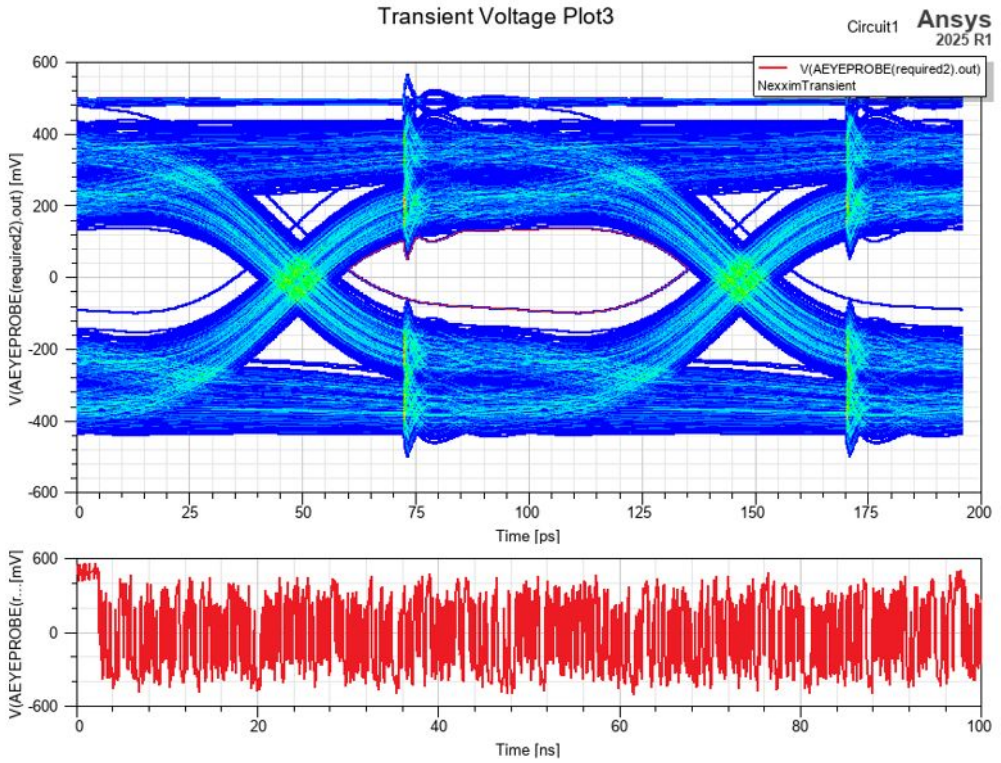

L=389mm
Differential S-parameter simulation results for:

**Gray: 18um Cu + 50um Dielectric FPC**
**Blue: 12um Cu + 25um Dielectric FPC**

# Eye Diagram results @ 10.24Gbps




12um copper
25um dielectric
55um trace width




18um copper
50um dielectric
93um trace width

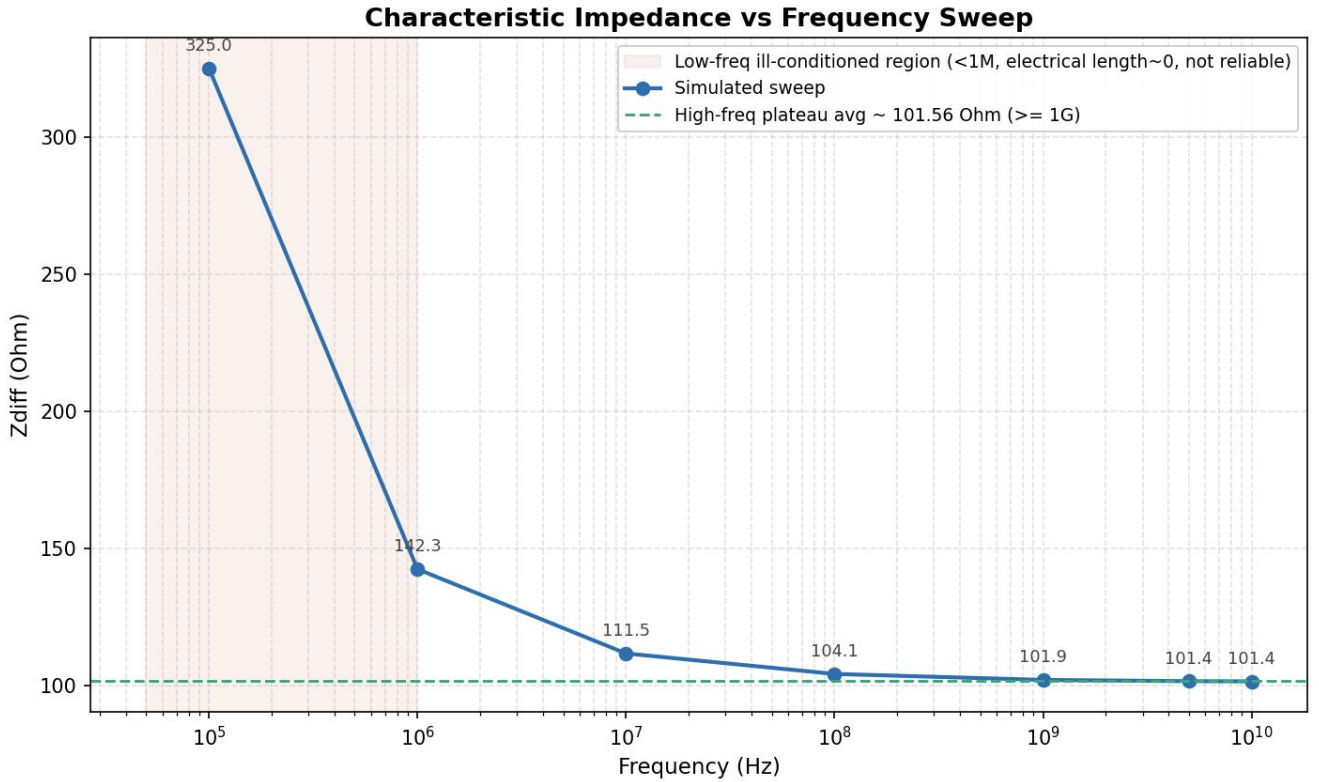
# Summary

- Performed Ansys simulation, the HSD traces on the BabyMOSAIX carrier board were simulated, yielding results consistent with those of Stefano.
- The same methodology was applied to simulate JLC_V1 FPC. The results show that high-frequency signal transmission characteristics are far from ideal.
- Increasing the perimeter of the trace to reduce signal loss on the trace has been confirmed to be a feasible approach.
- Based on JLC capability and Ansys, submit corresponding test structures to compare
  - Different thickness/width/spacing
  - Soldering vs wire-bonding vs direct connection

## Next step:

- Measure the performance of test structures with different thickness/width/spacing, to validate Ansys simulation.
- Use the Ansys simulation to optimize the disk FPC design

In Ansys, low-frequency simulations may produce anomalous values due to inherent limitations in the solver method. Taking the BabyMOSAIC carrier board structure as an example, characteristic impedance results at simulation frequencies above 1 GHz can generally be considered accurate.




| Frequency | 100k | 1M | 10M | 100M | 1G | 5G | 10G |
|---|---|---|---|---|---|---|---|
| Zdiff | 325 | 142.28 | 111.54 | 104.07 | 101.89 | 101.43 | 101.36 |

# Impedance calculation

JLC's suggestion for Zdiff = 100 **(measurement by JLC)**

Simple calculator based on empirical formula in IPC-2141

Ansys result

| | Width | Spacing | To GND | Z（with cover） | Z（without cover） | Frequency | Ansys（with cover） | Ansys（without cover） |
|---|---|---|---|---|---|---|---|---|
| 25um dielectric 1/3 oz copper 104 um thickness | 55 | 140 | 225 | 87.1 | 99.9 | 100M | 90.8 | 95.9 |
| | | | | | | 5.12G | 82.7 | 87.4 |
| | | | | | | 10.24G | 82.5 | 87.1 |
| comment | Should be trustable in JLC's production | | | reference only | | Should be trustable, too. The dielectric constant in the simulation maybe not very accurate | | |