ASIC Testing Status

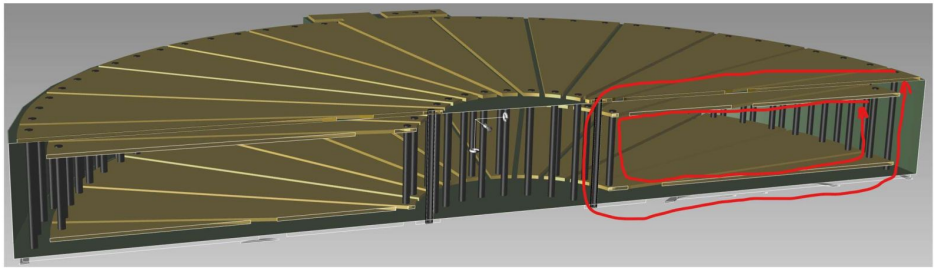
- EICROC1 Testboards
  - having odd new problems with the lab setup and the board – investigating [Alex, TL]
    - ADC data seems to be oscillating and/or jumping around coherently for all pixels
      - ground bounce? bad PS?
    - we will continue next week by redoing the entire setup and checking all components
      - PS, cables, connectors, etc.
  - plan to continue with the “fast readout” FPGA scheme [Prithwish]
  - 2 Tesboards have a wire-bonded EICROC1 ASIC but the 3rd is still not done
    - Note: the 3d will have some minor mods and will be connected to RBv1 eventually
- EICROC0A Tesboards [Alex]
  - plan is to make a common ZCU106 firmware for both EICROC1 and EICROC0A Testboards [TL] to gain more insight while cross-comparing [Alex]
  - ongoing…
- Roman Pots 3x ASIC board [Jack]
  - Jack, Christophe, Mike & TL held a meeting to go over final questions
  - we’ll have a final production review once Jack is ready with schematics & board layout in ~3 weeks
- FCFD RBv1 Testing [Rice]
  - Fermilab is making more testboards with the hope of sending one to Rice for RBv1 integration & testing [Sergey, TL]

BTOF Service Hybrid

- the detector mechanics is having a problem with the SH board height → our current 15mm height is too large
  - the height is *currently* driven by the size of Tim's coils for the bPOL48 DCDC converter
  - we need to make this total height (Readout Board & Power Board sandwich) 10 mm
    - this is a significant reduction
    - likely comes at a cost
- looking into using the PCB-style coil ala CERN's bPOL48 module ⇒
- new development (Gabor et al) is to make our own PCB coil and also redo the CERN module itself to decrease its size ⇒
- Note: pictures are Gabor's

Air-core toroid

Plan was to create a double turn 1.5uH toroid coil, but becasue of stackup change the result is 1.25uH
4 layers, dimeter is 20mm, height ~2.3mm



bPOL48_PS1V0, 55mm x 24mm x 3.1mm