AncASIC MPW1 Test at LBL - Updates

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Last update at ePIC SVT DSC meeting on 26th May 2026 - Slides

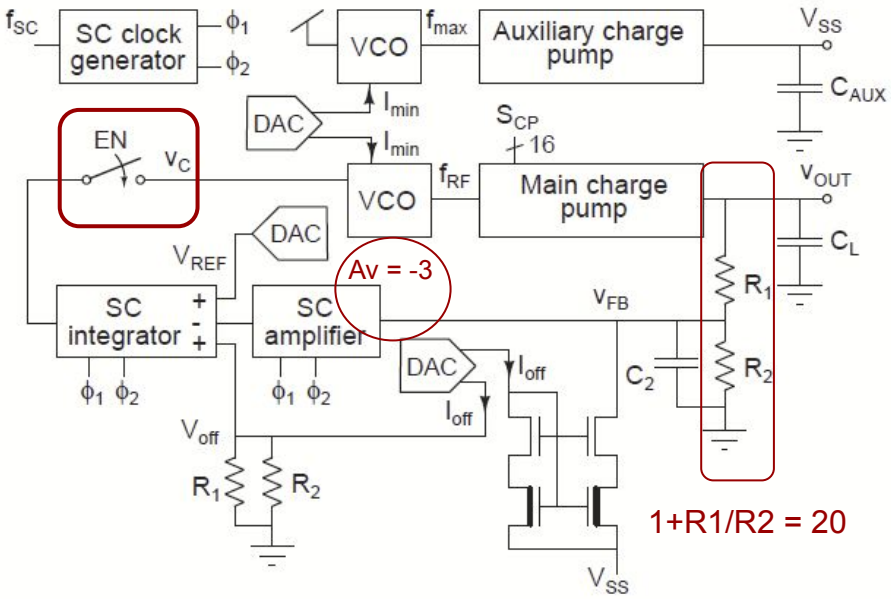
*Thanks to the BNL design team and Amanda Krieger at LBL for useful suggestions/discussions

Negative Voltage Generator

Content

- VOUT Range
- Load and Line Regulation
- Transient Response
- Noise Measurements
- NVBG + babyMOSS

Negative Voltage Generator



Top-level block diagram of the closed-loop NVG circuit

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In closed loop configuration,

- Vout = (-20/3)VREF
- VSS = -1.2 V

Programmable control parameters

Parameter	Description
Iinteg	bias current for the SC integrator
Ivco	bias current for the VCO
Ioff	bias current for the offset generator
EN_{CP}	enable branches of the main charge pump and RF driver
EN<2>	selects VCO control voltage (Vc) - 0 = external control voltage - 1 = output of the SC integrator
EN<1>	Enable RF clock for main charge pump
EN<0>	Enable RF clock for aux. charge pump

Open loop
Closed Loop

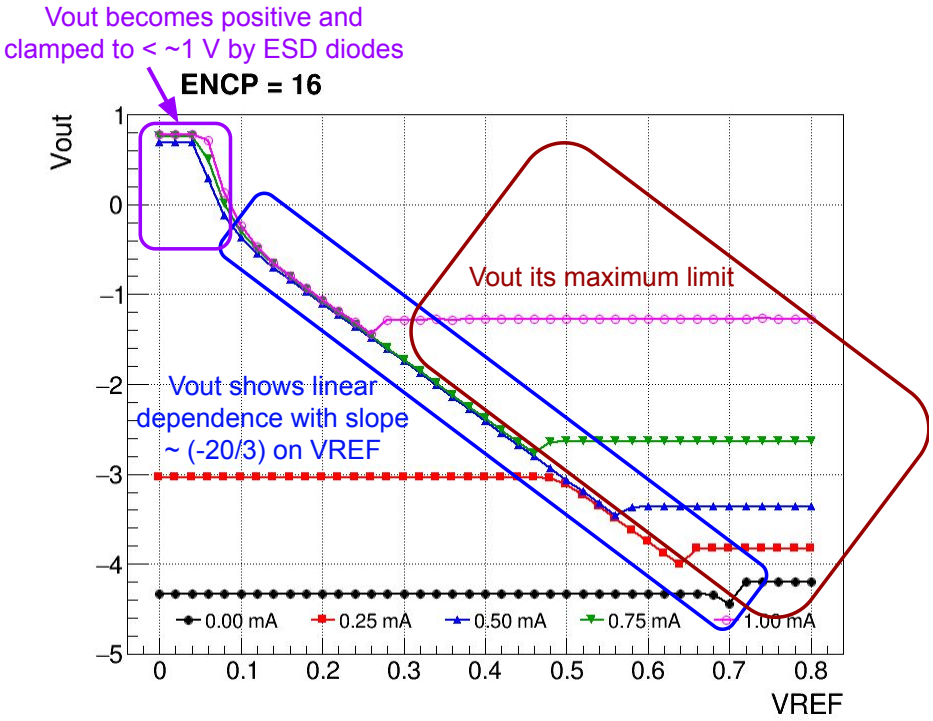
I2C Configuration: **EN = 111, Ioff, Ivco, Iint = 0000111**
CLK_SC: **1.2Vpp Square**
Power: **VDD = 1.2 V, GNDi = -5 V, VDDi = -5 V**

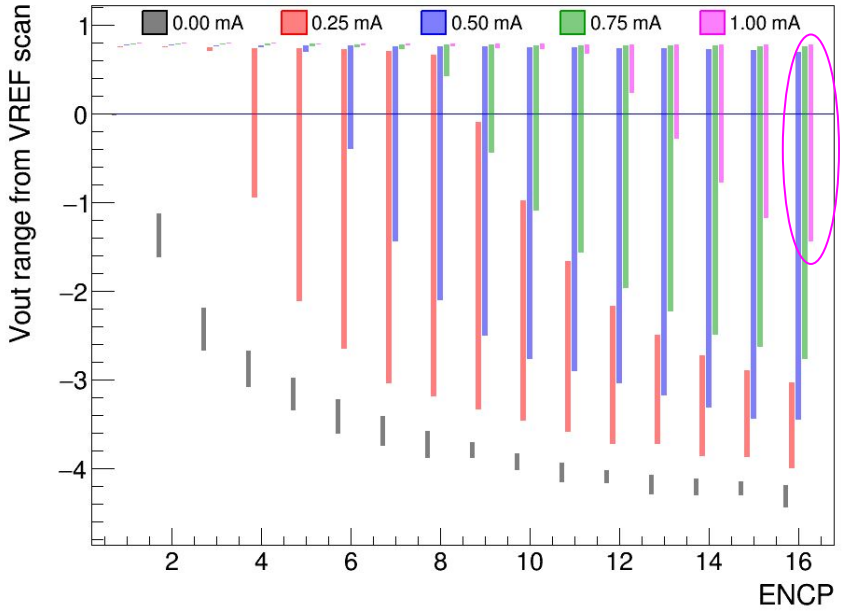
remain fixed during these measurements

NVBG VOUT Range

Negative Voltage Generator

I2C Configuration: EN = 111
Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 1 MHz
C_L = 1 nF





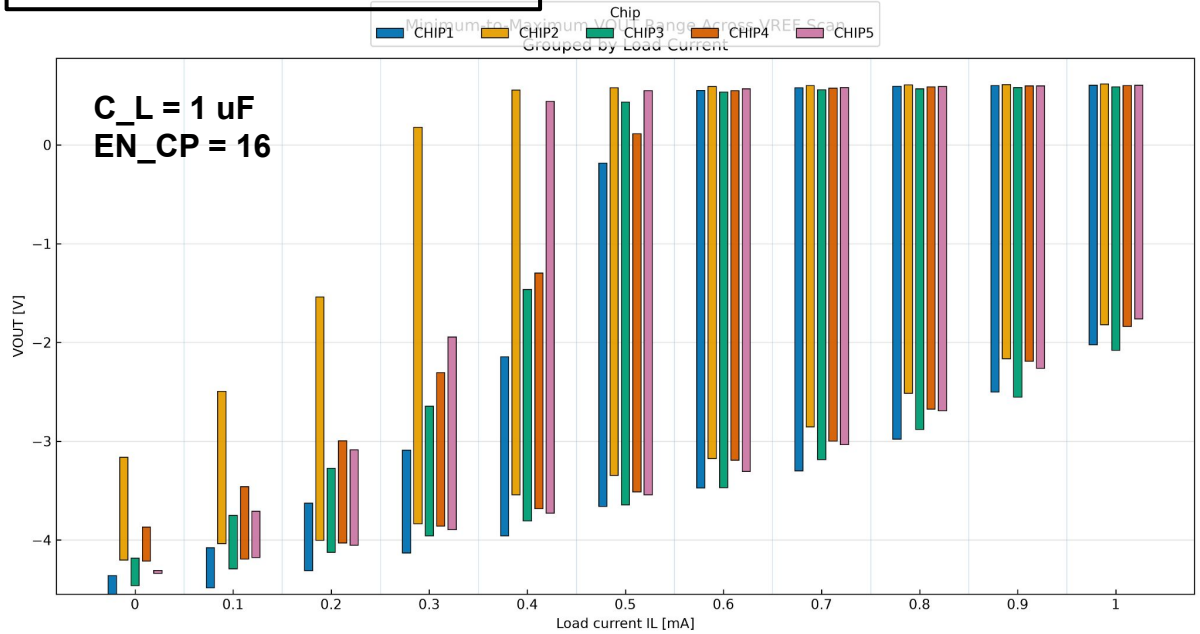
- Vout range from VREF (0 - 0.8V) scan for each ENCP (different load currents)
- **With 1 mA current load, for highest ENCP, Vout reach ~ -1.5 V**

I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz
C_L = 1 uF
VDD = 1.25 V

Negative Voltage Generator

Chip to chip variation

Multiple chips at room temperature



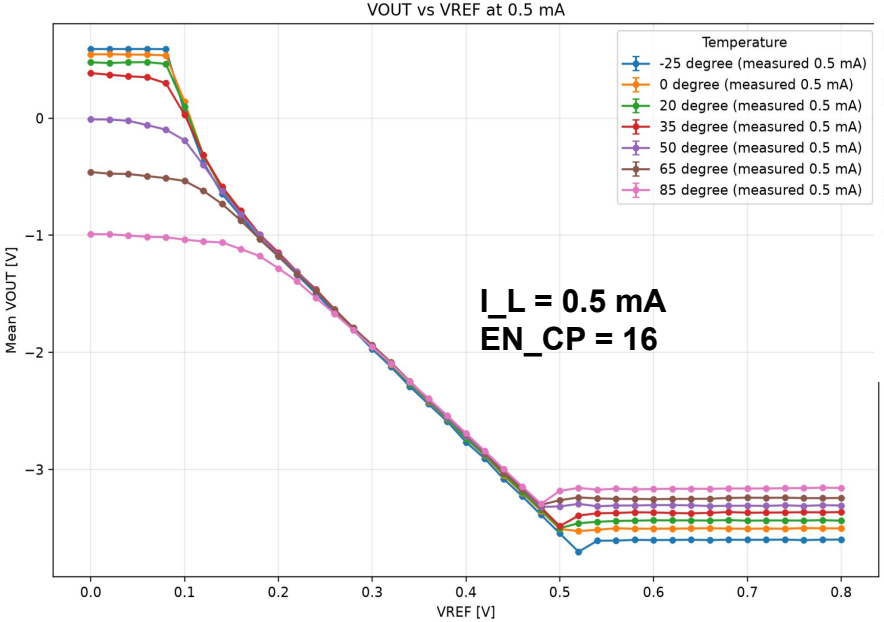
- VOUT range measured across five chips at ENCP = 16 for different load currents, with all other settings fixed.
- Some chip-to-chip variation is observed, particularly at lower load currents, while all chips show a similar load-dependent trend.
- Negative-voltage generation is maintained across all five chips up to IL=1mA

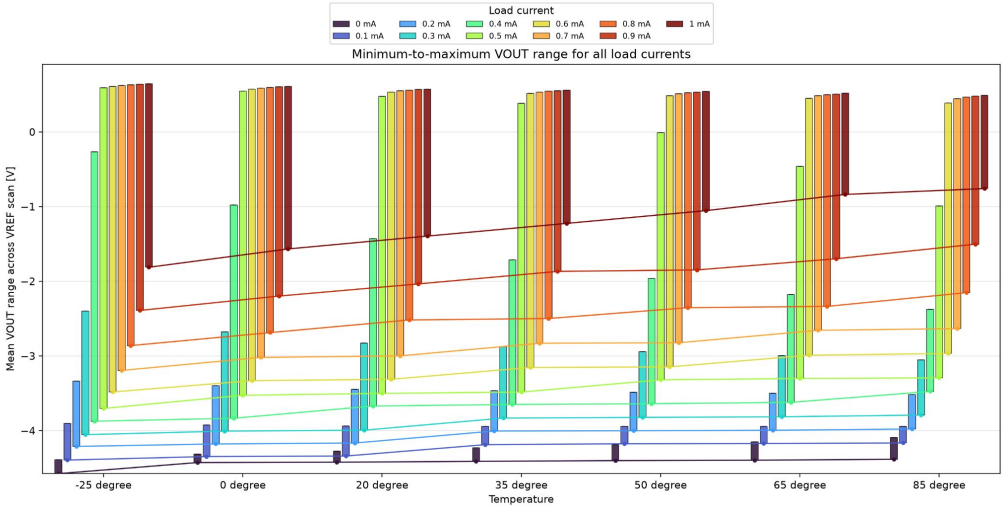
I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz
C_L = 1 uF

Negative Voltage Generator

Temperature dependence

Single chip: CHIP1

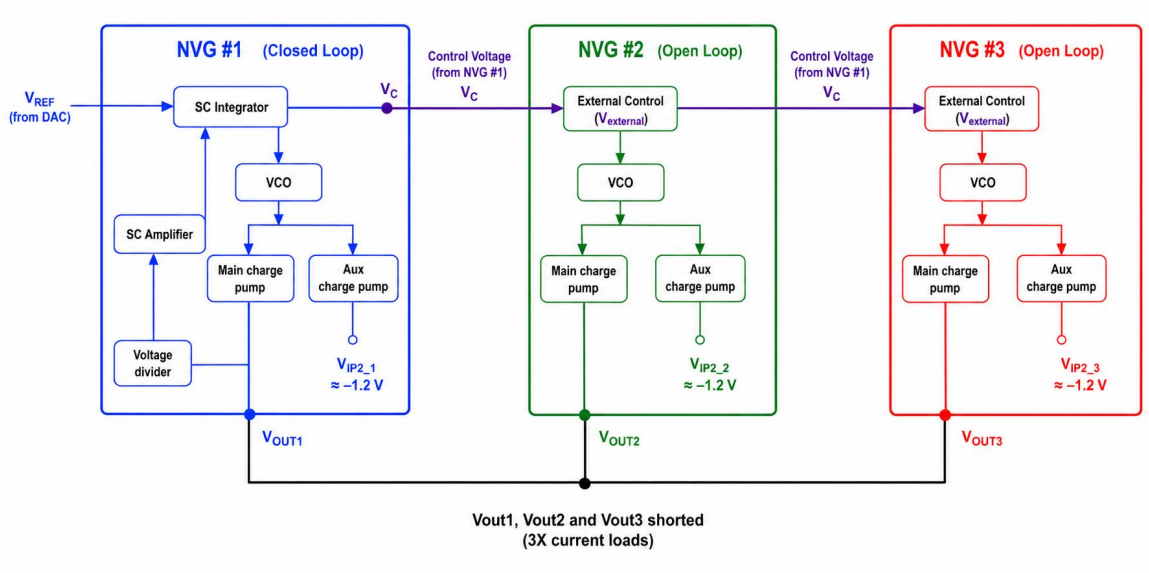




- NVG output range was measured over a temperature range from −25°C to 85°C.
- VOUT–VREF transition region narrows as temperature increases while all other parameters are kept constant.

Negative Voltage Generator

Three NVBGs in parallel

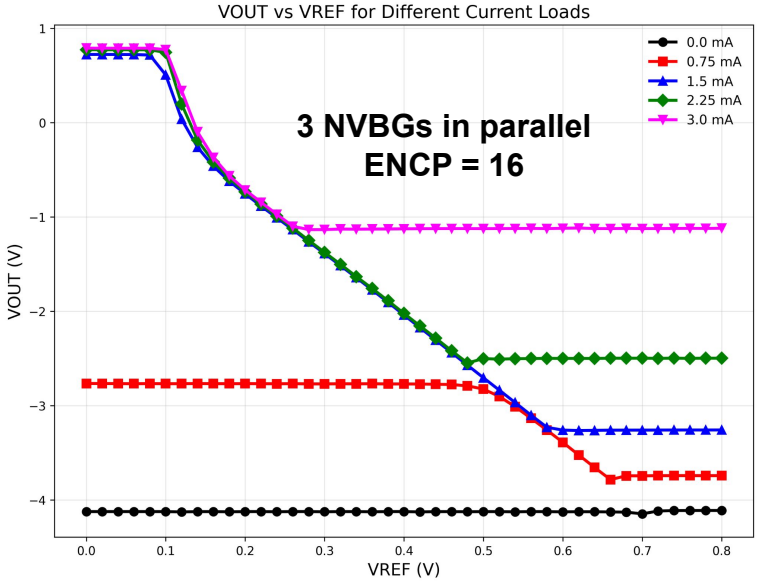


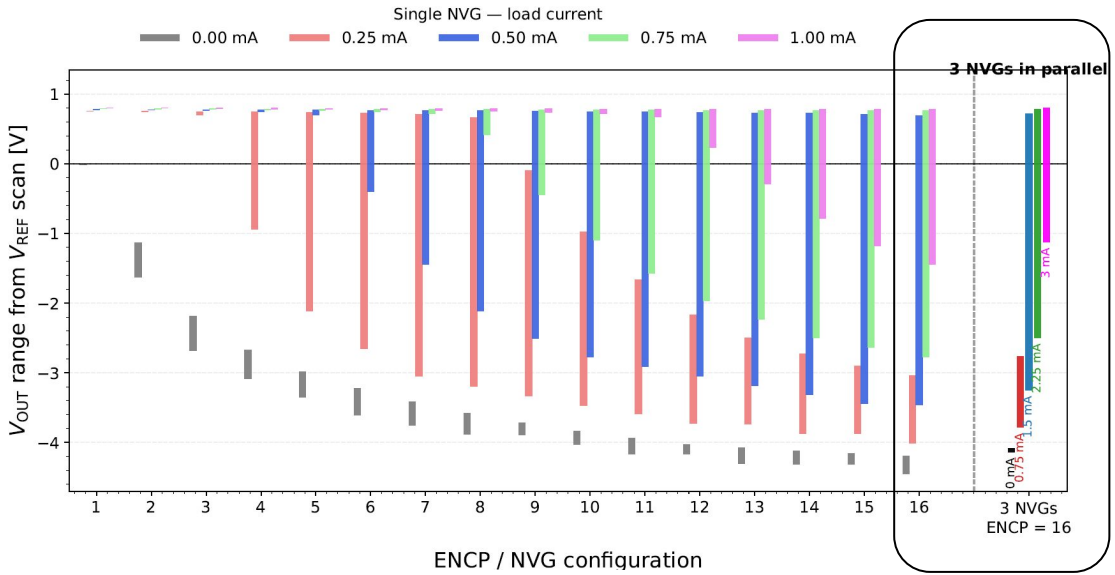
- To handle higher load currents multiple NVBGs can be connected in parallel
- Three NVBGs in parallel (one in closed loop and another two in open loop)
- v1p2 outputs of all NVBG separate, but Vout shorted together
- Vc from the closed-loop NVBG → external control for the open-loop NVBGs
- Test with load current increased up to 3 times the single-NVBG to evaluate parallel operation performance

I2C Configuration: Ioff, Ivco, Iint = 0000111
EN_NVG1 = 111, EN_NVG2 = 011, EN_NVG3 = 011
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 1 MHz
C_L = 1 nF

Negative Voltage Generator

Closed-loop and 2 opened loop NVGs in parallel



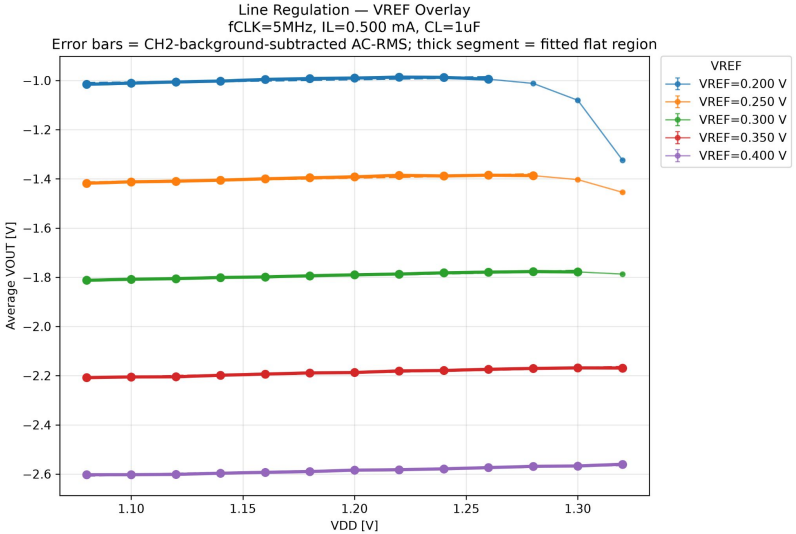


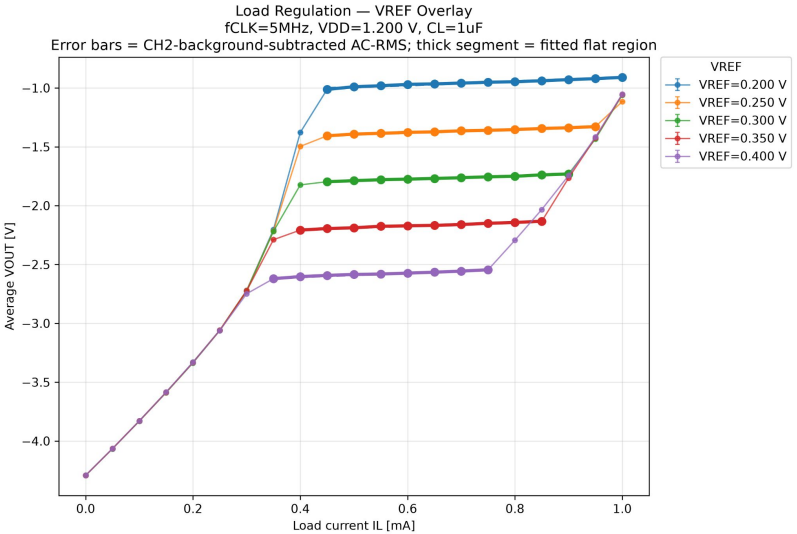
- Parallel operation of three NVBGs extends the load-current capability by 3X while maintaining a VOUT range comparable to a single NVBG
- 6 NVBGs in parallel are implemented in the new chip submission to support up to ~6 mA of load current

Load and Line Regulation

I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
Load: C_L = 1uF
CLK_SC: f_SC = 5 MHz

Negative Voltage Generator





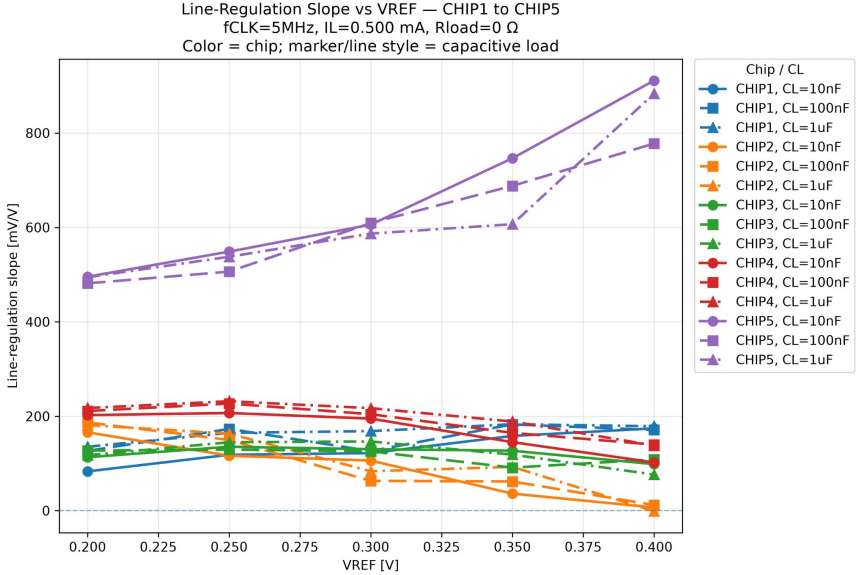
- VREF values within the transition region were selected for load and line regulation measurements.
- **Line regulation:** VDD varied by **±10% around the nominal 1.2 V**, with I_L = 0.5 mA fixed.
- **Load regulation:** I_L varied from **0 to 1 mA**, with VDD fixed at **1.2 V**.

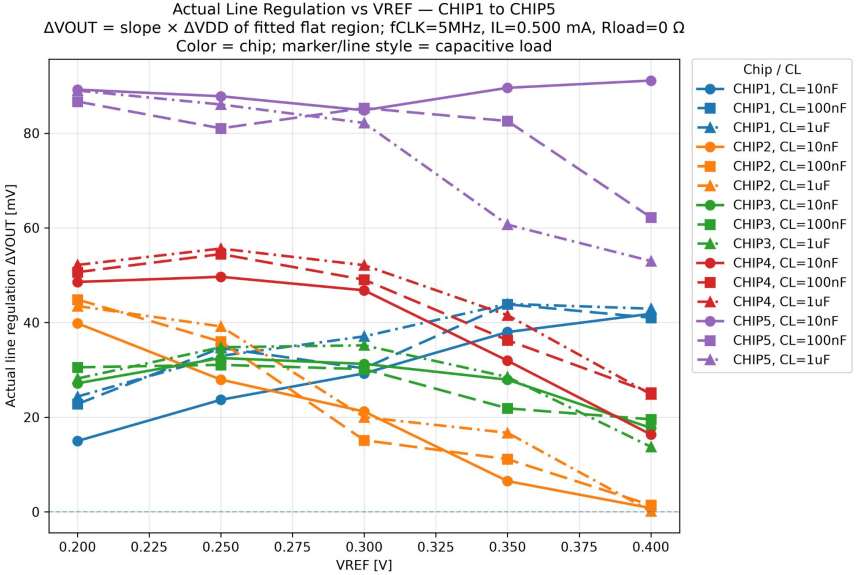
I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz

Negative Voltage Generator

Chip to chip variation

Line regulation





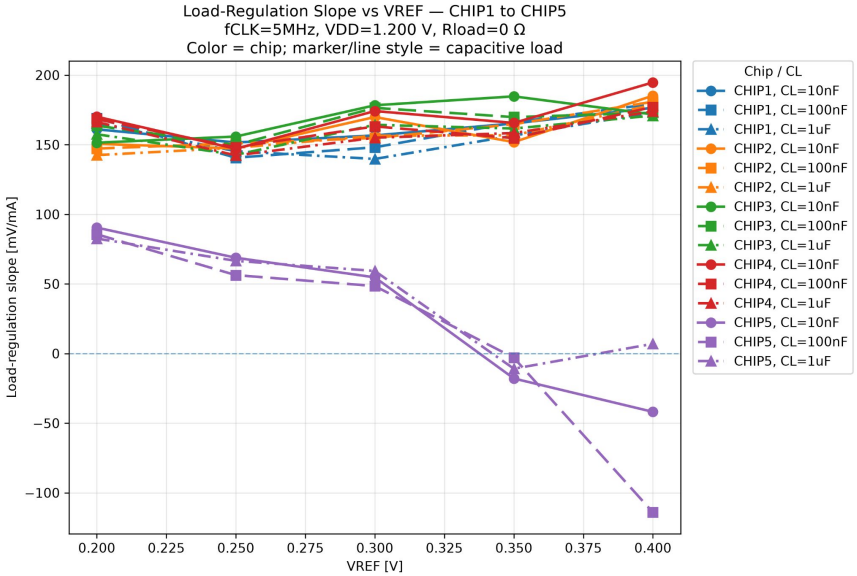
- Line regulation shows no strong dependence on VREF or load capacitance.
- CHIP5 exhibits larger line regulation than the other chips under the same measurement conditions.
- ΔVOUT = line-regulation slope × regulated VDD range estimates the overall VOUT variation within the regulated region, ranging from 0–50 mV across the measured chips.

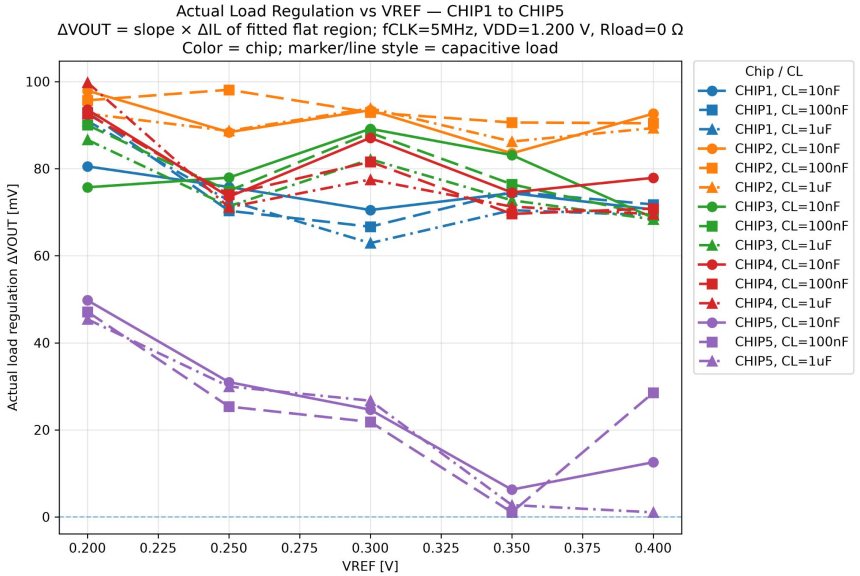
I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz

Negative Voltage Generator

Chip to chip variation

Load regulation



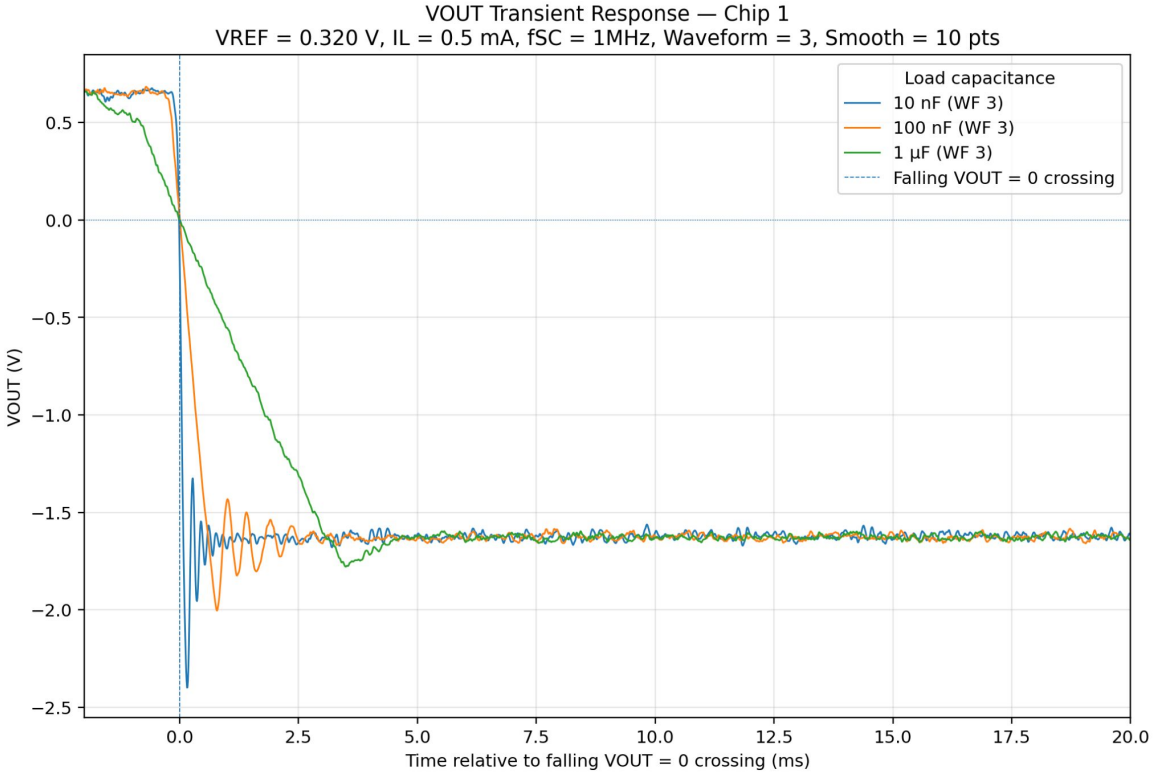


- Load regulation shows no strong dependence on VREF or load capacitance.
- CHIP5 exhibits smaller line regulation than the other chips under the same measurement conditions.
- ΔVOUT, defined as the load-regulation slope × regulated IL range, is used to estimate the overall VOUT variation across the regulated region and ranges from 60–100 mV across the measured chips.

NVBG Transient Response

I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V

Negative Voltage Generator

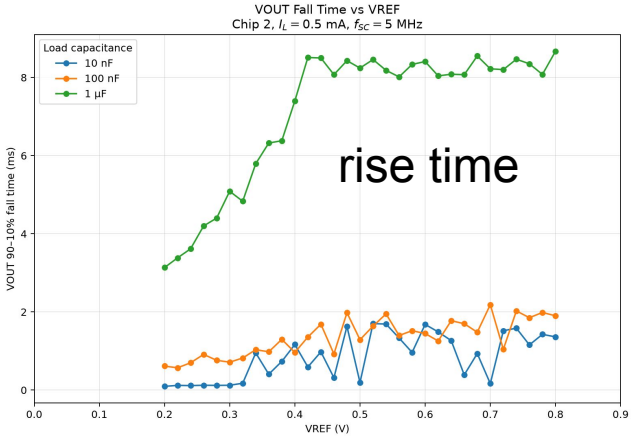


- Smaller C_L provides a faster VOUT transition, but results in larger undershoot and stronger ringing.
- Increasing C_L damps the transient response, significantly reducing undershoot and oscillations.
- This improved stability comes at the cost of a slower transition and longer settling time for larger C_L.

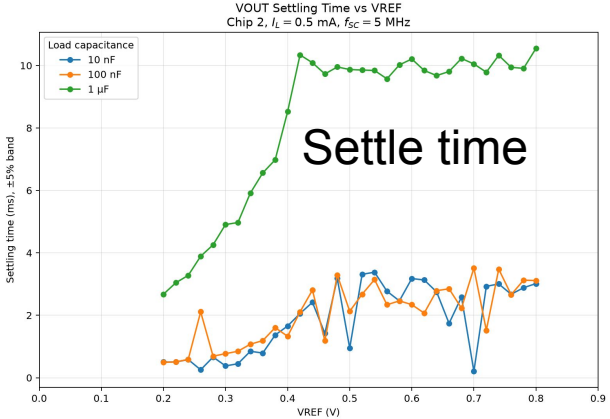
I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V

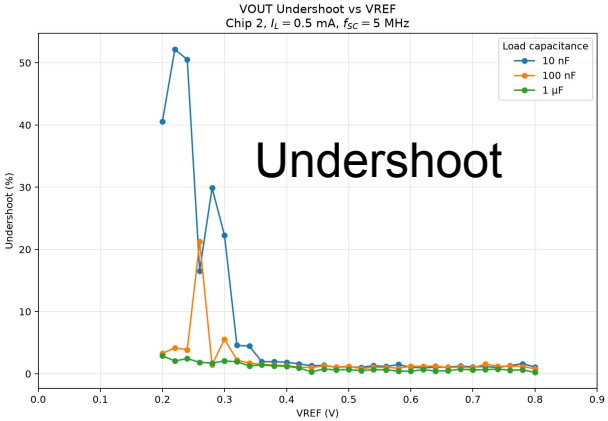
Negative Voltage Generator

10 -90 % of the falling edge



5% band +/- VOUT (steady state)



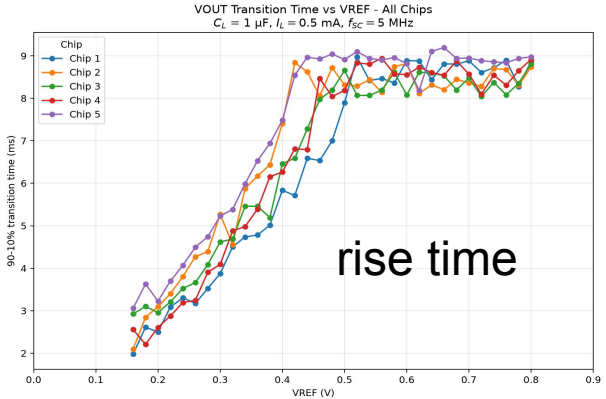


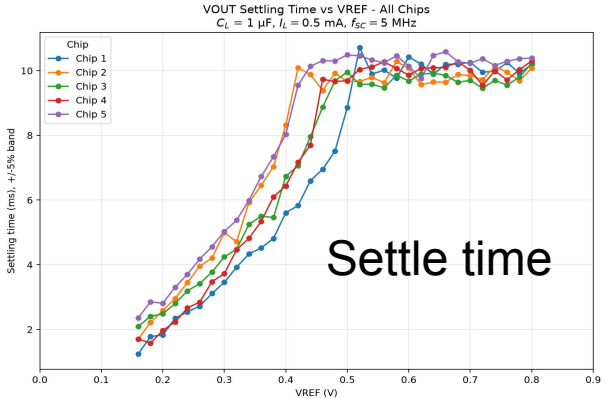
- Larger C_L increases both the 10–90% transition time and settling time, resulting in a slower transient response.
- Smaller C_L provides a faster response, but produces significantly larger undershoot, particularly near the onset of the VOUT−VREF transition region.
- Increasing C_L strongly suppresses the undershoot and oscillatory behavior, giving a more stable output response.

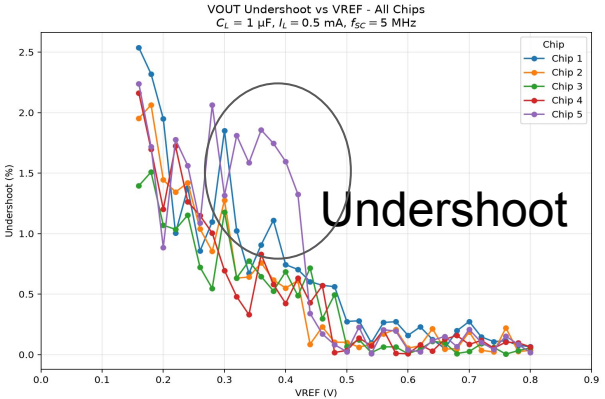
I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
Load: C_L = 1uF
CLK_SC: f_SC = 5 MHz

Negative Voltage Generator

Chip to chip variation







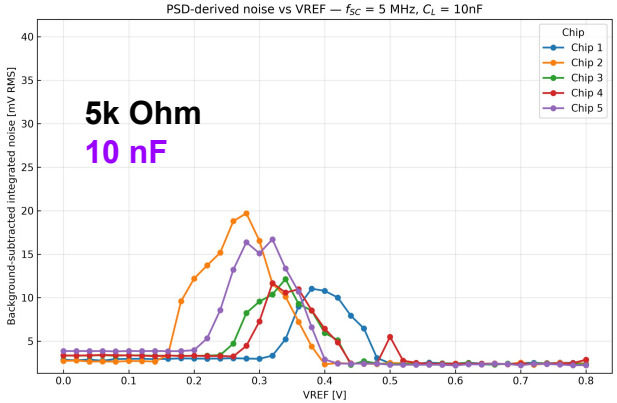
- Rise and settling times show consistent behavior across multiple chips for fixed I_L and C_L = 1 uF, reaching approximately 8–9 ms and 10 ms, respectively, at higher VREF.
- Undershoot decreases with increasing VREF and becomes minimal at higher VREF, indicating an increasingly stable VOUT
- CHIP5 exhibits a larger undershoot than the other chips in the transition region.

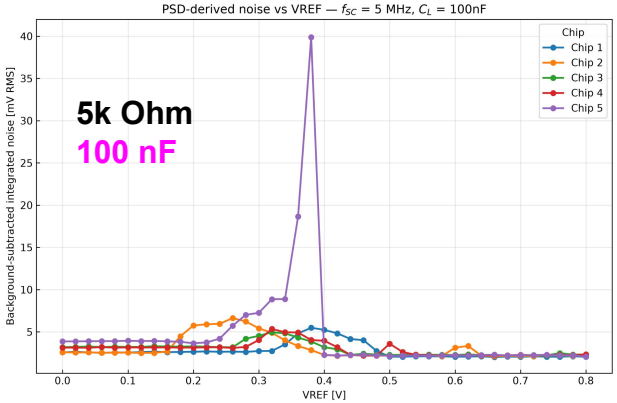
NVBG Noise Characterization

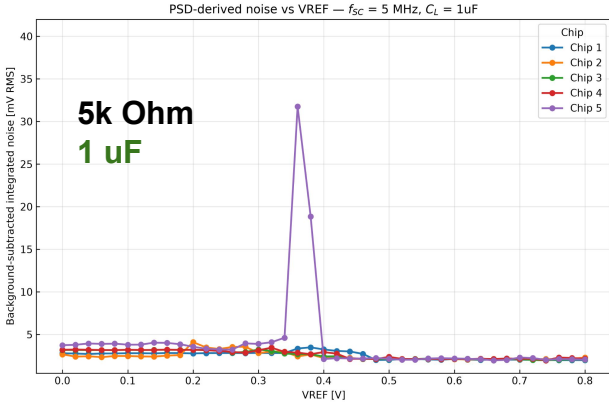
I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz

Negative Voltage Generator

Chip to chip variation







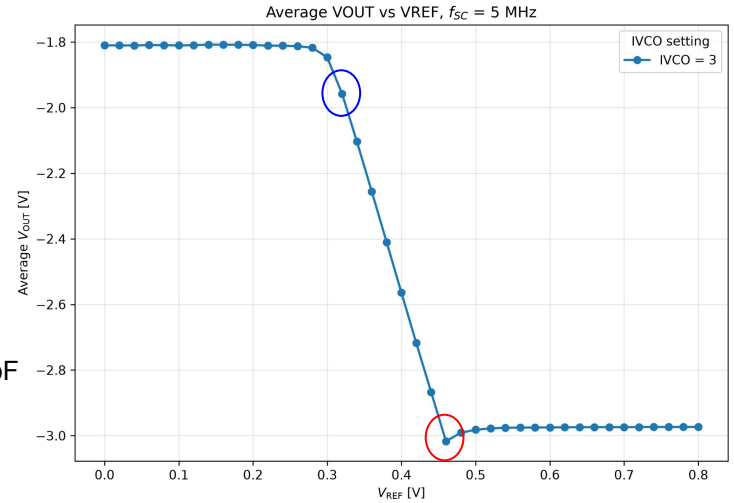
- Noise increases within the VOUT–VREF transition region for all tested chips.
- Increasing C_L strongly suppresses the noise enhancement, from ~10-20 mV at 10 nF to only a few mV at 1 µF
- CHIP5 shows larger noise value for both 100 nF and 1 uF capacitive loads
- At 10 nF, larger chip-to-chip variation is observed in both the peak noise and its VREF position.
- With larger C_L, the noise behavior becomes more uniform across chips, with only small chip-to-chip variation at 1 µF.

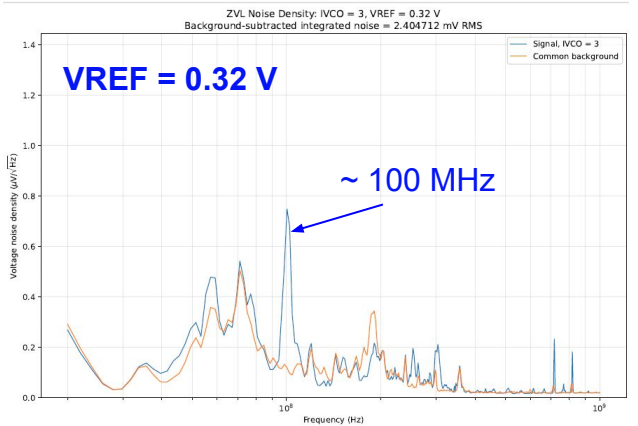
Negative Voltage Generator

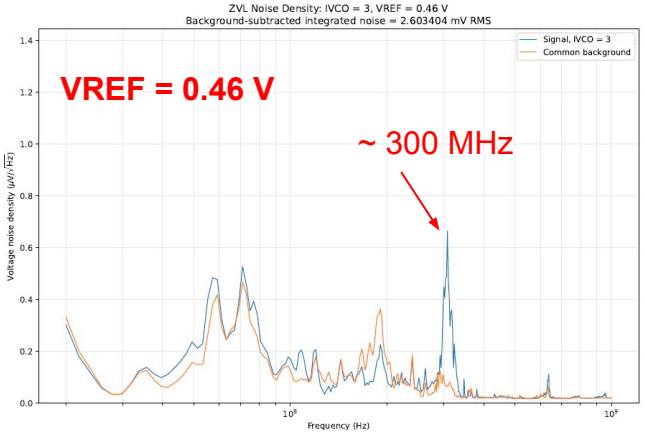
I2C Configuration: EN_CP = 16
Load: C_L = 1uF, R_L = 5k Ohm
CLK_SC: f_SC = 5 MHz
20 MHz hardware bandwidth limit: OFF

R&S ZVL Network Analyzer
Measured 20 MHz - 1GHz
RBW = 3 MHz

Tektronix P6201
Bandwidth 900 MHz
Attenuation × 1
Output impedance 50 Ω
Input impedance 100 kΩ // 3 pF





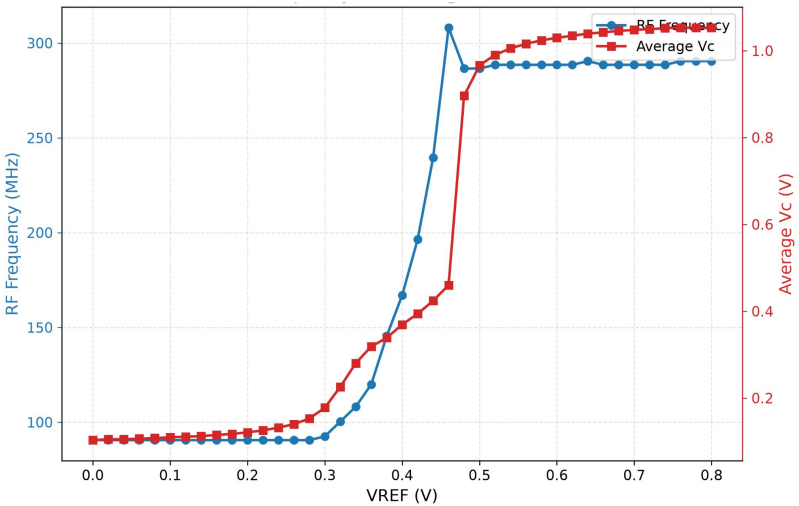


- R&S ZVL Network Analyzer used for noise spectral density measurements (20 MHz–1 GHz).
- Peak noise frequency shifts with VREF in the VOUT–VREF transition region.

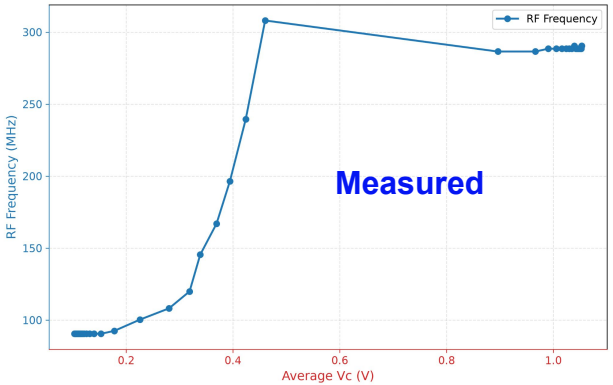
Negative Voltage Generator

I2C Configuration: EN_CP = 16
Load: C_L = 1uF, R_L = 5k Ohm
CLK_SC: f_SC = 5 MHz
20 MHz hardware bandwidth limit: OFF

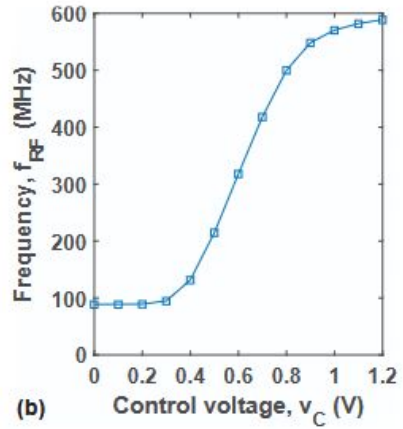
Peak noise frequency and Vc vs VREF



Peak noise frequency vs VREF



simulated tuning curve of VCO
DOI:10.1109/MWSCAS53549.2025.11244383

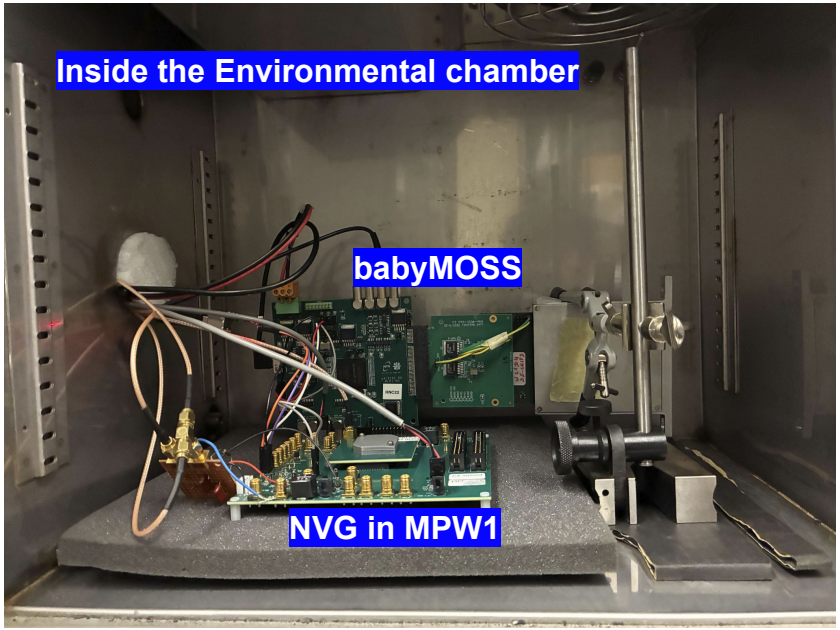


- Peak noise frequency follows a trend similar to simulation results but is limited up to ~300 MHz in the measurement.
- This supports that the dominant peaks observed in the NVG measurement originate from the on-chip VCO.

NVBG + babyMOSS

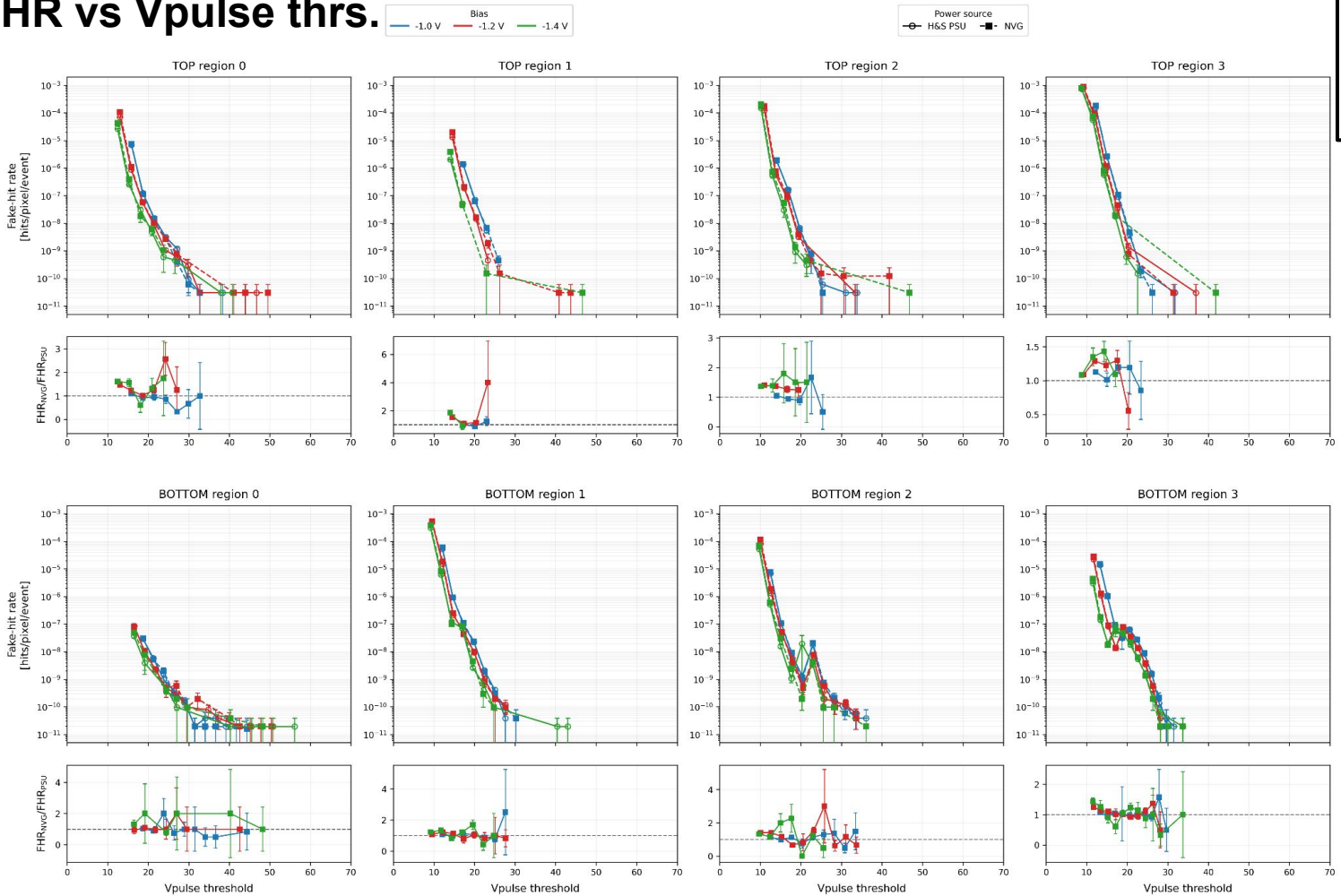
I2C Configuration: EN_CP = 11
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz
C_L = 1 uF

Negative Voltage Generator



- Compared the fake hit rate (FHR) of babyMOSS using the **R&S HMP4040** and **NVG** power supplies.
- Measurements performed at a stable 20°C in an environmental chamber to minimize temperature effects on FHR.
- DC output monitored using an oscilloscope, and noise spectral density monitored using a network analyzer.
- FHR measured for three bias voltages (−1.0, −1.2, and −1.4 V)
- FHR also measured for different capacitive loads at the Vout node.

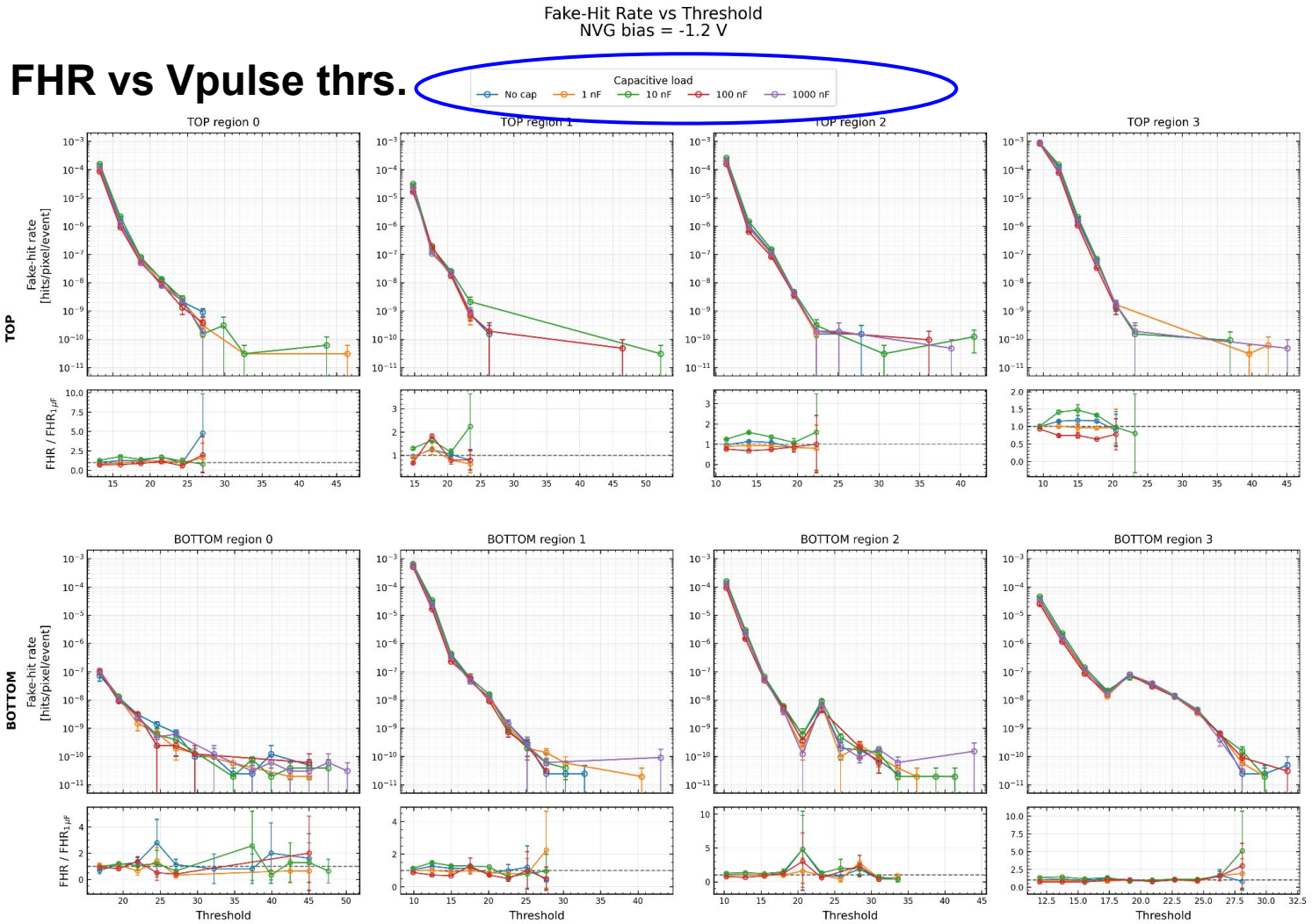
FHR vs Vpulse thrs.



I2C Configuration: EN_CP = 11
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz
C_L = 1 uF

- Fake hit rate (FHR) plotted as a function of Vpulse thresholds for different bias voltages.
- FHR measured with the NVG is in good agreement with that obtained using the R&S HMP4040

FHR vs Vpulse thrs.



I2C Configuration: EN_CP = 11
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz

- FHR measured as a function of Vpulse threshold using the NVG for different capacitive loads.
- FHR remains consistent across the tested capacitive loads, indicating negligible dependence on C_L.

Summary and Outlook

Summary

- Multiple NVGs can be operated in parallel, with one in closed loop and others in open loop, to support higher load current
- Tunable VOUT range of the NVG decreases with increasing temperature
- Dominant high frequency noise peaks observed in the NVG measurement originate from the on-chip VCO.
- Chip-to-chip variation was systematically studied, with all tested chips showing similar overall behavior with CHIP5 being the exception.
- babyMOSS FHR is comparable when biased with the NVG and a conventional power supply

Remaining works

- Measurements of PSRR

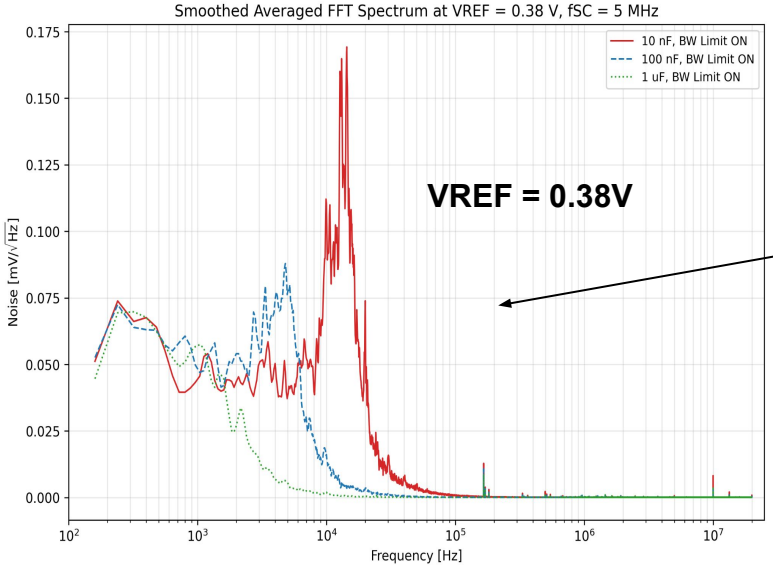
Extra slides

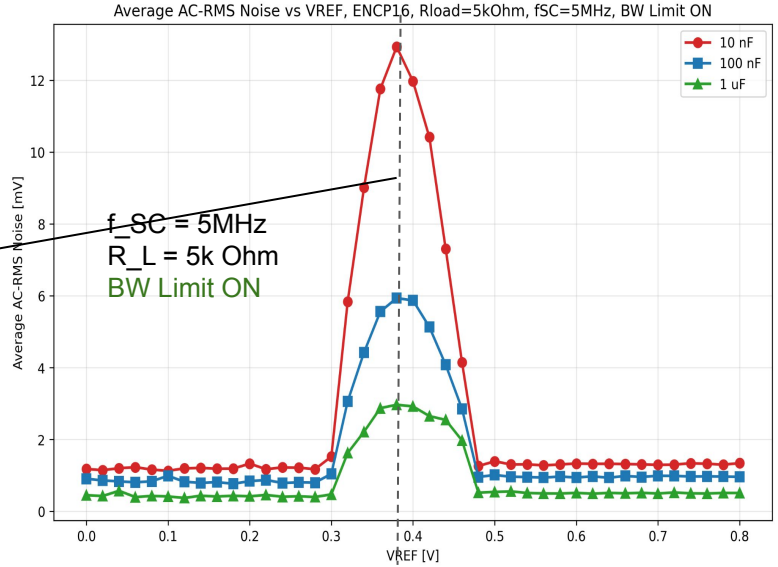
I2C Configuration: EN_CP = 16
Load: C_L = 10nF, 100nF, 1uF, R_L = 5k Ohm
CLK_SC: f_SC = 5 MHz
20 MHz hardware bandwidth limit: ON

Negative Voltage Generator

Noise measurements

Measurement performed with SMA cable





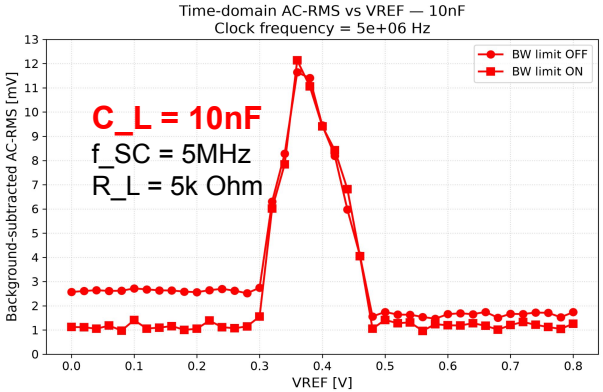
- Larger C_L provides substantial noise reduction at f_SC = 5 MHz
  - Peak AC-RMS noise decreases from ~13 mV (10 nF) to ~6 mV (100 nF) and ~3 mV (1 µF)
- Low-frequency noise component is progressively suppressed as the C_L increases

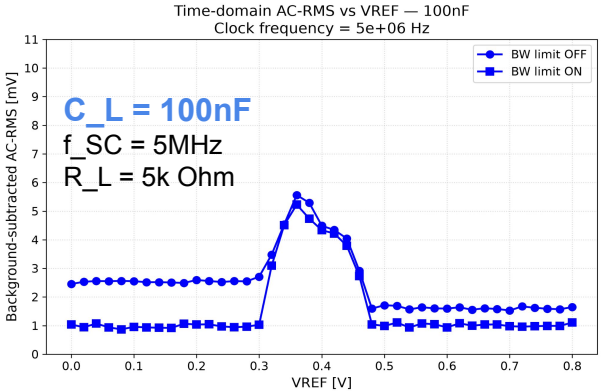
I2C Configuration: EN_CP = 16
Load: C_L = 10nF, 100nF, 1uF, R_L = 5k Ohm
CLK_SC: f_SC = 5 MHz
20 MHz hardware bandwidth limit: ON/OFF

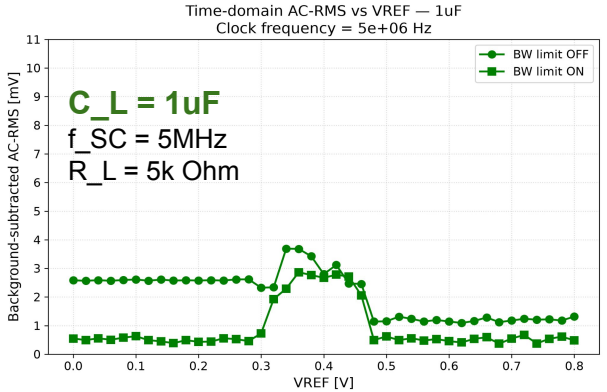
Negative Voltage Generator

Noise measurements

Measurement reperfromed with 500 MHz bandwidth 10:1 passive probe

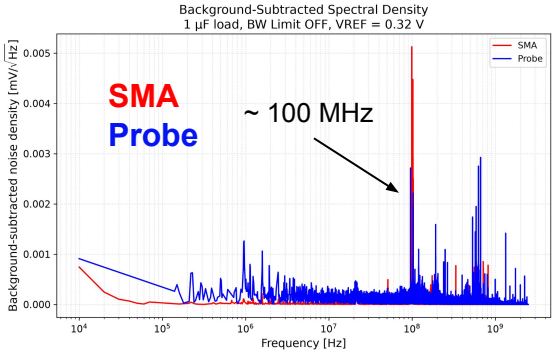






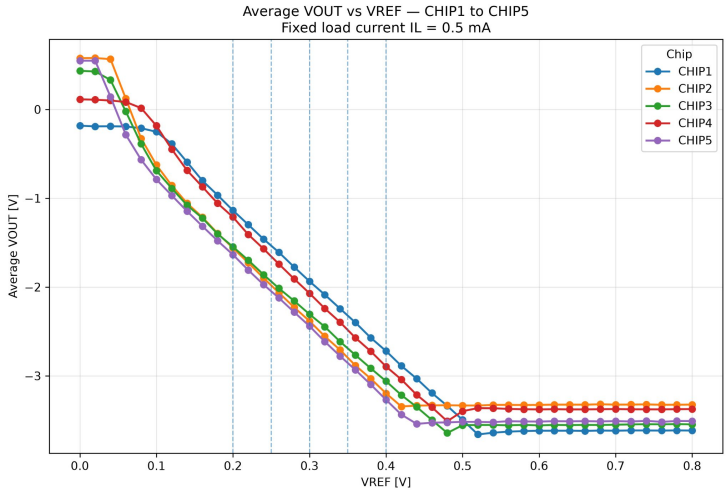
- Larger C_L provides substantial noise reduction at f_SC = 5 MHz even without the 20 MHz oscilloscope bandwidth limit.

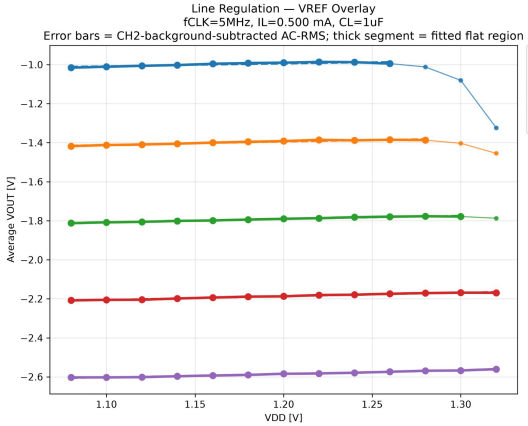
- High-frequency noise components are visible in the noise spectral domain

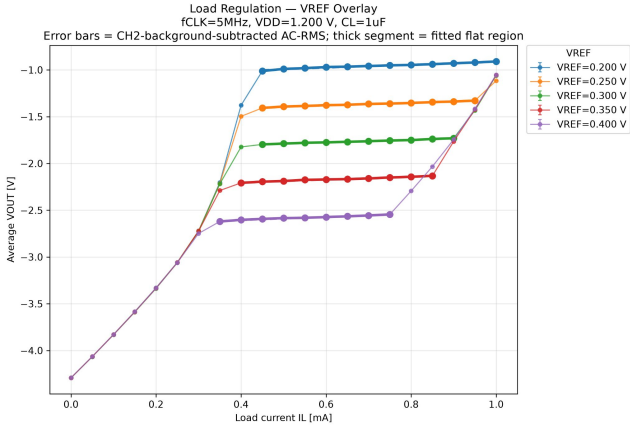


I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
Load: C_L = 1uF
CLK_SC: f_SC = 5 MHz

Negative Voltage Generator





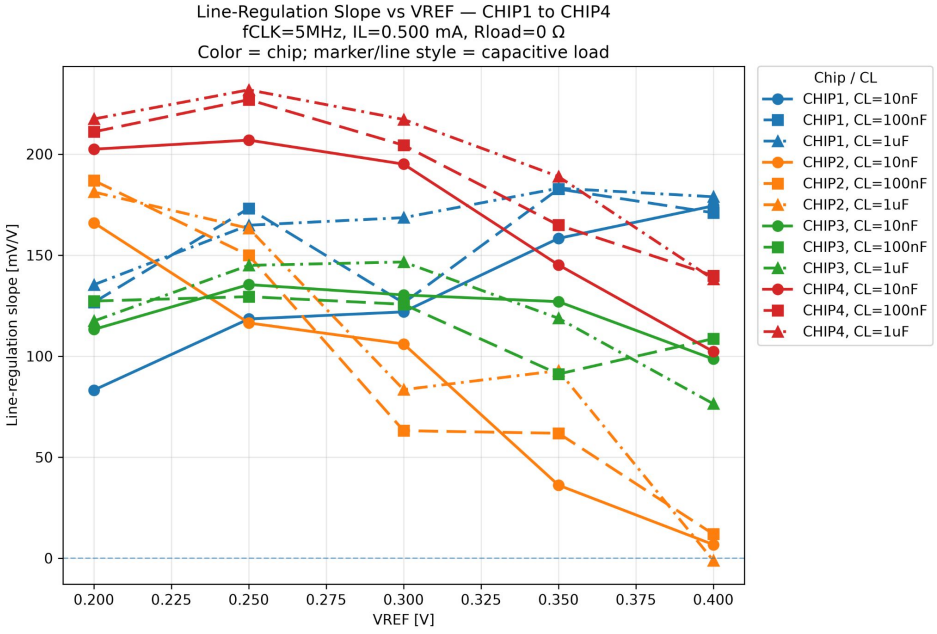


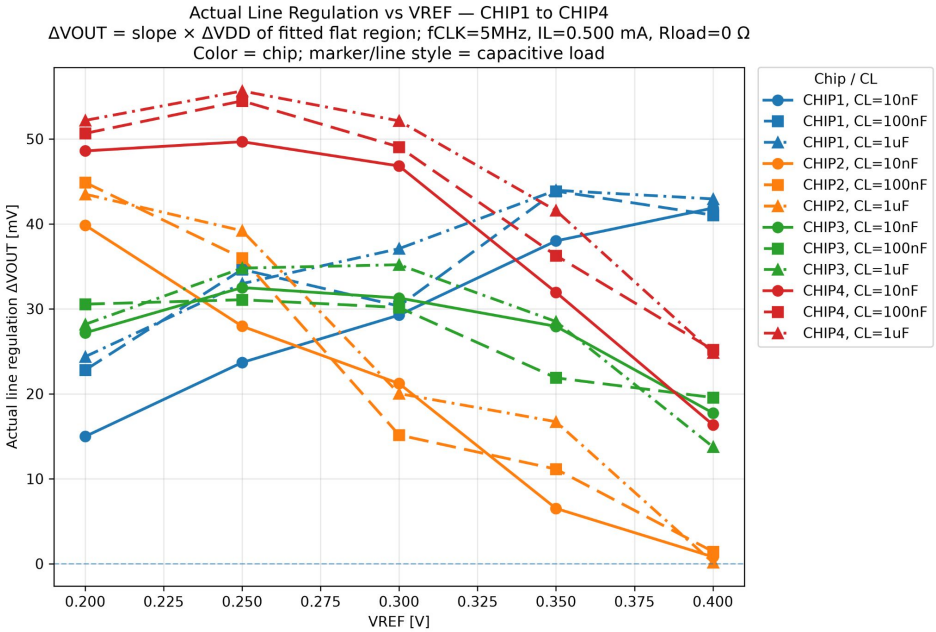
- VOUT follows VREF approximately linearly before reaching the lower output-voltage limit.
- VREF values within the transition region were selected for load and line regulation measurements.
- CHIP5 exhibited anomalously high noise and was therefore excluded from the chip-to-chip comparison.

I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz

Negative Voltage Generator

Line regulation



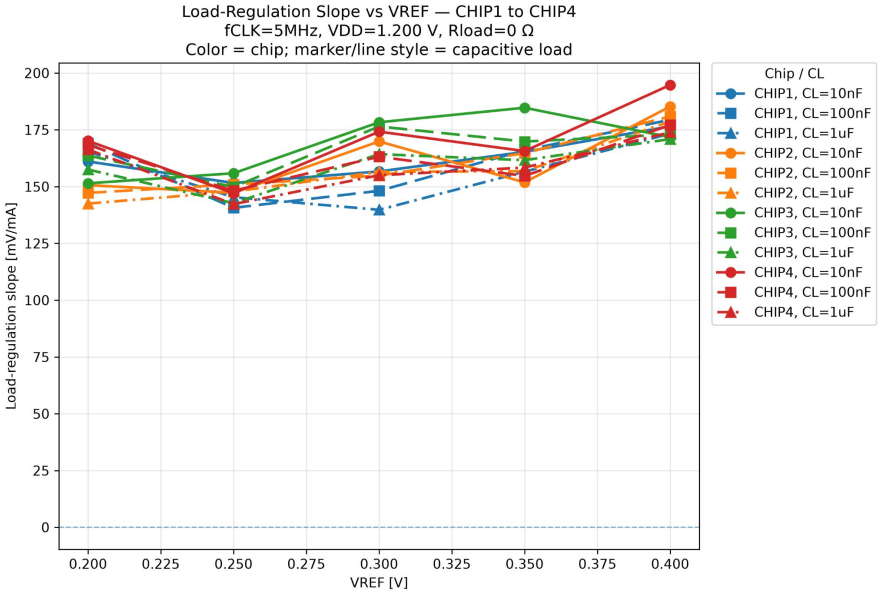


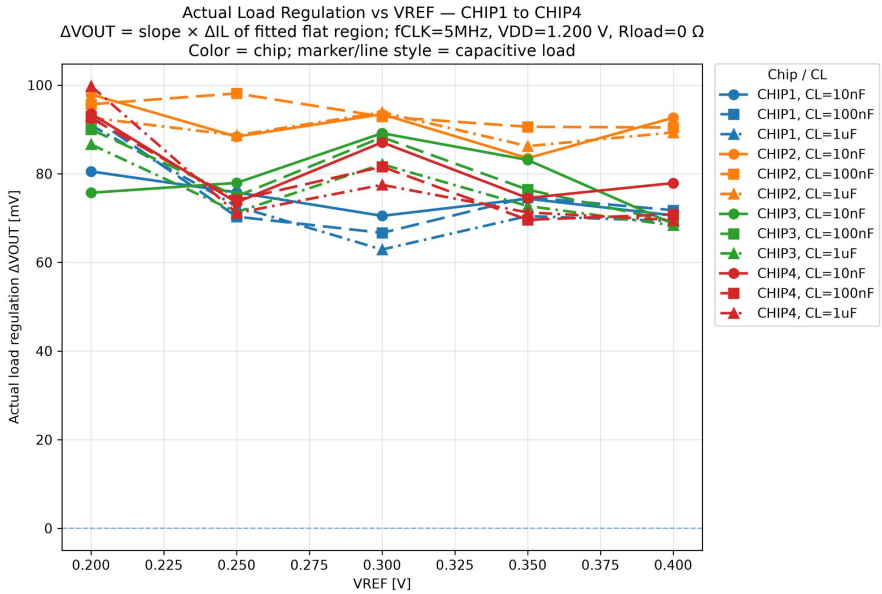
- Line regulation shows no strong dependence on VREF or load capacitance.
- ΔVOUT, defined as the line-regulation slope × regulated VDD range, is used to estimate the overall VOUT variation across the regulated region and ranges from 0–50 mV across the measured chips.

I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz

Negative Voltage Generator

Load regulation



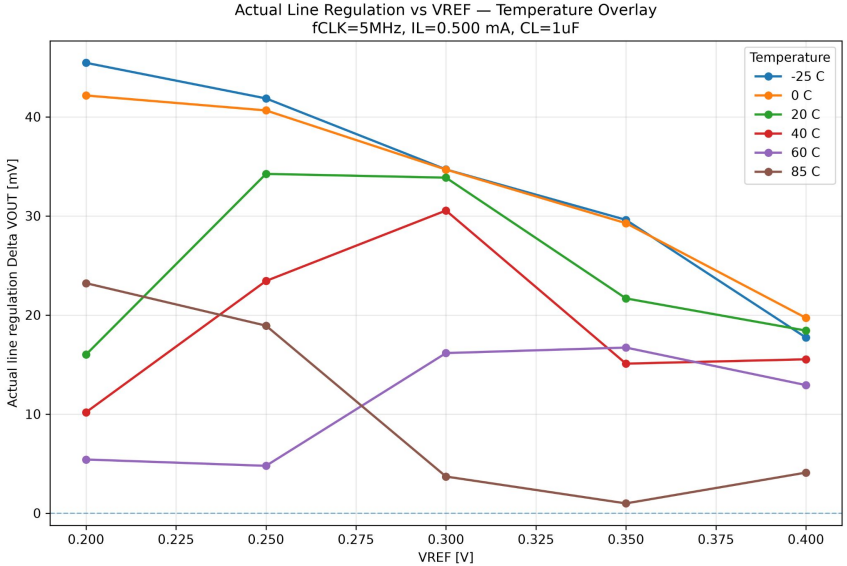


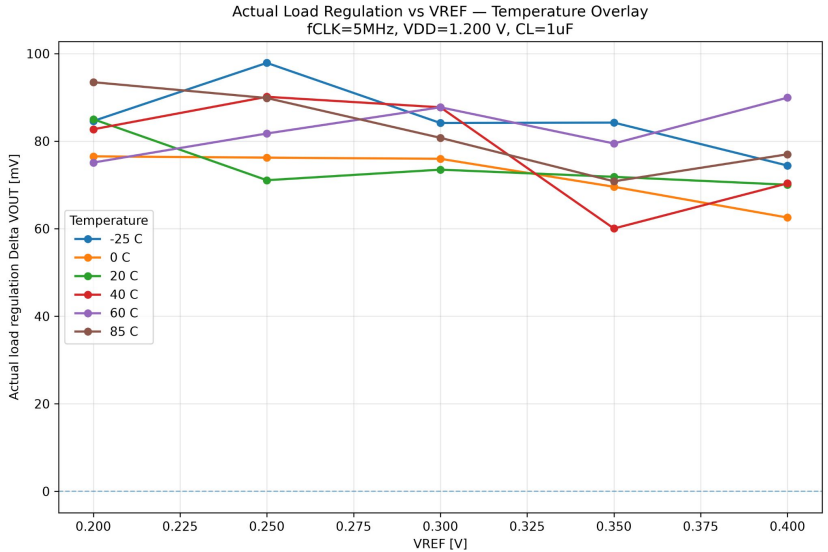
- Load regulation shows no strong dependence on VREF or load capacitance.
- ΔVOUT, defined as the load-regulation slope × regulated IL range, is used to estimate the overall VOUT variation across the regulated region and ranges from 60–100 mV across the measured chips.

I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
Load: C_L = 1uF
CLK_SC: f_SC = 5 MHz

Negative Voltage Generator

Line/load regulation



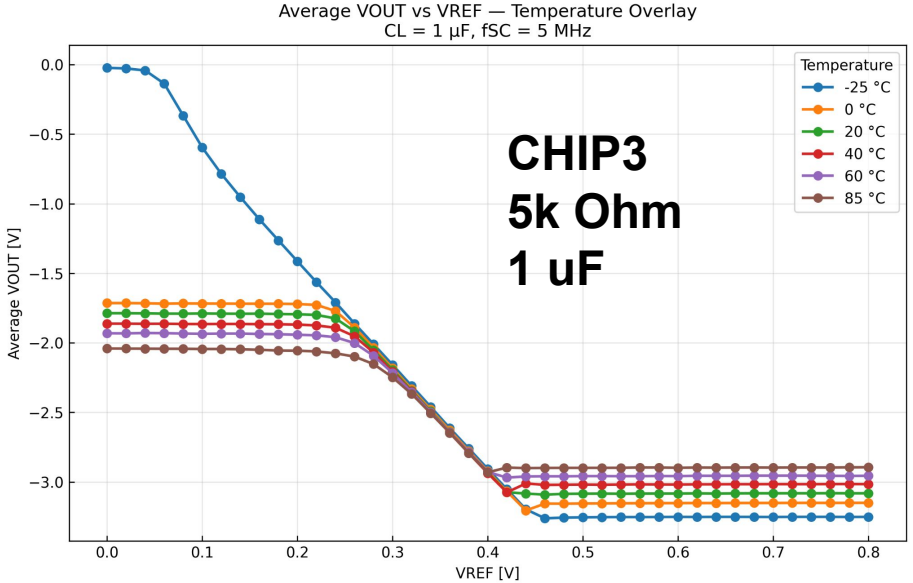


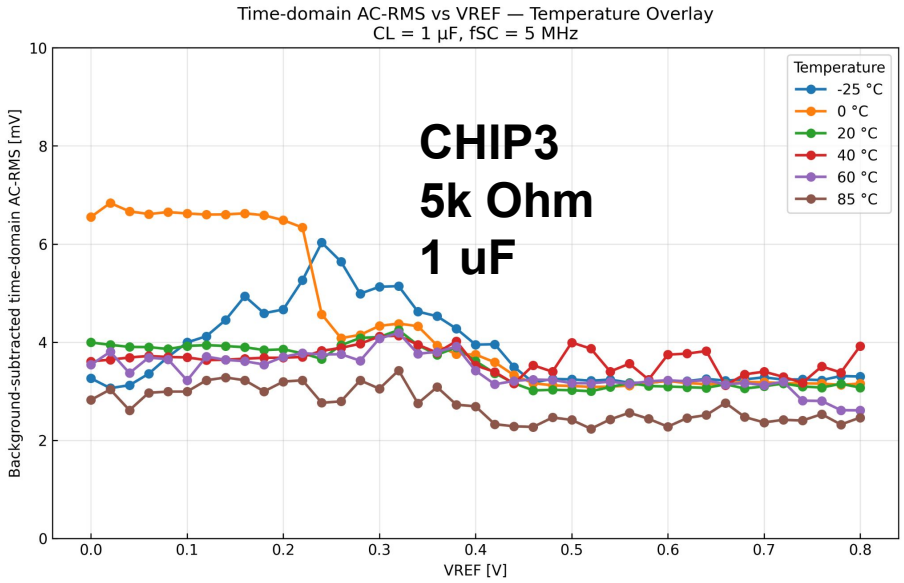
- Line and load regulation show no strong dependence on VREF or temperature.
- **Line regulation:** ΔVOUT remains within approximately 0–50 mV across the temperature range, consistent with the spread observed across multiple chips at room temperature.
- **Load regulation:** ΔVOUTremains within approximately 60–100 mV across the temperature range, also consistent with the room-temperature chip-to-chip variation.

I2C Configuration: EN_CP = 16
EN = 111, Ioff, Ivco, Iint = 0000111
CLK_SC: 1.2Vpp Square
Power: GNDi = -5 V, VDDi = -5 V
CLK_SC: f_SC = 5 MHz

Negative Voltage Generator

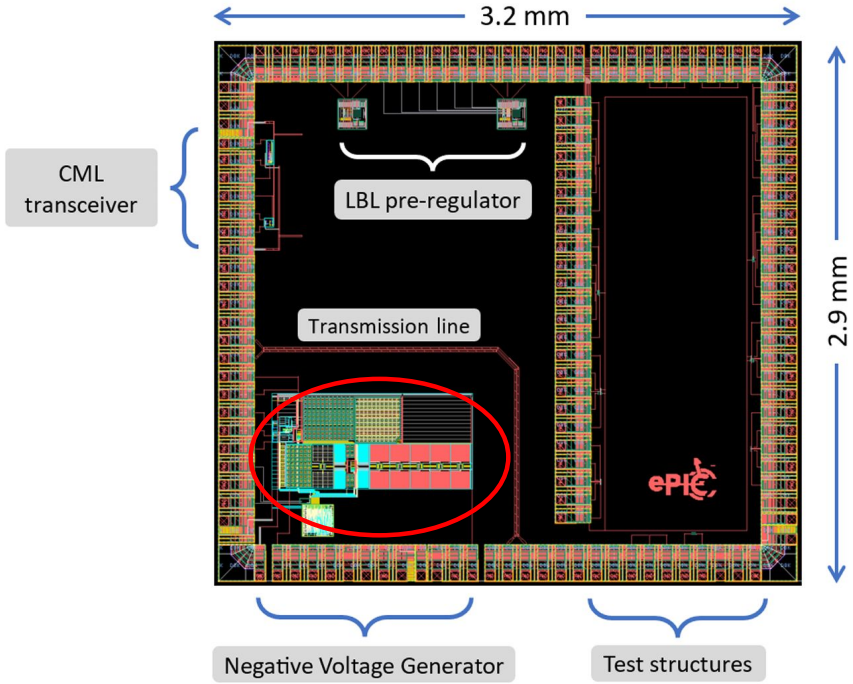
Noise





- The VOUT operating range shifts with temperature, while the transition region remains broadly similar.
- The noise level shows a clear temperature dependence, with larger variation at lower temperatures.
- At higher temperatures, the noise is generally lower and shows weaker dependence on VREF.

AncASIC MPW1



- ❑ A passthrough differential transmission line
- ❑ Current-mode logic (CML) transmitter and receiver
- ❑ SLDO Pre-regulator
- ❑ An I2C controller
- ❑ Negative voltage bias generator (NVBG)
- ❑ Test devices (MOSFET, BJT, resistor, etc.)

Instrument:

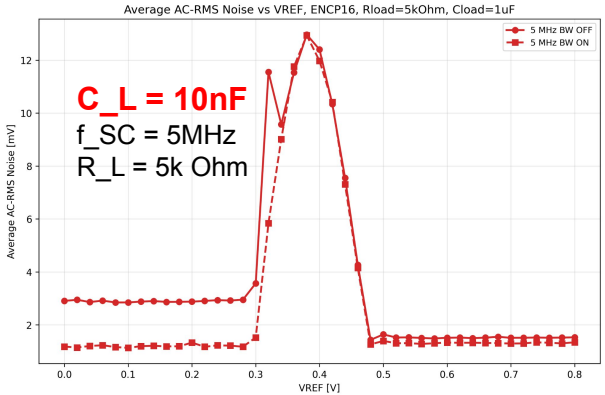
- Power supply for VDD
- Power supply for VREF
- Oscilloscope
- Clock generator for CLK_SC
- Signal generator for power VDD with ripple
- Environmental chamber for temperature test

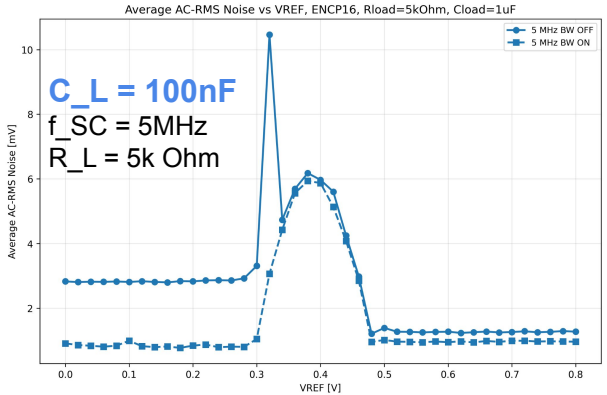
I2C Configuration: EN_CP = 16
Load: C_L = 10nF, 100nF, 1uF, R_L = 5k Ohm
CLK_SC: f_SC = 5 MHz
20 MHz hardware bandwidth limit: ON/OFF

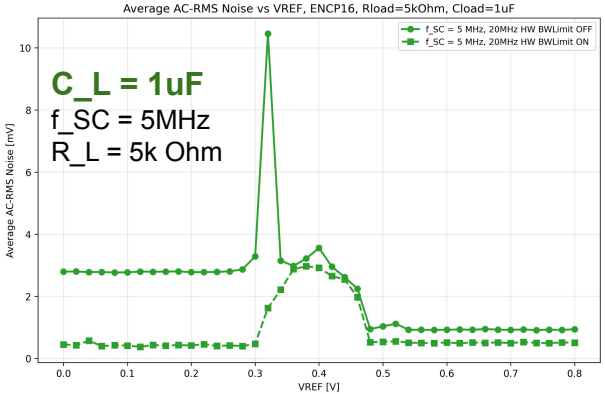
Negative Voltage Generator

Noise measurements

From last WP2 presentation (06.29.2026) - slide 17







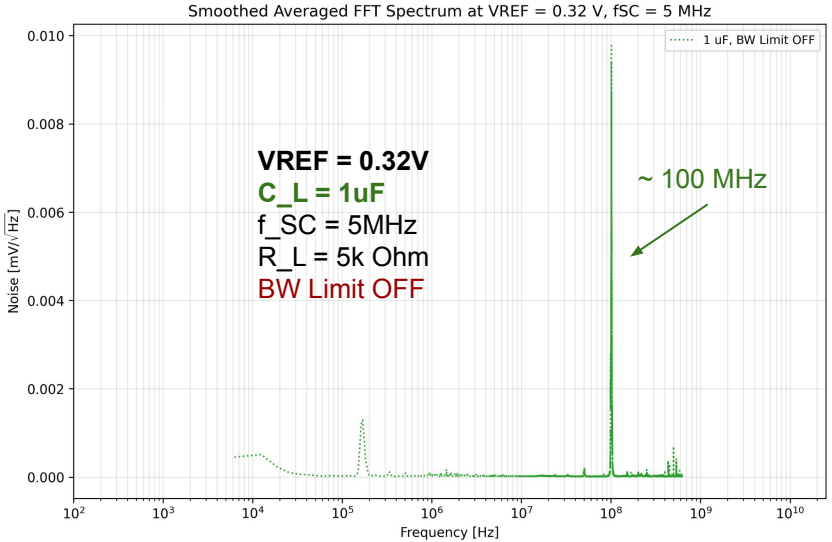
- 20 MHz oscilloscope bandwidth limit ON, at optimal f_SC, the noise peaks for 10 nF: ~13 mV, 100 nF: ~6 mV, 1 µF: ~3 mV
- A sharp spike in noise at the onset of VOUT-VREF transition region (VREF = 0.32 V in this case) when 20 MHz oscilloscope bandwidth limit OFF
- Noise spectral density reveals presence of ~ 100 MHz noiset at VREF = 0.32 V

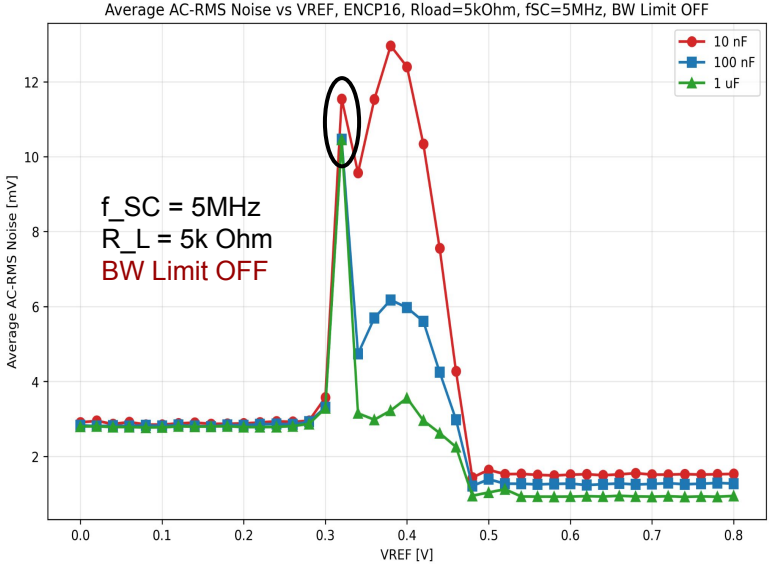
I2C Configuration: EN_CP = 16
Load: C_L = 10nF, 100nF, 1uF, R_L = 5k Ohm
CLK_SC: f_SC = 5 MHz
20 MHz hardware bandwidth limit: OFF

Negative Voltage Generator

Noise measurements

Measurement performed with SMA cable



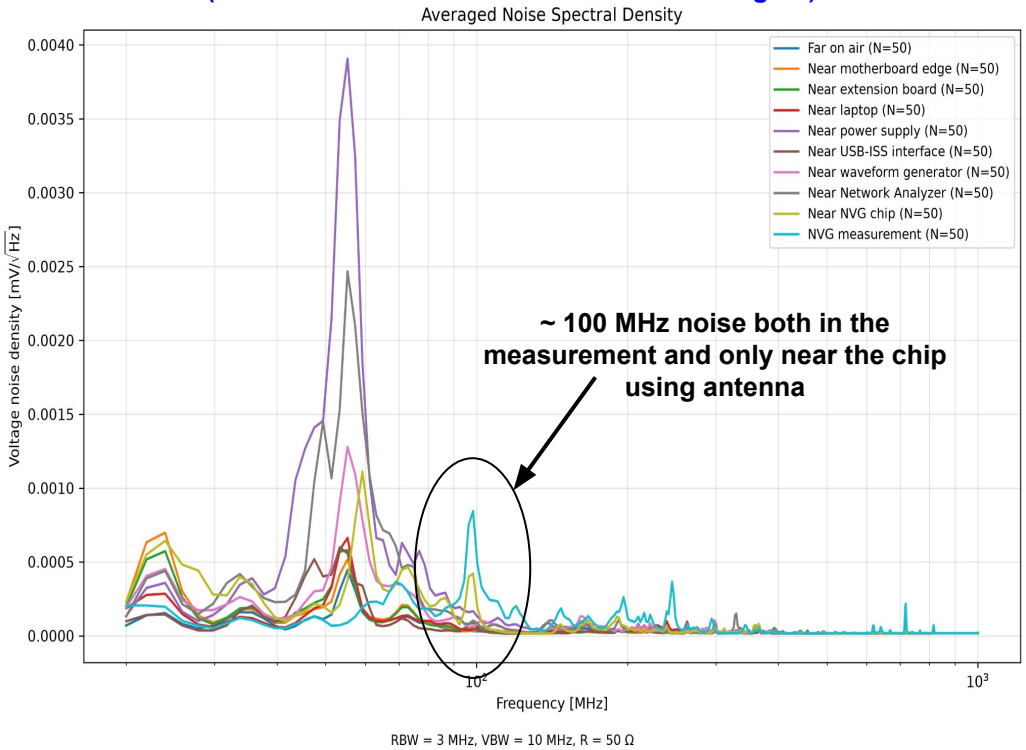


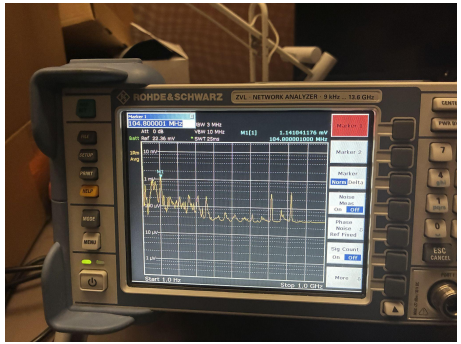
- Sharp peak near ~ 100 MHz noise and the noise amplitude likely enhanced
  - due to impedance mismatch between 50 Ohm SMA and 1MOhm oscilloscope termination
- Test performed with 500 MHz bandwidth 10:1 passive probe (10 MΩ input resistance)

Negative Voltage Generator

Noise measurements

VREF = 0.32 V
(at the start of the VOUT-VREF transition region)



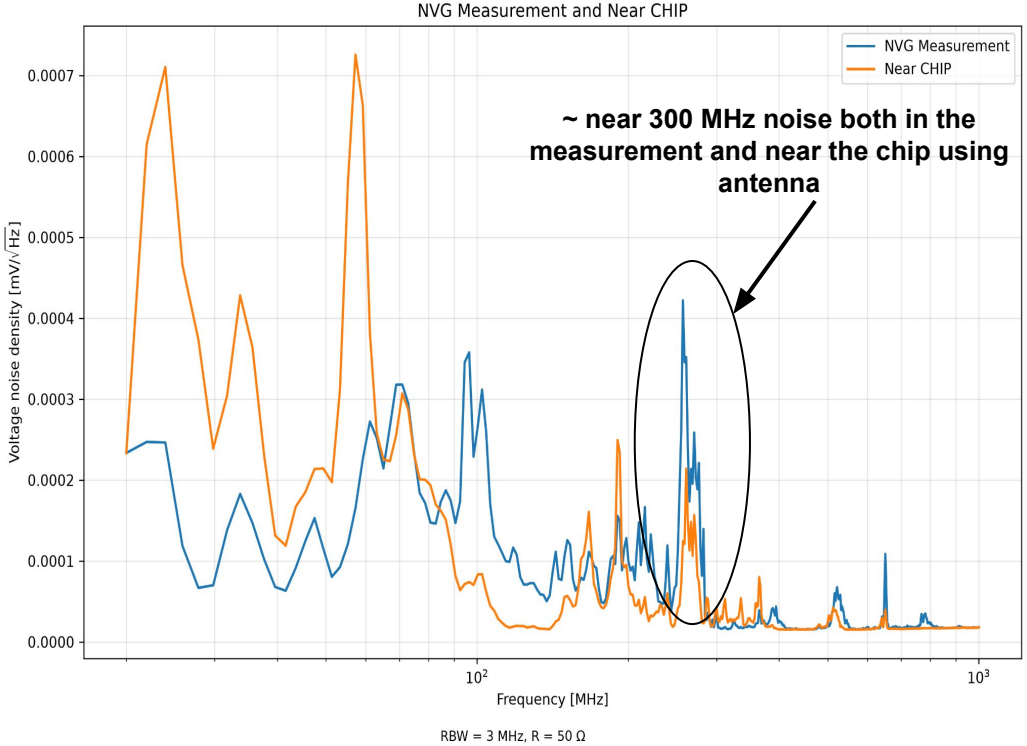


- **Near-chip with antenna:** Measured spectral peaks are consistent with the dominant frequency observed in the NVG noise spectrum.
- **Near electrical instruments:** An additional ~55 MHz spectral peak is detected, which is not prominent in the NVG measurement and is of unknown origin.
- This supports that the dominant peaks observed in the NVG measurement originate from the on-chip VCO.

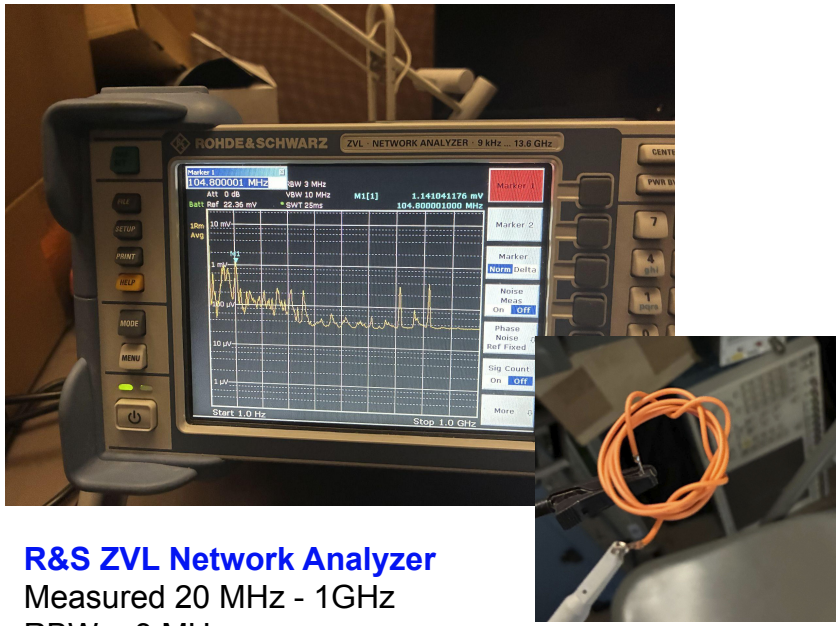
I2C Configuration: Closed Loop, Int. Vc, Main/Aux. CP ON, Ioff, Ivco, Iint = 0000111, EN_CP = 16
Load: C_L = 1uF, R_L = 5k Ohm
CLK_SC: f_SC = 5 MHz, 1.2Vpp Square
Power: VDD = 1.2 V, GNDi = -5 V, VDDi = -5 V

Measurement with Antenna

VREF = 0.46 V
(at the end of the VOUT-VREF transition region)



I2C Configuration: Closed Loop, Int. Vc, Main/Aux. CP ON, Ioff, Ivco, Iint = 0000111, EN_CP = 16
Load: C_L = 1uF, R_L = 5k Ohm
CLK_SC: f_SC = 5 MHz, 1.2Vpp Square
Power: VDD = 1.2 V, GNDi = -5 V, VDDi = -5 V



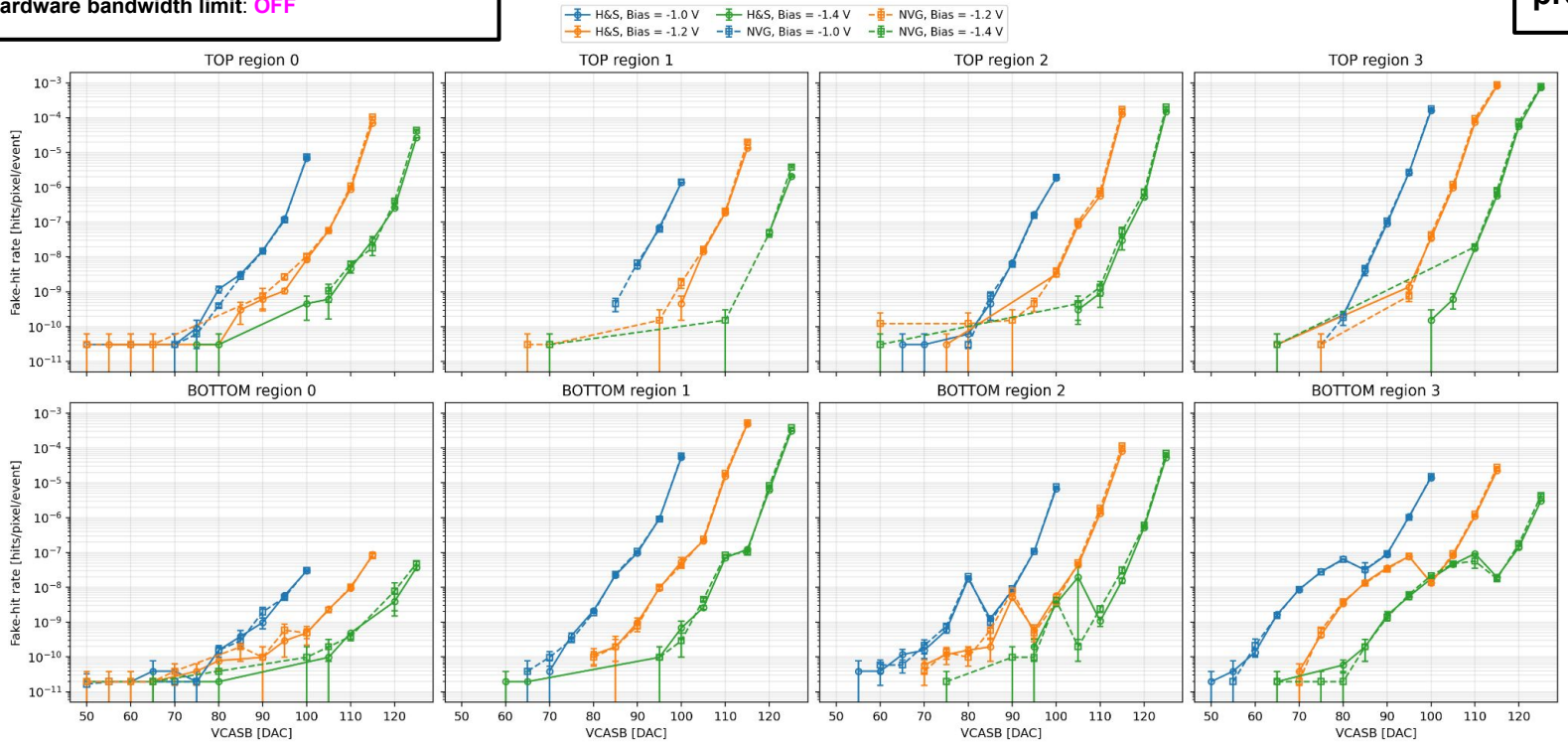
R&S ZVL Network Analyzer
Measured 20 MHz - 1GHz
RBW = 3 MHz
50 Traces with 1 sec sweep time
Averaged trace extracted

Tektronix P6201
Bandwidth 900 MHz
Attenuation × 1
Output impedance 50 Ω
Input impedance 100 kΩ // 3 pF

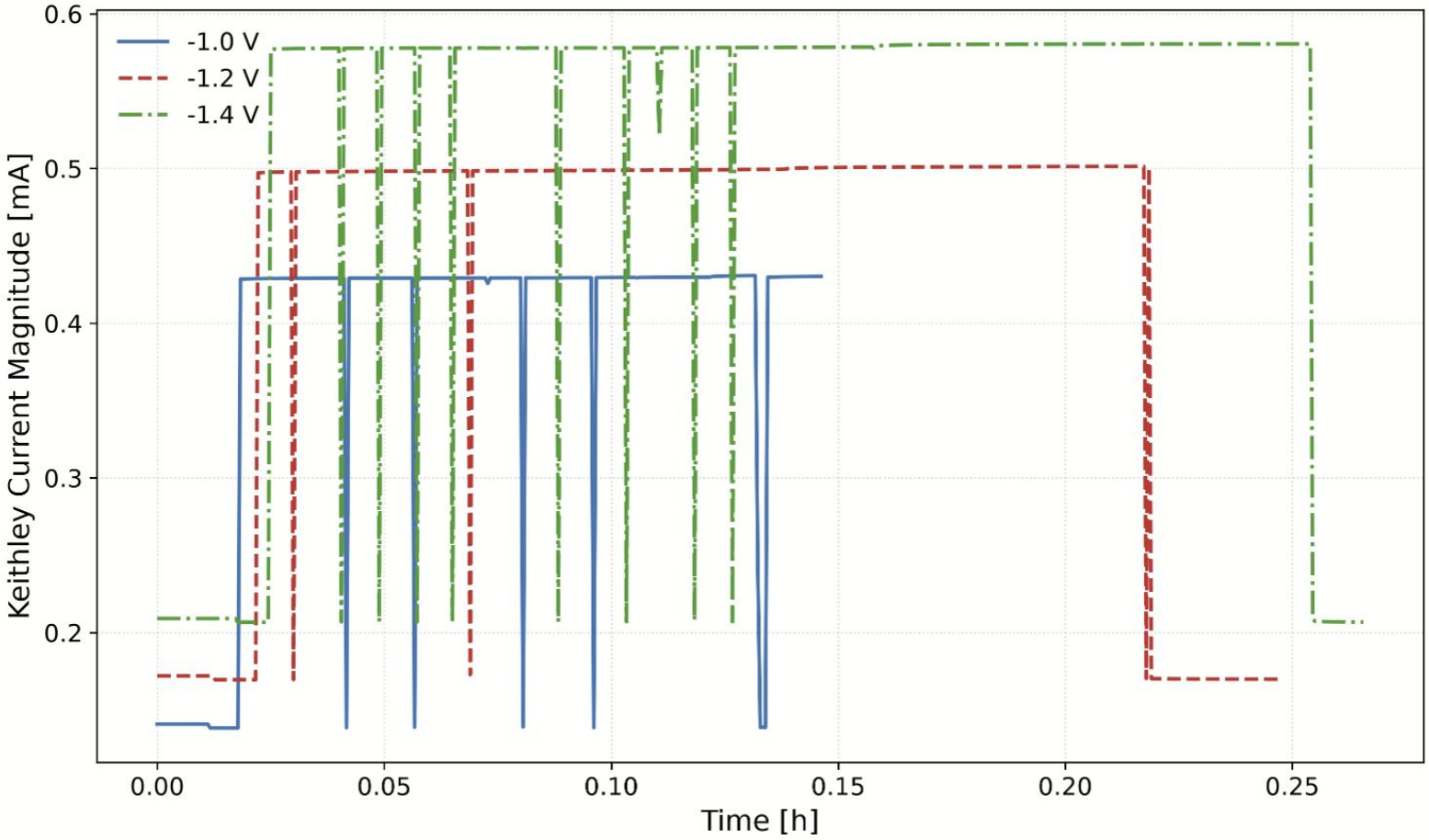
I2C Configuration: EN_CP = 16
Load: C_L = 1uF, R_L = 5k Ohm
CLK_SC: f_SC = 5 MHz
20 MHz hardware bandwidth limit: OFF

Negative Voltage Generator

preliminary

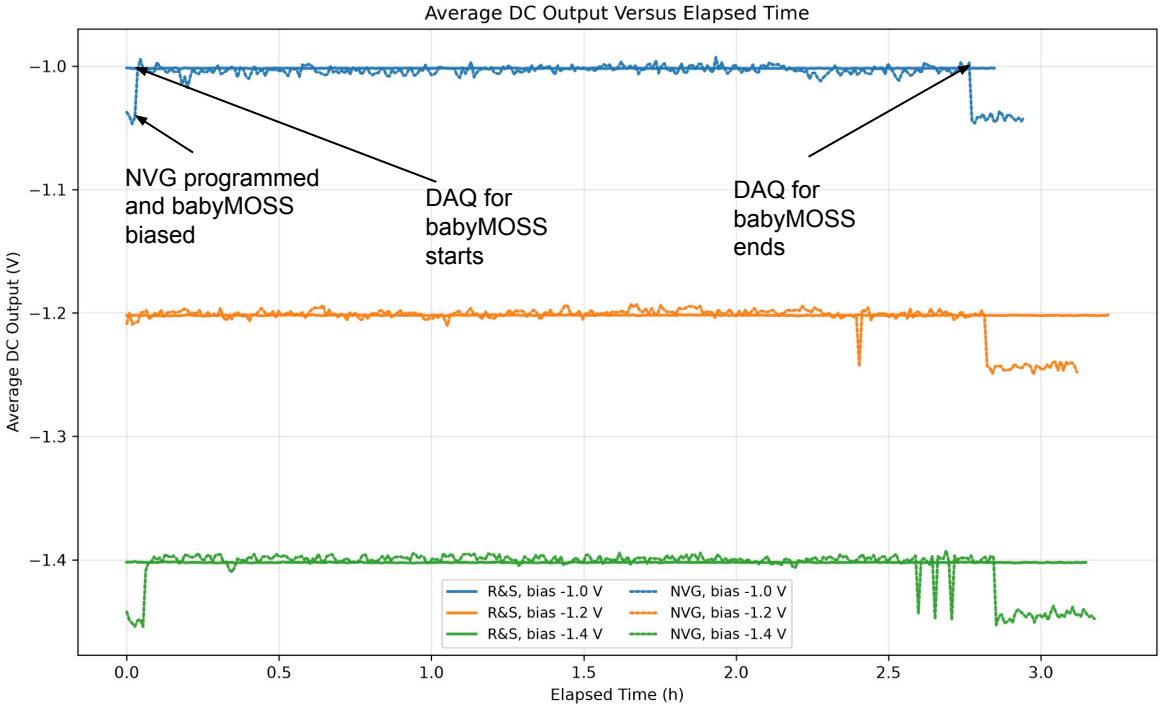


- Fake hit rate (FHR) was measured as a function of VCASB using the NVG for different bias voltages.
- FHR measured with the NVG is in good agreement with that obtained using the R&S HMP4040 across VCASB and different biases


-1.0 V
-1.2 V
-1.4 V
Keithley Current Magnitude [mA]
0.6
0.5
0.4
0.3
0.2
0.00
0.05
0.10
0.15
0.20
0.25
Time [h]

Negative Voltage Generator

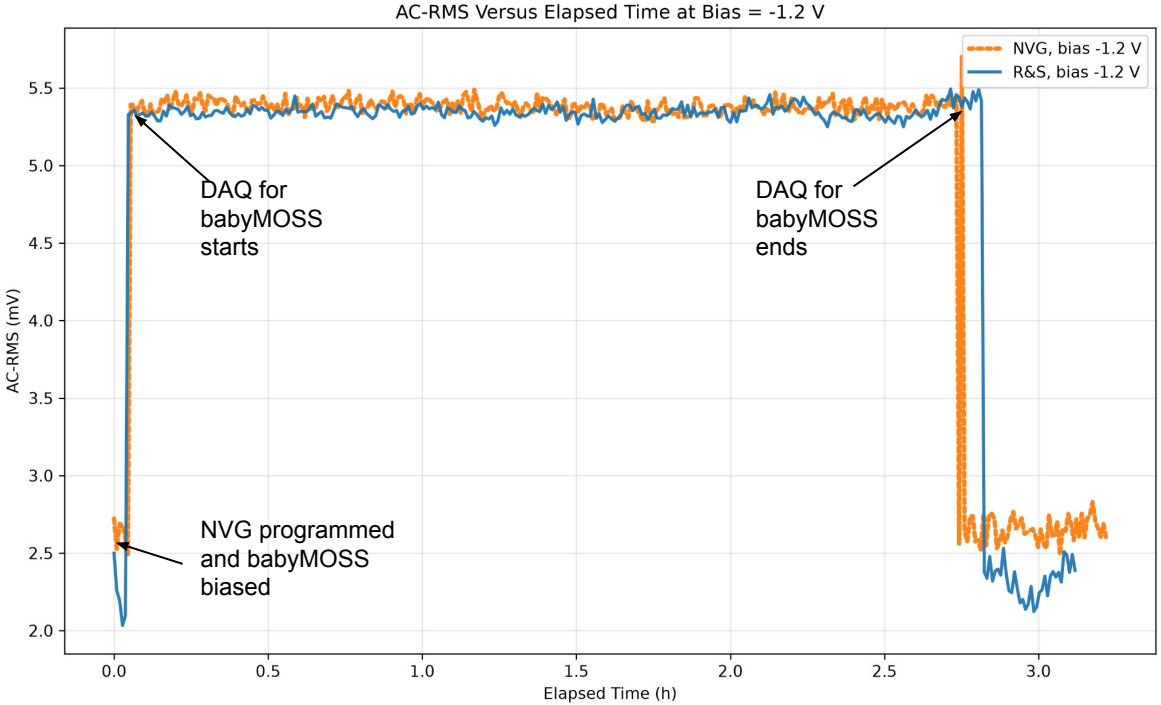
I2C Configuration: EN_CP = 16, I_VCO=0
Load: C_L = 1uF, R_L = 5k Ohm
CLK_SC: f_SC = 5 MHz
20 MHz hardware bandwidth limit: OFF



- R&S HMP4040 output remained stable throughout the measurement.
- NVG output exhibited ripple across the measurements
- ~40 mV shift in the NVG output occurred when the babyMOSS DAQ started, requiring manual VREF adjustment to restore the desired bias.
- Suggests that starting the DAQ slightly changes the load seen by the NVG.

I2C Configuration: EN_CP = 16, I_VCO=0
Load: C_L = 1uF, R_L = 5k Ohm
CLK_SC: f_SC = 5 MHz
20 MHz hardware bandwidth limit: OFF

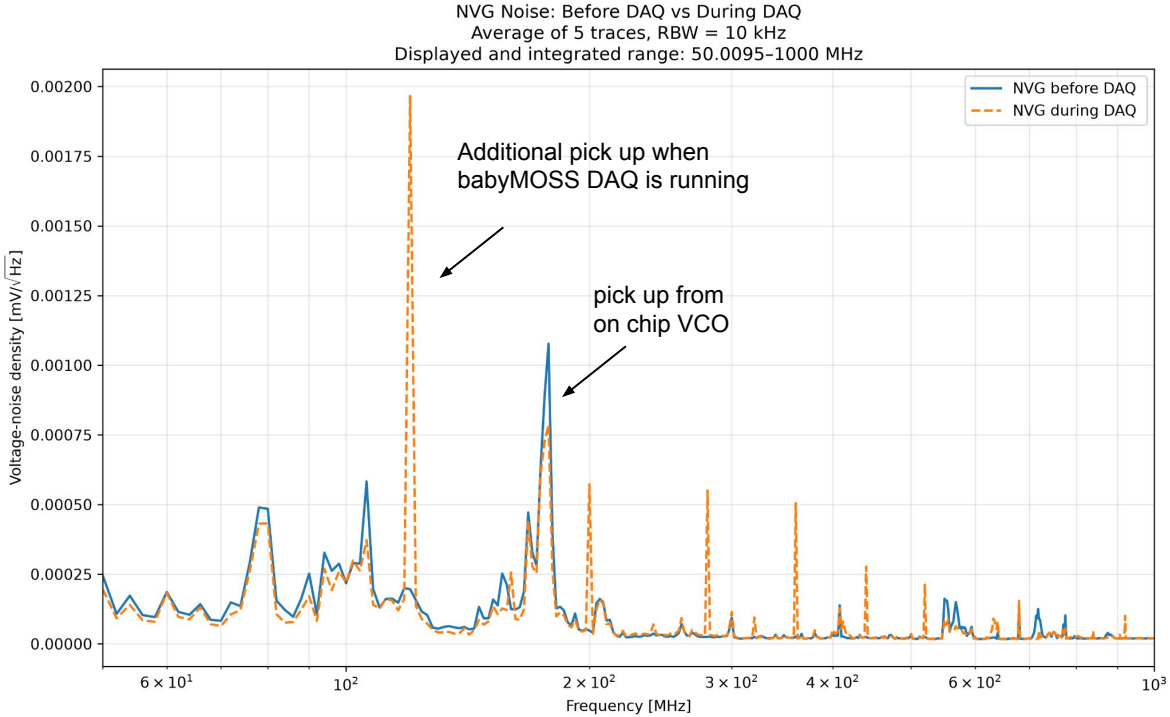
Negative Voltage Generator



- With the NVG programmed and the babyMOSS bias applied (DAQ idle), the measured noise was ~2 - 2.5 mV for both the NVG and R&S HMP4040
- During babyMOSS DAQ operation, the noise increased to ~5 mV for both power supplies
- Consistent increase suggests that running the babyMOSS DAQ introduces additional noise
- NVG noise spectral density was compared with the DAQ idle and running to investigate the DAQ-induced noise

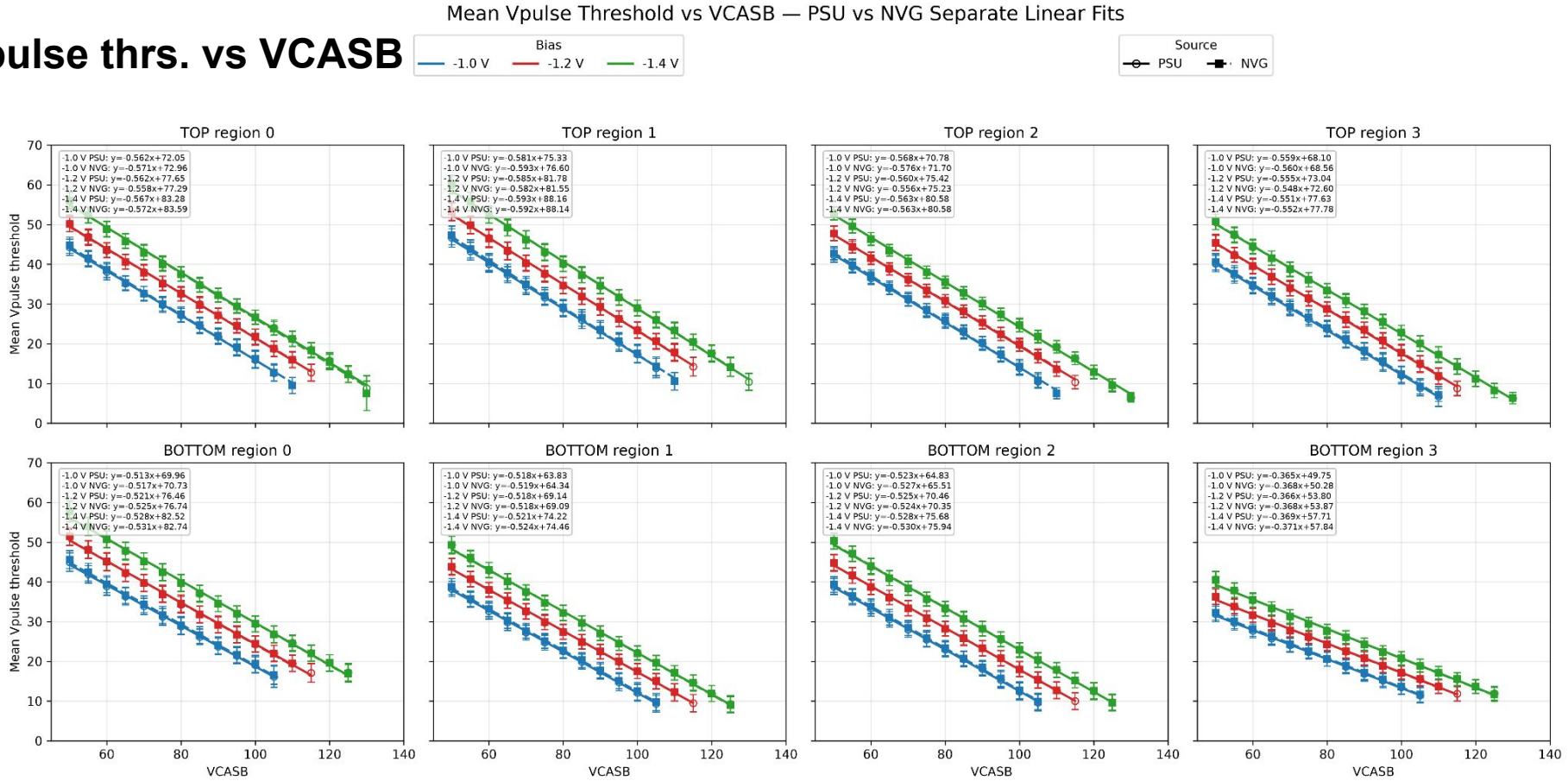
I2C Configuration: EN_CP = 16, I_VCO=0
Load: C_L = 1uF, R_L = 5k Ohm
CLK_SC: f_SC = 5 MHz
20 MHz hardware bandwidth limit: OFF

Negative Voltage Generator



- Noise spectral density was analyzed above 50 MHz, VCO operating range (~80–650 MHz).
- A common ~175 MHz peak from the on-chip VCO was observed with and without DAQ operation
- During babyMOSS DAQ running, an additional ~125 MHz peak and its higher harmonics appeared in the measurements
- Additional spectral components resulted in higher overall noise during babyMOSS DAQ in operation

Vpulse thrs. vs VCASB



- Good agreement between PSU and NVG for all 8 regions, fitted with straight line
- Fit function used to map VACSB to Vpulse thresholds