Barrel TOF Service Hybrid

Wei Li, Tonko Ljubicic, Mike Matveev (Rice University)
Tim Camarda (BNL)

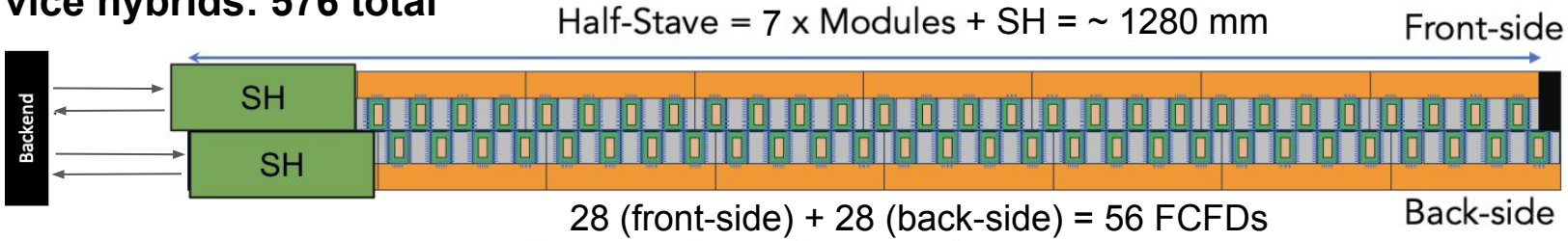
ePIC TOF DSC WG
09/17/2026

Barrel TOF service hybrids (SH)

Requirements:

- **Mechanical**: must fit within BTOF envelope. It is part of the detector.
- **Electrical**:
  - Readout 56 FCFDs per half-stave
  - Power 56 FCFDs per half-stave, w/ distance dependent voltage
  - Deliver BVs to 56 AC-LGADs strip sensors per half-stave
  - Power active components (lpGBT, VTRx+)
- **Thermal:** power section requires cooling (30% of a half-stave)
- **Interface:** compatible with FPC, input LV/BV

Service hybrids: 576 total



Requirements from ASICs - FCFD (FNAL)

FCFD requires:

- Analog: 1.2V, 2.5V
  - 2 mW (2.5) vs 1.6 mW (1.2) per ch
- Digital: 1.2V

Digital and analog 1.2 share the same input

Table 2: Preliminary estimate of power consumption of various blocks in FCFD 32- and 128-channel options. The totals are also shown for a single 128- and single 32-channel designs.

link

	Unit power(mW) (32-ch)	Unit power(mW) (128-ch)	Units in FCFD32	Units in FCFD128	FCFD32_Power(mW)	FCFD128_Power (mW)
analog_front	3.6	4	32	128	115.2	512
TDC	0.2	0.22	32	128	6.4	28.16
eRx	1	1	2	1	2	1
eTx	2	2	1	1	2	2
Readout16	30	30	2	8	60	240
Serializer	3	3	1	1	3	3
fc_decoder	5	5	1	1	5	5
data_aligner	2	2	1	0	2	0
I2C	2	2	1	1	2	2
Total (mW)					197.6	793.16

Power and current distribution:

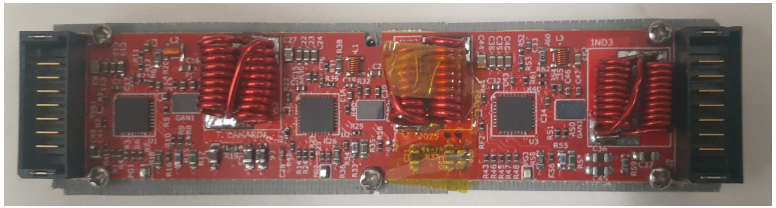
A bPOL48V provides up to 10W

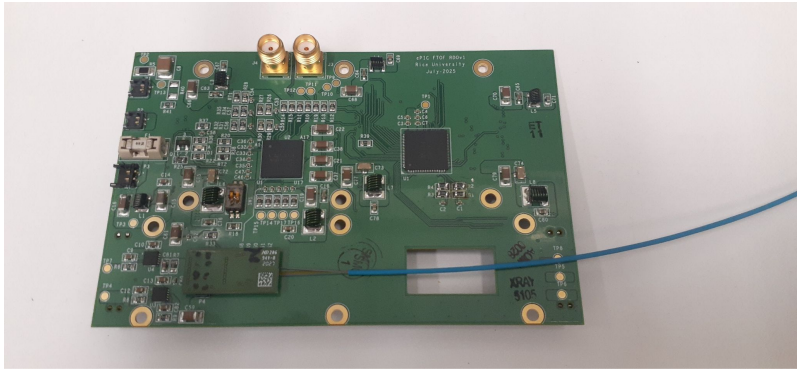
		Channel	ASIC	Stavelet (4 ASICs)	FPC line (2 stavelets)	Half-Stave (7 stavelets)
2.5V (Analog)	Power	2 mW	256 mW	1.02 W	**2.05 W**	**7.14 W**
	Current			0.41 A	**0.82 A**	**2.87 A**
1.2V (Analog)	Power	1.6 mW	205 mW	0.82 W	1.64 W	5.74 W
	Current			0.68 A	1.36 A	4.76 A
1.2V (Digital)	Power		330 mW	1.32 W	2.64 W	9.24 W
	Current			1.1 A	2.2 A	7.7 A
1.2 V (Total)	Power		535 mW	2.14 W	**4.28 W**	**15 W**
	Current			1.78 A	**3.57 A**	**12.46 A**

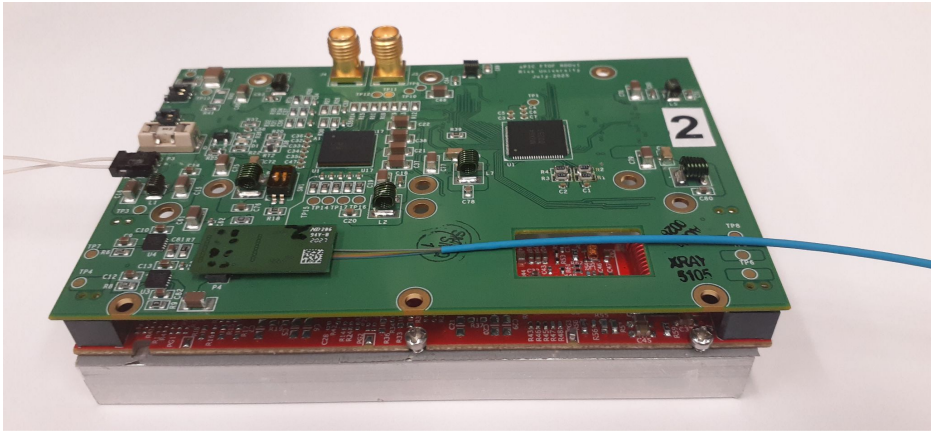
→ **1 bPOL48V for 2.5V**

→ **2 bPOL48Vs for 1.2V**

FTOF/FF SH



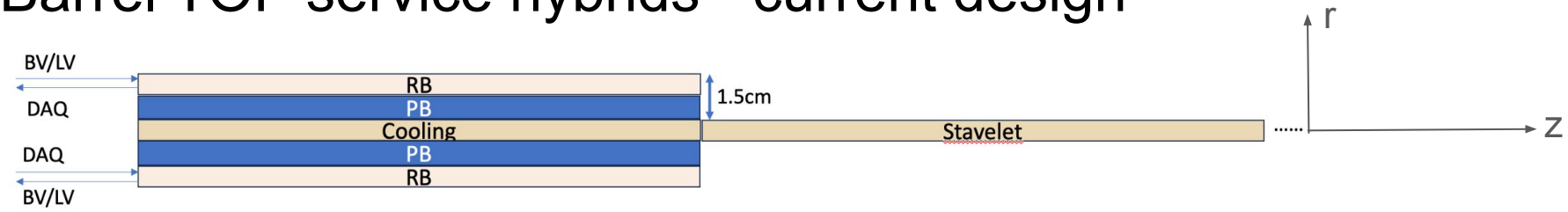




Proven design for FTOF/FF SH, serving 12 ASICs and similar heat load, has a thickness of ~14mm. BTOF requires one extra lpGBT.

Fixed output voltage (1.2V) to ASICs, while BTOF requires **1.2V+2.5V+distance dependence**

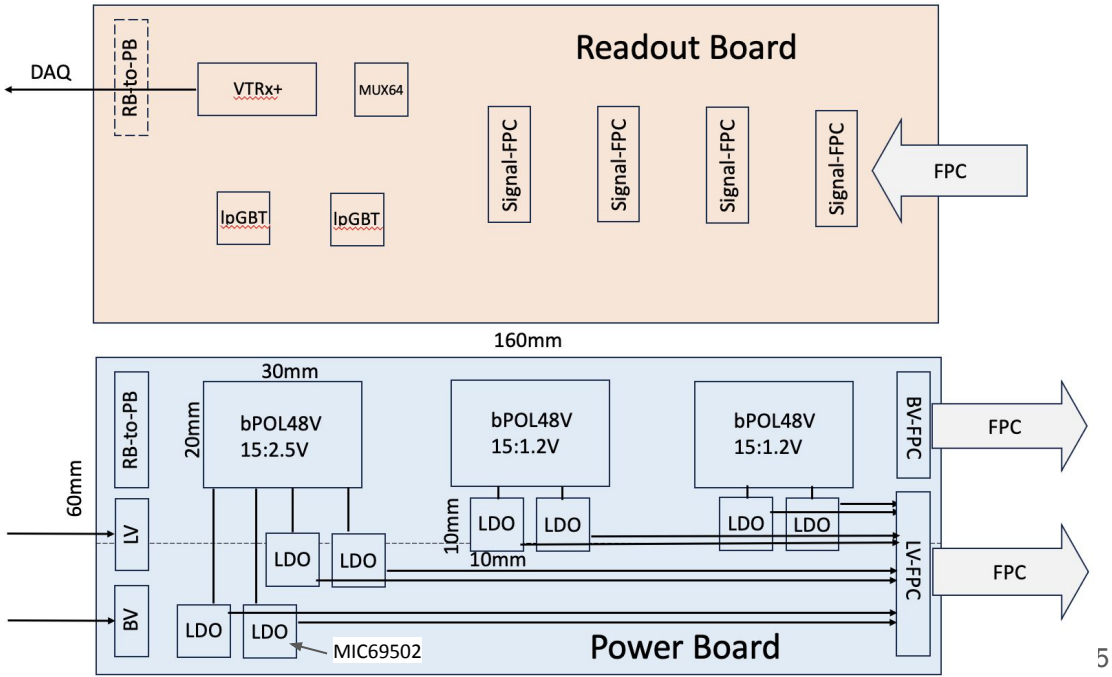
Barrel TOF service hybrids - current design



SHs at the end of each half-stave, on both faces:

- RB: 2 lpGBTs, 1VTRx+, 1 MUX64
- PB: 3 bPOL48Vs, 8 LDOs; **~9.4W** heat dissipation assuming 70% efficiency,

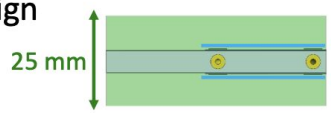
Based on FTOF SH design experience (details in the later talk)

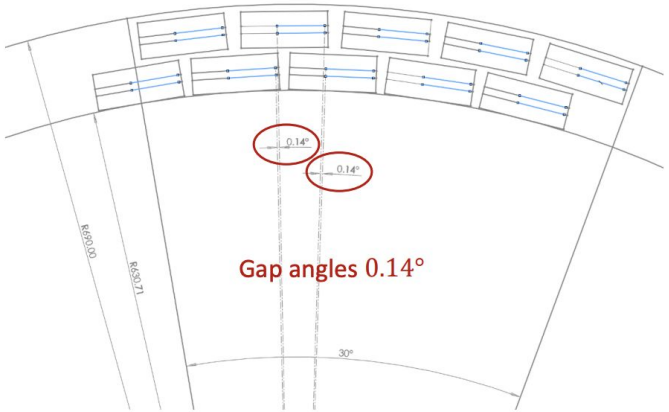


New mechanical constraints (9/10/26)

Barrel TOF Mechanical Design

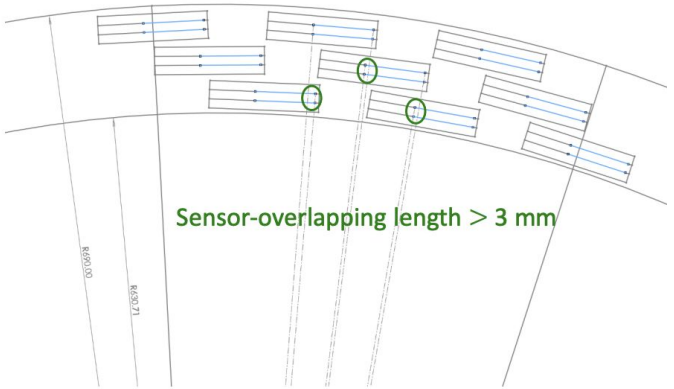
■ 2-layer design





- Sensors do NOT overlap in ϕ direction
- Overall acceptance on $r - \phi$ plane is 95.3%
- Thickness of Service Hybrid is 25 mm

■ 3-layer design

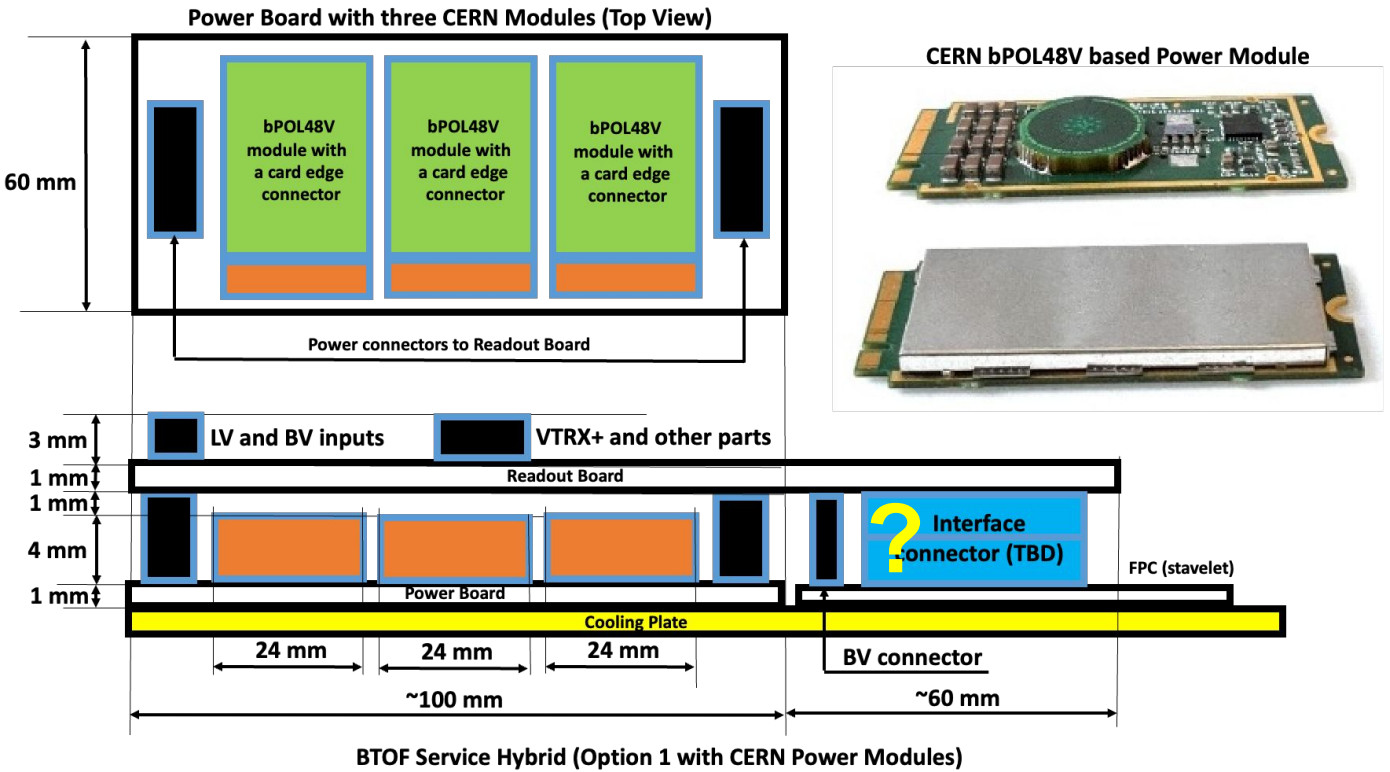


- Sensors overlap in ϕ direction
- Overlapping lengths more than 3 mm
- Overall acceptance is 100 %
- Thickness of Service Hybrid is 15 mm

Total thickness (incl. cooling structure) is 25mm; **~10mm for each SH (?)**

Alternative design:

(for 2-layer; 3 layer is not possible)

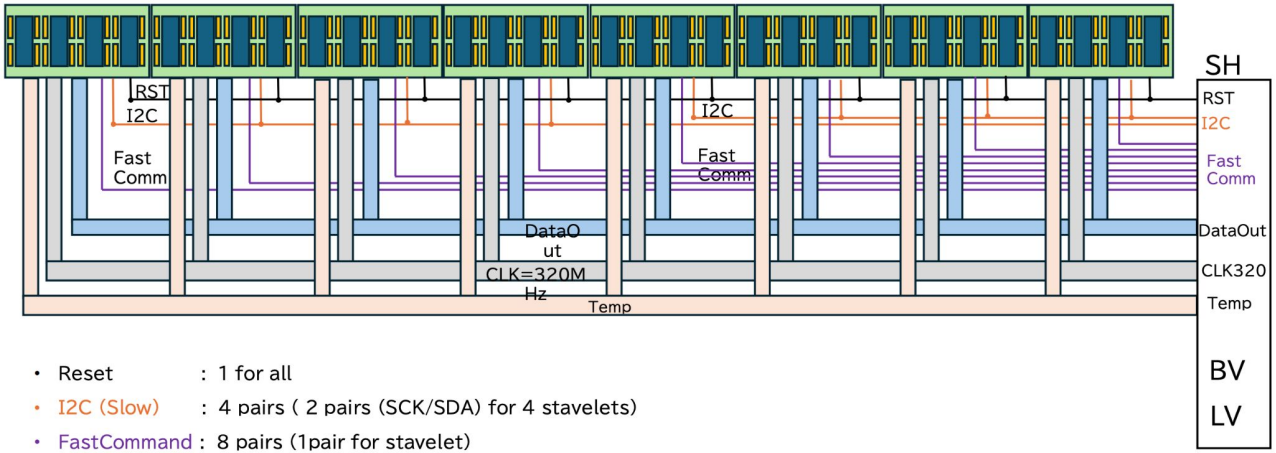


- Thinner DC-DC convertor: CERN module, PCB air core inductor
- LDOs moved to stavelets: no need to worry about voltage drop; improved output voltage stability
- ~240 CHF each; Need 3*2*144*2 = 1728 modules

Backups

FPC conceptual design (NARA)

Signal lines:



- Reset : 1 for all
- I2C (Slow) : 4 pairs (2 pairs (SCK/SDA) for 4 stavelets)
- FastCommand : 8 pairs (1pair for stavelet)
- DataOut : 32 pairs (320Mbps)
- CLK320 : 32 pairs (320MHz)
- Temperature : 32 pairs ?

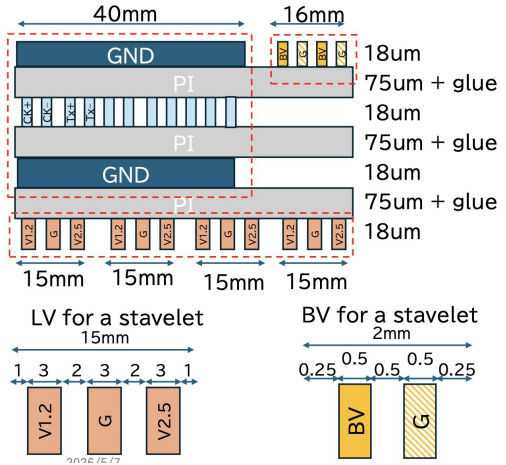
Signal Lines = 108 Pairs + 1
= 217 lines → 31mm width

+GND

# of LV lines: 4 (1.2V) + 4 (2.5V) + 4 (GND) = 12

# of BV lines: 8 (BV) + 8 (GND) = 16

Layer structure:



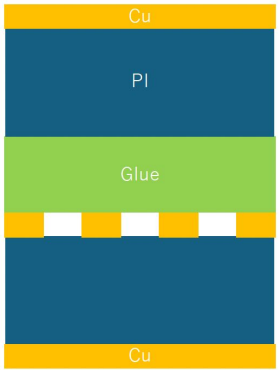
Simulation studies of FPC (NARA)

Recommendation:

- *Inclusion of additional simulation work on PCB design for transmission lines to define the technical performance and in particular for the resistivity on the BTOF*

- 1st FPC simulation with a simple assumption
  - Streight line with 135cm long
  - Designed Layer structure and line/space

Strip line structure
(Covered by top and bottom



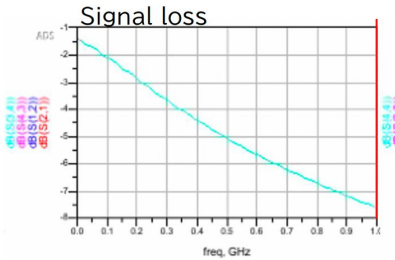
R-F755: PI:75um, Cu: 18um
PI er = 3.2

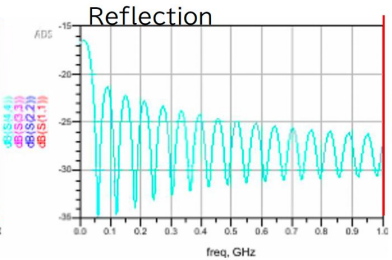
Glue sheet : YBL-000-OL、50um
er=2.5

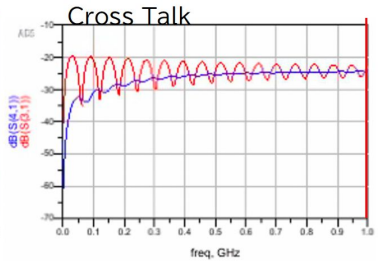
R-F755: PI:75um, Cu: 18um

Line width :70um, space btw lines:70um

Signal loss and reflection

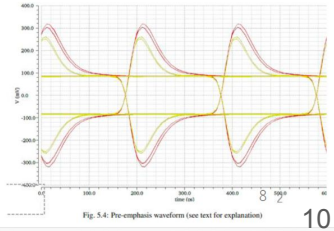






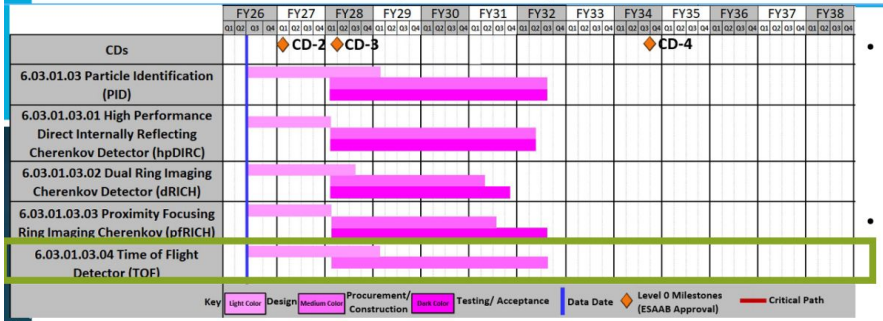
- Evaluate the distortion at 0.8~1GHz (2.5 x reference freq. (320MHz))
  - Signal loss : -7.5 dB = 42%
  - Reflection : -28 dB = 4%
  - CrossTalk : -25 dB = 6%
- These values are good enough for 320MHz clock
  - This is ideal case (simple straight line), redo with the realistic condition
  - lpGBT can use “pre-emphasis” which help the pulse shape
  - Need the driver characteristics of the FCFD driver

Pre-emphasis of lpGBT

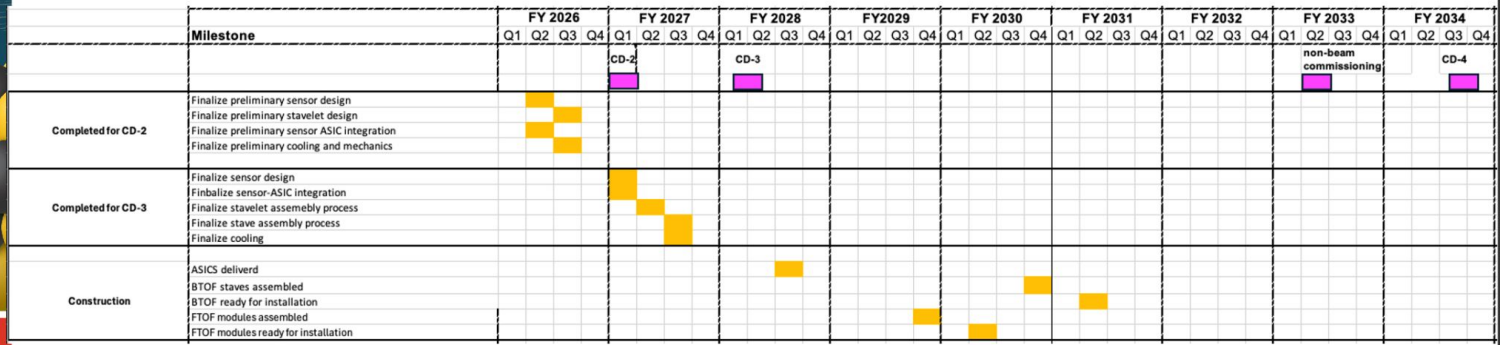


Schedule (TOF)

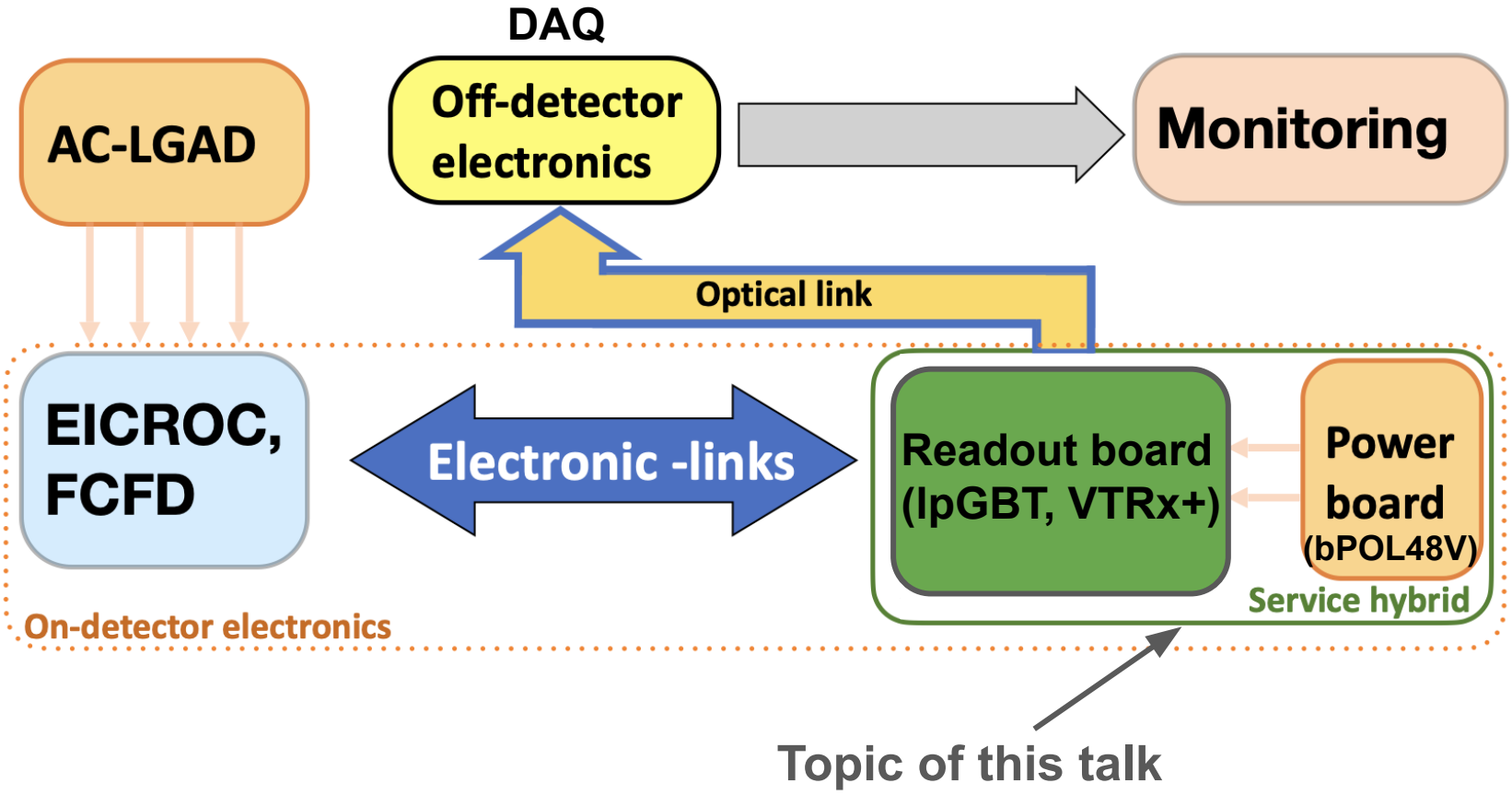
Charge #2



- Key Schedule Drivers/Assumptions:
  - BTOF : Assuming FCFD ASIC becomes available mid of CY2028 for BTOF stave preproduction article.
  - FTOF : Assuming EICROC ASIC becomes available during mid of CY2028 so preproduction can begin by mid calendar year 2028.
- Key Take Away : Significant reliance on ASIC development



Overview of TOF readout chain



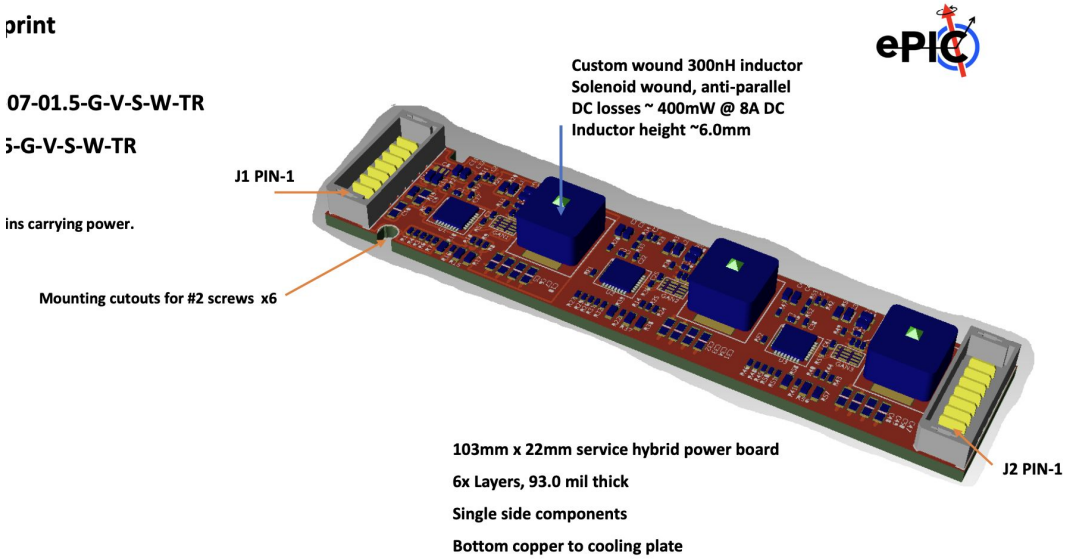
TOF ASIC specs and data rate

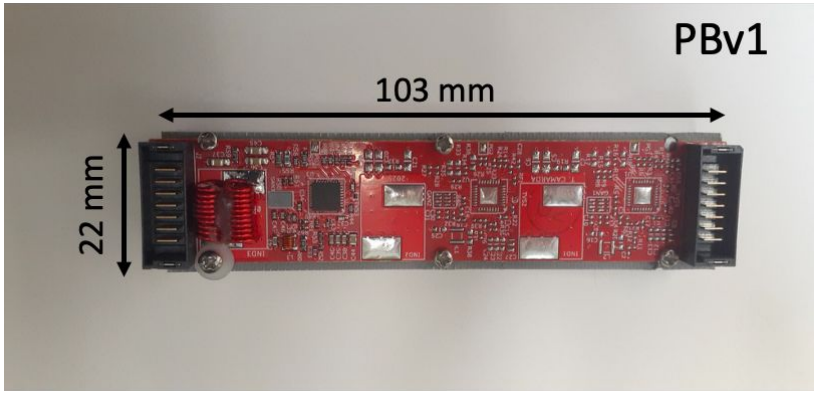
	Both EICROC2 (FTOF) and FCFD (BTOF)
Clock	320 MHz (40 MHz internal)
Fast Command	8 bits @ 320 Mbs
Data Lane #	1
Data Rate	320 Mbs
Zero-suppressed data	Yes
Streaming	Yes
Control Iface	I2C @ 1 Mbs

⇐ Both ASICs will be readout using CERN lpGBT and VTRX+ ASICs with associated protocols

⇐ These are the most important specifications for ASIC readout & control via **lpGBT** so we wanted to make them the same to simplify interfacing

Forward TOF SH prototype - PBv1





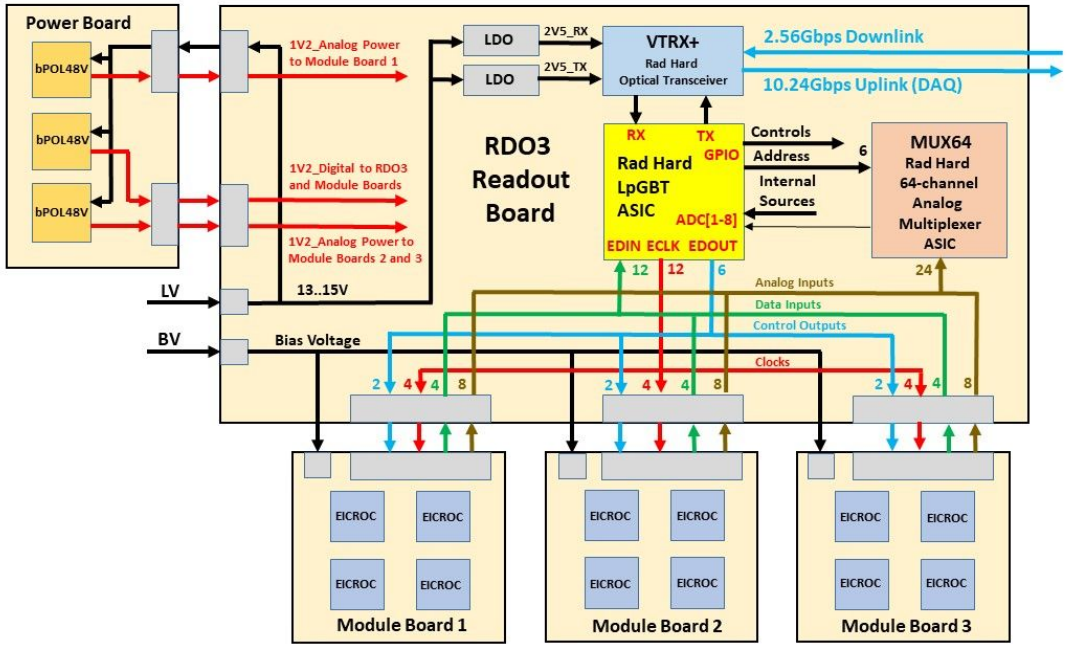
1 PBv1 w/ 3 bPOL48V and 2 PBv1 w/ 1 bPOL48 V assembled and being tested

(1x channel PBv1 already in use to power RBv1)

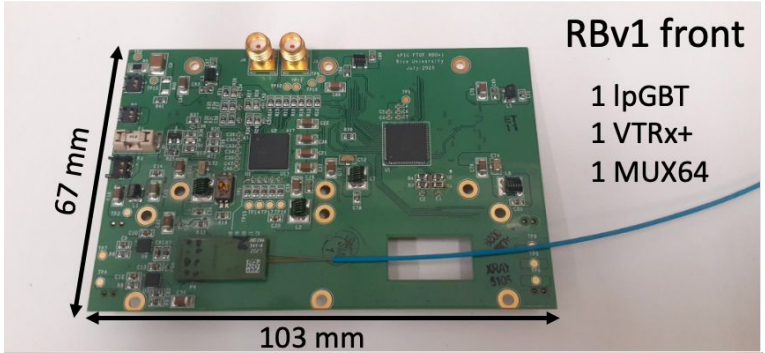
More PB to be assembled with the availability of 10 more bPOL48V chips

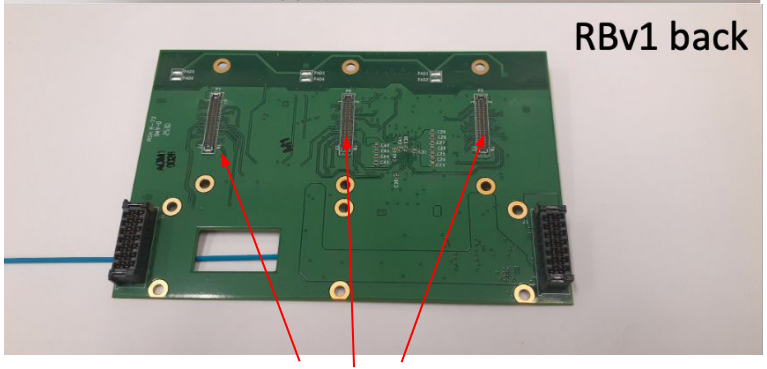
Forward TOF SH prototype - RBv1

RBv1 schematics



6 boards assembled





Module connector:
78-pin Kyocera
245897078002829+