

ePIC SVT WP3 Meeting, October 1, 2026

Disk FPC Updates

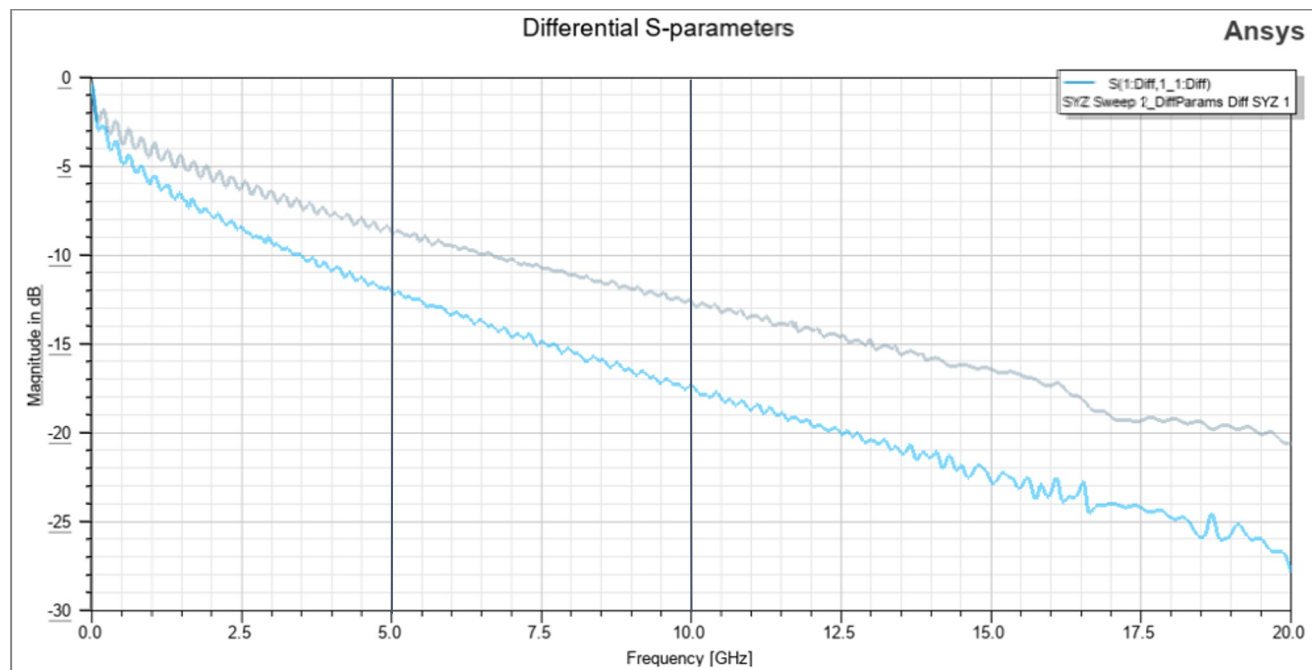
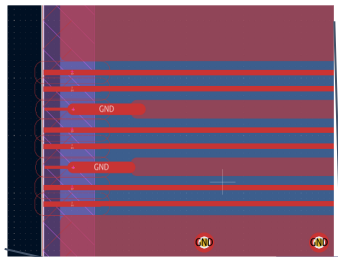
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Available cross section for JLC FPC (2-layer)

	Thickness(um)	
Cover layer	27.5	50
Copper	12	18
Dielectric	25	50
Copper	12	18
Cover layer	27.5	50
Total thickness	104	185
suggested trace width	55	93
suggested trace spacing	140	152
perimeter	134	222

JLC has suggested width/space for the cross section with 104um & 185um total thickness.

Test structures with JLC's Available Stack-up



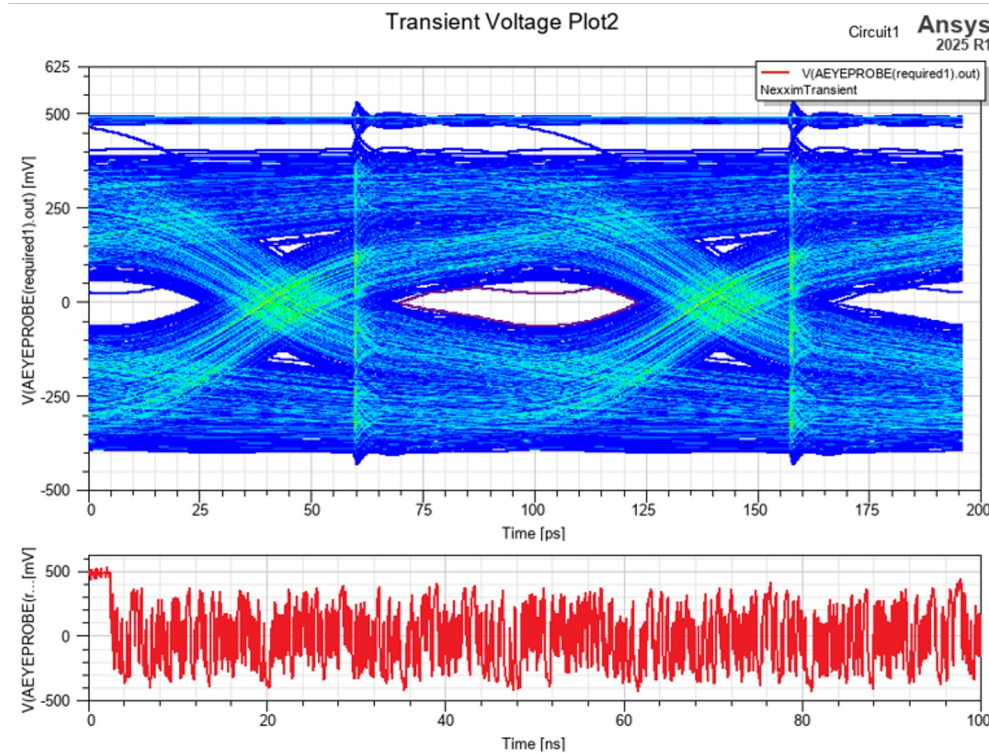
L=389mm

Differential S-parameter simulation results for:

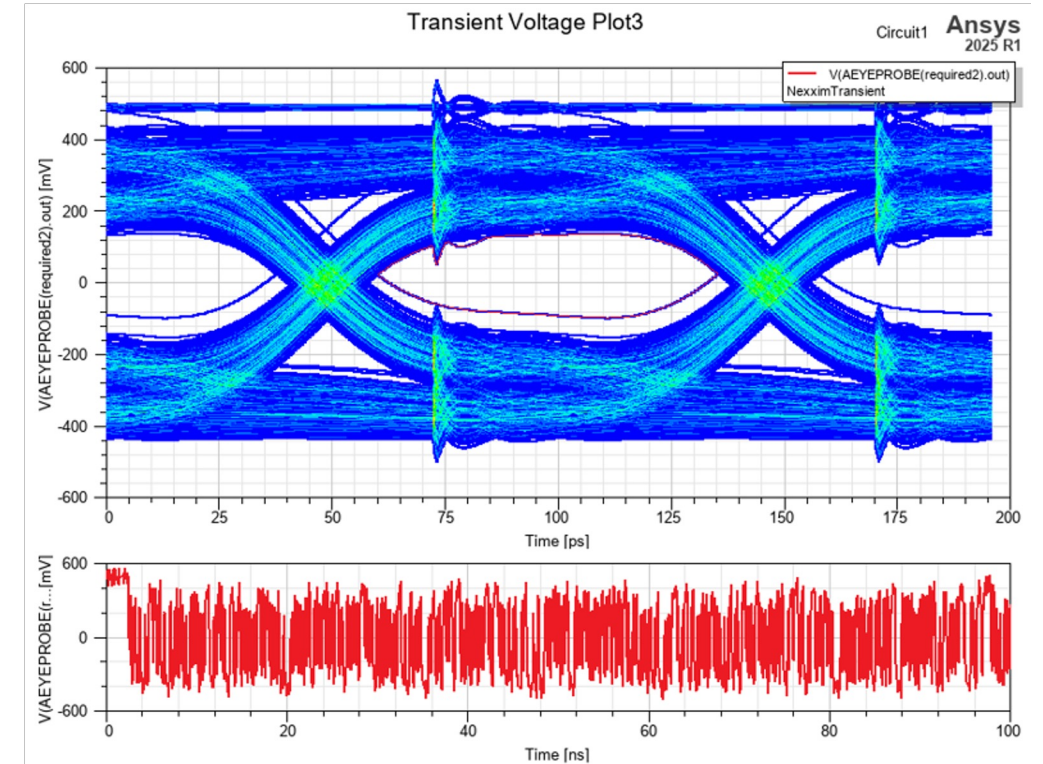
Gray: 18um Cu + 50um Dielectric FPC

Blue: 12um Cu + 25um Dielectric FPC

Eye Diagram results @ 10.24Gbps



12um copper
25um dielectric
55um trace width



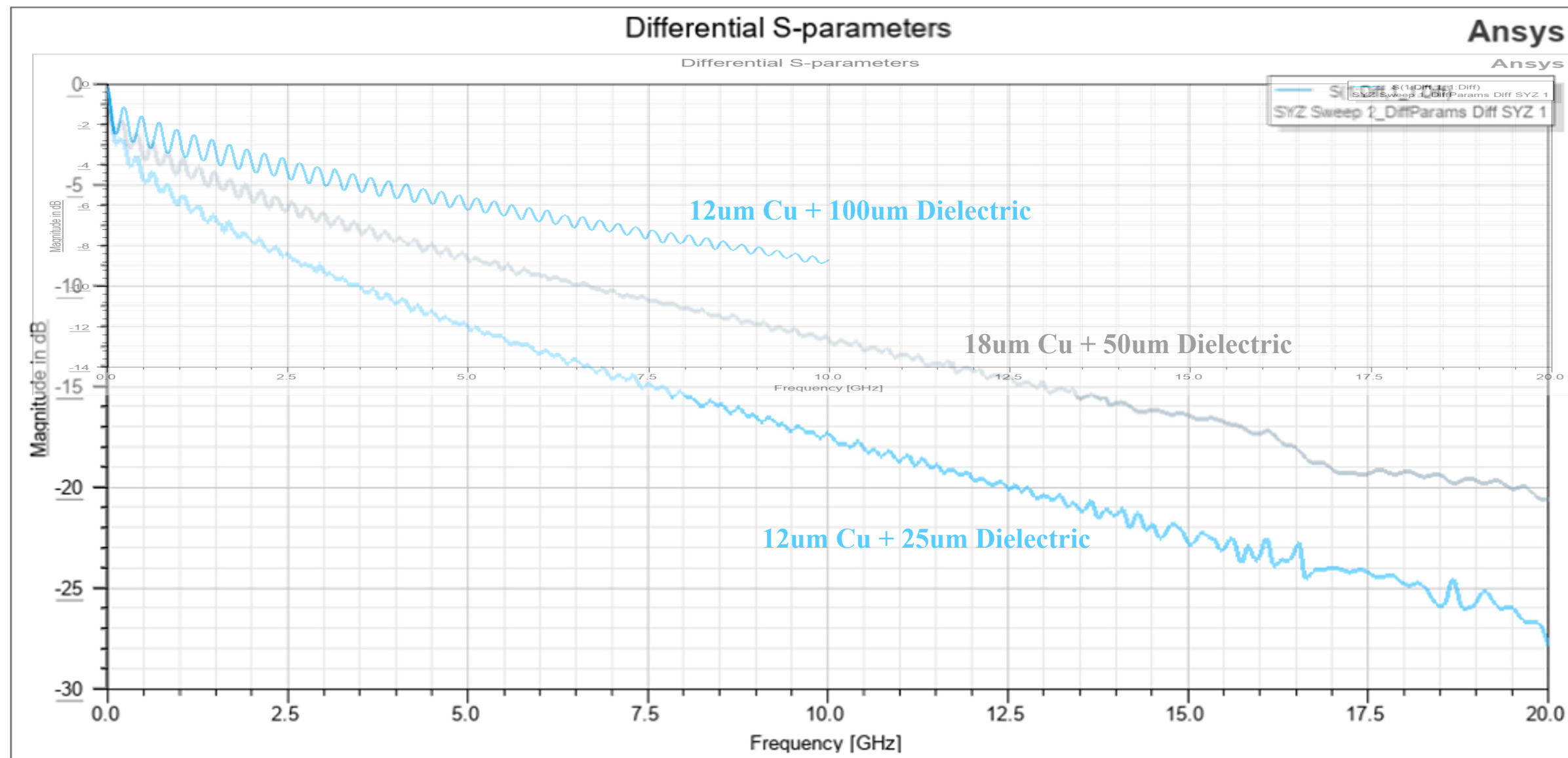
18um copper
50um dielectric
93um trace width

Available cross section for JLC FPC (4-layer)

	Thickness(um)	
Cover layer	27.5	27.5
Copper	12 (L1)	12 (L1)
Dielectric	62.5	100
Copper	12 (L3)	12 (L4)
Cover layer	27.5	27.5
Total thickness	131.5	179
HSD trace width	110	190
HSD trace spacing	160	200
HSD perimeter	244	404
SC trace width	70	80
SC trace spacing	60	60
SC perimeter	164	184

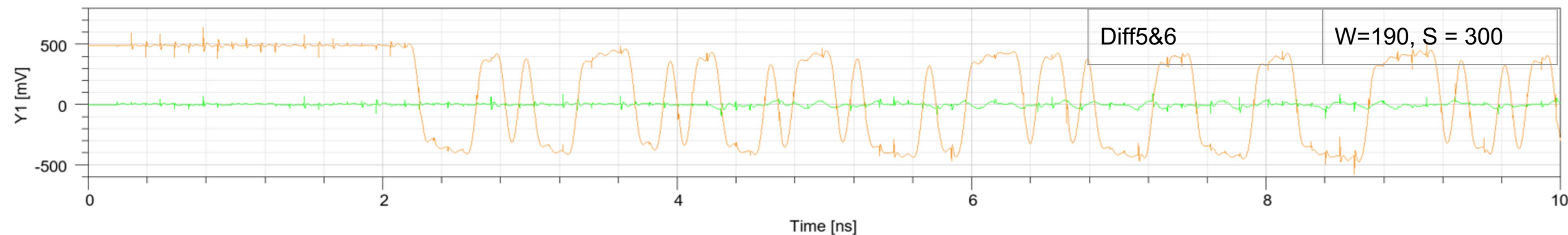
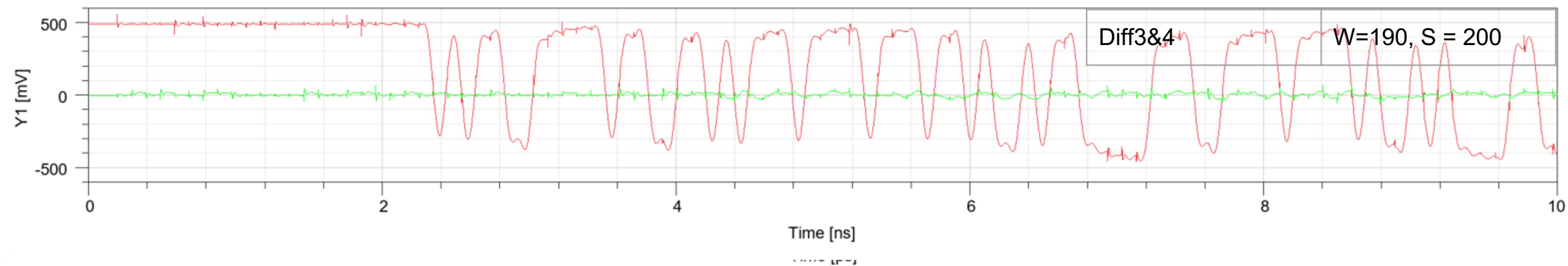
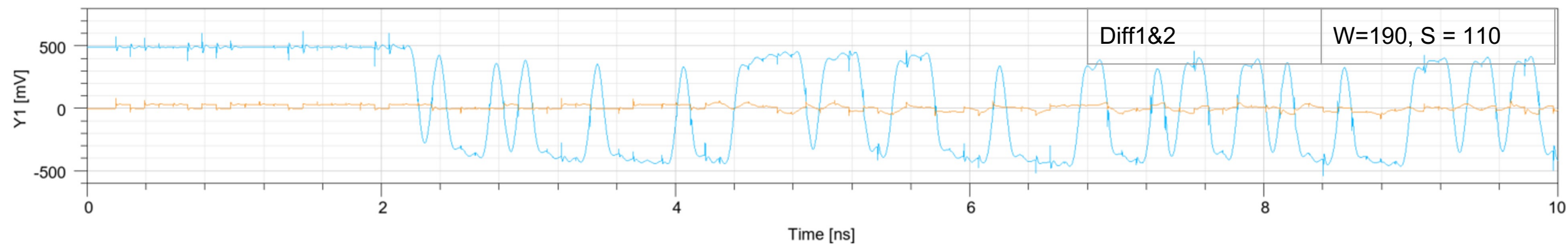
HSD and SC widths and spacings are calculated so that the impedance is around 100 Ohms

Test structures with JLC's Available Stack-up





Cross-Talk vs Spacing



Summary and Outlook

- Performed Ansys simulation, the HSD traces on the BabyMOSAIX carrier board were simulated, yielding results consistent with those of Stefano.
- The same methodology was applied to simulate JLC_V1 FPC. The results show that high-frequency signal transmission characteristics are far from ideal.
- Increasing the perimeter of the trace to reduce signal loss on the trace has been confirmed to be a feasible approach.
- Submitting Cu-based test structures to compare signal transmission and cross-talk with
 - Different thickness/width/spacing
 - Soldering vs wire-bonding vs direct connection
- Measure the performance of test structures with different thickness/width/spacing, to validate Ansys simulation, and use the Ansys simulation to optimize the disk FPC design