

May 12, 2026

FCFD: Barrel ToF Readout Chip

Artur Apresyan



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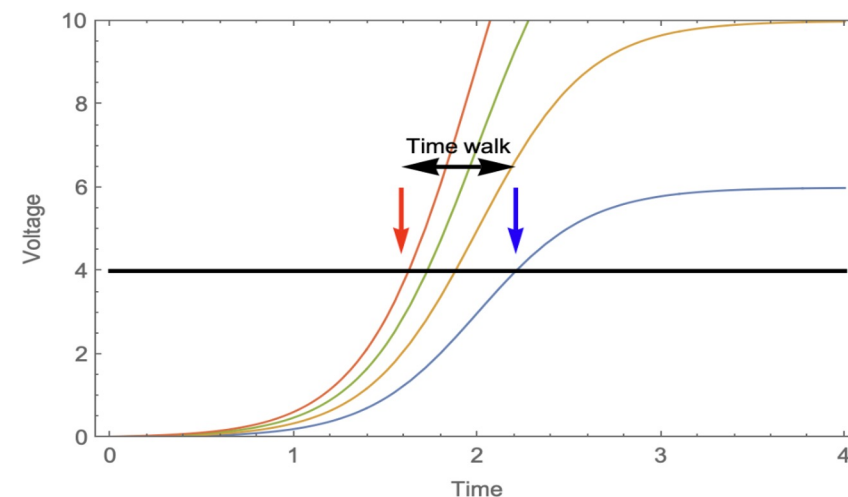


Charge of the review

1. Are the technical performance requirements appropriately defined and complete for this stage of the project?
2. Are the plans for the various sub-systems appropriately documented and complete for this stage of the project?
3. Are the current plans for the detector likely to achieve the technical performance requirements, with a low risk for cost increases, schedule delays, and technical problems?
4. Are the schedule assumptions for the fabrication of the various sub-systems and assembly plans reasonable and consistent with the overall detector schedule?
5. Have ESH&Q and QA considerations been adequately incorporated into the plans at their present stage?
6. Have the recommendations from previous reviews been adequately addressed?

⚙️ Constant Fraction Discriminator

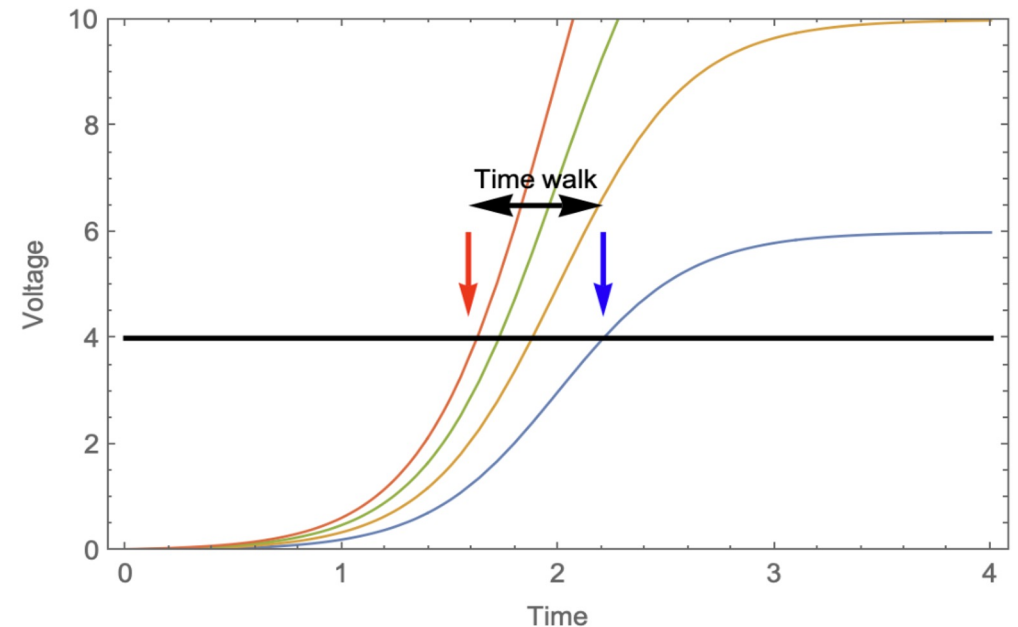
- A robust fast-timing measurement technique
- CFD approach achieves excellent performance, especially for low S/N systems, such as LGADs (NIM A 940 (2019), pp 119-124)
 - CFD-based readout is simple in operation and maintenance
 - No need to maintain the calibration and monitoring system, computing workflows, database maintenance, payloads, etc
 - Time-walk effect is well known & must be corrected for best performance
- A hardware-enabled correction via CFD built into the readout ASIC design offers much simpler solution





Constant Fraction Discriminator (CFD)

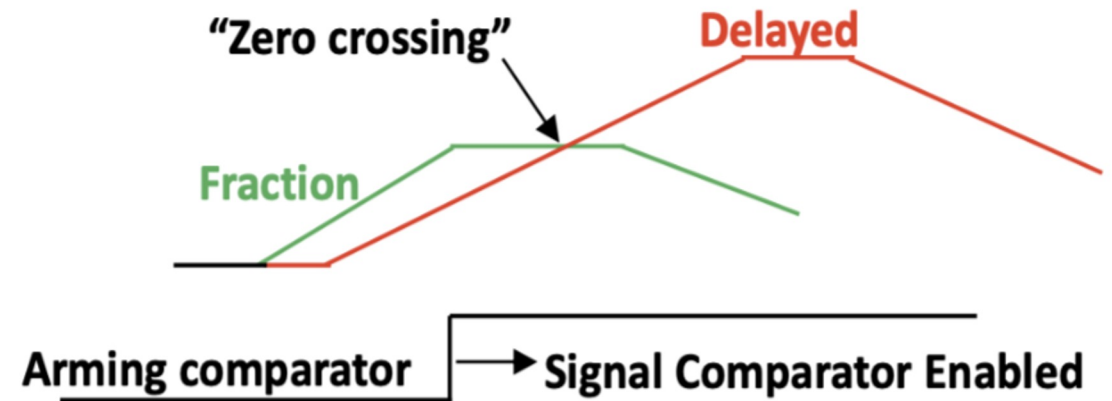
- Time-walk effect is well known & must be corrected for best performance
- Conventionally addressed with online or offline corrections via some type of LUT
- A hardware-enabled correction via CFD built into the readout ASIC design offers much simpler solution



FCFD Readout for Timing Detectors

- Developed for application for (AC-)LGAD sensors for MIP signals
- But can be used for many types of precision timing detectors

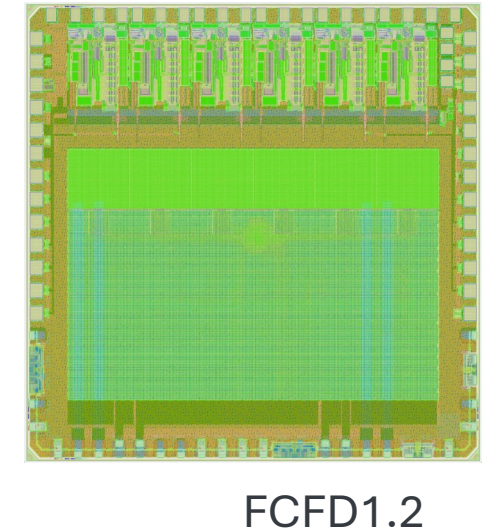
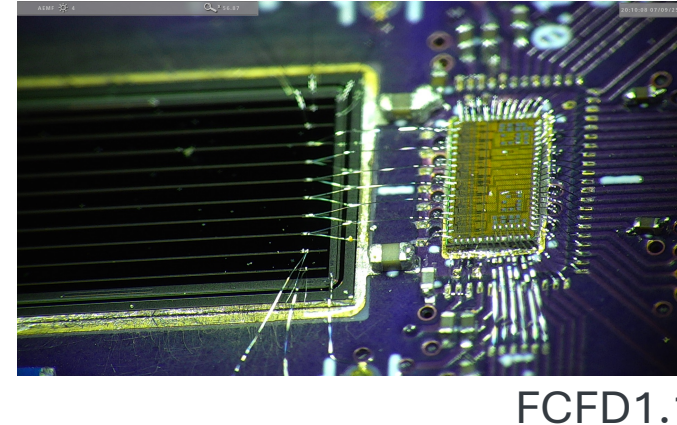
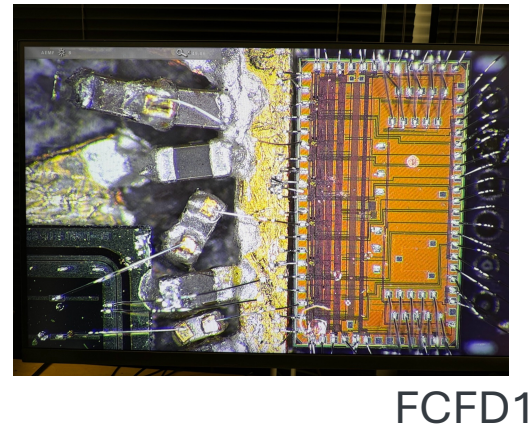
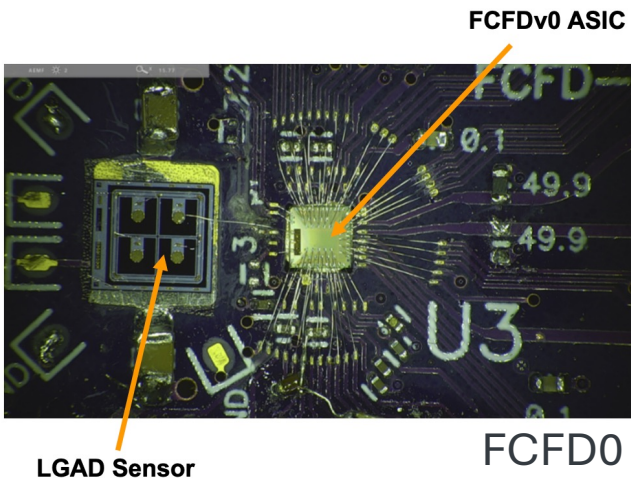
- Main features of the FCFD are:
 - Integrator & Follower to create the “fraction” signal
 - Comparator for “arming” and timestamping



A. Apresyan et. al, **NIM A 1056, 2023, p168655**
<https://doi.org/10.1016/j.nima.2023.168655>

FCFD prototypes

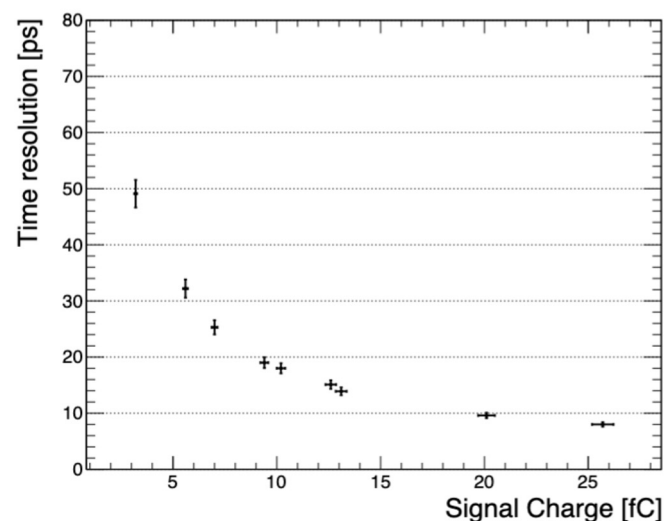
- Several versions of the FCFD chip produced, in TSMC 65 nm node
 - **FCFD0**: first prototype: **fabricated in 2021 and tested in 2022**
 - **FCFD1**: optimized for strip AC-LGAD & position reconstruction: **fabricated and tested in 2024**
 - **FCFD1.1**: optimized for 1-cm long AC-LGAD for ePIC bTOF: **fabricated and tested in 2025**
 - **FCFD1.2**: first full-functionality chip for ePIC bTOF: **submitted in April 2026**:
 - **FCFD2** will be the first full functionality, **full-size** 32-channel chip: **receive near the end 2027**
 - **FCFD3**: final version: **receive near the end 2028** (*consistent with detector construction schedule*)



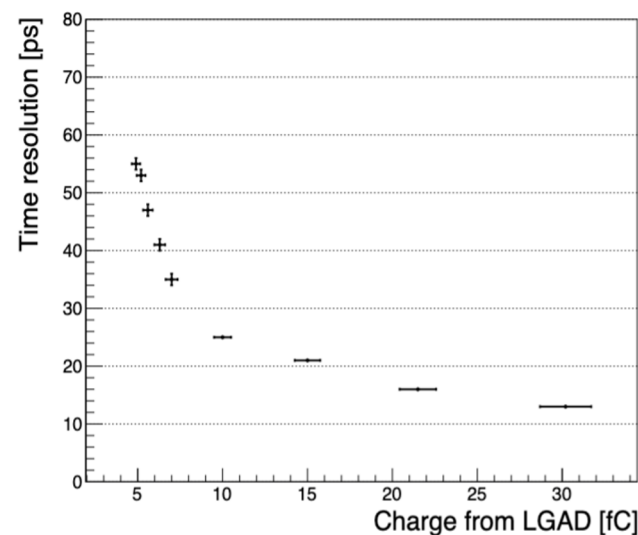
FCFD0 prototype

Charge #3

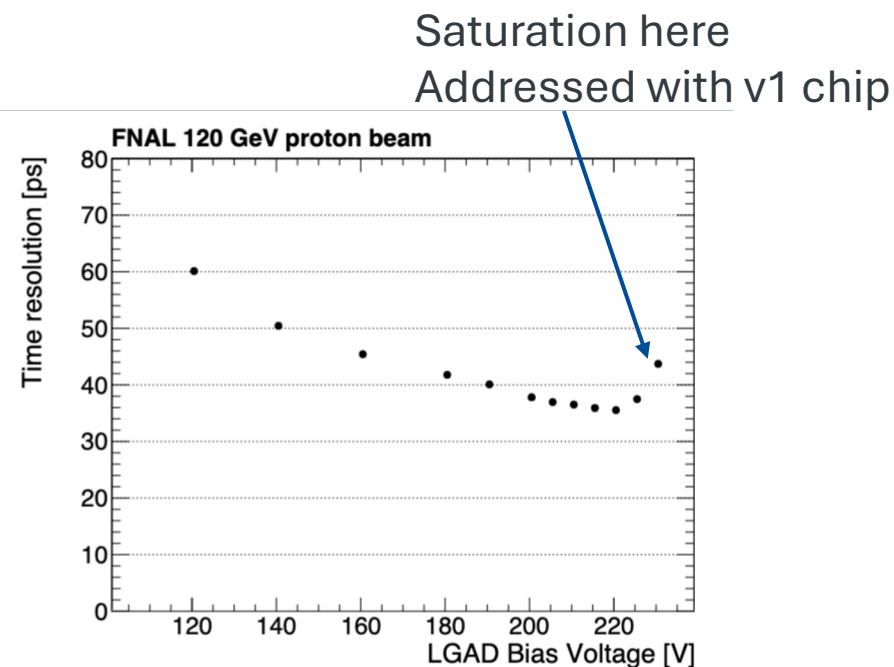
- FCFD0 performance evaluated using multiple types of signals:
 - Charge-injected signal
 - Picosecond Laser signal
 - Radioactive Source signal
 - Proton Beam signal



Charge Injection: intrinsic jitter



Laser signal on LGADs



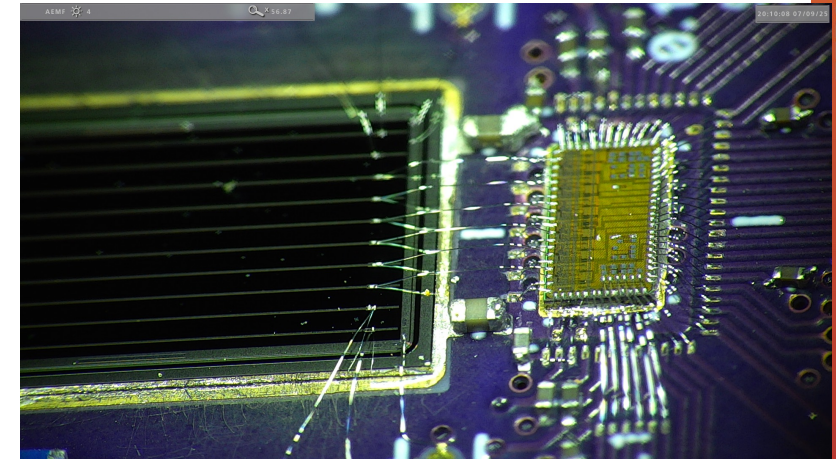
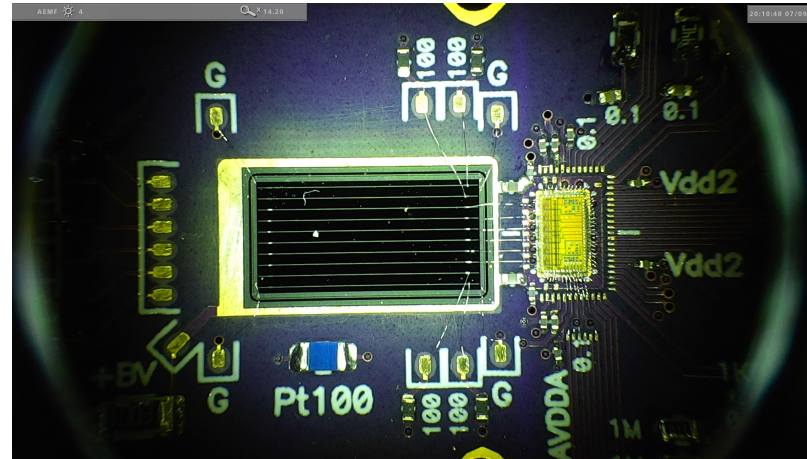
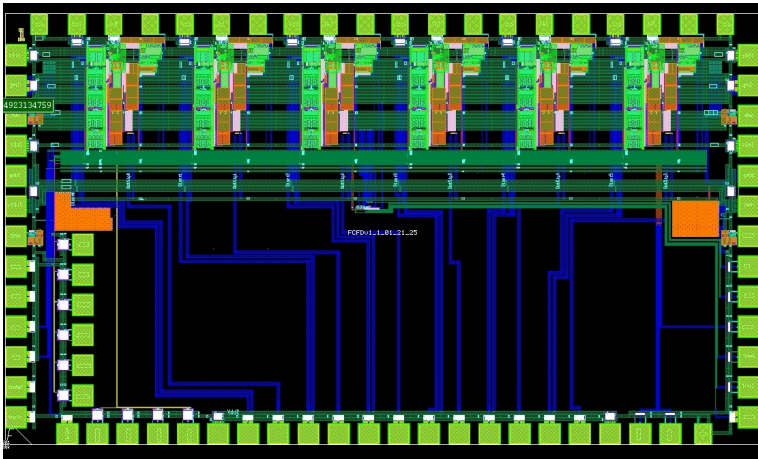
Test beam in FNAL

Sensor specifications

- AC-LGAD sensors and FCFD codesigned together for optimal performance
- **AC-LGAD sensors:**
 - 50 μm thick AC-LGAD sensor
 - 1 cm long strip sensor
 - 500 μm pitch, 50 μm wide metal strips
 - Number of strips per sensor-side: 64
 - Sheet resistance: 1600 Ω/square
 - Sensor RC-properties as reported in NIM A 1089 (**2026**) 171599 (shown in backup)
- Signal properties
 - Dynamic range: 10 - 70 fC; signal MPV : 25 fC; occupancy: O(10) Hz per channel
- Radiation environment after 10 years of running
 - TID: 1 krad; 1 MeV neutron: $3 \times 10^{10} \text{ n}_{\text{eq}}/\text{cm}^2$

FCFD1.1 prototype

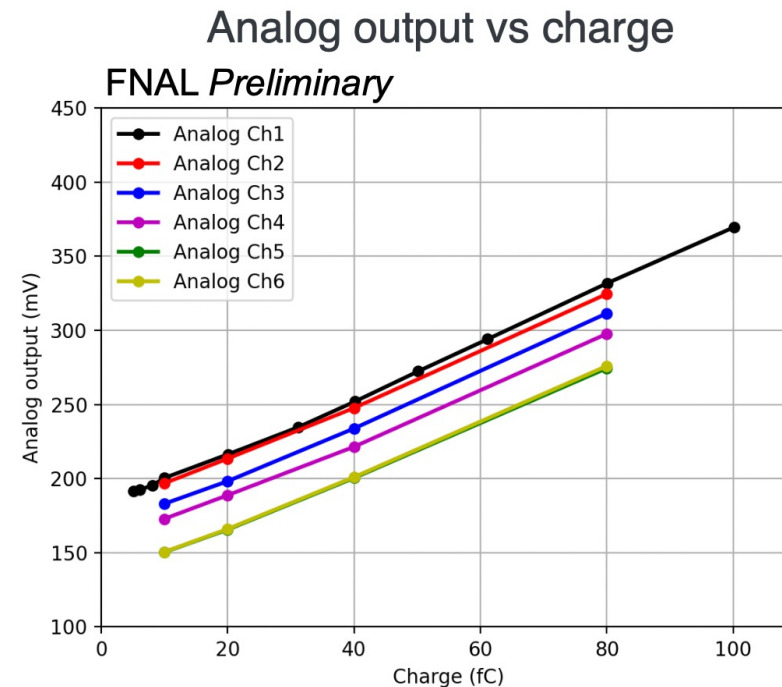
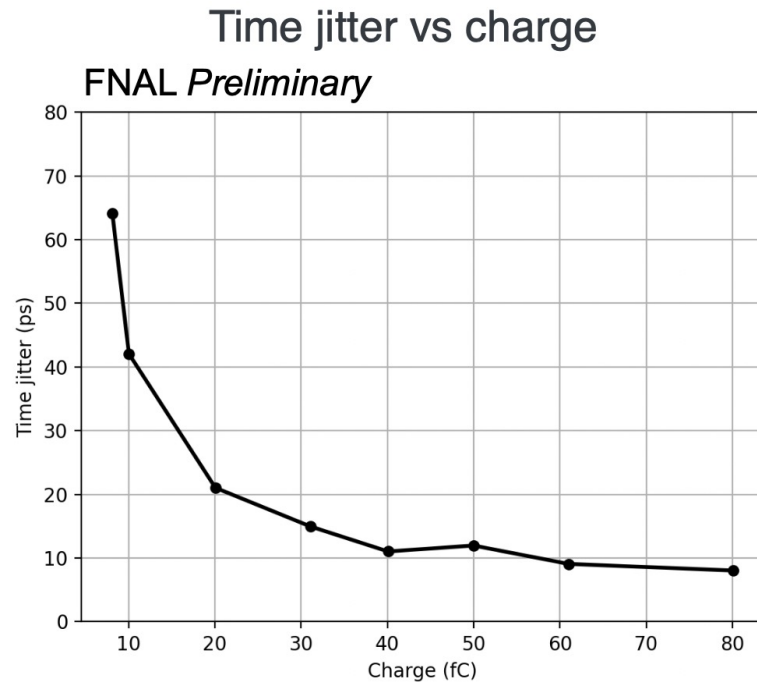
- Designed with the specifications listed on the previous page
- Fully analog readout: discriminator and amplitude output, read out by oscilloscope
- Design was **submitted on Feb 19, 2025**, received in **June 2025**.
- Wirebonded to a HPK 1-cm strip sensors, 6 strips connected
 - Sensor specs as presented on previous slide



Laboratory measurements of FCFD1.1

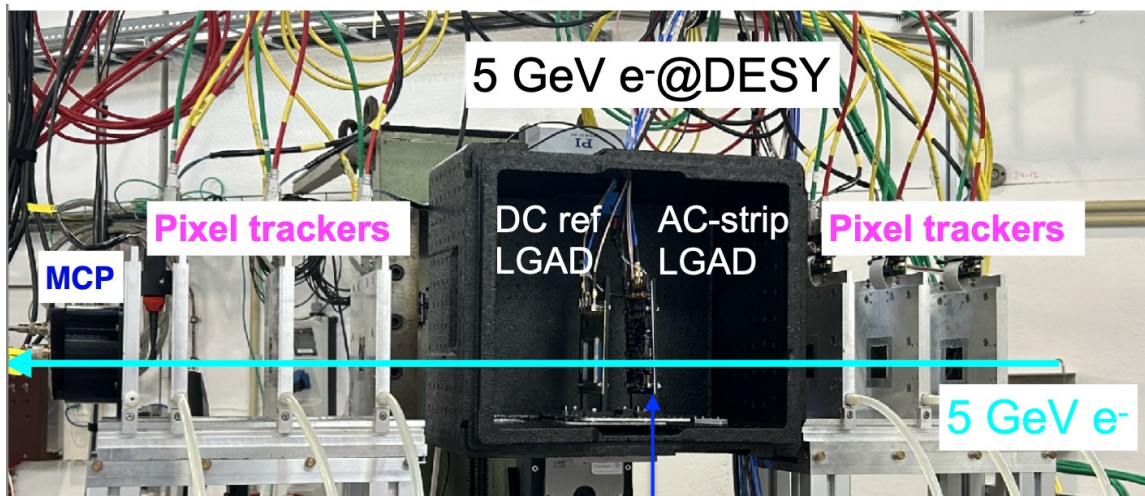
Charge #3

- Charge injection measurements:
 - Jitter measurements consistent with simulation and specs
 - Amplitude measurements: all channels behave as expected, linear in the range



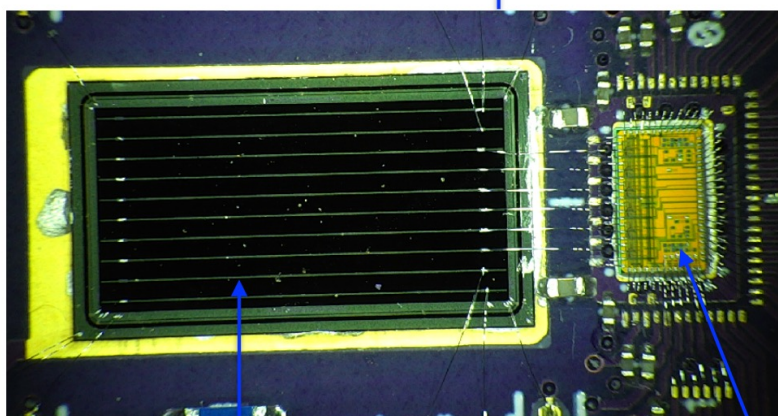
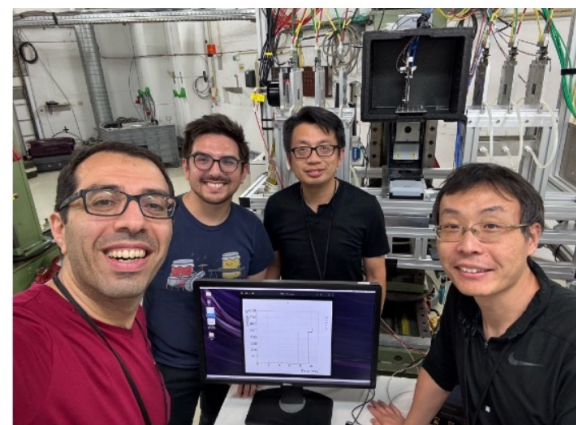
FCFD1.1 test beams in 2025

- Test-beams in summer 2025 at DESY (5GeV e-) and CERN (120GeV p)



- Tracking with $\sim 5 \mu\text{m}$ resolution
- Time reference detector with $\sim 10 \text{ ps}$ resolution (MCP)
- DAQ: high bandwidth, high ADC resolution 8-channel scope

crew@DESY (July, 2025)



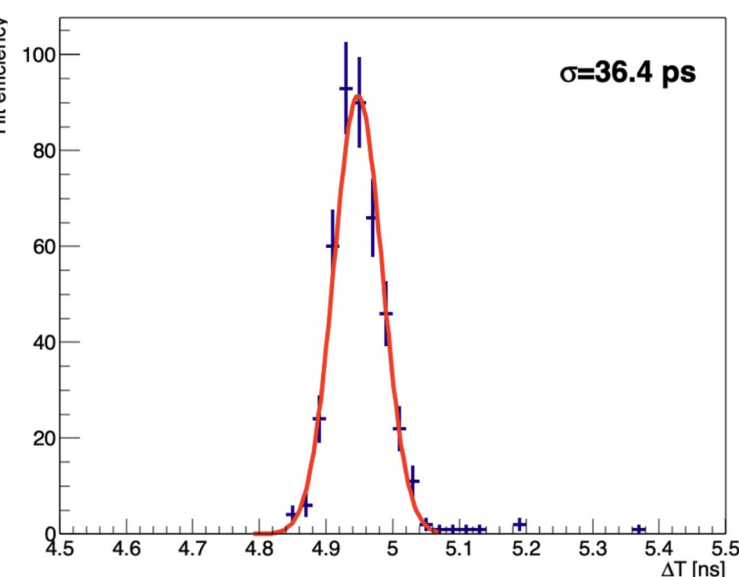
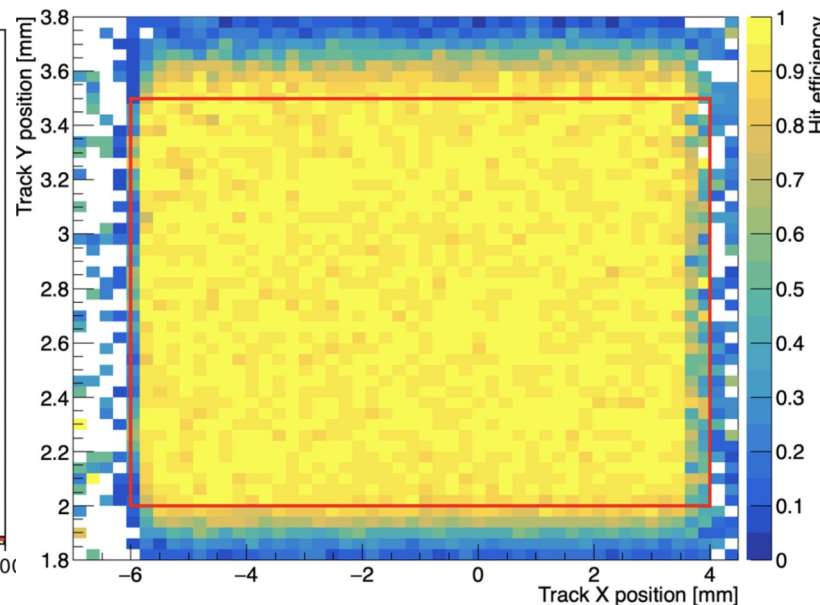
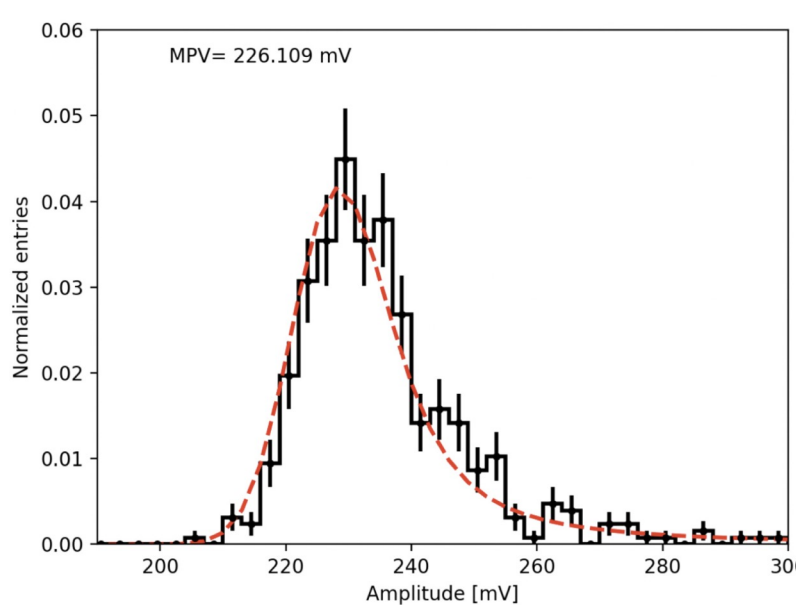
1cm strips, 500um pitch, 50um metal electrode, 50um thick

FCFD-V1.1

FCFD1.1 test beams in 2025

Charge #3

- Measurements of performance in DESY and CERN test beam
 - **100%** signal detection efficiency
 - Measured **time resolution** ~ 40 ps across sensor surface
 - Measured **spatial resolution** ~ 15 - 20 μm
 - Fully efficient across the sensor surface
- Results published in NIM A 1089 (2026) 171599

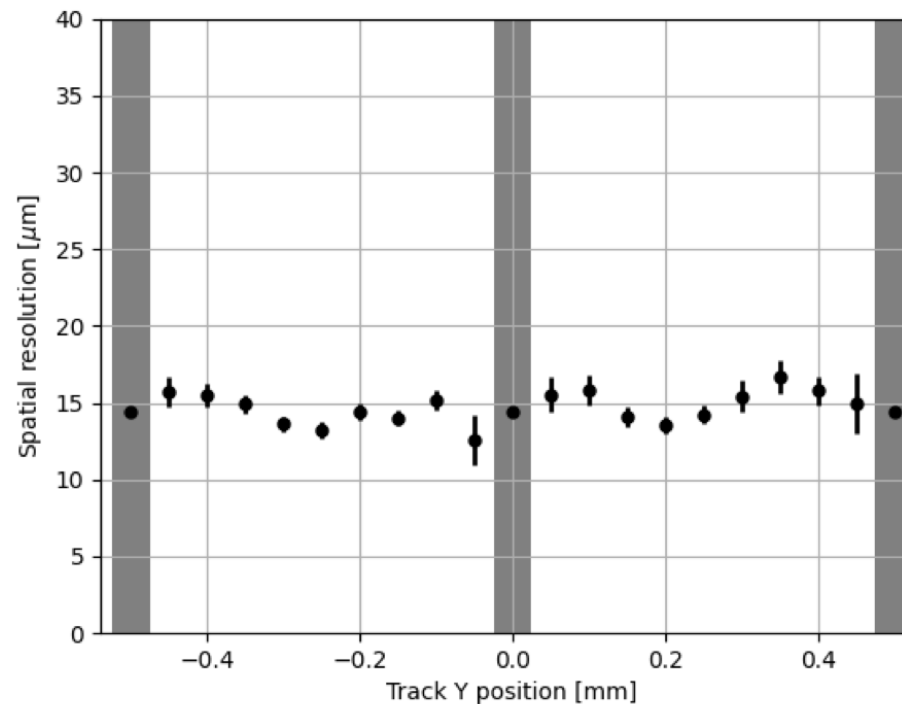
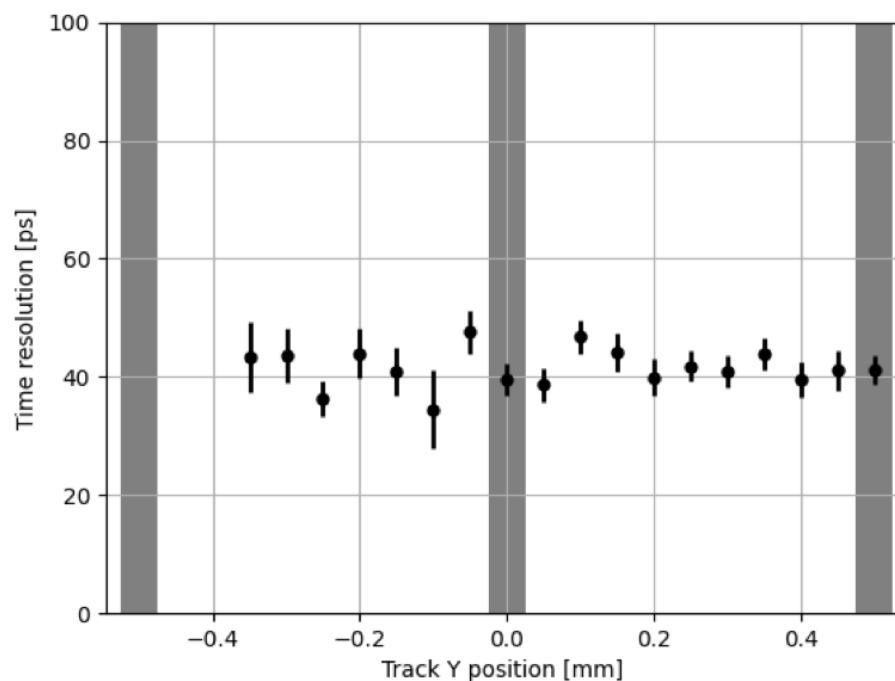




FCFD1.1 test beams in 2025

Charge #3

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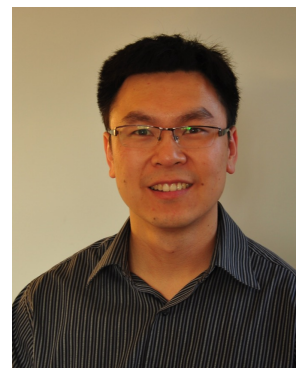
The FCFD development team



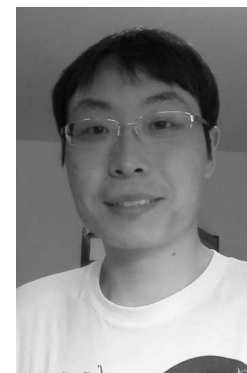
A. Apresyan



C. Pena



S. Xie



S. Wu



C. Gingu



D. Gong



N. Kharwadkar



S. Los



C. Syal



T. Zimmerman

Performance Specifications

- Components that go into overall timing:

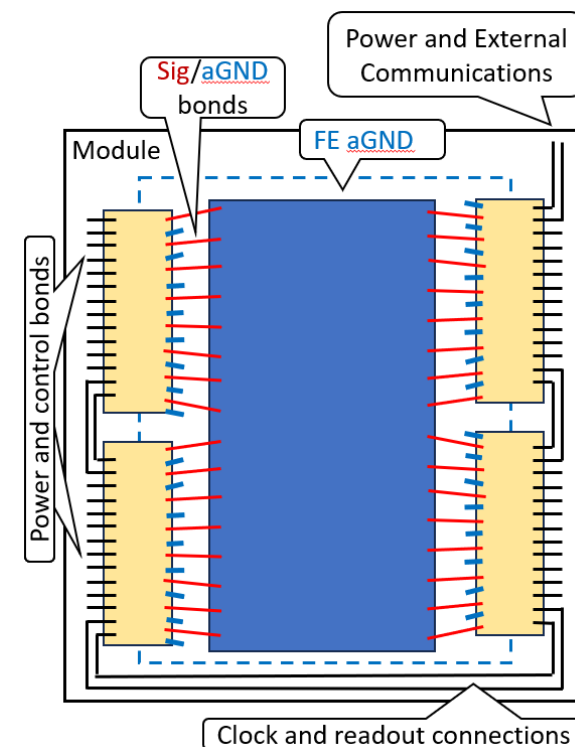
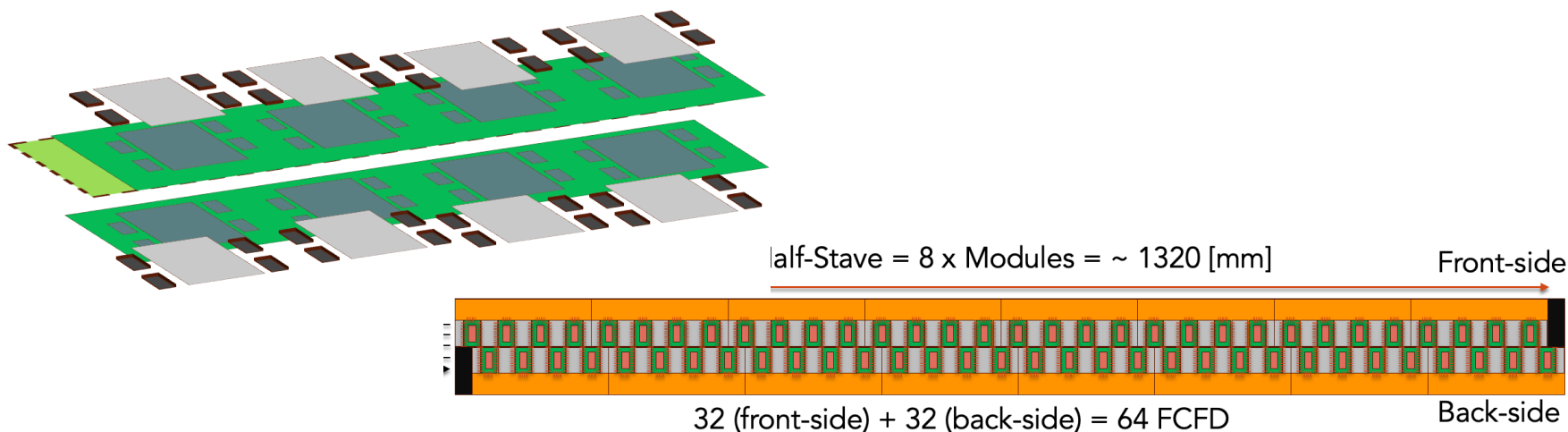
- $\sigma_T^2 = \sigma_{\text{LGAD}}^2 + \sigma_{\text{preamp/disc}}^2 + \sigma_{\text{Internal Clock}}^2 + \sigma_{\text{System Clock}}^2 + \sigma_{\text{TDC}}^2$

Component	Spec
LGAD+ preamp/discriminator	~40 ps
Internal clock distribution	< 10 ps
System clock distribution	< 10 ps
TDC binning	< 10 ps
Total	~ 45 ps

- Time resolution $\sigma_T \sim 45 \text{ ps}$
- Position resolution:
 - 30 μm in polar angle: **5-bit ADC**

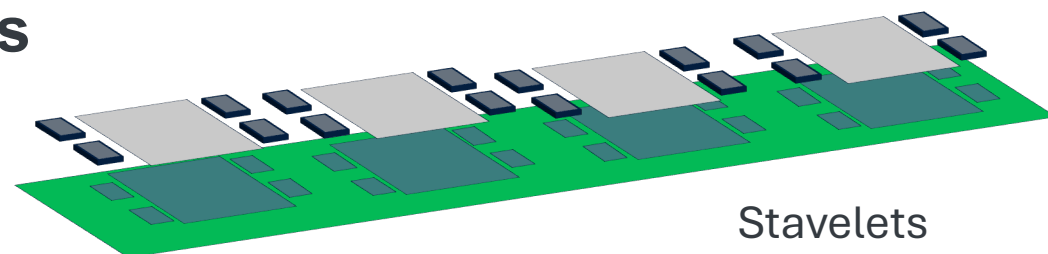
Physical interfaces and constraints

- Each sensor has 64x2 sets of strips, with 500 μm pitch
- Constraint from the system-side is to use single data line per sensor
 - Interface is **one IpGBT elink per 128 channels**
- Each sensor mounted on individual **stavelets**
- Voltage and current requirements
 - Need **2.5 V** and **1.2 V** voltages for the operation of analog
 - Need **1.2 V** for digital



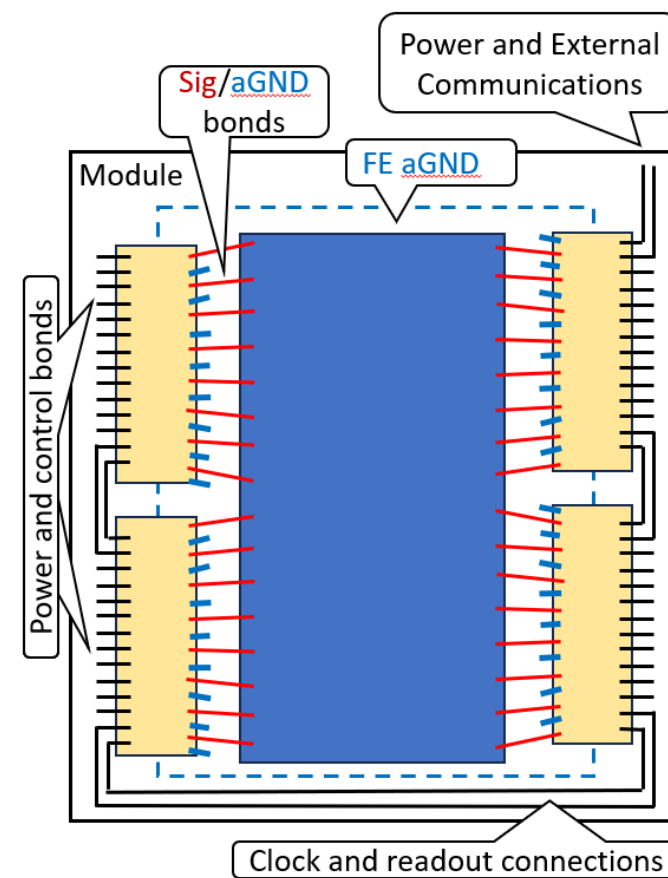
- Each sensor has 4 dedicated readout ASICs

- Simple assemblies for testing
- Easy aGND/dGND separation
- Plenty of real estate for IO and power



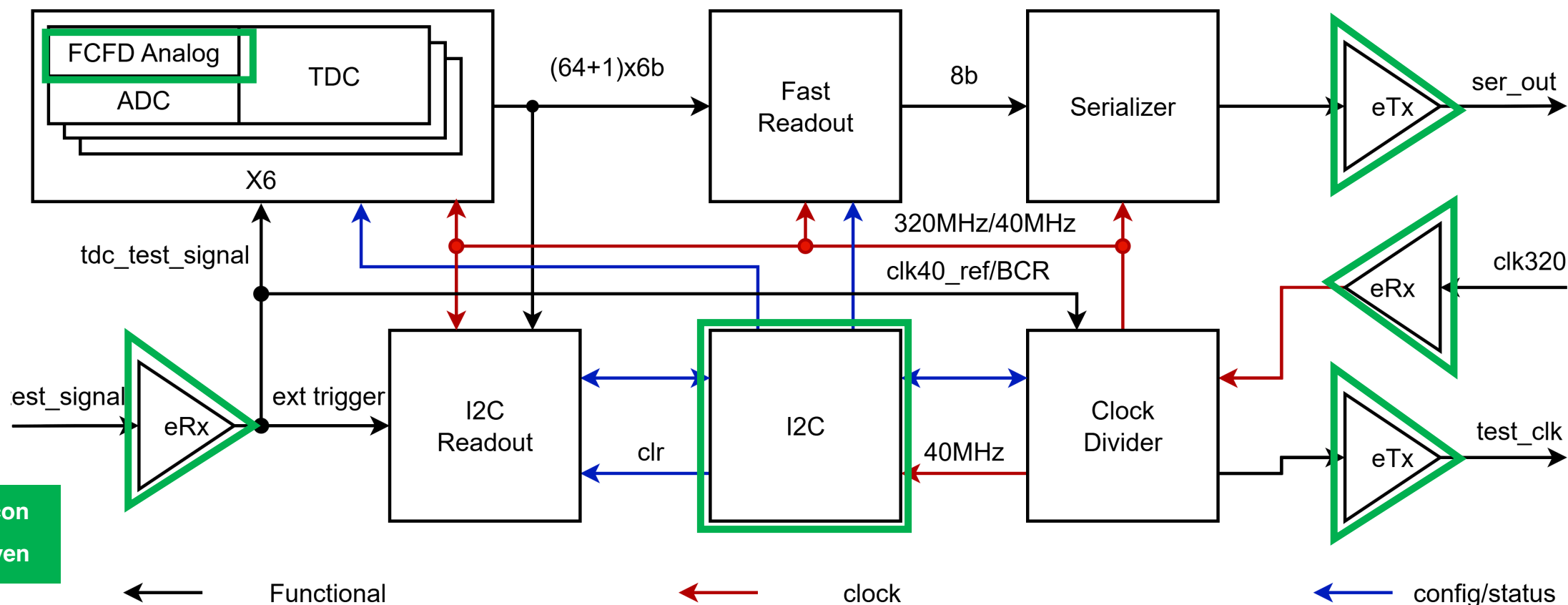
- FCFD channel counts**

- Practical chip size and aspect ratio 14-15 by 2-3 mm
- Direct wire-bonding to the sensor
- Channel pitch slightly smaller than that of the sensor (0.5mm) so to butt two chips along the sensor.
- Small fan-out angles (1mm shift for 3-4mm long bonds)
- All 4 ASICs are connected in a single readout chain
- Optimal channel count is 32-channels per chip
 - Changed from last review: was *128-channels*



FCFD1.2 prototype

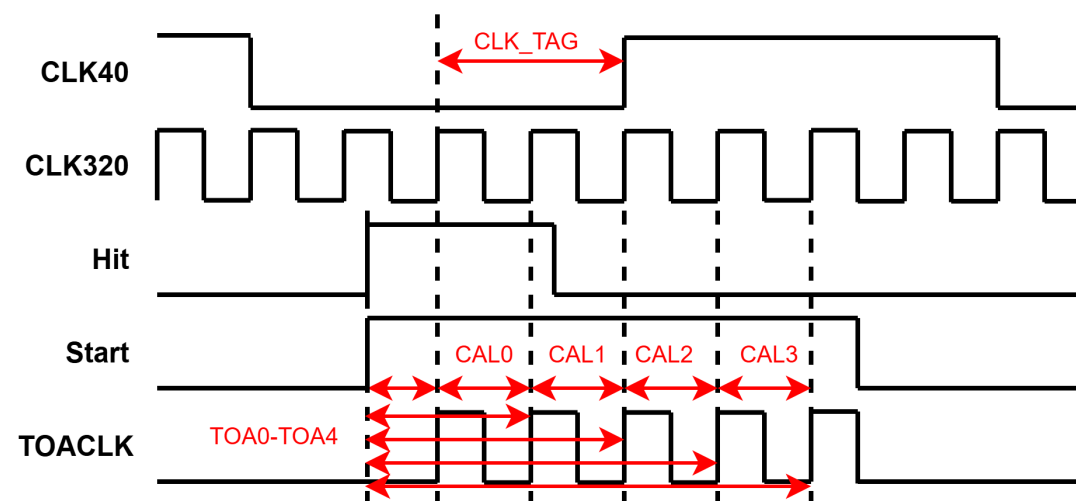
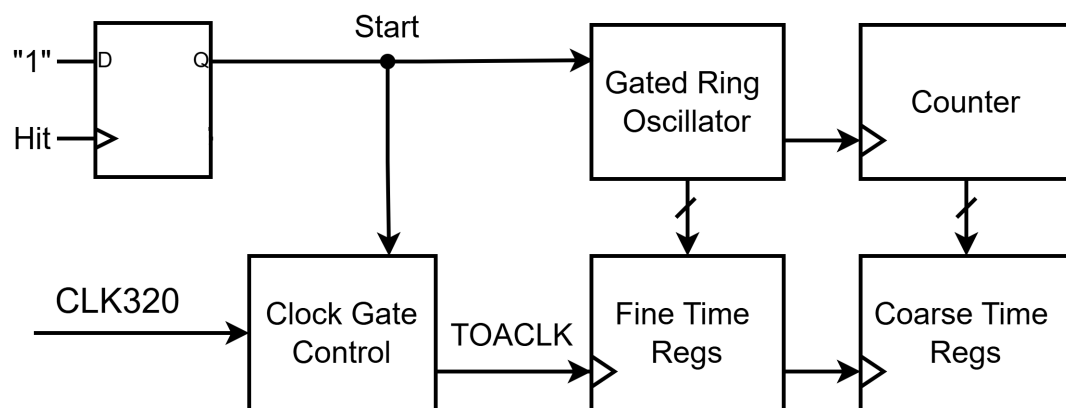
- This prototype will implement and test components beyond the FCFD analog
 - This version focuses on digitization (ADC/TDC), readout (fast/I2C) and configuration (I2C)
 - Fast readout builds data frame; I2C readout uses self/ext trigger



Silicon
proven

Self-calibrating multi-cycle TDC

- Requirements:
 - Precise time (<10 ps); Low power (~100 uW); Low occupancy (<100 Hz); No blind timing windows;
- Adopted self-calibrating, multi-cycles TDC architecture.
 - Using regular 320 MHz clock signal; using regular foundry digital standard cells
- Robust against power supply, temperature and mismatch
- The number of timestamps is programmable, up to 64

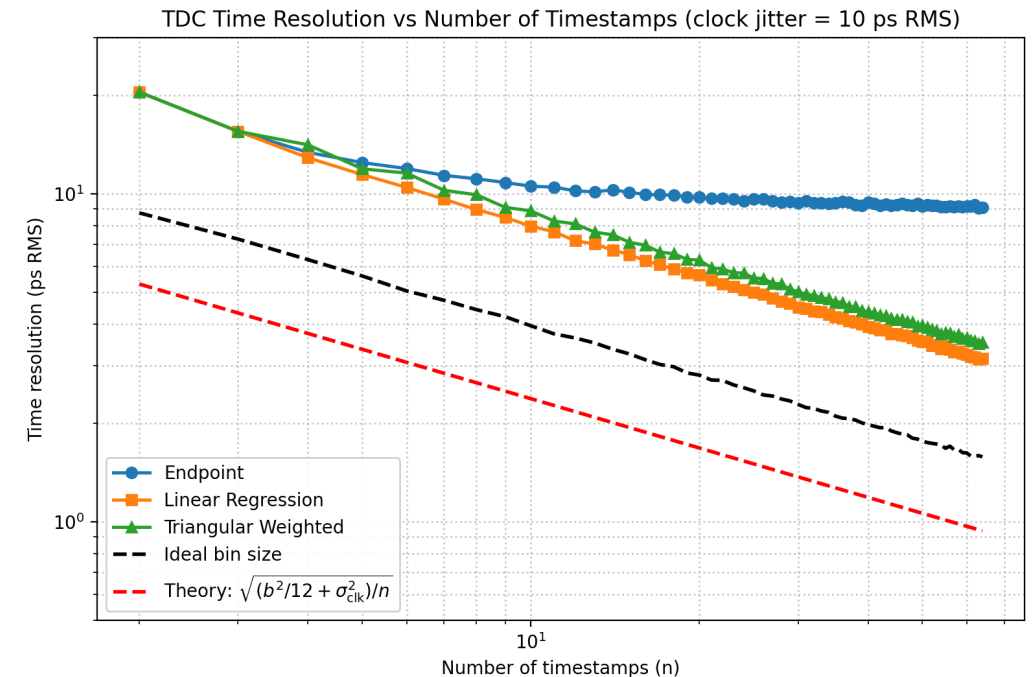
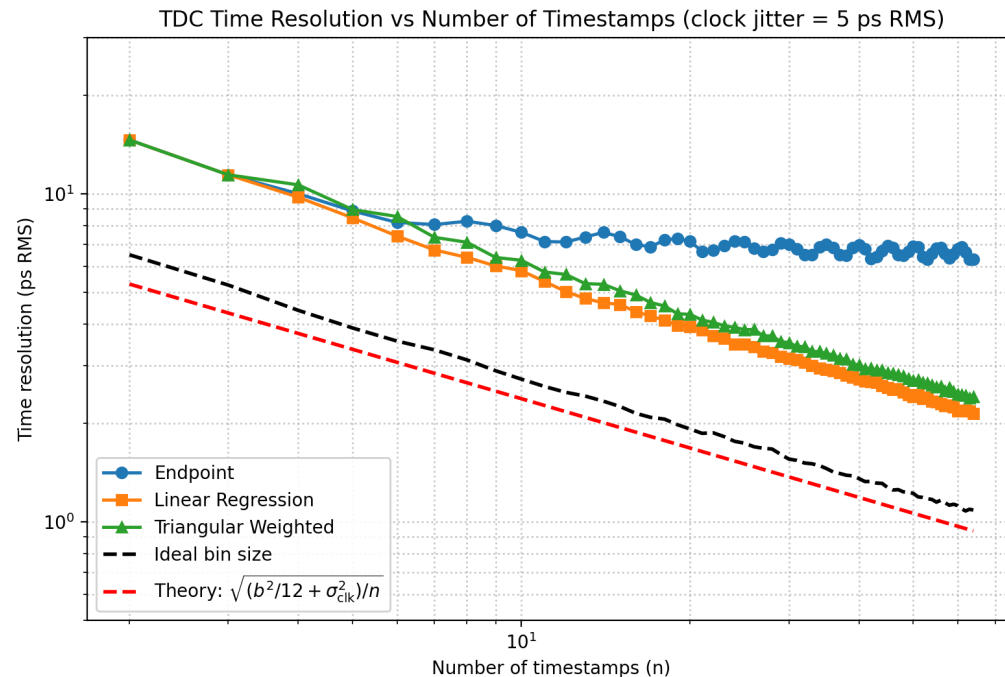
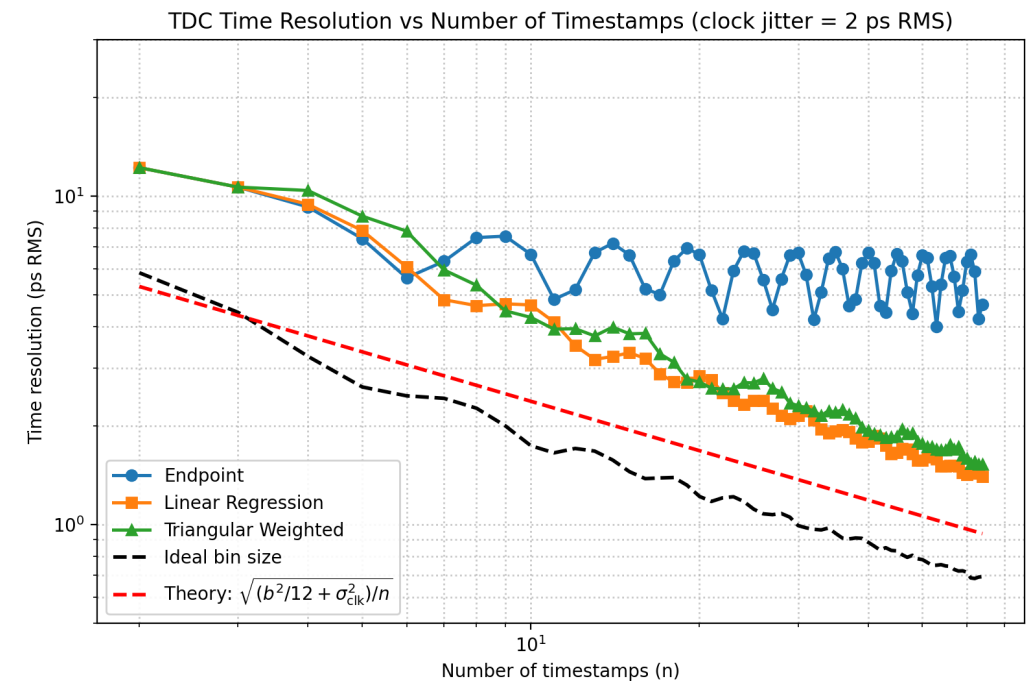




Clock jitter effects

- Multi-cycle averaging suppresses the noise resolution.

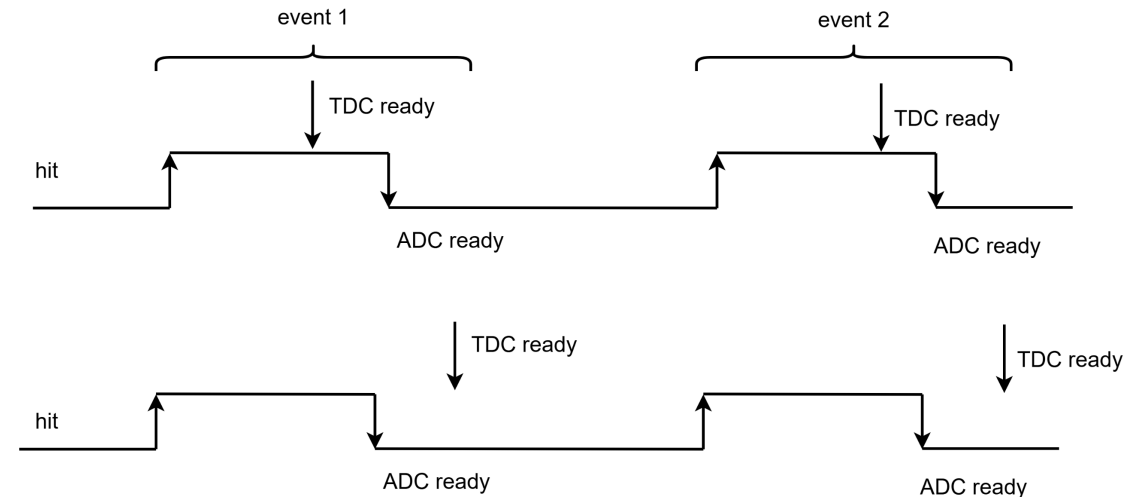
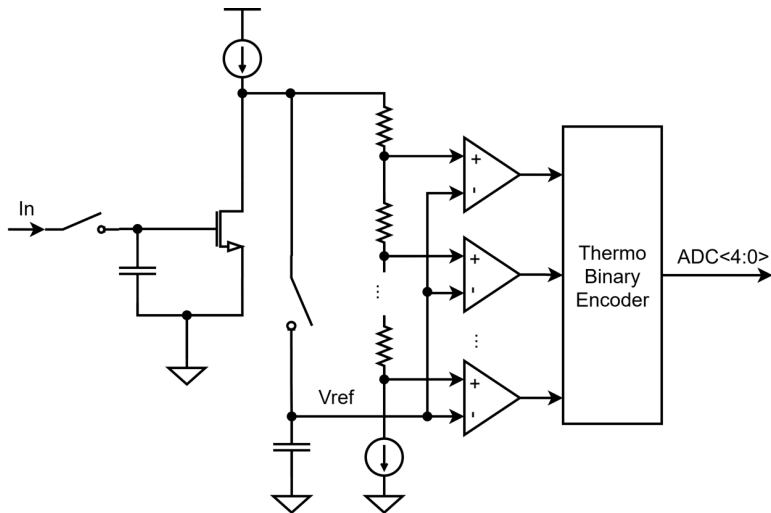
Clock Jitter (RMS)	2 ps	5 ps	10 ps
N=16	3.8	4.9	7.0
N=32	2.2	3.4	4.9
N=63	1.5	2.4	3.5





ADC for amplitude readout

- 5 bits flash ADC design
 - The LSB corresponds to 1.5 fC with a dynamic range up to 75 fC
 - ADC data is ready on the falling edge of the hit signal
- Timing-sequencing logic is implemented to maintain ADC/TDC alignment.
 - ADC data are latched on the falling edge of the hit signal.
 - Timeout logic is implemented to recover the TDC from abnormal conditions.



I2C Readout

- We implemented two methods for FCFD readout:
 - **Fast Readout** and **I2C-readout**
- I2C-Readout: extract data from TDC module using the I2C bus
 - Main purpose is commissioning and debugging
- The module provides limited capability for I2C slow readout
 - Does not have multi events storage capability
 - Only one hit is acquired, and then waiting to be readout.

Fast Readout

- Collect the TDC hit data, packages them into framed words, and transmit the resulting stream over a serial output link at 320 Mbps.
- When a TDC channel reports a hit, Fast Readout evaluates:
 - If enough space is available, the module accepts the event, formats the TDC data into a data frame, and schedules the frame for transmission.
 - Otherwise, drop the event and increment a missing counter

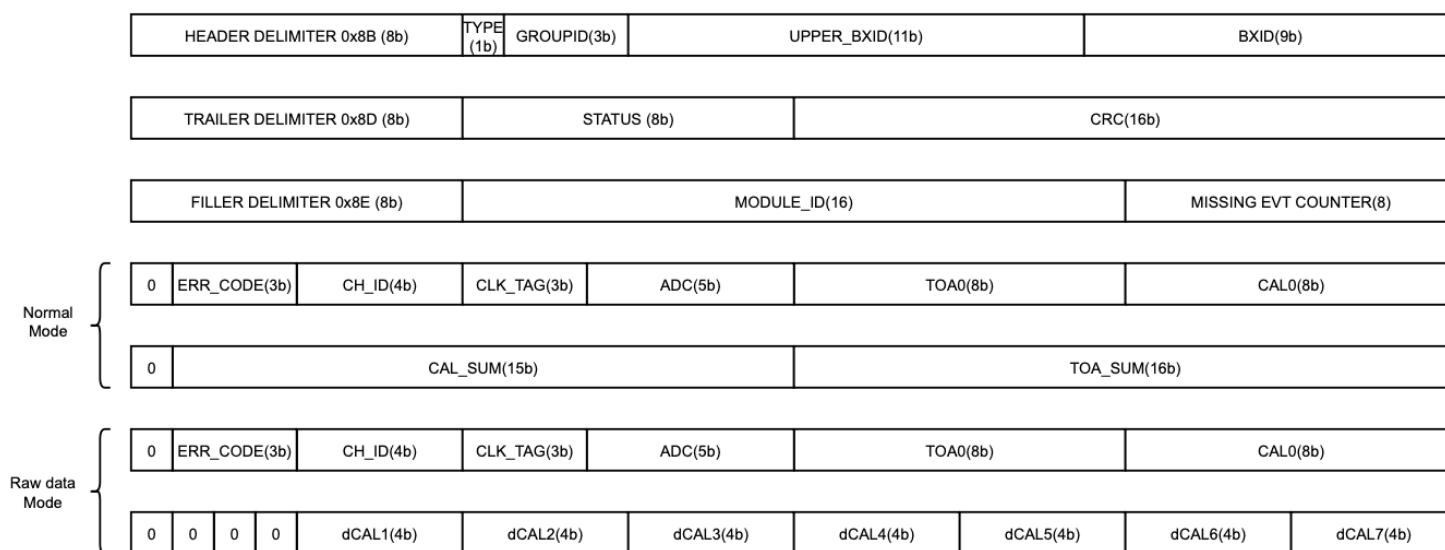


Figure 1: The FCFD data frame definition

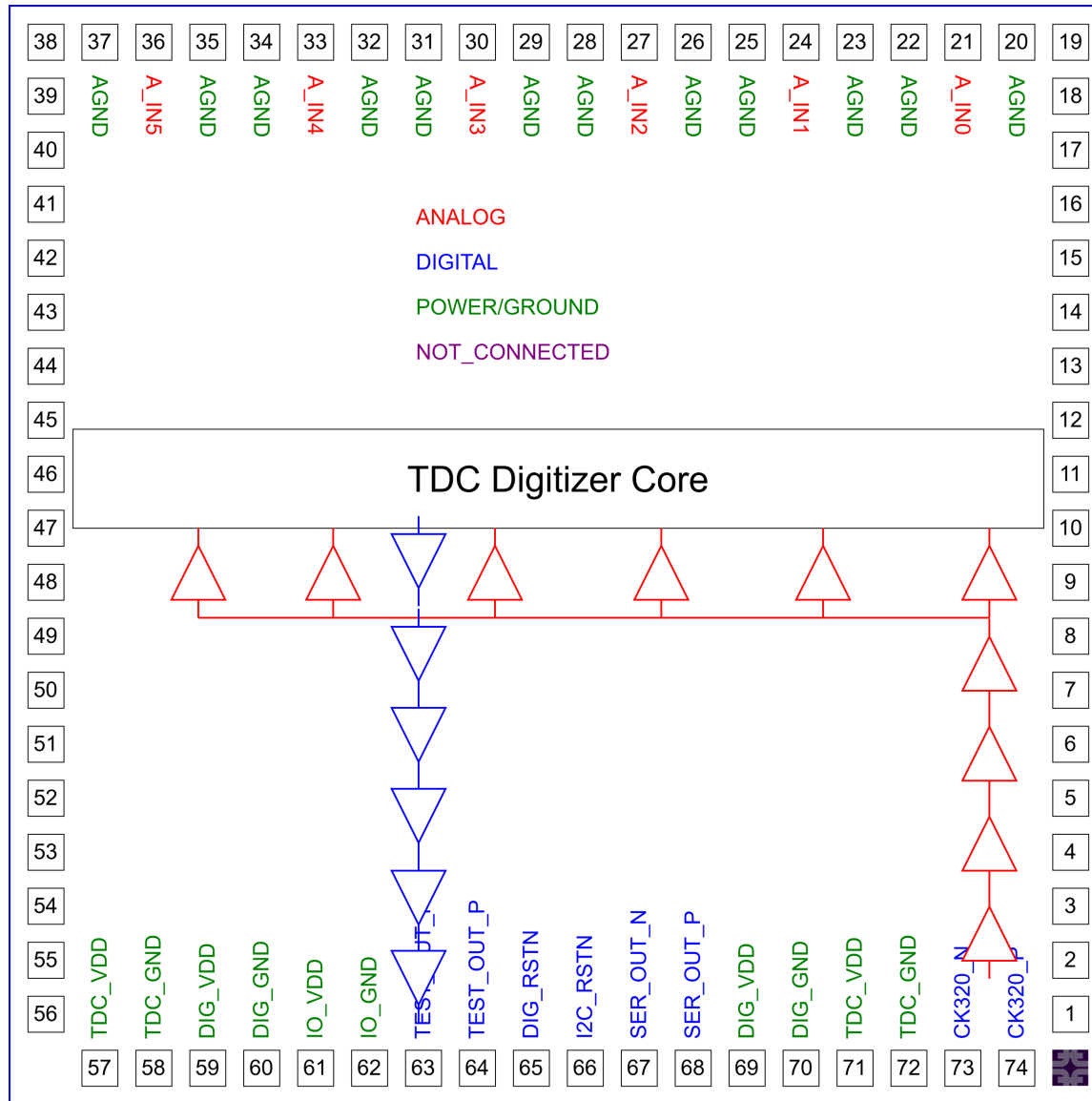
Chip floorplan

- Chip size: 3300x3000 μm
- 6 channels, 450 μm width per channel
- Analog integration for several large modules: frontend, 6 TDCs, globalDigital and pad ring





Clock distribution



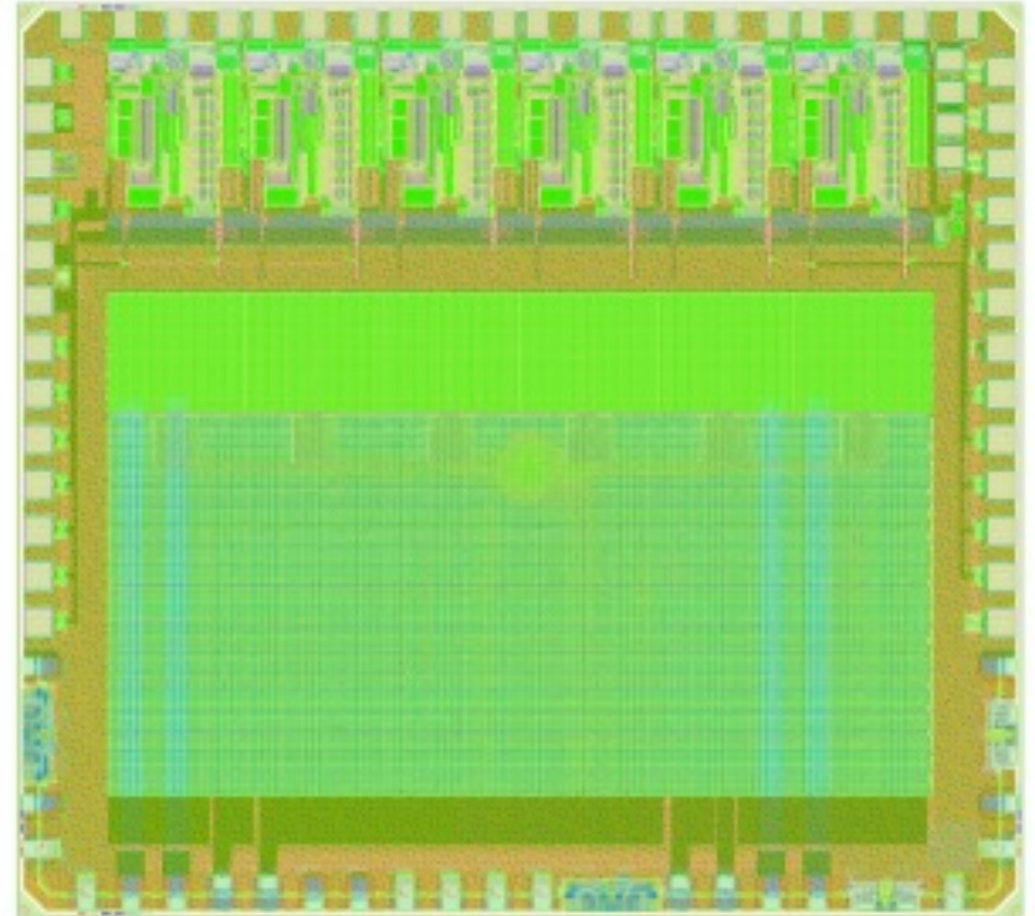
- Clk320 routed in digital power domain with clearance to other digital circuits.
- A return clock signal is output for test purpose, to evaluate the daisy-chain model for modules



Status of FCFD1.2

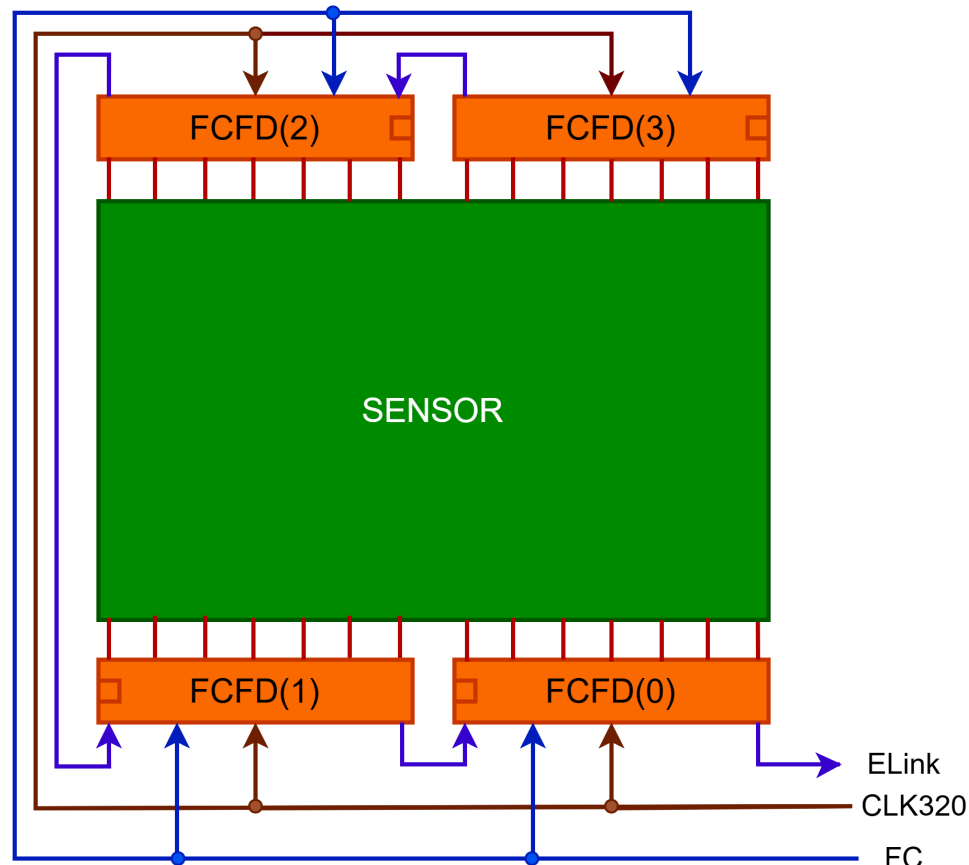
Charge #2

- FCFD1.2 was submitted on April 12, 2026
- Expect the chips back from TSMC in middle of July
- Currently working on the design of the test boards and development of the readout firmware
- Extensive testing planned for testing of the all-new ingredients separately, and the whole chip together



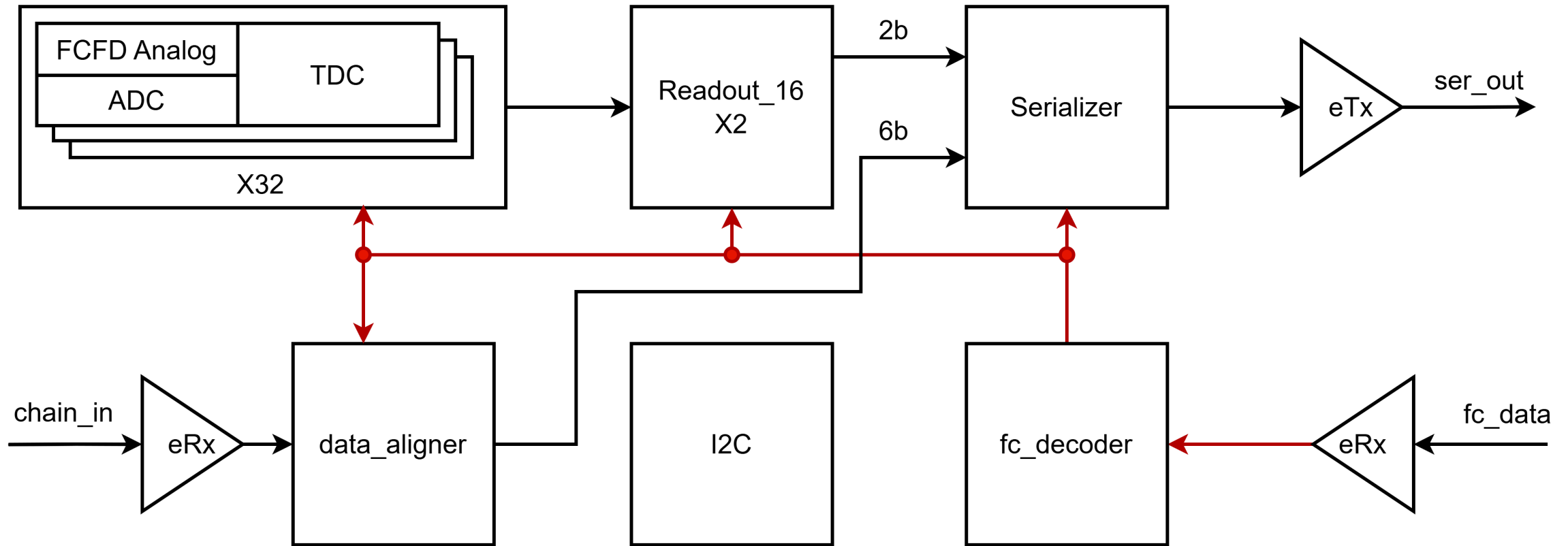


FCFD2 in the readout system



- FCFD2 has 32 channels, with analog input signals routed from one side of the chip.
- Assuming a hit rate of 30 Hz, the raw data rate per chip is approximately 130 kbps, which is far below the 320 Mbps bandwidth of a single ELink.
- This makes on-chip data aggregation a natural design choice.
- A chain structure was selected to simplify the I/O design.
- Both the clock and FC signals are distributed using a multidrop scheme. The clock signal quality will be evaluated during FCFD v1.2 testing.

Extension to 32-channel FCFD2



- Scaling up to the larger chip; Expand readout from 6 channels to 16 channels while keep data frame definition.
- Triplication for radiation protection
- Add a Fast-command decoder
- Add chaining stage for data alignment logic



Power consumption

Charge #1, 2, 6

	Unit power(mW) (32-ch)	Units in FCFD32	FCFD32_Power(mW)
analog_front (2.5V)	2	32	64
analog_front (1.2V)	1.6	32	51.2
TDC	0.2	32	6.4
eRx	1	2	2
eTx	2	1	2
Readout16	30	2	60
Serializer	3	1	3
fc_decoder	5	1	5
data_aligner	2	1	2
I2C	2	1	2
Total (mW)			197.6
Total (mW) for 2.5V			64
Total (mW) for 1.2V			133.6

Summary

- FCFD : codesigned with the sensor and full-system constraints in mind, and the design is well advanced
- Many rounds of prototyping and characterization since 2021 demonstrated its robust performance
 - Performance of the analog front-end demonstrated
 - Latest version FCFD1.2 is the next big step towards the bTOF
 - Extensive testing and characterization of the prototype with IR-laser, sources, and beams is being planned
 - System-tests with prototype stavelets will enable early testing of the full system
- The FCFD2 is planned for production in the end of 2027, and FCFD3 towards the end of 2028, and consistent with detector construction schedule



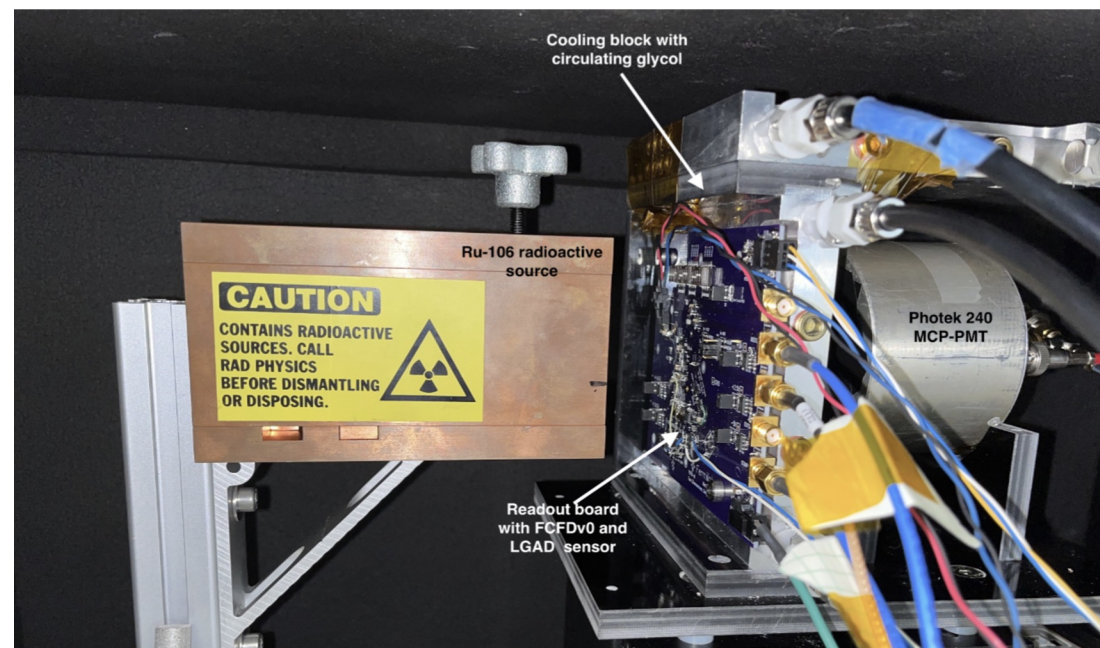
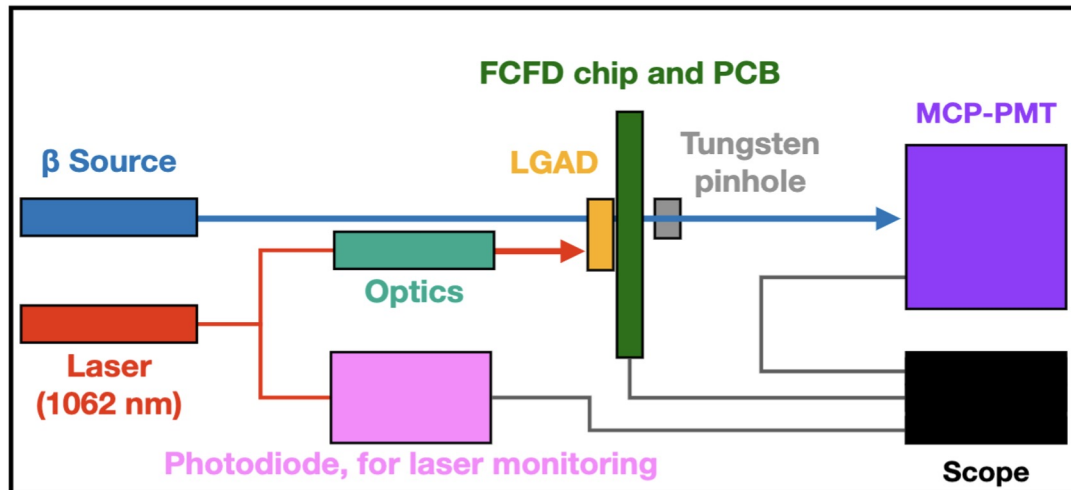
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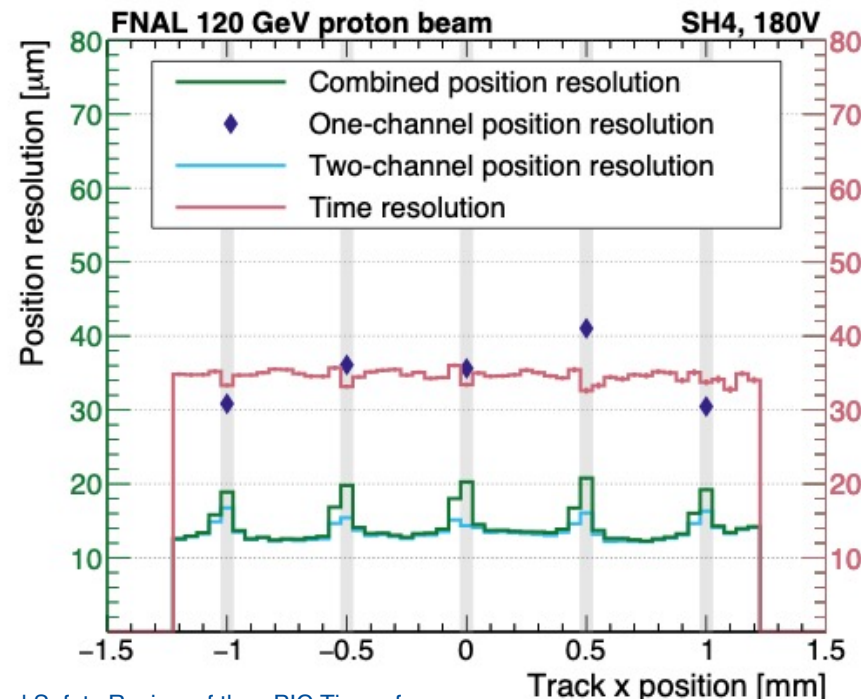
⚙️ Performance measurements setup

- We measure performance of the prototypes using several types of signals
 - Charge injection, picosecond IR-laser, β -source, and test beam
- Dark box with motorized stages, enabling laser injection and beta source
 - Collimator and MCP time reference detector ensures straight trajectories: get beta rates of about 2-3Hz at best alignment



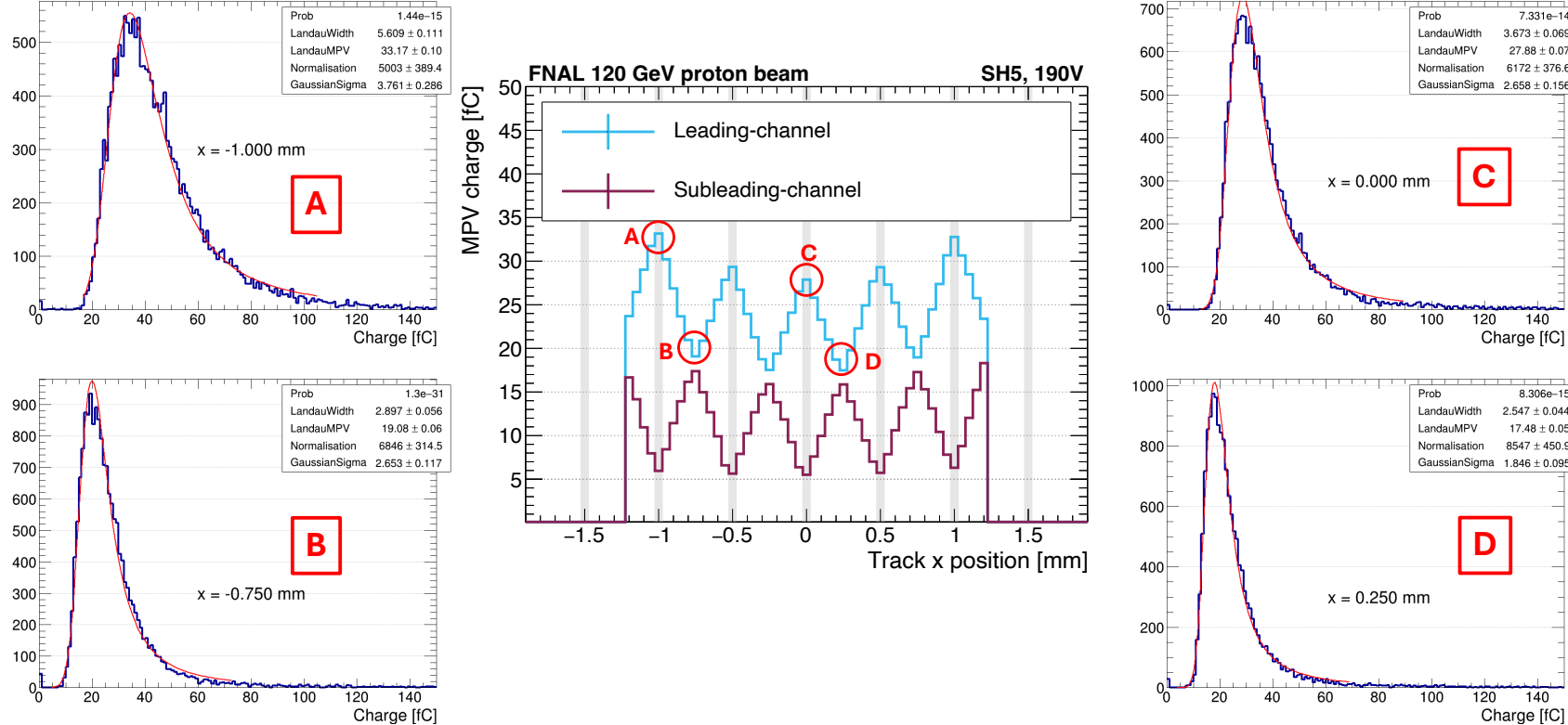
Time resolution measured in test beam

- Time resolution is measured by combining leading and sub-leading channels
- Measurements performed on dedicated readout boards using commercial amplifiers and with full waveform analysis
- More details in the paper: [arXiv:2407.09928](https://arxiv.org/abs/2407.09928)





Signal characteristics



- Signal characteristics that went into plot on previous page
 - Dynamic range: 10 - 70 fC
 - Signal MPV : 25 fC
 - Jitter at MPV : around 20 ps



Sensor properties

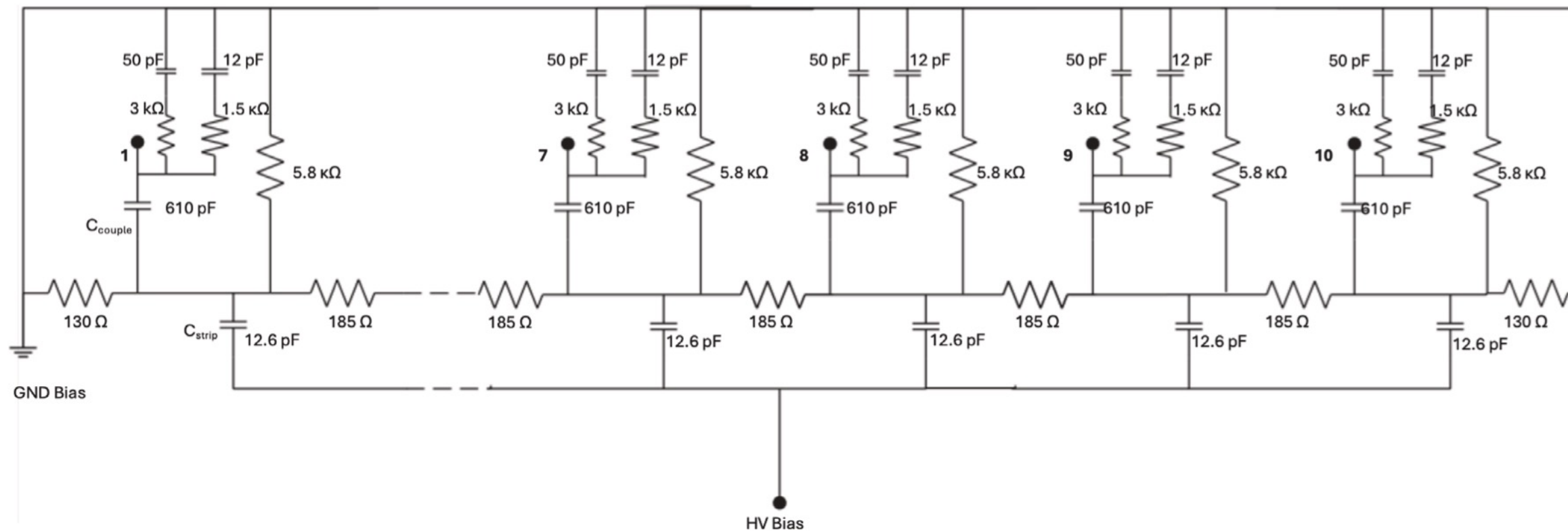


Fig. 5. The schematic diagram of the extracted model for the 1-cm long AC-LGAD strip sensor.