

AC-LGAD Readout Chain Report

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For the AC-LGAD Readout Team (Rice, BNL)
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U.S. DEPARTMENT
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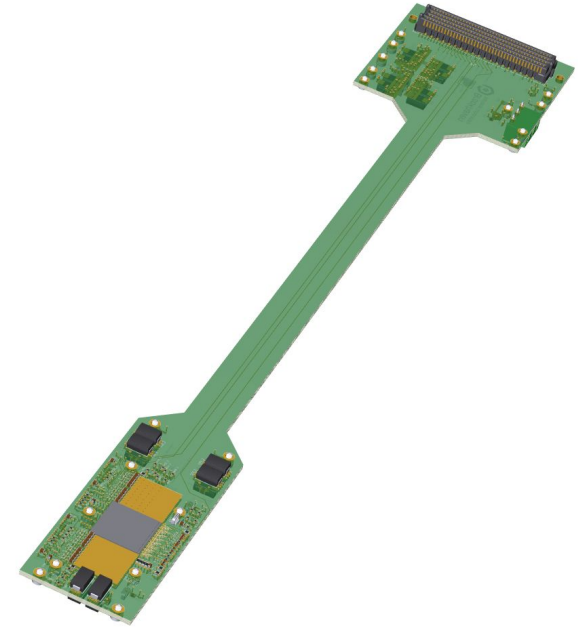
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EICROC Status

- ZCU106 FPGA integration
 - common FW completed (with readout SW)
 - *tested and working*
 - EICROC1, EICROC0A commissioned
 - EICROC0 planned for next week
 - 1 EICROC1 Testboard and 1 ZCU106 also at Rice for further evaluation
- EICROC1 and RBv1 integration started
 - EICROC1 Testboard modified at BNL and connected to RBv1 via Mike's adapter
 - and then fibered to AXAU15 connected over PCIe to a PC for readout
 - ⇒ full readout chain
 - I2C works
 - 320 MHz clock from IpGBT to EICROC1 is *working*
 - Various control lines from IpGBT (e.g. RESETB, etc) are *working*
 - I2C lines are *working* after a particularly tricky required modification to the Testboard
 - Mike's adapter card *works*
 - RBv1 is working, FW is working, SW is working
 - Milestone!
 - Next step (this & next week) is the EICROC1 data readout over IpGBT into the PC
 - expected to go reasonably quickly due to the significant amount of experience gained with FPGAs

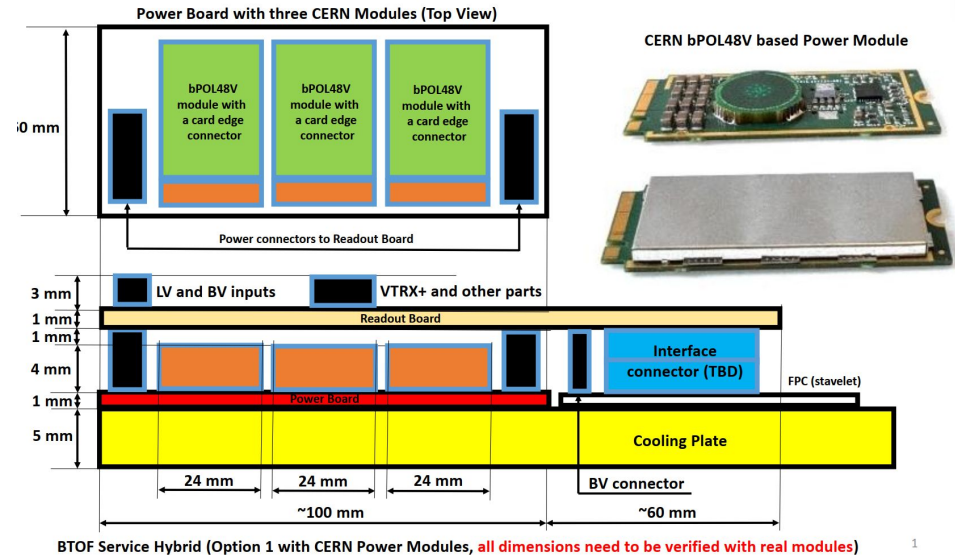
Roman Pots 3x ASIC Module

- Jack (BNL) designed an ASIC Module for Roman Pots and friends
 - 3X EICROC1 ASICs
 - FMC connector for readout & control
 - can be connected to ZCU106
 - can also be connected to RBv1 with Mike's adapter
 - long PCB simulates a longer cable required for RP
 - lots and lots of testpoints and conservative powering approaches
 - expected to be slimmed down after testing
 - with input from Alex, Christophe, Mike, TL
- Schematics & Layout complete
 - internal mini Review started, to be completed early next week
- Expect 5-10 pieces produced



Barrel TOF Service Hybrid

- discussions within the BTOF Group (especially mechanics) about the dimensions of the SH... ongoing...
 - requirements keep changing week-to-week so not yet ready – waiting for external decisions
 - low profile DC-DC converters required – considering CERN's bPOL48 modules [Mike]
 - or event better, the new Hungarian modules currently in development [Gabor, Norbert]
 - additional open questions are the choice of the signal connector as well as the power distribution
 - all of this needs information from the FPC designers
 - Mike presented some ideas but we are still waiting...



Summary

- Moving forward...
- Expectations within a month:
 - EICROC1 integrated with RBv1 (aka lpGBT)
 - Roman Pot 3x ASIC Module PCB's in production
 - FCFD integrated with RBv1?
 - although waiting for the Fermilab Testboard and ASIC
 - BTOF SH design complete?
 - although we depend on external decisions