10 psTOF (mRPC) Update

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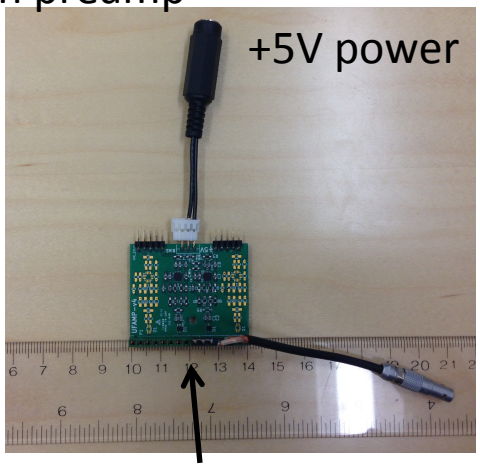
Since July 2017…

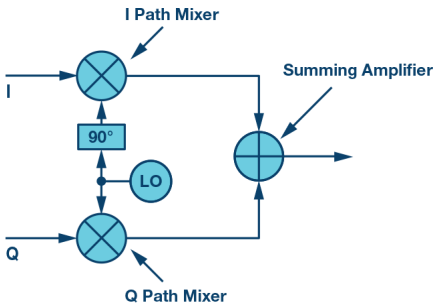
- $5K funding to CCNY group
  - Only funding mRPC TOF has ever received from EIC Detector R&D program (previous 1 FTE post-doc was funded under eRD10)
  - Funding sent to CCNY a couple of months ago. Little done so far on this, except undergraduate students learning part-time about RF design.
  - This summer they should be working full time on it
    - Meeting next week between BNL and CCNY
- Previously requested funding to develop sub-10 ps capable DRS4-based electronics readout card that could work at the EIC
  - Main feature that needs to be added is modification of DRS4 eval board to one based ROI based readout
  - Not funded by EIC R&D, but recently received SBIR Phase I funding with BK Technology.
- Working toward sPHENIX mRPC prototype of barrel TOF
  - In Heavy Ion Collisions only TOF can work due to high multiplicities.
  - Heavy interest from several HI groups (China, Japan, US) for even 20 ps TOF
  - If this goes through, use this as a test bed for EIC implementation

UFAMP Preamp Work

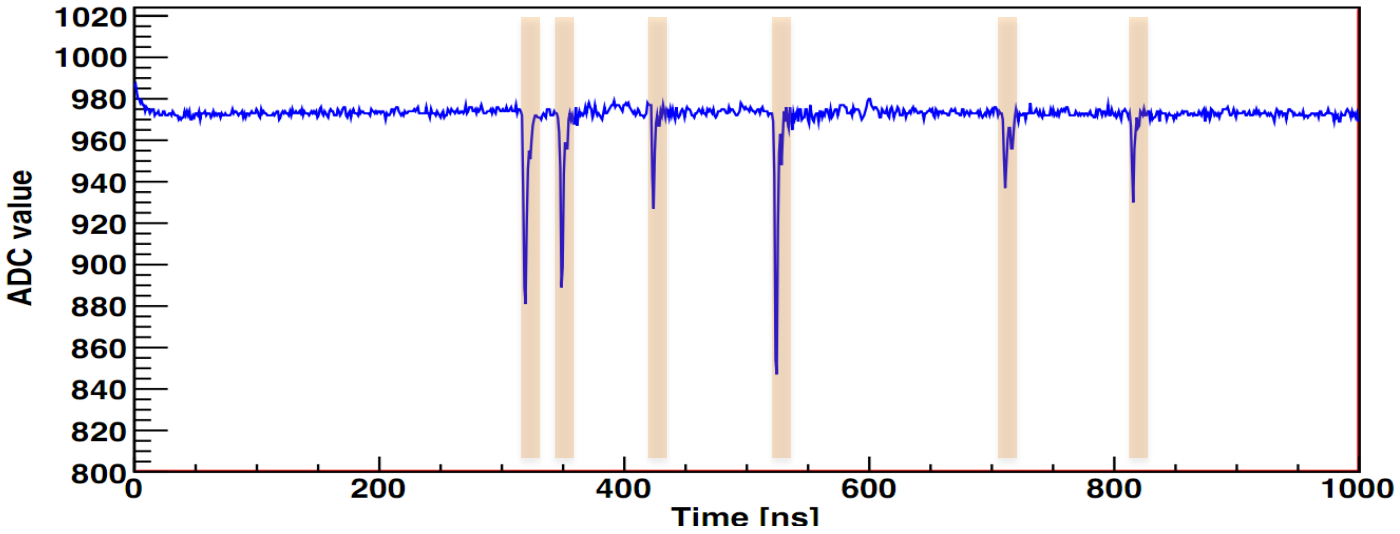
4 ch preamp



- Needs removal of parasitic capacitor to restore 900 MHz bandwidth from 300 MHz – done
- Impedance matching to inputs to reduce oscillation in signal
  - Now thinking how to do summation of 4 signals better
  - Use RF Mixer?



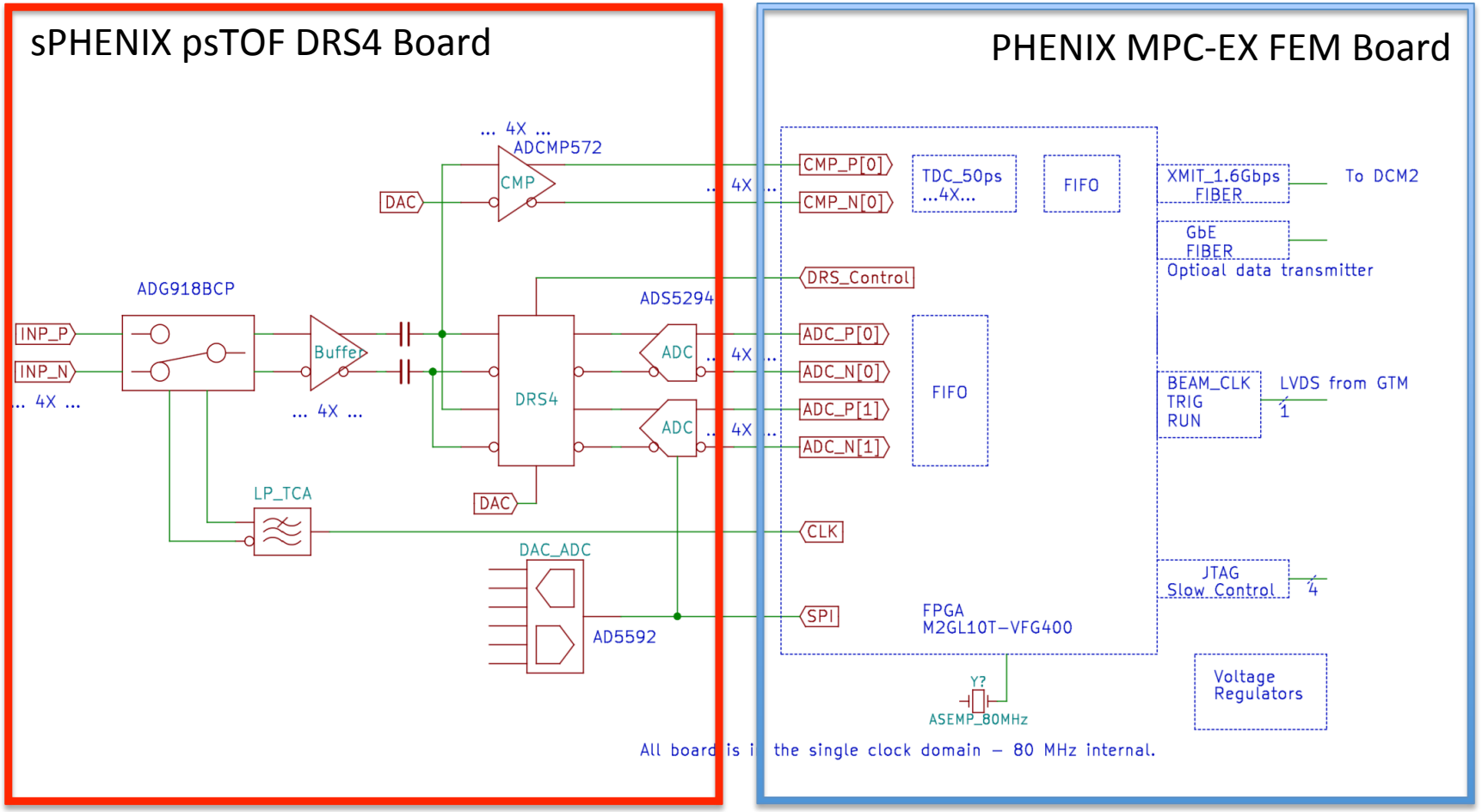
Region of Interest (Windowed) Readout



- DRS4 running at 5 GSPS takes 200 ns to fill 1024 SCA buffer
- Collider trigger signals require at least a few µs to be sent to FEM
  - PHENIX trigger latency is 4 µs >> 200 ns.
- To solve this, we propose to use the ROI readout for the DRS4 – have a fast LOCAL threshold trigger on each channel, and digitize small window immediately
- Need to generate accurate timestamp for ROI (my main worry right now)
- Digitizing a 6 ns window with a 37.52 MHz ADC (4x RHIC clock), takes ~3 µs (1+2 overhead), where the DRS4 is dead
- Q: What is deadtime effect? At 100 kHz Au+Au rate, we expect about 500 tracks on average per event, over 10K channels, or 5 kHz hit rate on one channel
  - Poisson prob P(N>=2; 5 kHz hits and 3 us deadtime) ~ 1.5% lost events

DRS4 ROI Electronics Block Diagram

Preamp Input



- Block diagram for DRS4 prototype board using windowed readout for EIC
- psTOF DRS4 Board layout hopefully done by end of July
- China funding passed 1st review, but need another review. Money won't come until early next year. Likely to consider asking EIC R&D committee for funding.

Electronics (DRS4FEM & AARDVARC)

- SBIR Phase I to develop DRS4FEM
  - Basically a subset of the DRS4 eval board that enables ROI readout to overcome problems with short buffer depth (200 ns of signals becomes very long)
  - Use 8 channels instead of 4 (4 channels x 2 ends on one mRPC module)
  - Maintain ~1-2 ps resolution
  - 1 year to build this out (Phase I schedule)
  - Read out with existing PHENIX MPC-EX FPGA Board
- Alternate solution
  - AARDVARC ASIC from NALU Scientific
  - It's their waveform digitizer that is designed to be capable of sub-10 ps resolution
  - ROI readout possible as well, deep buffer
  - 1st tape out expected late Summer/Fall this year

Clock Propagation

Si5338

SILICON LABS

I²C-PROGRAMMABLE ANY-FREQUENCY, ANY-OUTPUT QUAD CLOCK GENERATOR

Features

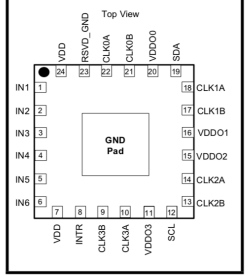
- Low power MultiSynth™ technology enables independent, any-frequency synthesis on four differential output drivers
- PCIe Gen 1/2/3/4 Common Clock and Gen 3 SRNS compliant
- Highly-configurable output drivers with up to four differential outputs, eight single-ended clock outputs, or a combination of both
- Low phase jitter of 0.7 ps RMS typ
- High precision synthesis allows true zero ppm frequency accuracy on all outputs
- Flexible input reference:
  - External crystal: 8 to 30 MHz
  - CMOS input: 5 to 200 MHz
  - SSTL/HSTL input: 5 to 350 MHz
  - Differential input: 5 to 710 MHz
- Independently configurable outputs support any frequency or format:
  - LVPECL/LVDS: 0.16 to 710 MHz
  - HCSL: 0.16 to 250 MHz
  - CMOS: 0.16 to 200 MHz
  - SSTL/HSTL: 0.16 to 350 MHz
- Independent output voltage per driver: 1.5, 1.8, 2.5, or 3.3 V
- Single supply core with excellent PSRR: 1.8, 2.5, 3.3 V
- Independent frequency increment/decrement feature enables glitchless frequency adjustments in 1 ppm steps
- Independent phase adjustment on each of the output drivers with an accuracy of ≤20 ps steps
- Highly configurable spread spectrum (SSC) on any output:
  - Any frequency from 5 to 350 MHz
  - Any spread from 0.5 to 5.0%
  - Any modulation rate from 33 to 63 kHz
- External feedback mode allows zero-delay mode
- Loss of lock and loss of signal alarms
- I²C/SMBus compatible interface
- Easy to use programming software
- Small size: 4 x 4 mm, 24-QFN
- Low power: 45 mA core supply typ
- Wide temperature range: –40 to +85 °C

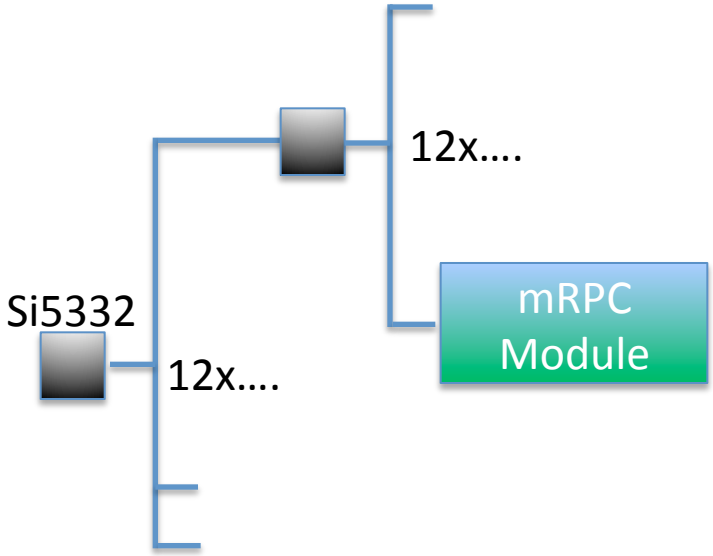
Applications

- Ethernet switch/router
- PCIe Gen1/2/3/4
- Broadcast video/audio timing
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fibre Channel, SAN
- Telecom line cards
- 1 GbE and 10 GbE

Ordering Information:
See page 42.

Pin Assignments





- Generic problem in TOF systems to propagate clock out to several meters with low jitter
- Testing above solution, which takes clock and fans it out to several identical outputs with sub-ps jitter
  - Si5332 has 1 clock in and 12 out and 230 fs jitter
- For sPHENIX Barrel, need 1500 modules
  - 3 levels of 12x clock propagation (144 Si5332 needed)
  - Jitter naively should be sqrt(3)*230 fs