

Modular, low cost readout electronics for mRICH at EIC

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EIC- mRICH Requirements

Problem statement:

- Readout of compact H13700 MCP-PMT
- Compact and dense: 256 channels in 2"x2"
- Timing resolution: ~100ps
- Long buffer
- Abutted tiles
- Might convert to SiPM array later
- Minimize analog cabling (noise and cost)



EIC- mRICH Proposed Solution

1st gen mRICH prototype based on existing TARGETX chip:

- 1GSa/s full waveform sampling
- 16 us trigger buffer
- 16 channels
- Built-in comparator generates trigger primitives
- Low cost 250nm CMOS
- Avoid costly cabling

Already used in 4 projects – developed FW/SW base:

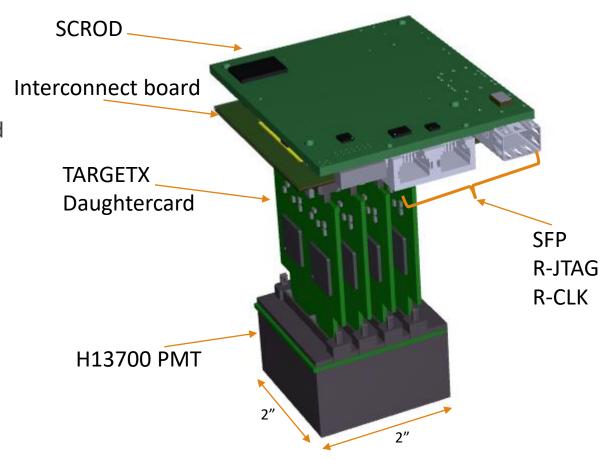
- Belle II KLM upgrade, ~20k SiPM channels
- Borehole Muon Detector (BMD) prototype: ~100 SiPM channels
- Hawaii Muon Beamline (HMB): ~60 SiPM channels
- Cherenkov Telescope Array (CTA) ~2k SiPM or PMT /telescope



Rev 1.0 Design – building block

Benefits:

- Better mechanical fitting and PCB routing
- Placed 4x TARGETX chips on one daughtercard
- SCROD (s6 FPGA) boards already fabricated and tested
- Interconnect card purely passive routing
- Reuse KLM detector readout FW and SW
- Can readout all 256 PMT channels
- Compatible with abutting 2x2 PMTs



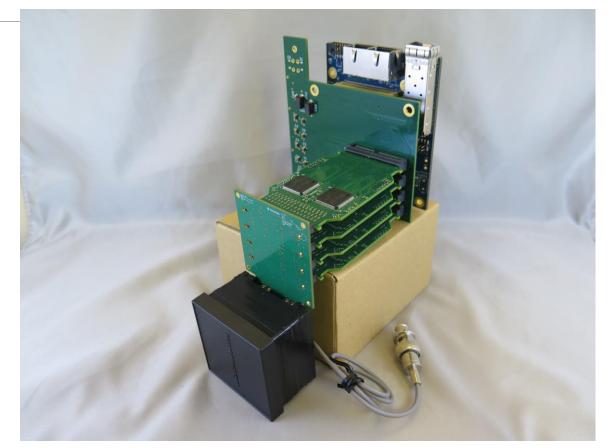


TargetX based readout for PMT

All boards/mechanical assembled for 1x PMT

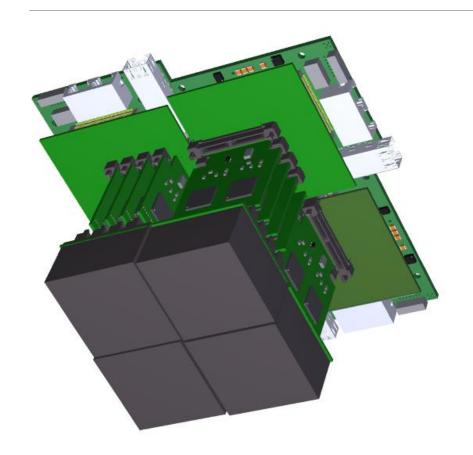
FW is variation/recompile of Belle II TARGETX based readout – almost ready

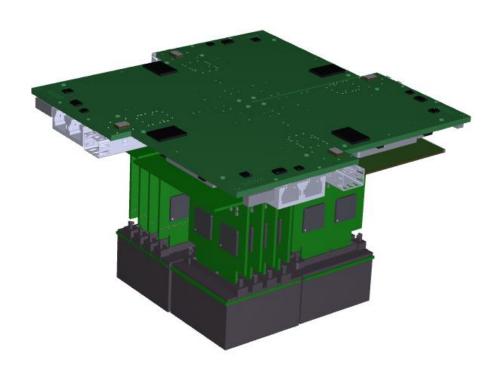
Ethernet based interface





Full 1024 channel readout

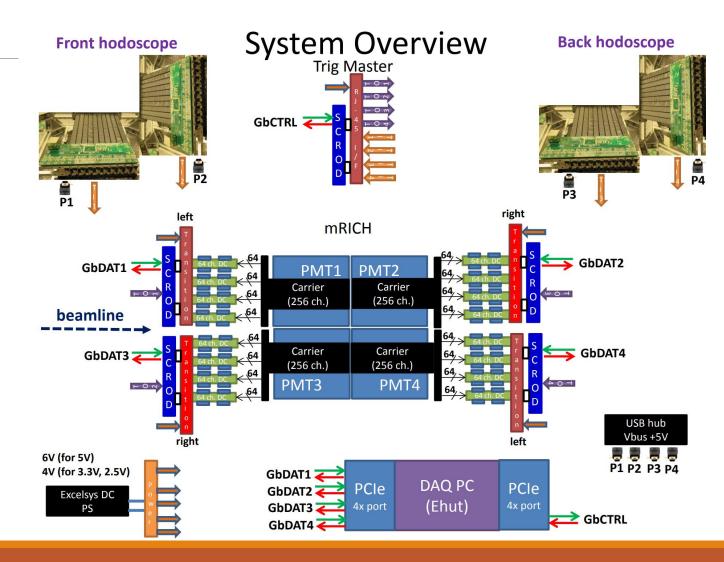






Hodoscope Readout

- TargetX based HW
- All mechanical and electrical assembly done
- 2x FW required:
 - Daughtercard(DC)
 - SCROD (data aggregator)
- FW Status:
 - Compiled
 - Communications up
 - Register read/write ok
 - Python Scripts working
 - Scanning regs/thresholds now





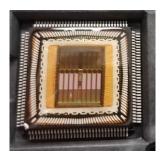
Progress

Hodoscope setup replicated and under test at UH

1x PMT readout module ready for FW testing

2nd generation roadmap: SiREAD

- Specialized full waveform sampling SiPM/PMT readout System-on-Chip with proto 32 channels
- Initial testing of SiREAD complete results to be presented at NSS/Sydney
- Various small 'bugs' found in chip that require re-submission
- Will evaluate another Phase I SBIR attempt soon





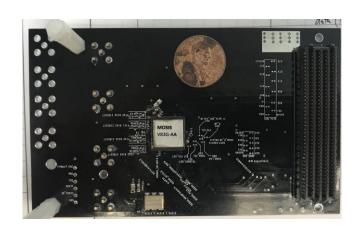




Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Readout	Available Date
ASoC	3-5	0.8	32k	8 (4 proto)	35	Fast serial	July 2018
AARDVARC	6-10	2.5	32k	4-8	4-8	Fast serial	Aug 2018

- **ASoC**: Analog to digital converter System-on-Chip
 - Rev 1 under test –Ongoing Phase II eval card available end of July
- AARDVARC: Variable rate readout chip for fast timing and low deadtime
 - Rev 1 under test Recommended for Phase II





ASoC Eval Card

All chips, are designed with commercial grade tools and licenses and can be sold once commercialized.

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