The LHCb Upgraded Readout Architecture

Fast Readout Control for the Upgraded Readout Architecture of the LHCb Experiment at CERN

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The New Timing and Fast Readout Control System (S-TFC)

- Distributed timing, trigger and synchronous commands
- Manages the dispatching of events to the Processing Farm
- Rate regulates the system taking into account back-pressure on the TFC

Distribution of Fast and Slow Control Commands

New S-TFC system controls the entire readout architecture:
- Transmits timing, fast and slow control to the Front-End via the same optical link, sharing the bandwidth
- Transmits timing and fast control to the Readout Board via optical links and/or ATCA backplane
- Transmits synchronous LHC clock to entire readout architecture

System must be sufficiently robust to ensure synchronicity across the entire readout architecture, buffer control and event management.

System must be sufficiently flexible to allow changes on-the-fly in order to satisfy evolving requirements

System must be used in test-benches and test-stands in order to test compatibility with global specifications [1].

System must be interfaced to all components of the readout architecture.

The New Timing and Fast Readout Control System (S-TFC)

- Fan-out timing and control information (TFC) to Readout Boards
- Fan-in throttle information from Readout Boards
- Distributes TFC information to FE
- Distributes control configuration data to FE
- Receives control monitoring data from FE

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Fast and Slow Control to FE via same optical link

- FE & Readout Interface Board
- FE / to Readout Boards
- Readout Boards
- LHC Interfaces

TFC

= clock receiver

= clock transmitter

1.

2.

3.

4.

 Protocol drivers build GBT-SCA packets with addressing scheme and bus type for associated GBT-SCA user busses to selected FE chip (GBT-SCA supported protocols)

Clock Distribution

LHC Interface

- GBTx
- CCPC
- PCie Slave

Memory Map with internal addressing scheme for GBT-SCA chips + FE chips addressing, e-link addressing and bus type: content of memory loaded from ECS

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Global Simulation

Clock-level global simulation under development:
- general-purpose framework
- tool independent
- shared across collaboration

Used to validate new Front-End electronics and readout logic:

References: