Fast Readout Control for the Upgraded Readout Architecture of the LHCb Experiment at CERN

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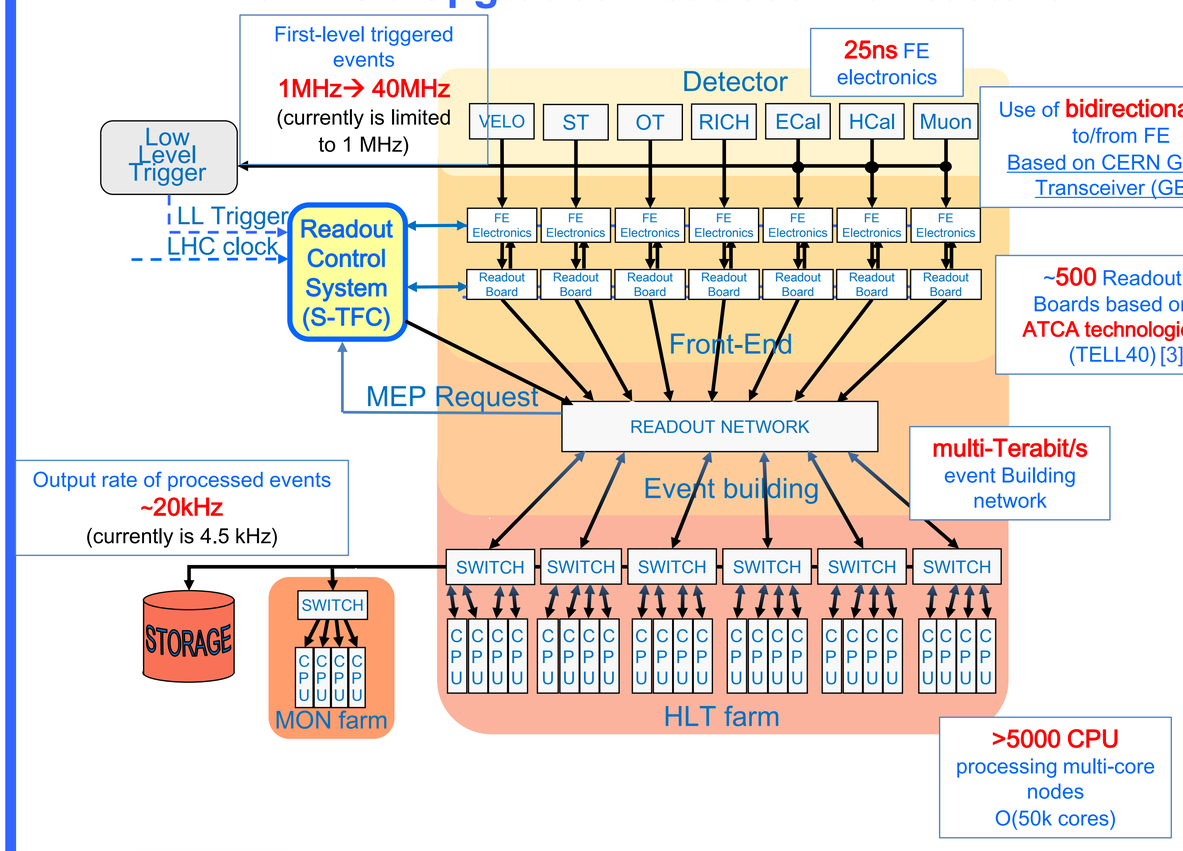
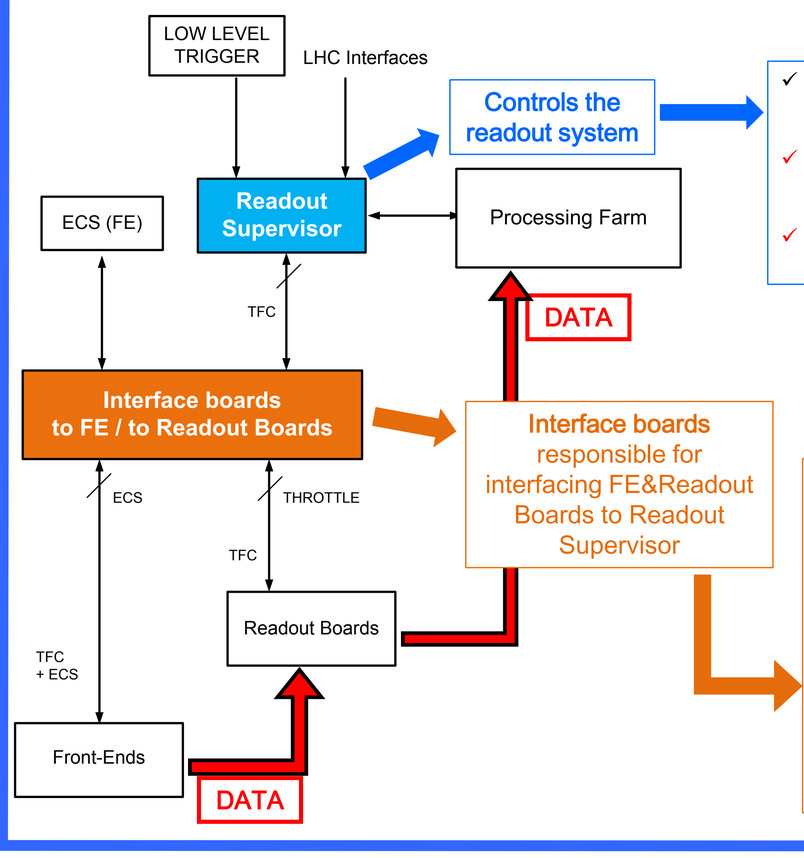
The LHCb Upgraded Readout Architecture



The New Timing and Fast Readout Control System (S-TFC)



- ✓ Distributes timing, trigger and synchronous commands
- ✓ Manages the dispatching of events to the Processing Farm
- ✓ Rate regulates the system taking into account back-pressure/throttle

- ✓ Fan-out timing and control information (TFC) to Readout Boards
- ✓ Fan-in Throttle information from Readout Boards
- ✓ Distributes TFC information to FE
- ✓ Distributes control configuration data to FE
- ✓ Receives control monitoring data from FE

Distribution of Fast and Slow Control Commands

New S-TFC system controls the entire readout architecture:

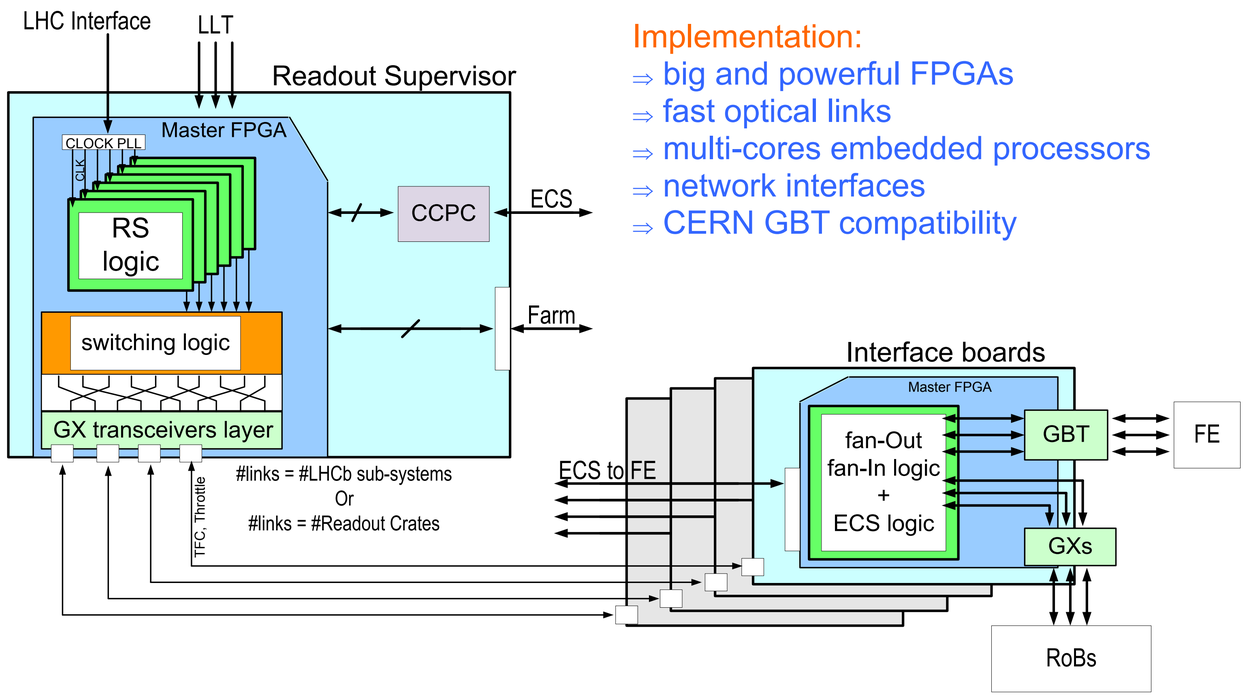
⇒ Transmits timing, fast and slow control to the Front-End via the same optical link, sharing the bandwidth
⇒ Transmits timing and fast control to the Readout Board via optical links and/or ATCA backplane
⇒ Transmits synchronous LHC clock to entire readout architecture

System must be sufficiently robust to ensure synchronicity across the entire readout architecture, buffer control and event management.

System must be sufficiently flexible to allow changes on-the-fly in order to satisfy evolving requirements

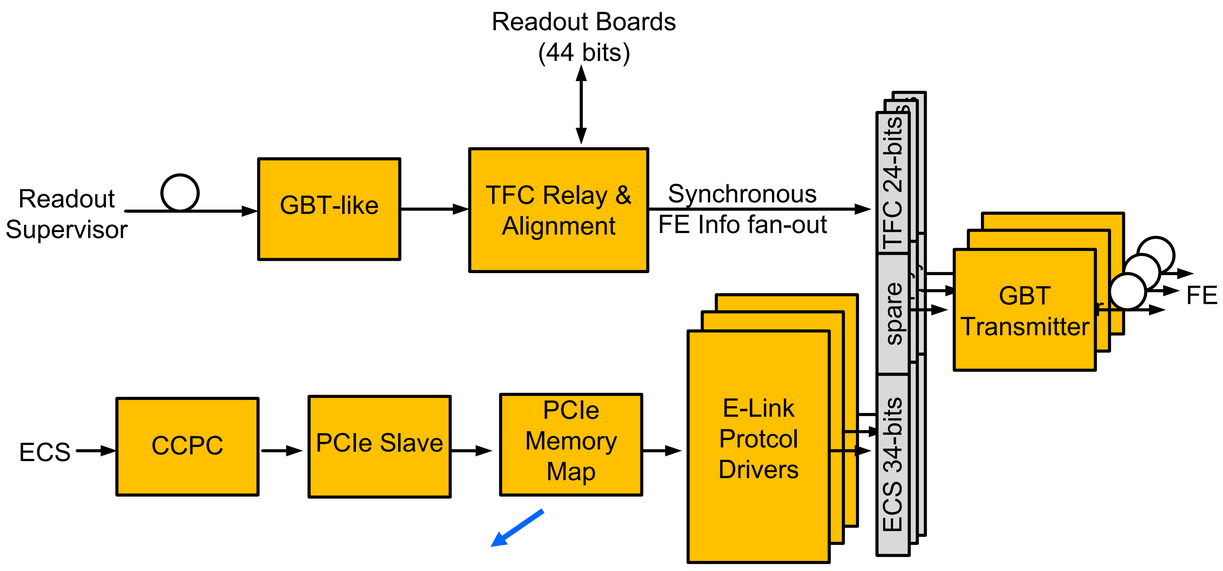
System must be used in test-benches and test-stands in order to test compatibility with global specifications [1].

System must be interfaced to all components of the readout architecture.



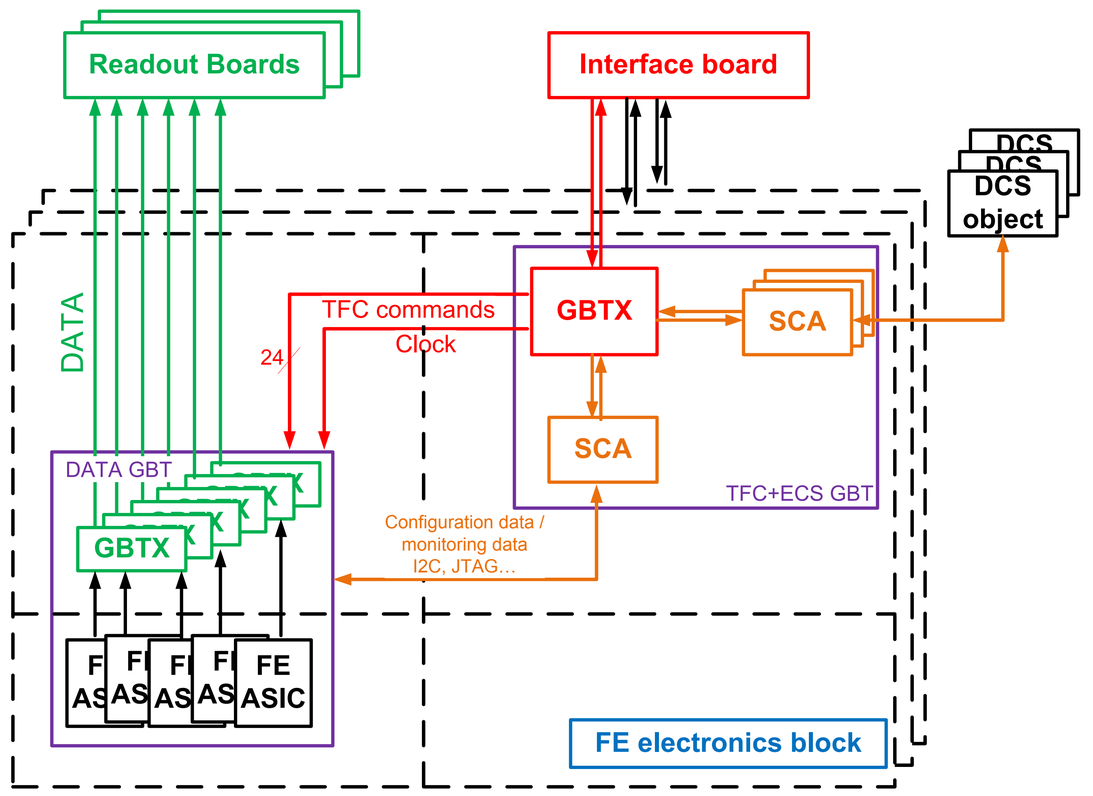
Implementation:
⇒ big and powerful FPGAs
⇒ fast optical links
⇒ multi-cores embedded processors
⇒ network interfaces
⇒ CERN GBT compatibility

Fast and Slow Control to FE via same optical link

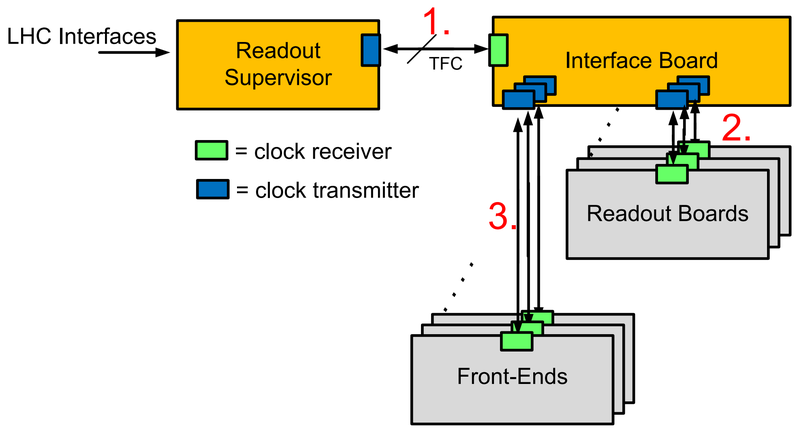


Memory Map with internal addressing scheme for GBT-SCA chips + FE chips addressing, e-link addressing and bus type: content of memory loaded from ECS

Protocol drivers build GBT-SCA packets with addressing scheme and bus type for associated GBT-SCA user busses to selected FE chip (GBT-SCA supported protocols)



Clock Distribution



Particular care must be given to the clock distribution in order to have full control of phase and latency across three types of links:

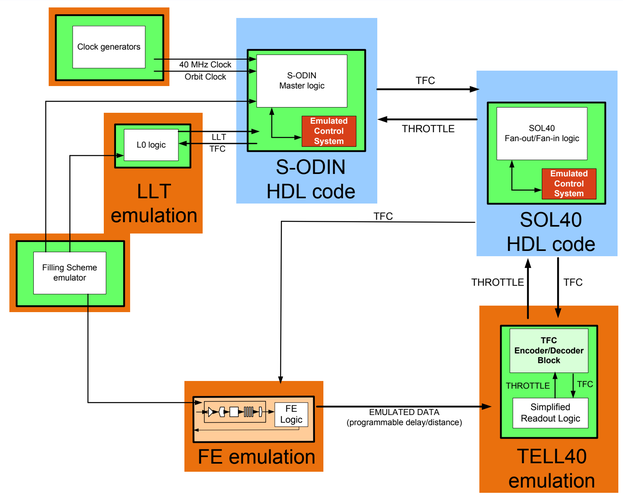
1. FPGA-to-FPGA links via optical fibers
   - need validation of FPGA technologies
2. FPGA-to-FPGA links via ATCA backplane or optical links
3. GBT-to-GBT links via optical fibers
   - include clock distribution to each FE chip

Global Simulation

Clock-level global simulation under development:

- general-purpose framework
- tool independent
- shared across collaboration

Used to validate new Front-End electronics and readout logic.



References:
[1] K. Wyllie, et al., “Electronics Architecture of the LHCb Upgrade”, CERN LHCb Public Note, LHCb-PUB-2011-011
[2] F. Alessio, R. Jacobsson, “System-level specifications of the Timing and Fast Control system for the LHCb Upgrade”, CERN LHCb Public Note, LHCb-PUB-2012-001
[3] J-P Cachemiche et al., “Study for the LHCb upgrade readout board”, JINST 5 (2010) C12036
[4] Moreira P et al., “The GBT Project”, Proceedings of TWEPP09, pp. 342-346