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Readout Control for the Upgraded Readout Architecture of the LHCb experiment at CERN

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The LHCb experiment at CERN has proposed an upgrade towards a full 40 MHz readout system in order to run between five and ten times its initial design luminosity with an upgraded LHCb detector. As a consequence, the various LHCb sub-systems in the readout architecture will be upgraded to cope with higher sub-detector occupancies, higher rate, and higher readout load. The new architecture, new functionalities, and the first hardware implementation of a new LHCb Readout Control system (commonly referred to as S-TFC) for the upgraded LHCb experiment is here presented. Our attention is focused in describing solutions for the distribution of clock and timing information to control the entire upgraded readout architecture by profiting of a bidirectional optical network and powerful FPGAs, including a real-time mechanism to synchronize the entire system. Solutions and implementations are presented, together with first results on the simulation and the validation of the system.

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