The new radiation-hard optical links for the ATLAS pixel detector

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OUTLINE
Lessons learned…
IBL/nSQP opto-board
- overview
- assembly experience
- radiation hardness
- production

Summary/Conclusions

Pixel Optical Data Links

Optical data transmission preferred over copper wire links:

optical fibers are lower in mass than copper

higher data transmission rate over long distances (80m)

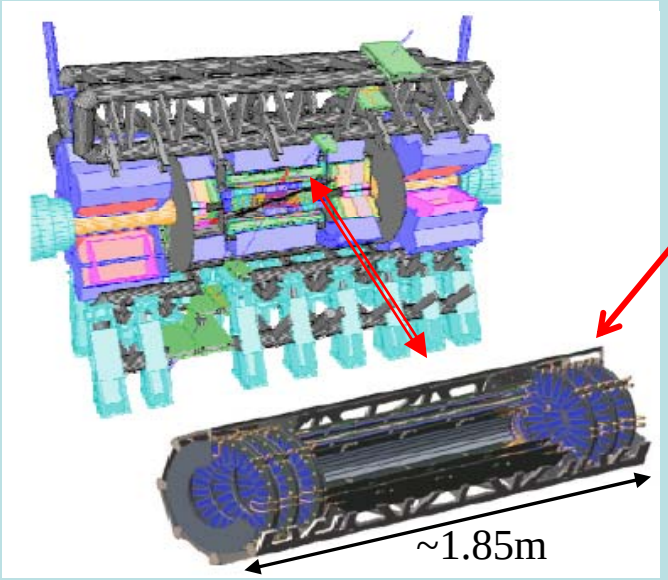
no ground loop between front and back end electronics

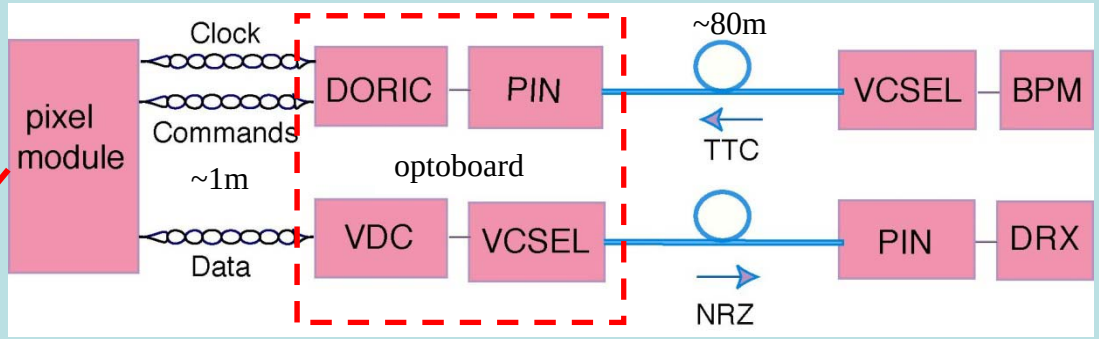
Optical Transmitter: VCSEL (vertical cavity surface-emitting laser)

Optical Receiver: PIN diode

Can be packaged in one, four, twelve channels

Work in the radiation environment of the LHC





VCSEL: Vertical Cavity Surface Emitting Laser diode
VDC: VCSEL Driver Circuit
PIN: PiN diode
DORIC: Digital Optical Receiver Integrated Circuit

The pre-IBL Opto-board

Optical signal ⇔ electrical signal conversion occurs here

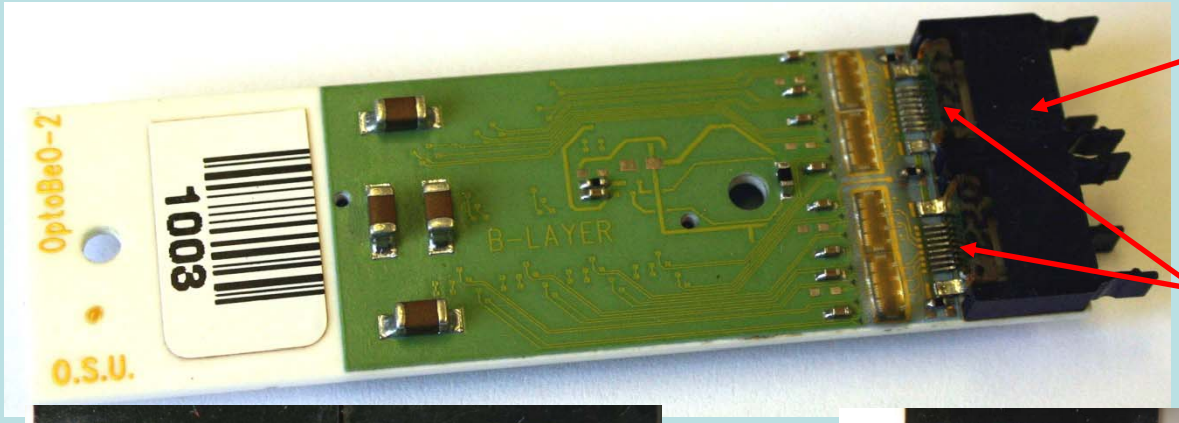
Contains 7 optical links, each link serving one Pixel module

Fabricated in 2 flavors

- Layer B: for inner barrel, 2 data links per module for high occupancy
- Layer D: for outer barrel and disks 1 and 2

Fabricated with BeO for heat management

44 *B* boards
228 *D* boards

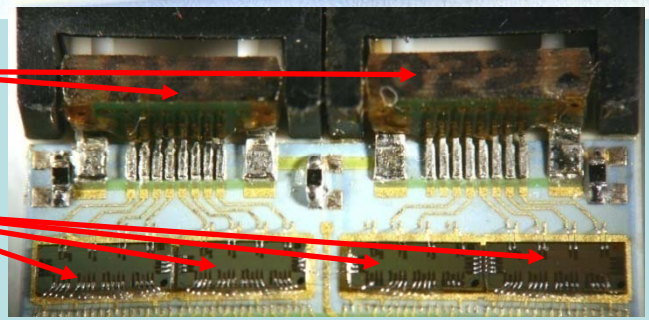


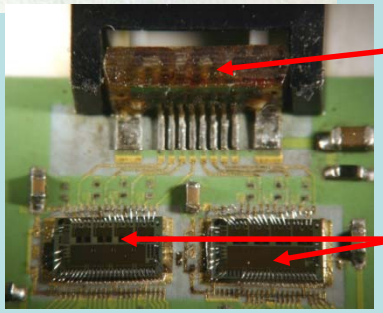
Housing

Opto-pack

VCSEL array

VDC





Pin array

DORIC

Pixel Opto-board Lessons 2010-12

On opto-boards, only 1 confirmed VCSEL death (connected but not lasing)

- We were saved by the low humidity environment

There are some weak links (besides the VCSELs) we have addressed on the new opto-boards

- Single Iset line (pin) per board
  - ☺Added a redundant pin to the 80/100 pin connector (nSQP/IBL)
- Soldering of opto-packs
  - ☹Suspect 15 VCSEL and 6 PIN failures due to cold solder joints
  - ☺New Opto-pack connections are wire bonded
- DORIC reset daisy chain
  - ☹Some DORIC channels/modules hard to configure have a broken reset line
  - ☺Added an redundant pin on the 80 pin connector
  - ☺Improved routing so no more daisy chaining through chips

IBL/nSQP Opto-board Overview

Use same 0.25 μm DORIC /VDC ASIC chips as present pixel opto-boards

Use copper+Polyimide instead of BeO for the PCB

Switch to industry standard MTP fiber connector and OSU opto-pack

Switch to fully qualified Finisar VCSEL and ULM PIN arrays

Finisar V850-2093-001 ULMPIN-04-TN-U0112U

nSQP: 2 flavors of opto-boards (for legacy fiber mapping)

- B-Layer
- D-Tall
- All equipped with 14 DTO / 7 TTC (enables operation at higher rates)

IBL: 1 flavor of opto-board

- 16 DTO / 8 TTC

DTO: data output signal
TTC: timing, trigger, control signal

nSQP/IBL Opto-Board Prototyping

We have constructed

- 10 nSQP B-boards
  - 5 for irradiation
  - 5 for system tests (2 to CERN 1 to SLAC, 1 to BERN, 1 to Wuppertal)
- 6 nSQP D-boards
  - All for system tests (4 to CERN)
    - 2 failed QA
      - 1 with bad wire-bonds
      - 1 with a bad DORIC (slipped through test in 2005)
- 6 IBL boards
  - All for system tests (5 to CERN, 1 to SLAC)

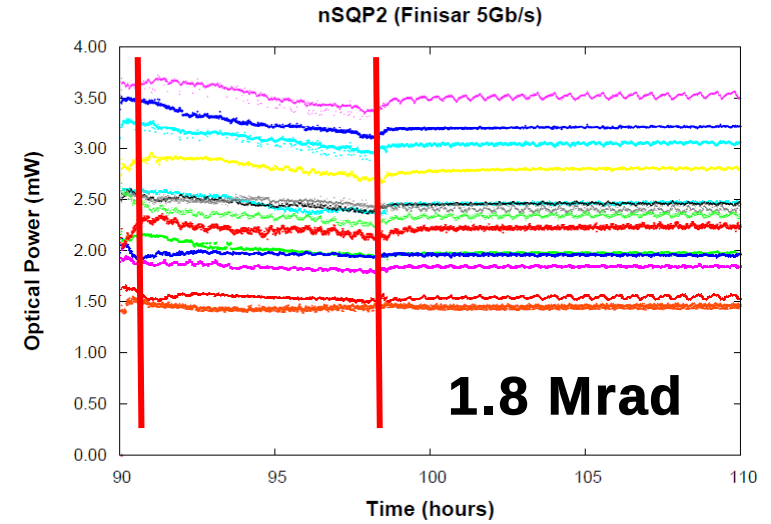
No complaints received on distributed boards

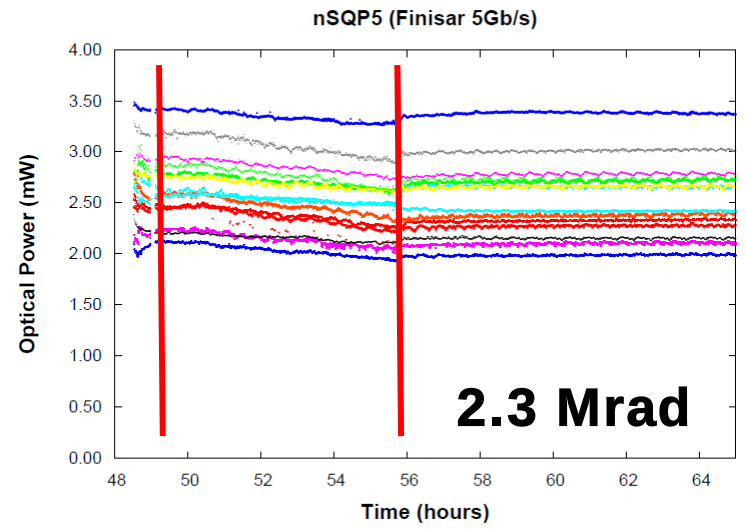
Opto-board Radiation Hardness

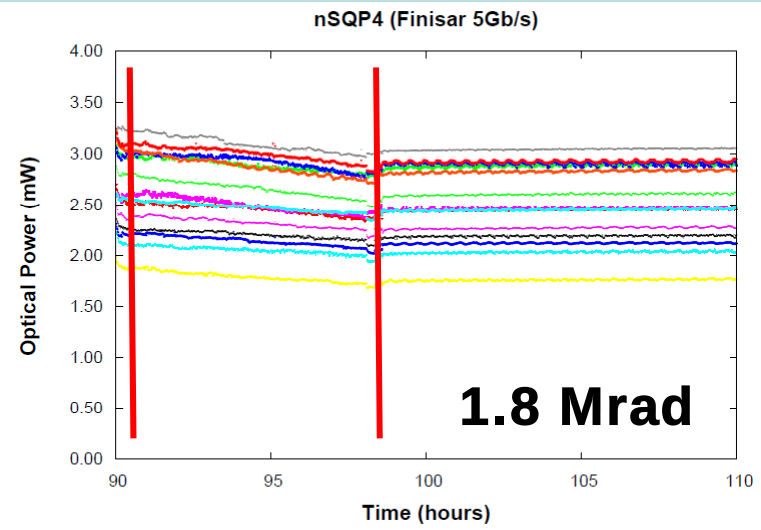
- 0.25 μm DORIC and VDC ASICs well exercised
  - Dedicated ASIC irradiation to 61 Mrad (2003)
  - 4 production opto-boards to 30 Mrad (2004)
  - 10 opto-boards to 30 Mrad for VCSEL/PIN SEU R&D (2006-9)
- VCSEL/PIN qualified
- Opto-boards exercised
  - Constructed 6 nSQP B-Layer boards in July 2011
  - Used Finisar 5Gb/s VCSELs and ULM PINs on OSU Opto-packs
  - Irradiated 2 sets of 2 boards with 24 GeV protons @ CERN
    - First set 8×10^{13} p/cm^2 → 1.8 Mrad (18 KGy)
    - Second set 10.4×10^{13} p/cm^2 → 2.3 Mrad (23 KGy)
  - Test successful: No failed channels , PIN current thresholds for no bit errors remained constant, modest decrease in output optical power, boards fully functional after irradiation
- Since IBL board of identical construction, no need to repeat

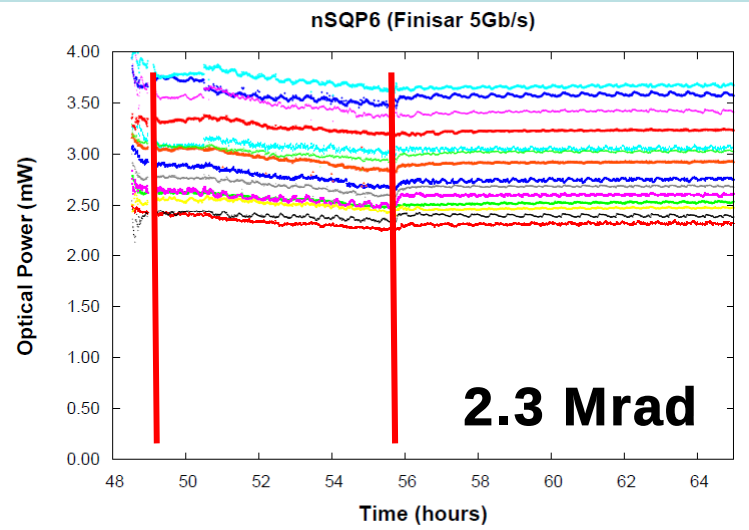
nSQP B-Layer Irradiation

Modest degradation in VCSEL output power





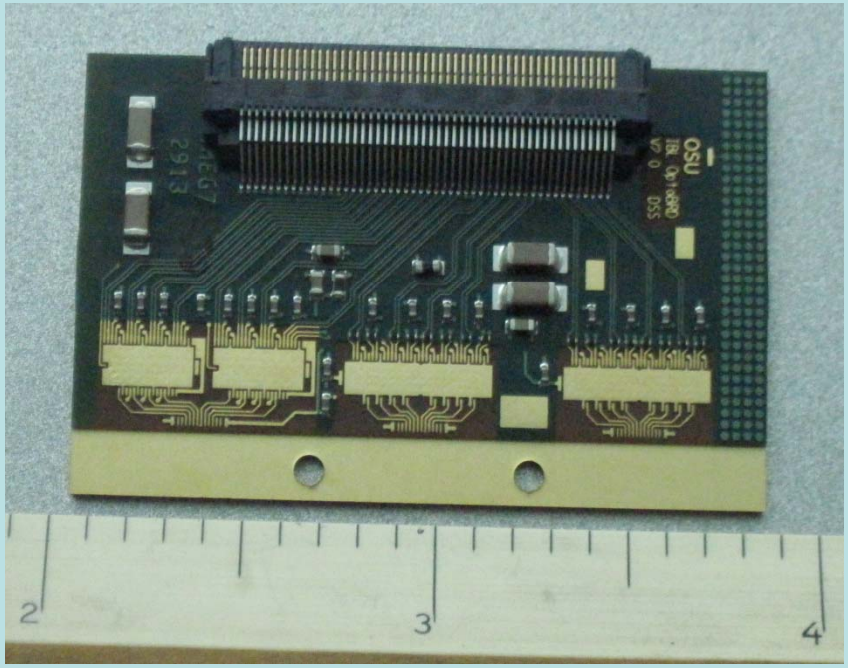




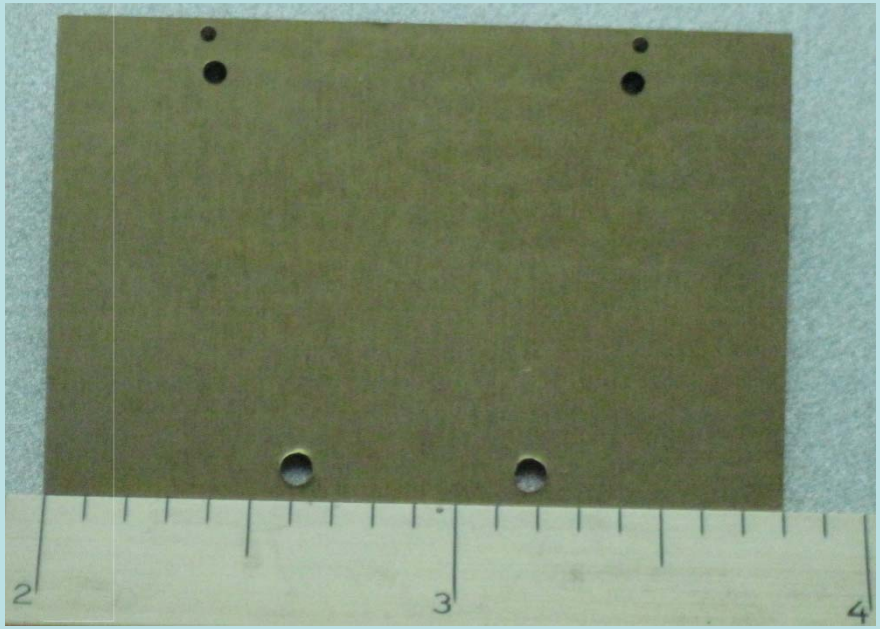
IBL/nSQP Opto-boards

Mounting of passive components (outside vendor)

- Electrical open/short test
- 30 mm x 46 mm PCB
- 6-layer board
- Use copper for thermal management



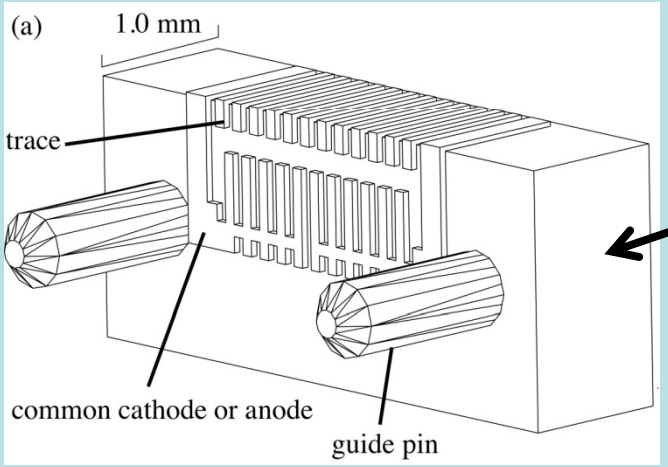
Component side
passive components mounted by vender
Everything else mounted at Ohio State



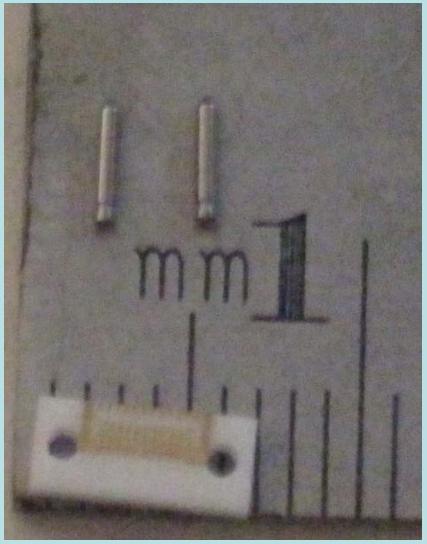
Backside
1mm thick copper backing plate
slides into cooling rail

Opto-Pack Production

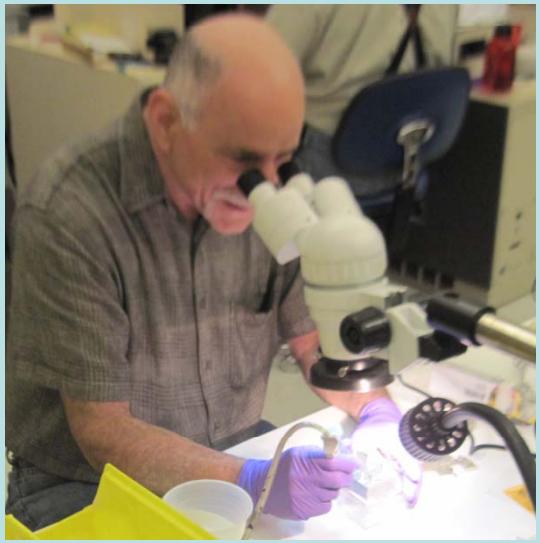
Opto-pack holds a VCSEL or PIN array
Alignment of fiber to PIN/VCSEL is critical



Substrate
BeO for VCSELs (thermal management)
Alumina for PINs



"bare" opto-pack and guide pins



gluing guide pins into opto-pack

opto-pack with guide pins

Opto-Pack Production

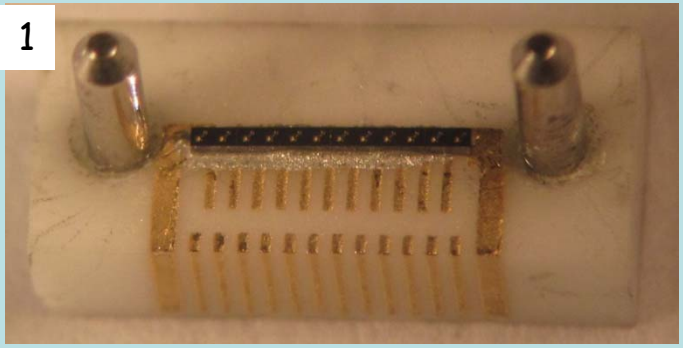
Produce opto-packs (2 VCSEL, 1 PIN per opto-board)

PIN/VCSEL array must be put on Opto-pack & connected to traces

VCSEL QA: LIV, reverse bias looking for ESD

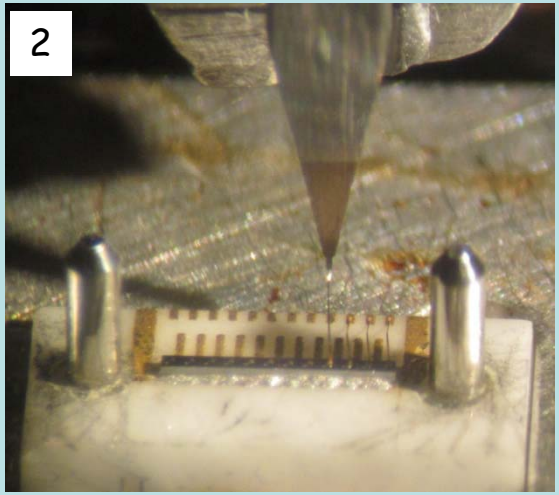
PIN QA: dark current, illuminate with 1mW & measure responsivity, check specs

1



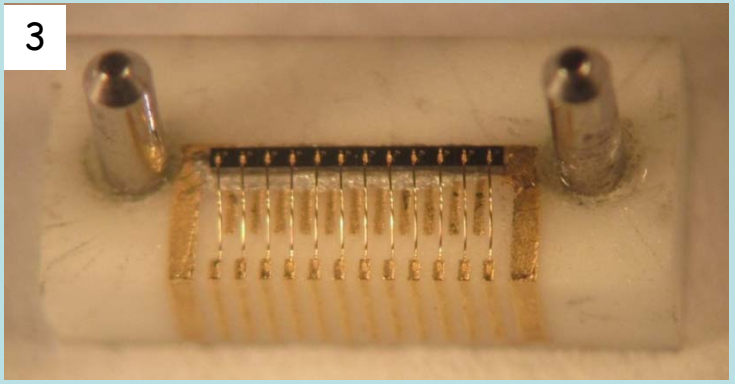
PIN/VCSEL array glued to opto-pack

2



wire bonding to PIN/VCSEL

3



wire bonded PIN/VCSEL array

4

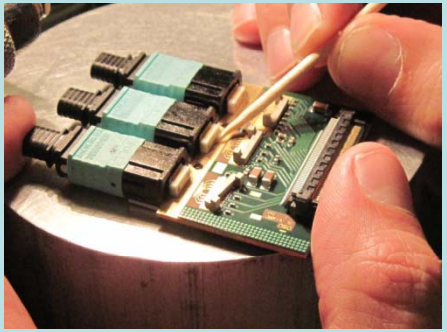
dust cover installed

Opto-board Production Procedure

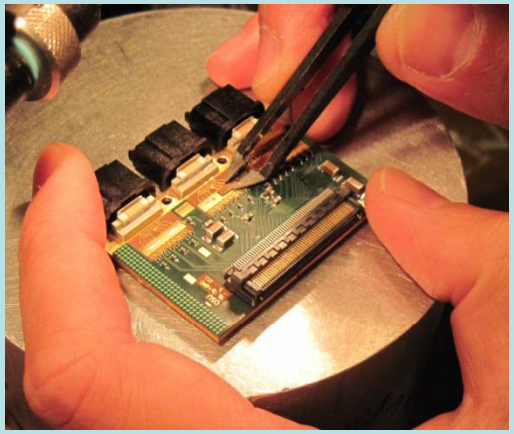
Mounting of optical connectors

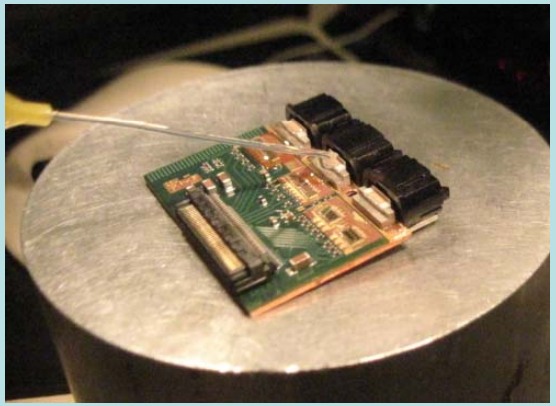
Wire bonding chips to board, board to opto-packs

Mounting of opto-packs



Mounting of DORIC & VDC





Encapsulation of wire bonds

Opto-board Q/A Procedure

Go/No Go Test

check optical power, all channels error free

Burn in: 72hrs @ 50° C, powered

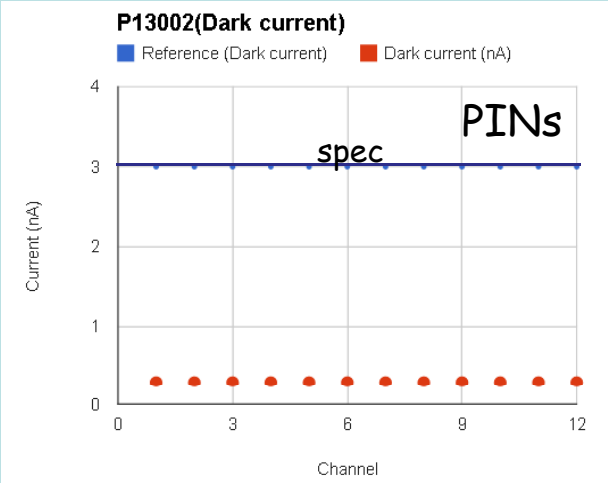
Thermal cycling: 0° C -> + 50° C, 10 cycles, 2hrs per cycle

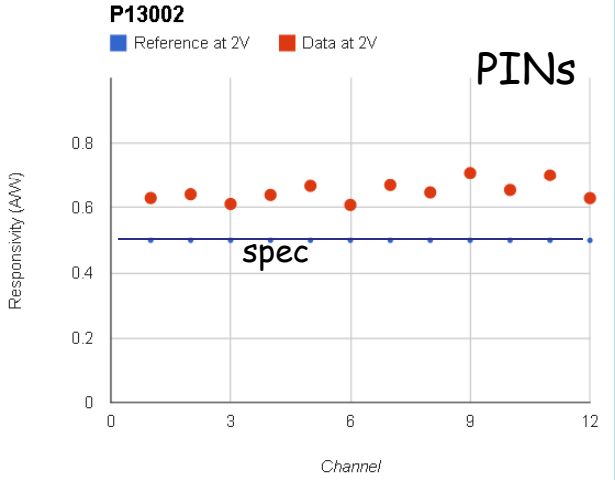
Full electrical and optical QA at 10° C

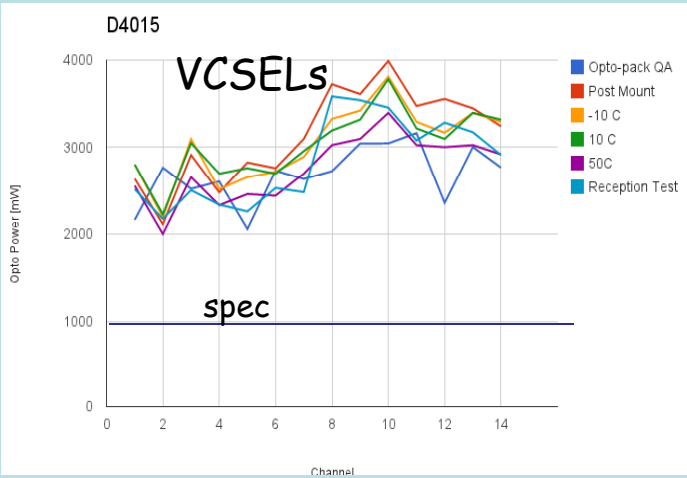
error free for 1 hr at 10° C (data at 40 Mbits)

measure optical power at 0, 10, 10, 50° C

check LVDS, jitter, rise/fall time, duty cycle







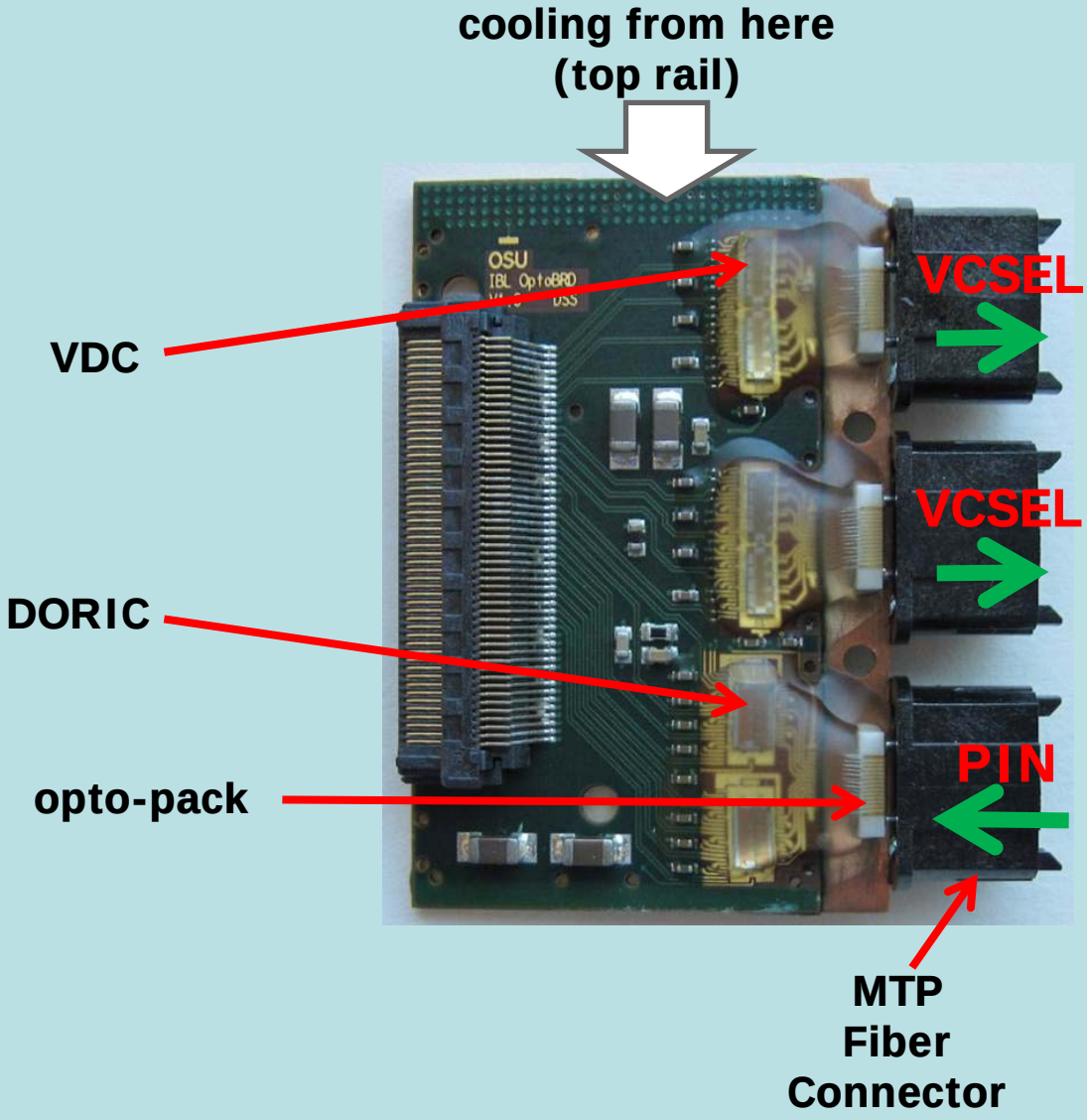
Send to CERN

Reception Test at CERN

Go/No Go Test

Install

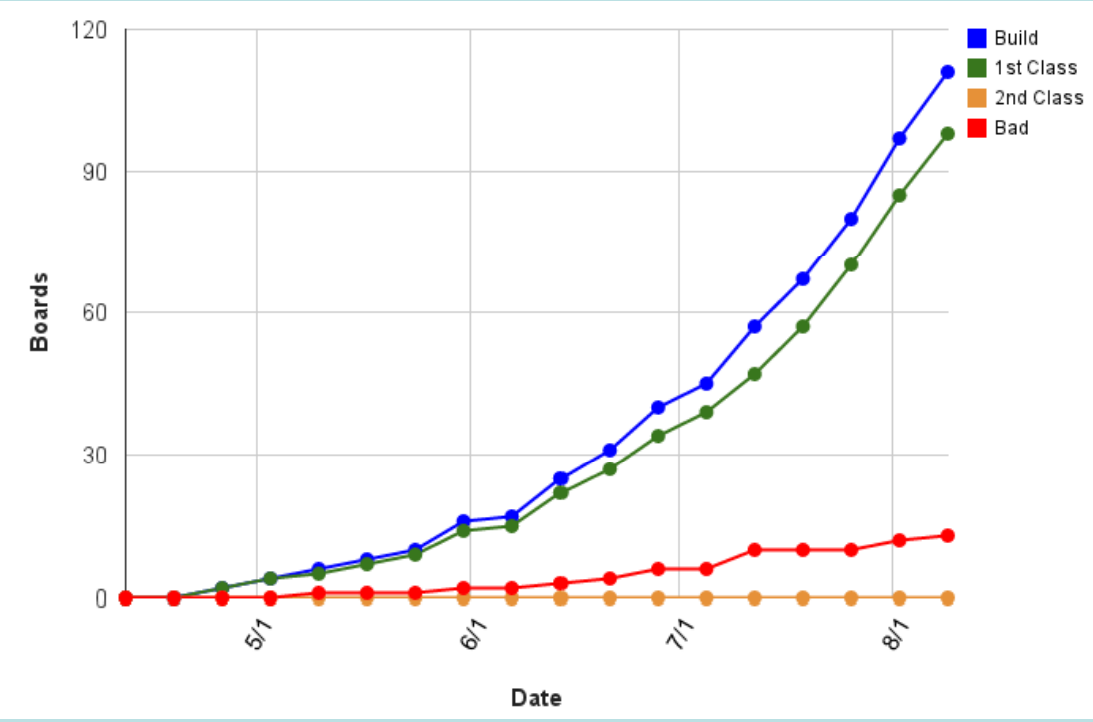
Completed Opto-board



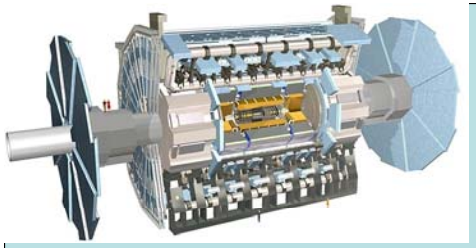
IBL/nSQP Opto-board Summary

We have been in production for ~ 3 months

	needed	completed	Status
nSQP B-layer	44	55	Done
nSQP D-Tall	228	37	Waiting for PCBs
IBL	28	6	In progress

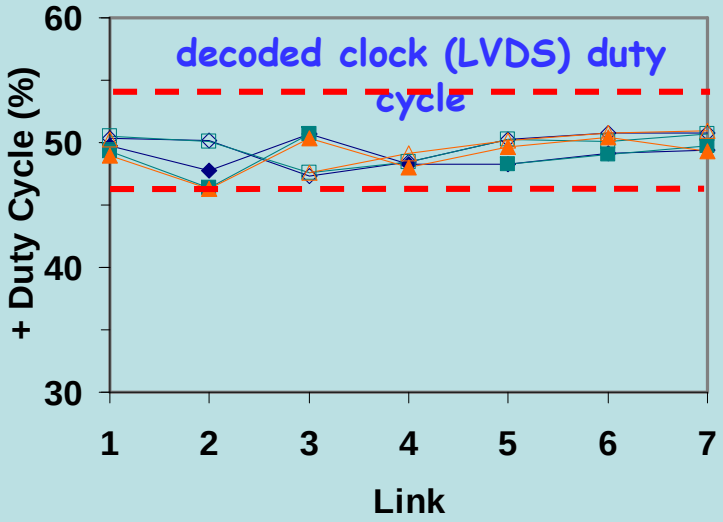


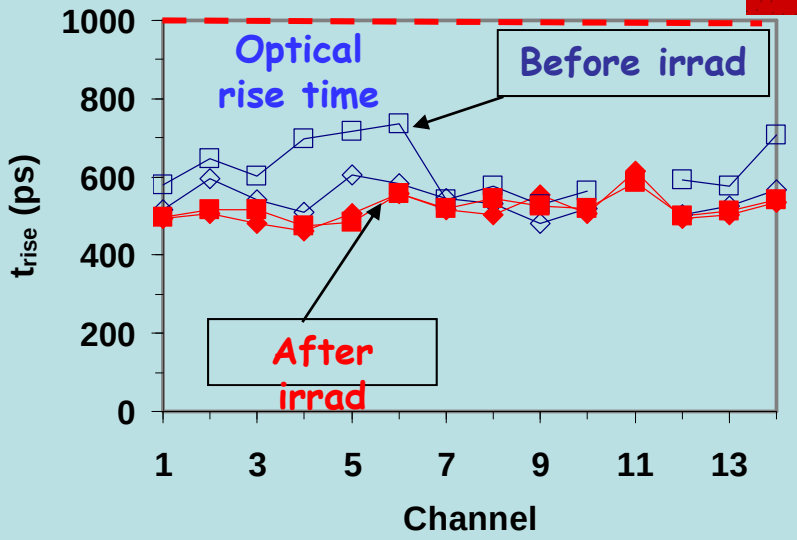
Expect to finish production late fall.

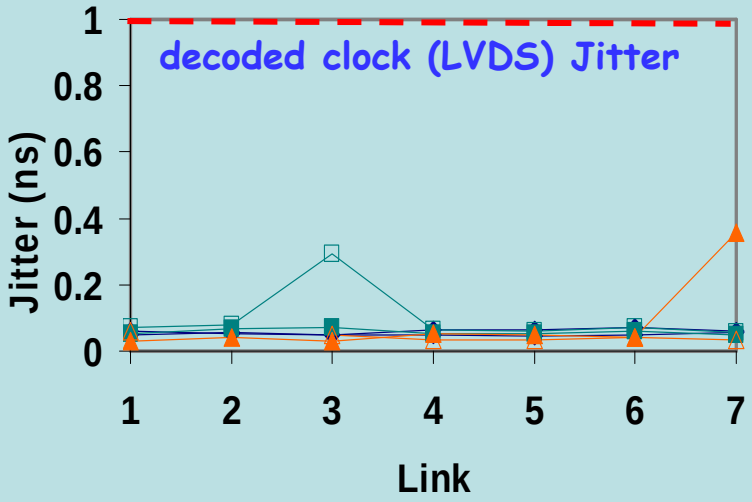


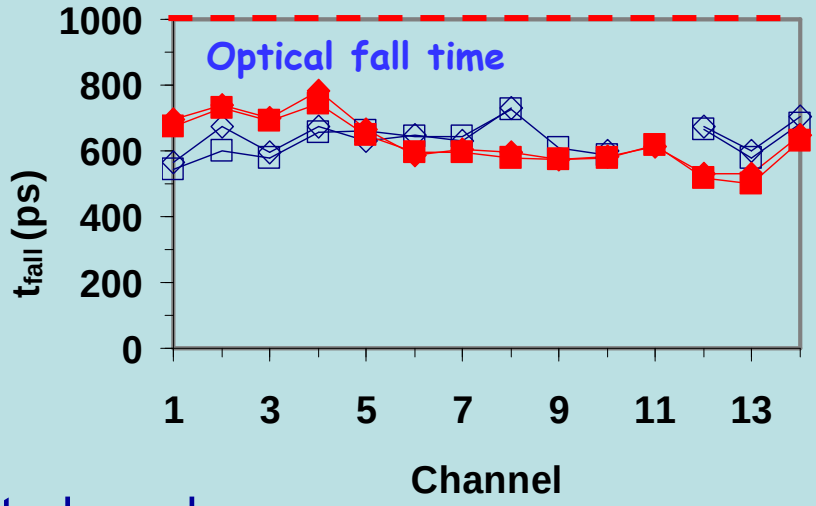
Extra Slides

Rise/Fall times, Jitter, and Duty Cycle





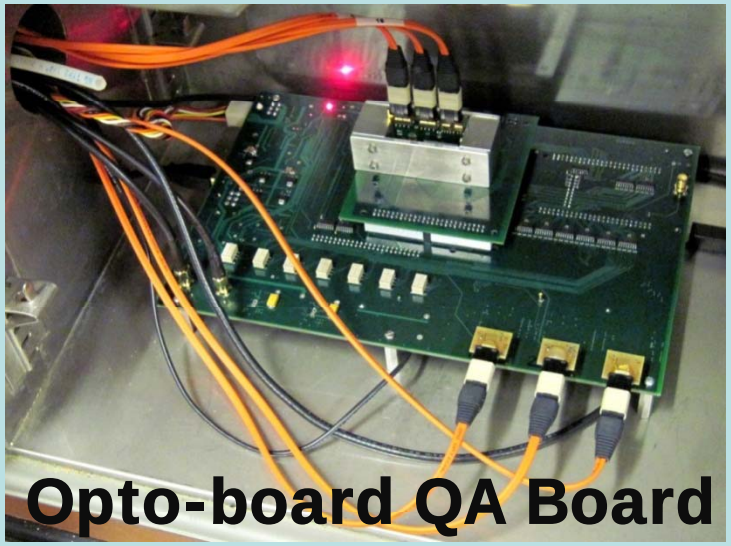


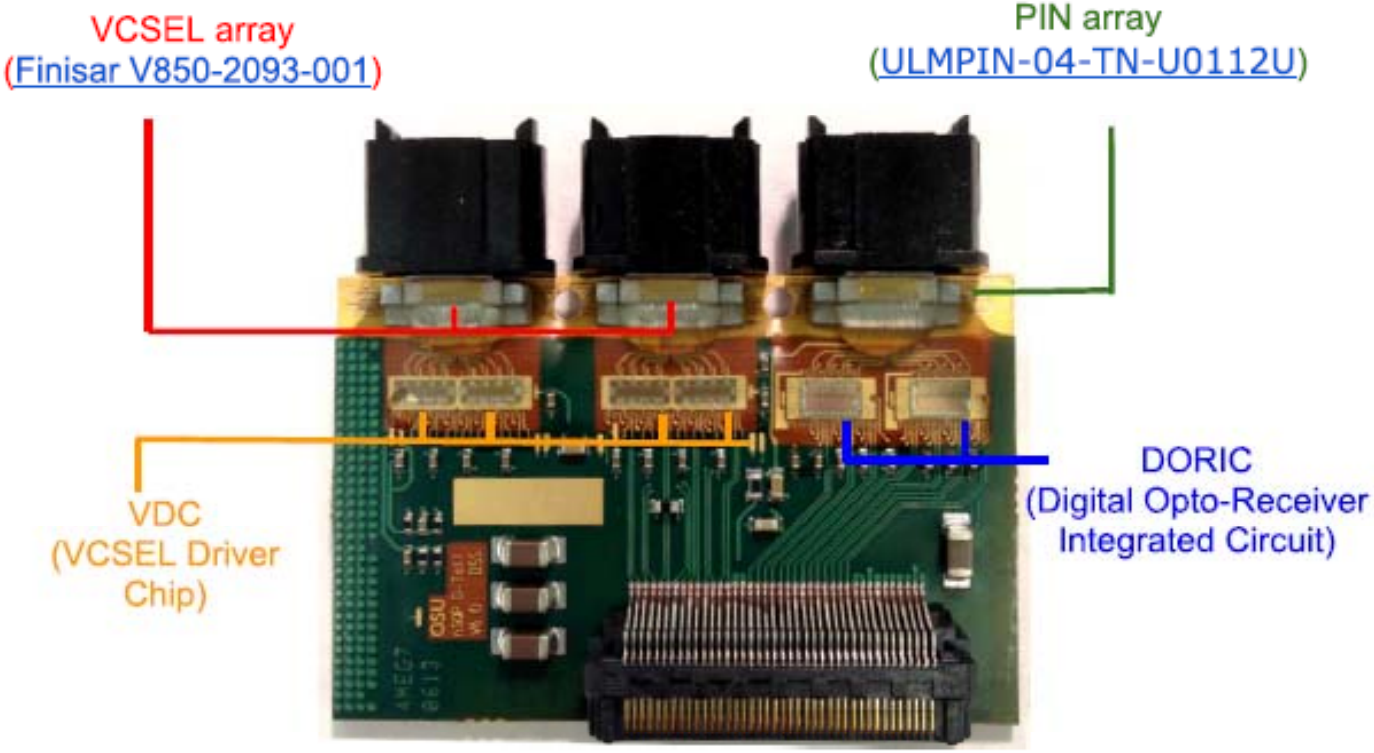


- Each plot shows the results for two opto-boards
- No degradation in rise/fall times
- Decoded clock duty cycle and jitter within the limits after irradiation

Opto-board Reception Tests at CERN

- Delivered and setup a copy of the QA system from OSU at CERN
- Reception test
  - Optical power must be consistent with OSU QA
  - Check that delivered boards operate with no bit errors at PIN current of 100 μA – 1 mA
- System test
  - All boards should be tested within a replica of the full readout chain after passing the reception


Opto-board QA Board



Encapsulation : Dymax 9001 V.3.1
Mounting glue : Loctite Hysol EA 9396
Epoxy : Epotek H20E

Fiber maps:

- B-Layer
- D-Tall
- IBL