Radiation-Hard/High-Speed Parallel Optical Links

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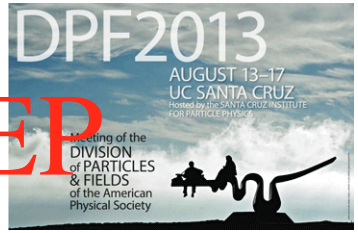
Outline

- Introduction to a compact solution
- Results with 5 Gb/s VCSEL array driver
- Preliminary Design of 10 Gb/s VCSEL array driver
- Summary

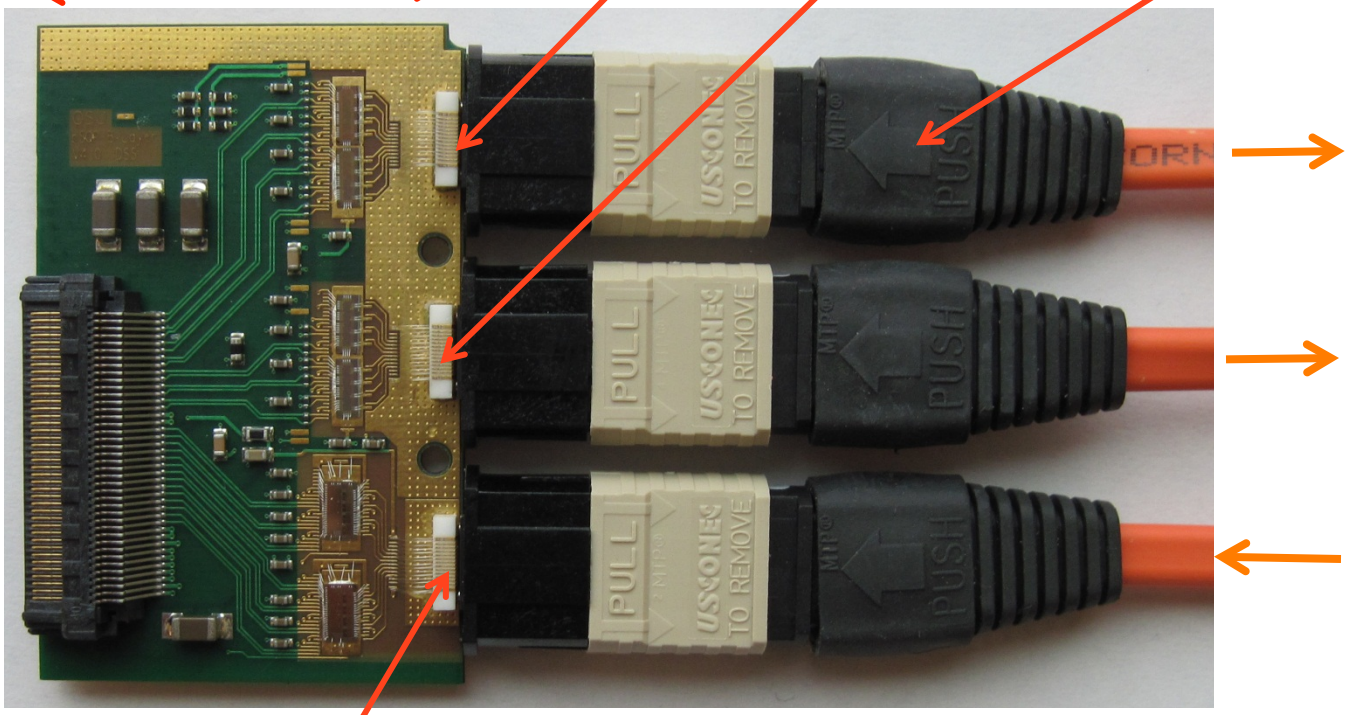
Use of VCSEL Arrays in HEP



- Widely used in off-detector (no radiation) data transmission
- First on-detector implementation in pixel detector of ATLAS
  - experience has been positive
    - VCSELs used are humidity sensitive but they are installed in very low humidity location
    - modern VCSELs are humidity tolerant
    - opto-links built by OSU have ~0.1% broken links
    - ⇨ will use arrays for next pixel detector upgrade (IBL)

New Parallel Optical Engine

- Improved design for new pixel layer of ATLAS
  - use 12-channel VCSEL and PIN arrays
  - ⇨ 36 optical channels

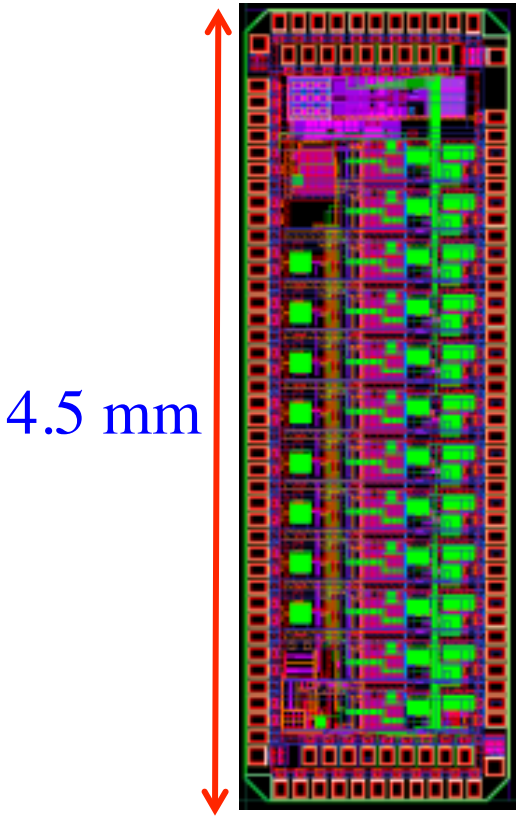


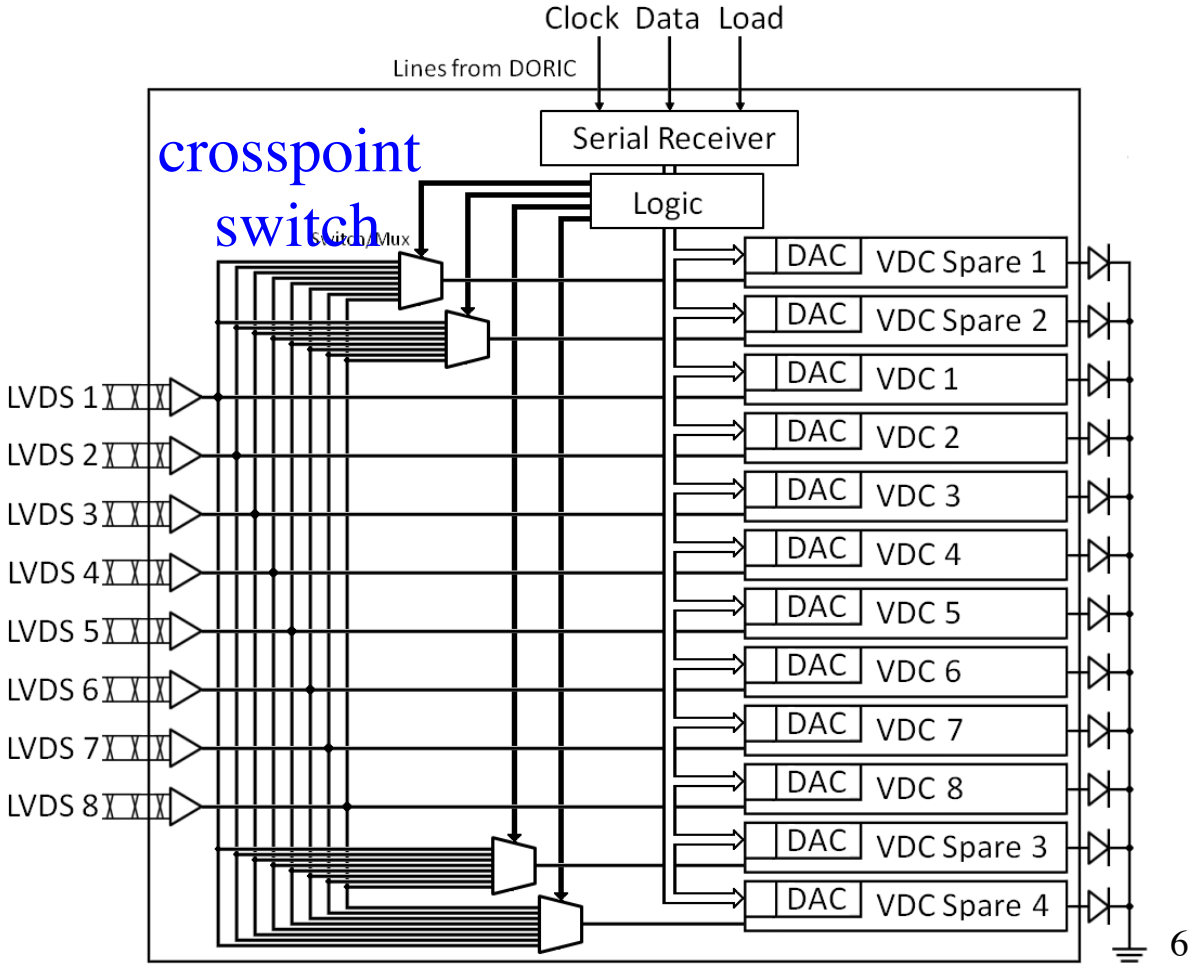
New 12-Channel VCSEL Driver

- New ASIC designed using 130 nm CMOS
- Incorporate improvements taking advantage of experience from 1st generation parallel optical engine:
  - ✔ redundancy to bypass a broken VCSEL
    - special thanks to FE-I4 group (Roberto Beccherle et al.) for command decoder circuit
  - ✔ power-on reset in case of communication failure:
    - ✔ no signal steering
    - ✔ 10 mA modulation current (on current)
    - ✔ 1 mA bias current (off current)
- Will only operate at 160 Mb/s for new pixel layer but designed ASIC to operate at much higher speed (5 Gb/s) to gain experience in designing high-speed parallel driver

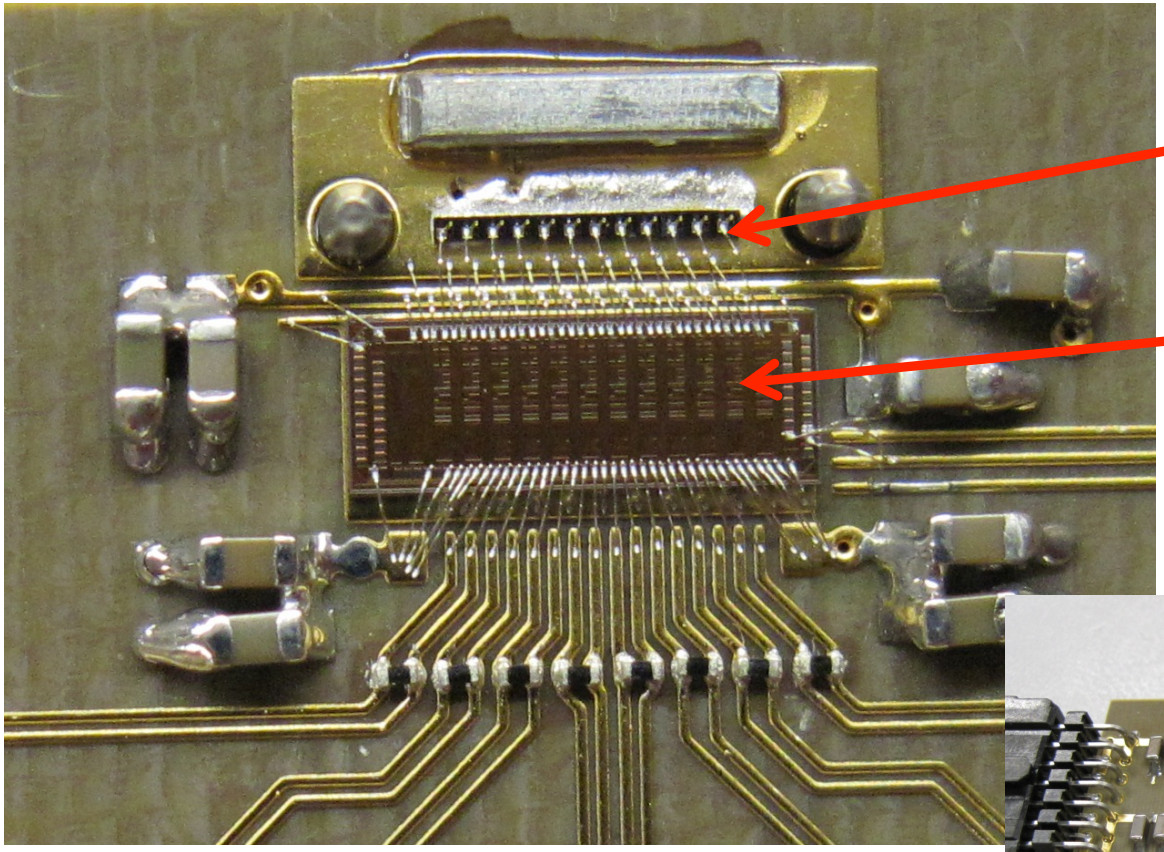
New VCSEL Array Driver

- Only inner 8 channels connected to new pixel modules
  - future driver could reserve only one channel for redundancy





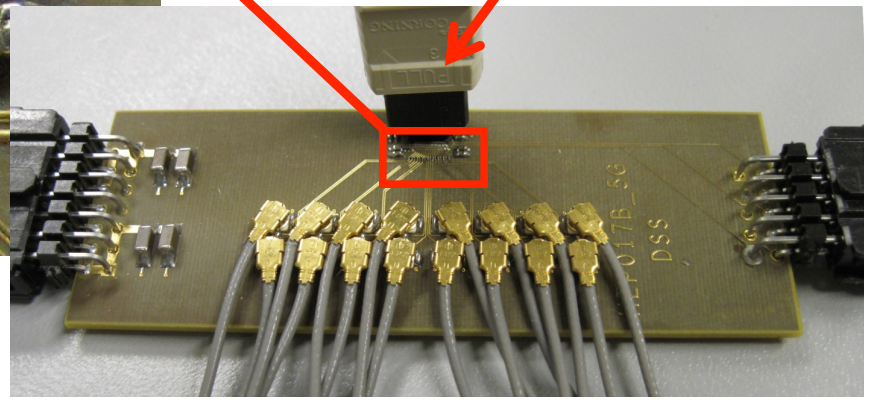
High-Speed Test Configuration



10 Gb/s ULM
VCSEL array

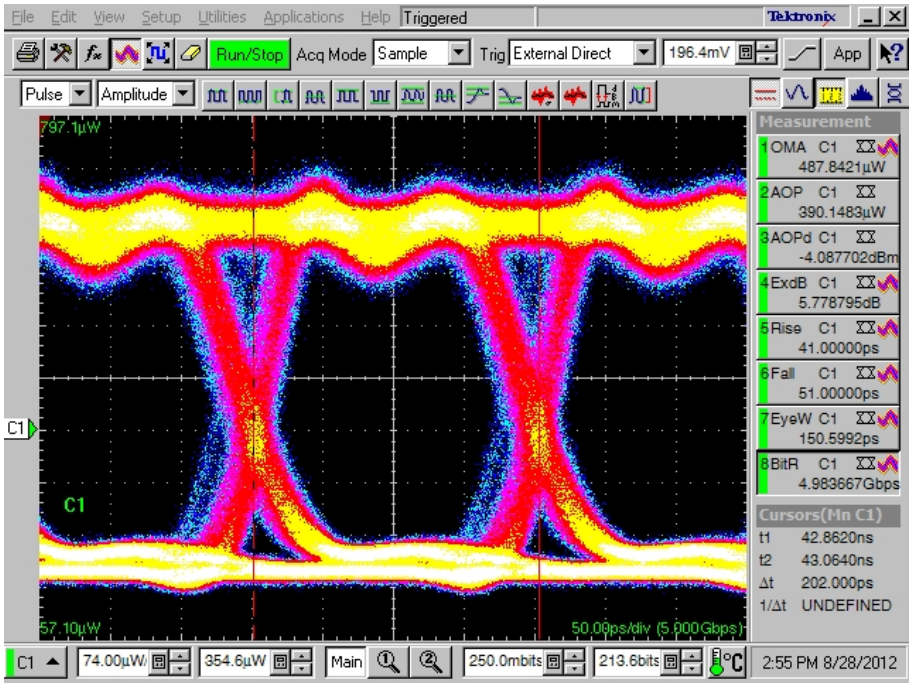
VCSEL
array driver

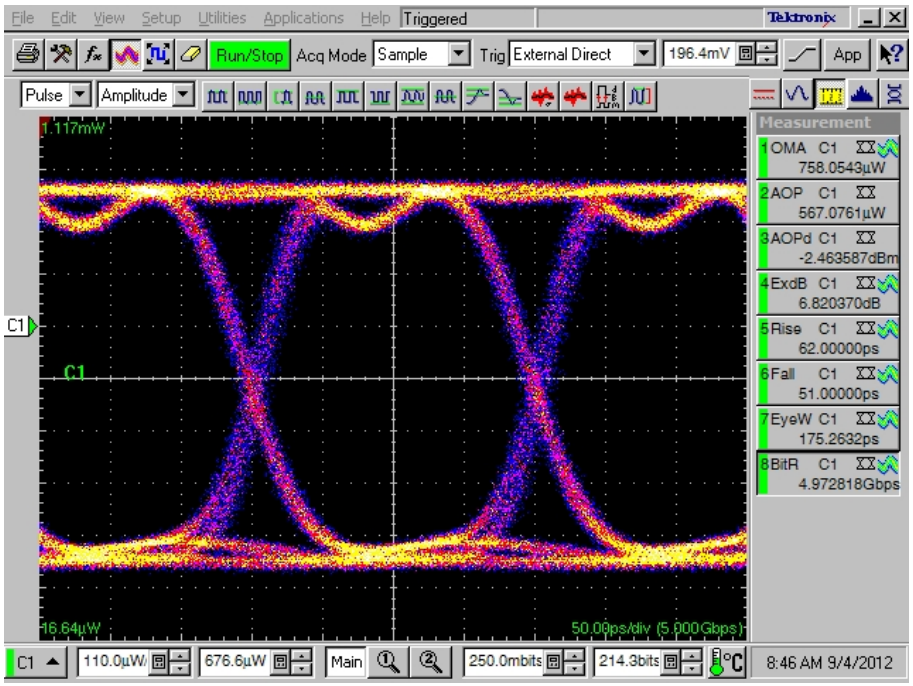
MPO connector



Optical Eye Diagram

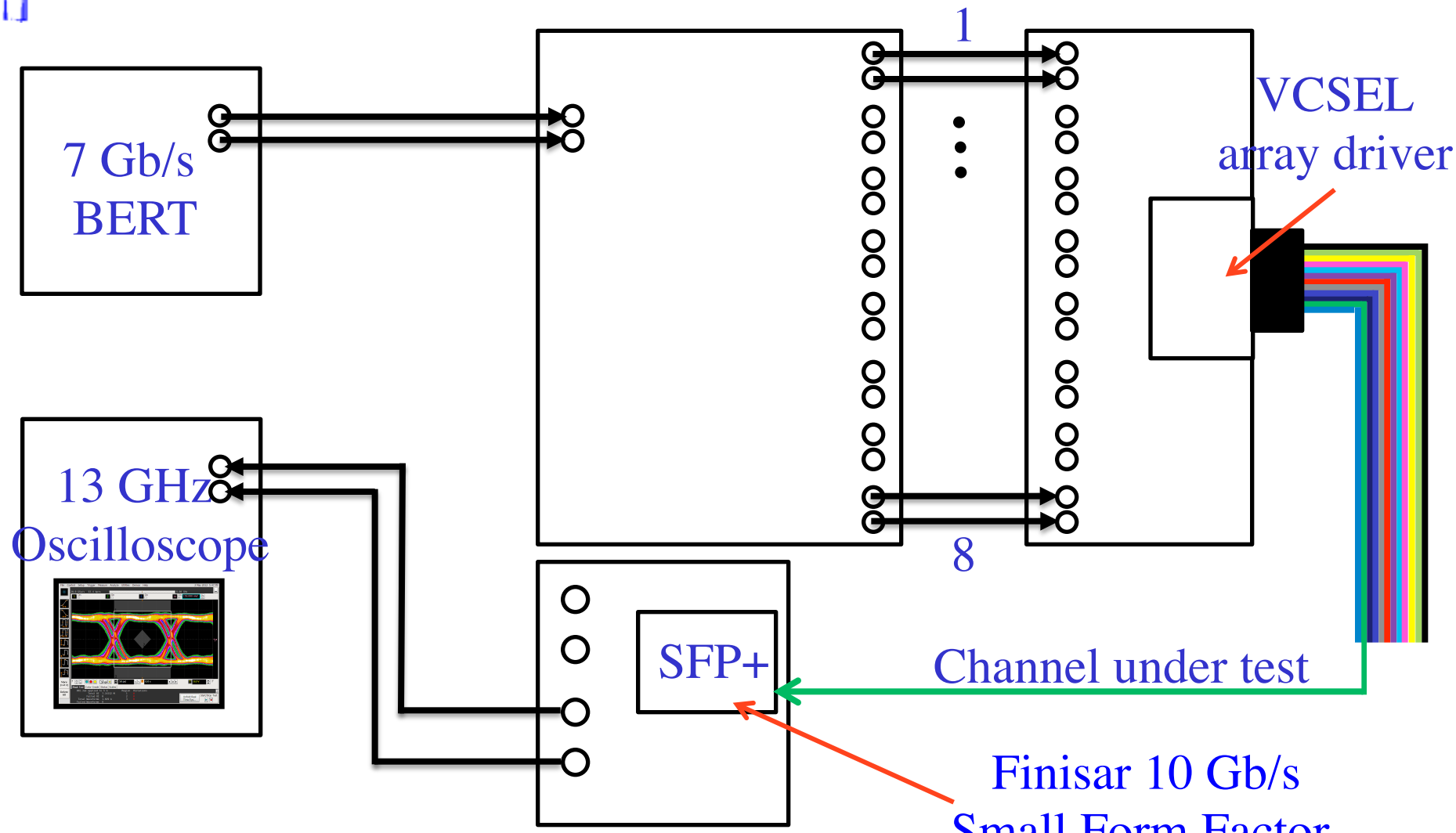
SFP+: single channel





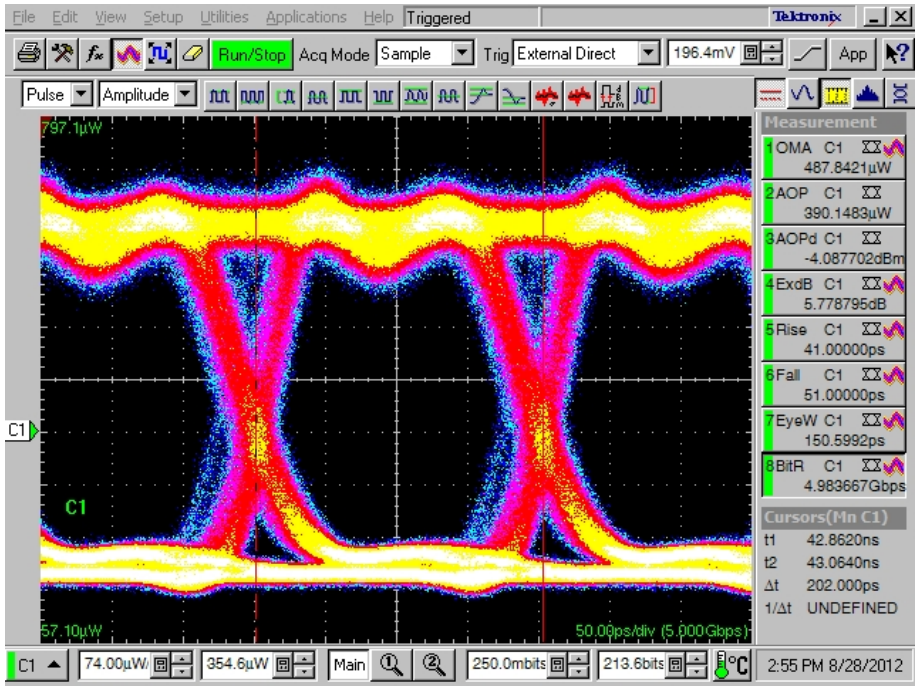
- optical eye diagram @ 5 Gb/s is quite acceptable
  - special thanks to Alan Prosser @ Fermilab for use of equipment

SFP+ as Optical Probe

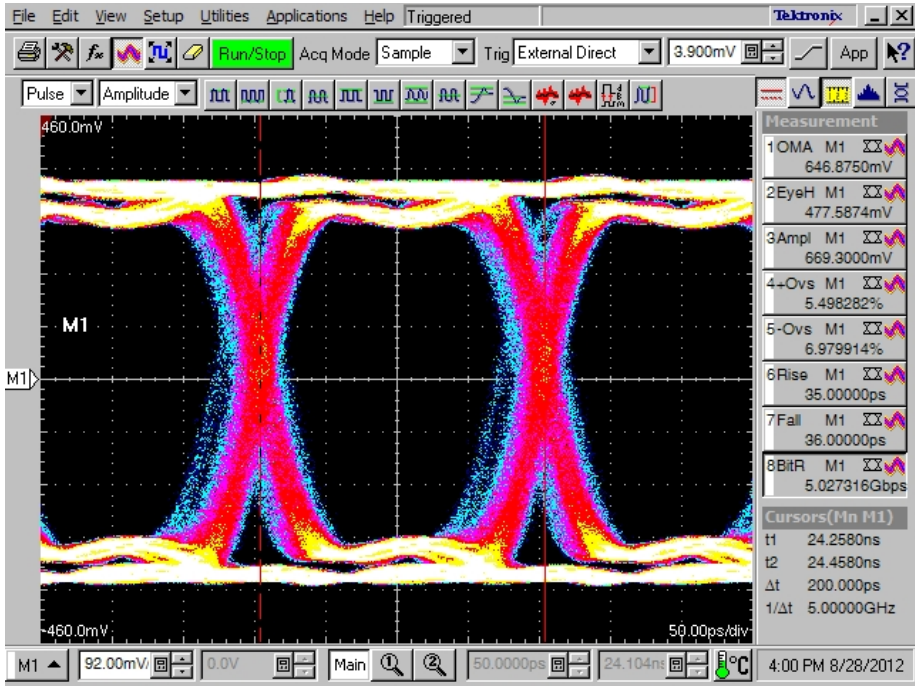


Optical Probe vs. SFP+

Optical probe

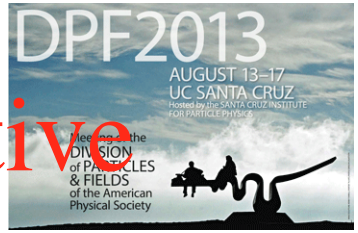


SFP+

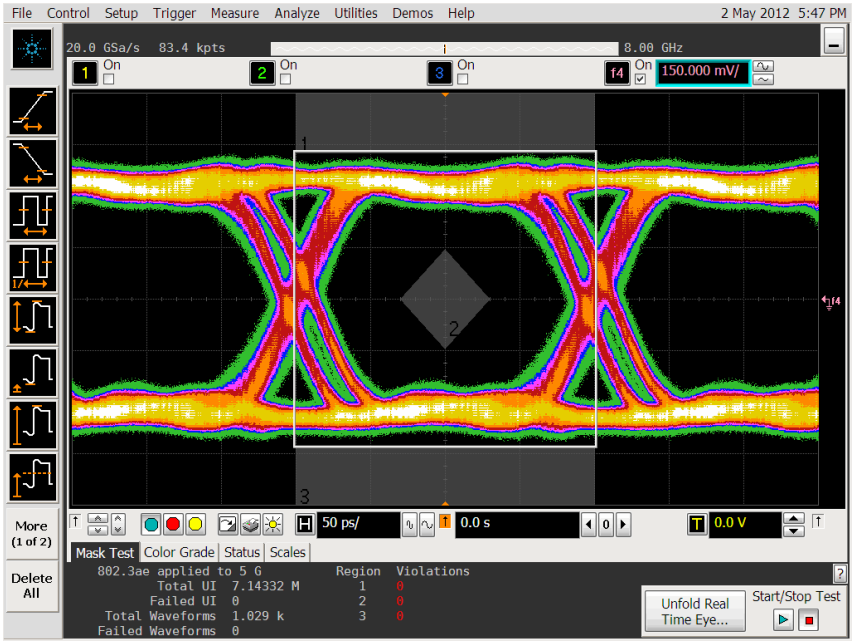


- SFP+ cleans up the eye by slightly improving the rise/fall times

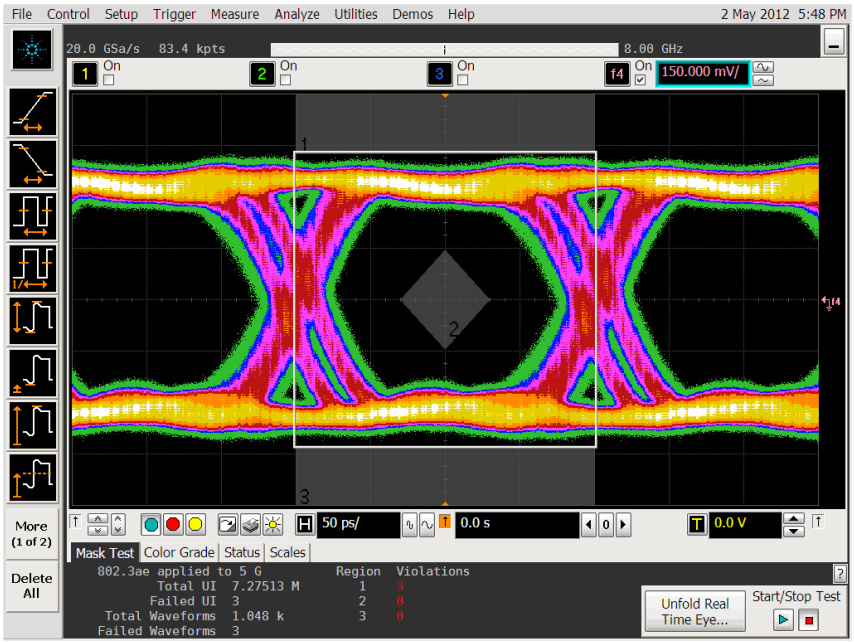
Eye with One/All Channels Active



One channel active

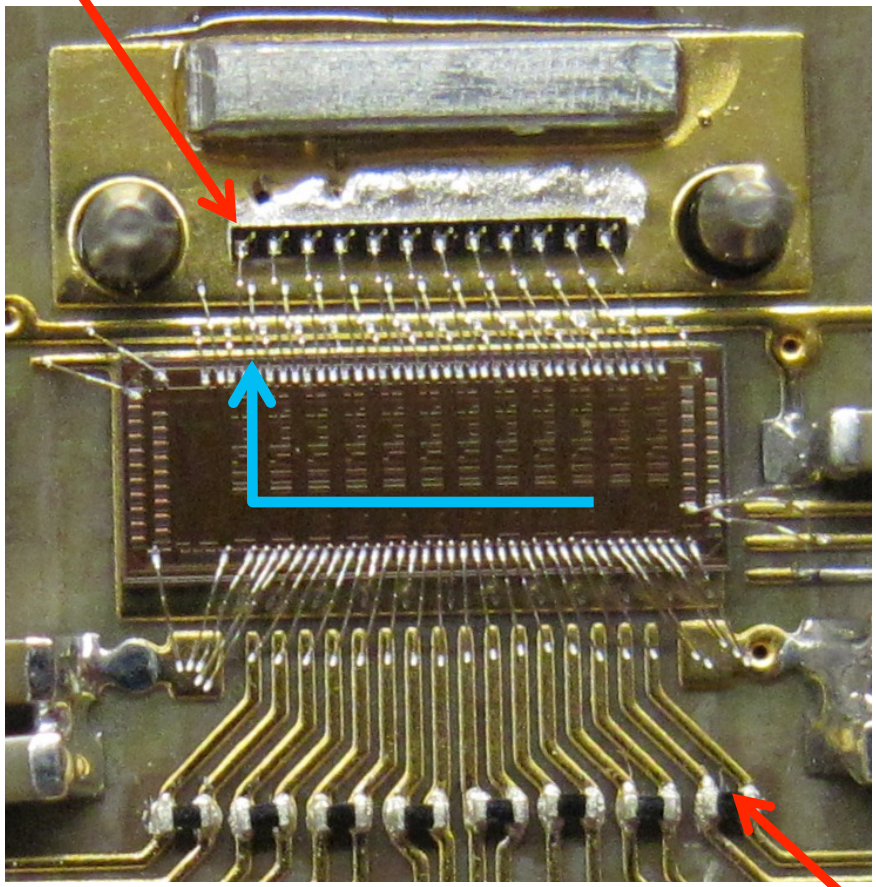


All channels active



- all channels work @ 5 Gb/s with bit error rate < 5×10^{-13} for all channels active
- jitter increases with all channels active but still passes the mask test

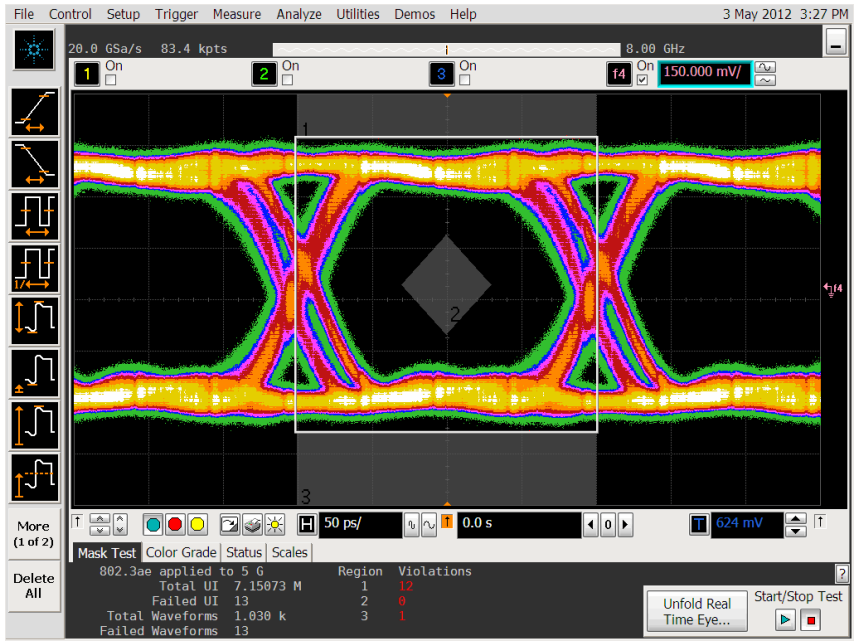
Effect of Steering on Eye



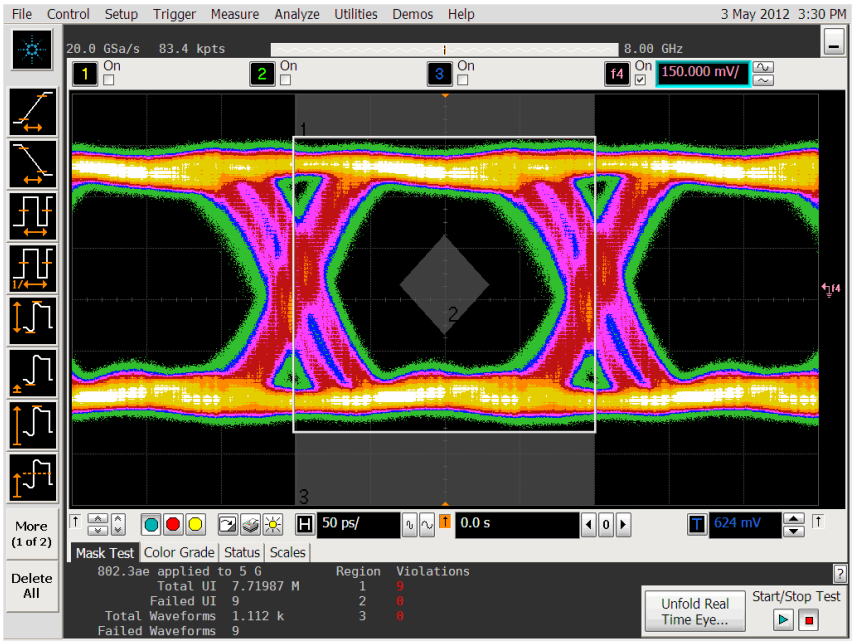
Receiving LVDS signal from channel 8, steering to VCSEL spare 1

Effect of Steering on Eye

Spare 1 output with other channels off

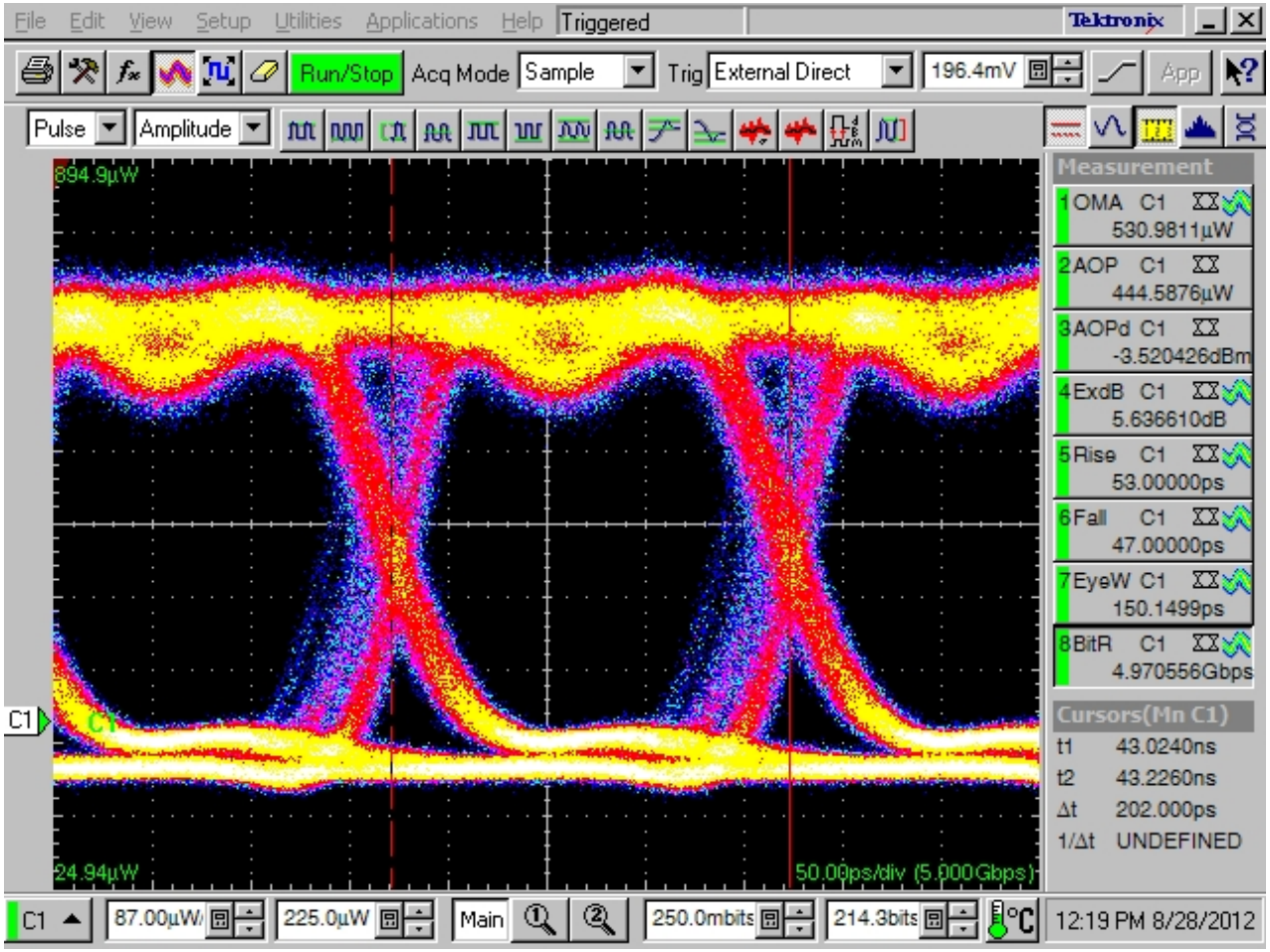


Spare 1 output with all channels active



- steered channel still passes the mask test
  - jitter increases with all channels active

Optical Eye Diagram of Steered Signal

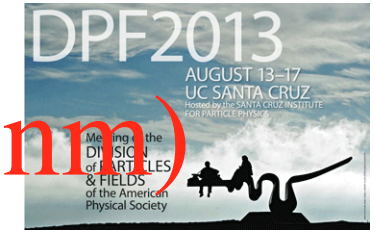


- optical eye diagram of steered signal @ 5 Gb/s is quite acceptable

Radiation Hardness

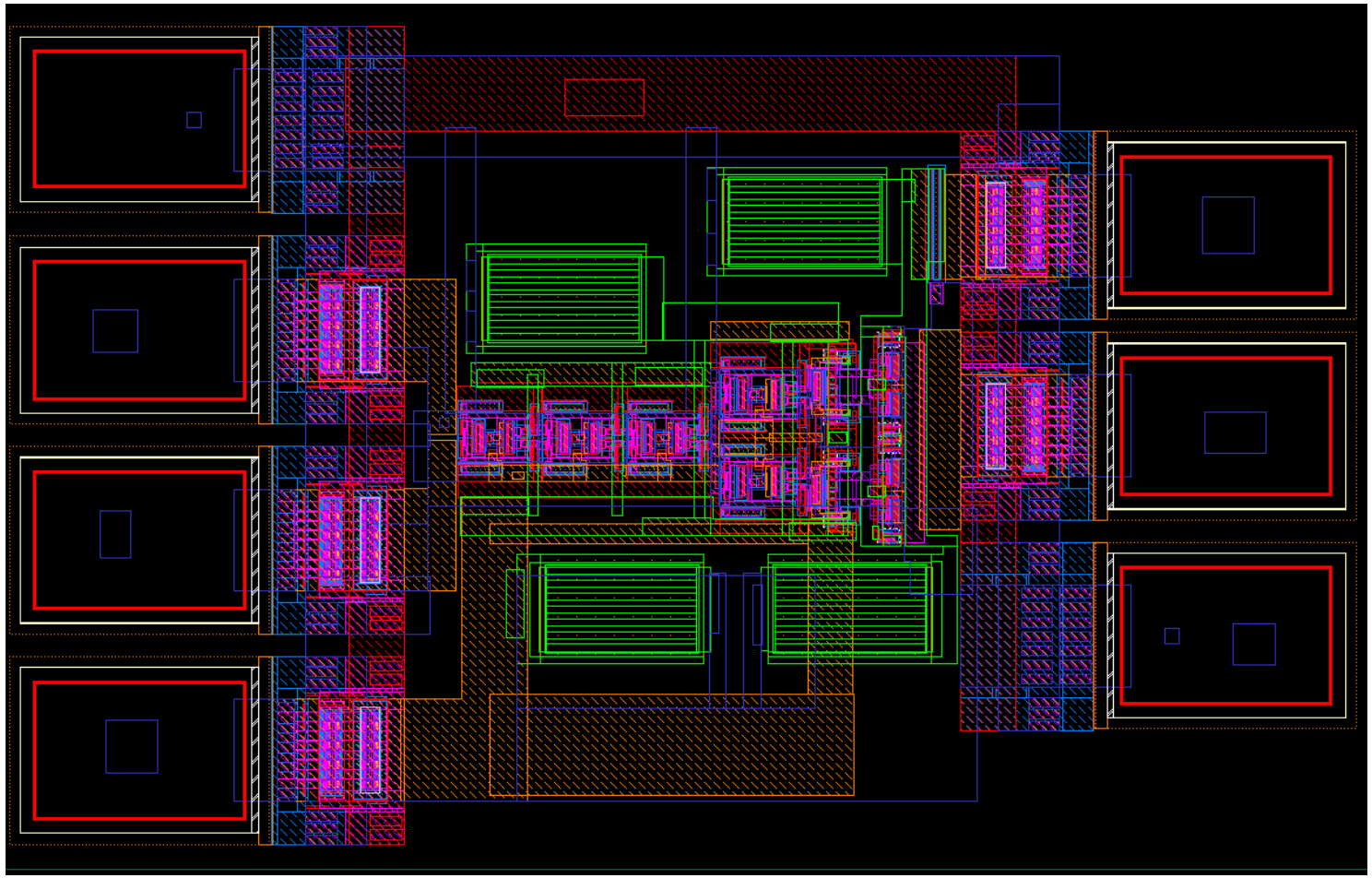
- 10 Gb/s VCSEL arrays have been proven to be radiation hard to tens of Mrad
  - send signal on ~1 m micro co-ax cables to less radiation and more serviceable location
- VCSEL array drivers + ULM 10 Gb/s VCSELs were irradiated with 24 GeV protons at CERN last August to 1.51×10^{15} protons/cm^2 (33 Mrad in GaAs)
  - Preliminary tests show problems operating at 5 Gb/s unless VDD increased (4 Gb/s is fine)
  - Suspect VCSEL damage (threshold shifts) to be the cause of reduced speed
    - need to confirm this with a separate irradiation

10 Gb/s VCSEL Driver (130 nm)

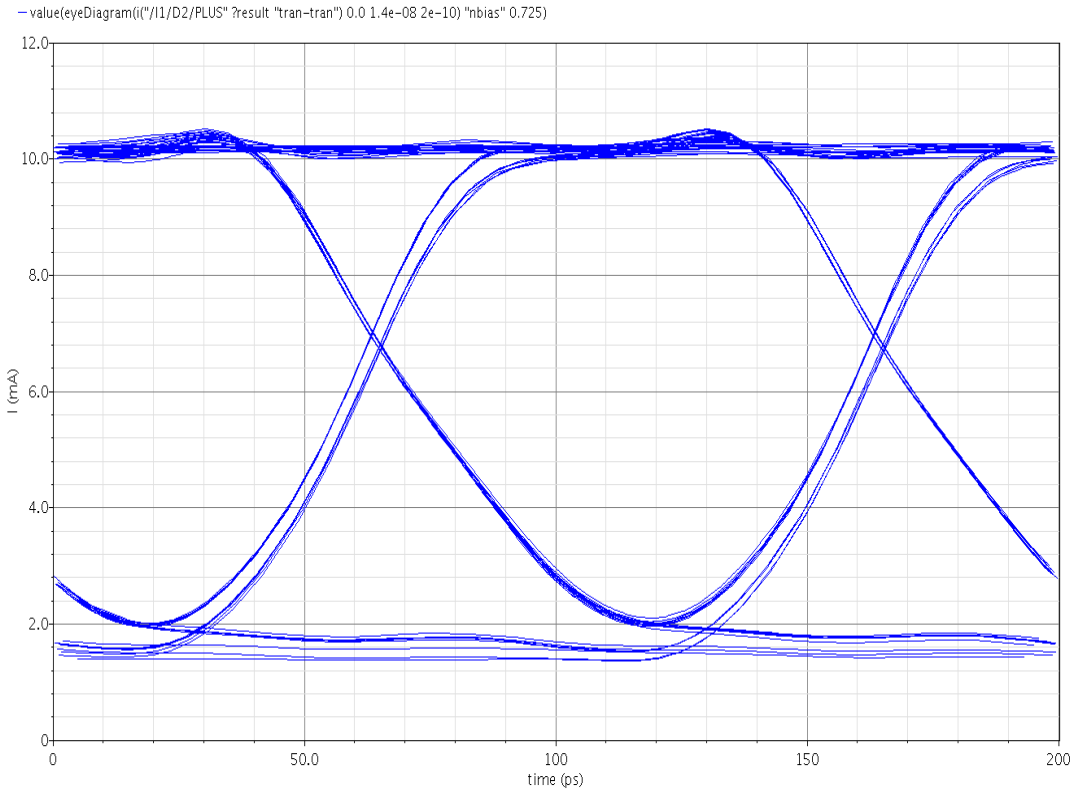


- 10 Gb/s transmission needed
  for ATLAS inner pixel layer and LAr readout upgrades
  - joint ATLAS/CMS proposal funded
    via US DOE generic R&D program
  - preliminary work indicates that
    we can achieve 10 Gb/s in 130 nm CMOS
  - have a working layout but would like to optimize further

10 Gb/s VCSEL Driver Layout



10 Gb/s VCSEL Driver



simulation of extracted layout of driver stage with parasitics of bond pads and proven version of VCSEL model

Future Plan

- planning to port design to 65 nm CMOS
  - recently signed non-disclosure agreement (NDA) with TSMC
  - plan for 4-channel prototype submission by end of this year
- recommended for funding of MRI proposal (OSU+SMU) to NSF
  - OSU will acquire high-speed, modern equipment to replace equipment acquired with previous MRI in 2003
  - special thanks to NSF for enabling US to continue the leading role in the optical link R&D and fabrication

Summary

- VCSEL array offers compact solution to data transmission
- 5 Gb/s VCSEL array driver successfully prototyped
- Currently designing 10 Gb/s VCSEL array driver