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Radiation-Hard/High-Speed Parallel Optical Engine

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The LHC at CERN is now the highest energy and luminosity collider in the world. Upgrades to the accelerator are currently being planned to further increase the energy and luminosity. The detectors must be upgraded to take advantage of the planned accelerator upgrades. This requires the optical links to transmit data at much higher speed to handle the much increased luminosity. We will present the results from three R&D projects. The goal of the R&D is to develop an ASIC that contains an array of 12 high-speed drivers to operate an array of 12 VCSELs (Vertical Cavity Surface Emitting Lasers). With the spacing of 250 μm between two VCSELs, the width of an optical array is only 3 mm. High speed VCSEL arrays operating at 10 Gb/s are now readily available and have been proven to be radiation-hard in our previous studies. This allows the deployment of a compact 120 Gb/s parallel optical engines at a high radiation location close to the interaction region where space is at a premium.
We incorporate the experience gained from the fabrication and operation of the optical link system of the current ATLAS pixel detector into the design of the new ASICs. For the first R&D project, the ASIC is a 12-channel VCSEL array driver operating at 5 Gb/s per channel. Each channel has an LVDS receiver, an 8-bit DAC, and a VCSEL driver. The 8-bit DAC is used to set the VCSEL modulation current. There is also a single 8-bit DAC to set the bias currents of all channels simultaneously. A scheme for redundancy has also been implemented to allow bypassing of a broken VCSEL. To enable operation in case of a failure in the communication link to the ASIC, we have included a power on reset circuit that will set the ASICs to a default configuration with no signal steering and the VCSEL modulation current to 10 mA. The ASIC was designed using a 130 nm CMOS process to enhance the radiation-hardness. The performance of the fabricated ASIC at 5 Gb/s is satisfactory. We are able to program the bias and modulation currents and to bypass a broken VCSEL channel. The power-on reset circuits have been successfully implemented.

For the second R&D project, we modify the design of the ASIC to operate at 10 Gb/s. The 5 Gb/s VCSEL driver uses thick oxide transistors in order to provide sufficient voltage to drive the VCSEL. This is not practical for the high speed operation. We therefore modify the architecture to use thin oxide transistors and add a negative VCSEL bias voltage. We simulate the extracted layout with parasitic capacitance, inductance, and resistance from the VCSEL itself and the wire bonds and pads used for connecting the VCSEL to the ASIC. The simulated eye diagram is open, indicating that it is possible to design an ASIC to operate at 10 Gb/s using a 130 nm CMOS process.

For the third R&D project, we plan to export the design to a 65 nm CMOS process to further increase the operating margin at 10 Gb/s. This will allow us to compare this design to the 130 nm design which is not as expensive. We will present the preliminary results from this design.

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