Silicon strip prototypes for the Phase-II upgrade of the ATLAS tracker for the HL-LHC

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... and help from many others

Santa Cruz (CA), 16th Aug 2013

The LHC schedule

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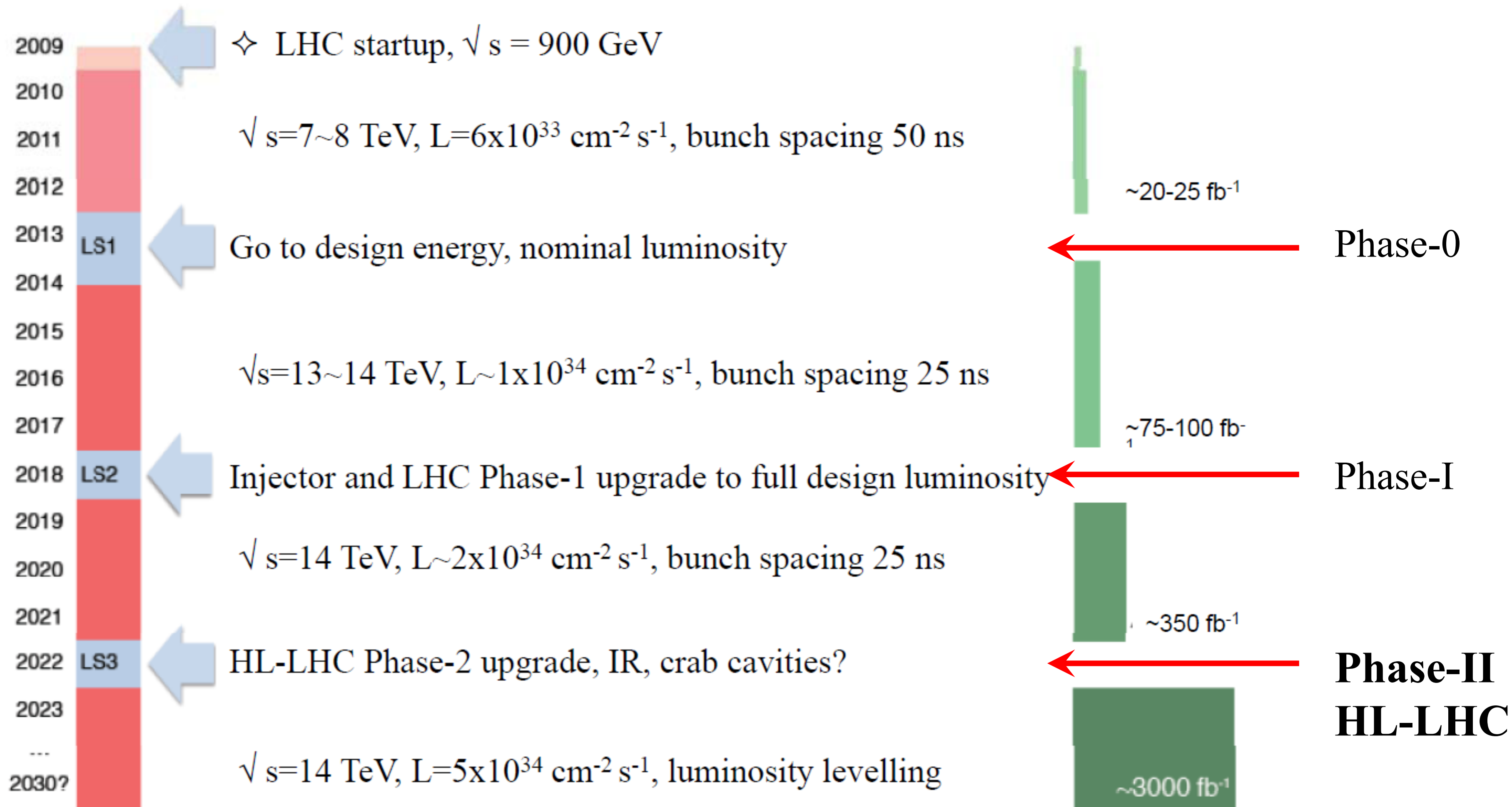
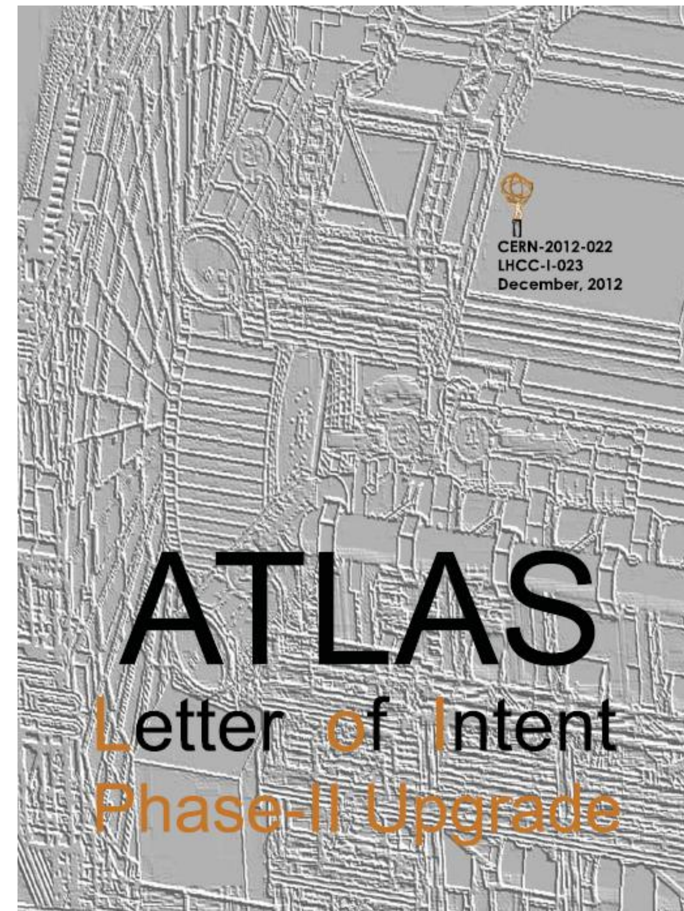


The ATLAS Phase-II upgrade

Major ATLAS upgrades for the HL-LHC upgrade:

- **Tracking**
  - **Major revision, new Inner tracker including LVL1 trigger capability + new services**
- Calorimetry
  - New Front and back-end electronics, including trigger, new forward calo if proven necessary Fix Lar hadronic cold electronics if necessary
- Muon system
  - Increase trigger capability in the big wheels, add additional trigger inner layers in the barrel. New FE electronics
- Trigger/DAQ
  - Major revision
- Common systems
  - New TAS and forward shieldind. Major infrastructure consolidation, including safety systems



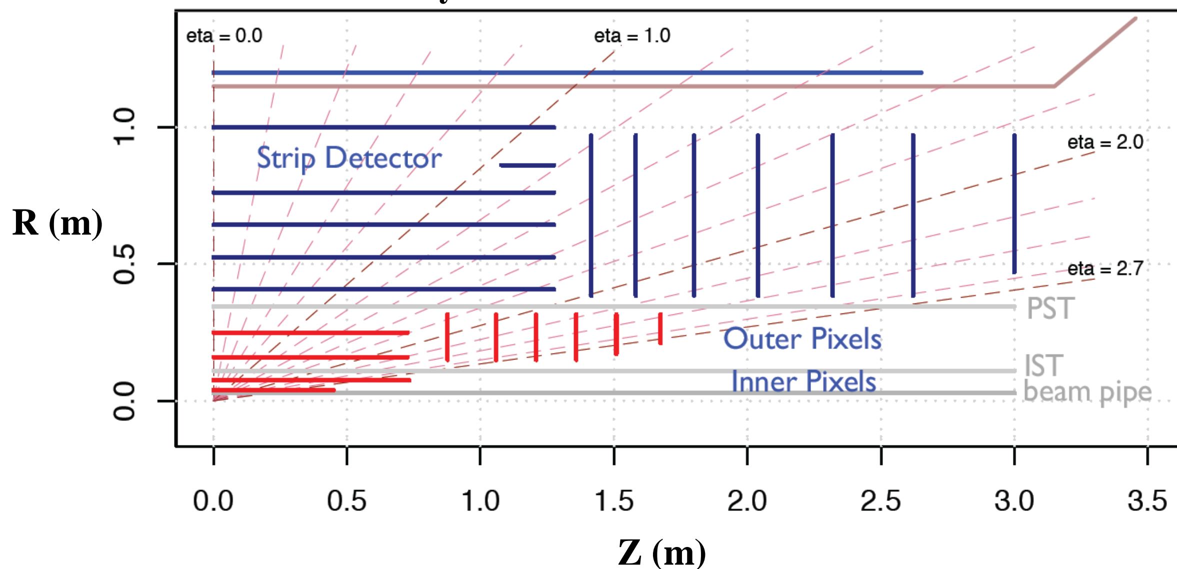
http://cds.cern.ch/record/1502664?ln=en

ATLAS Phase-II LoI released on Jan 2013

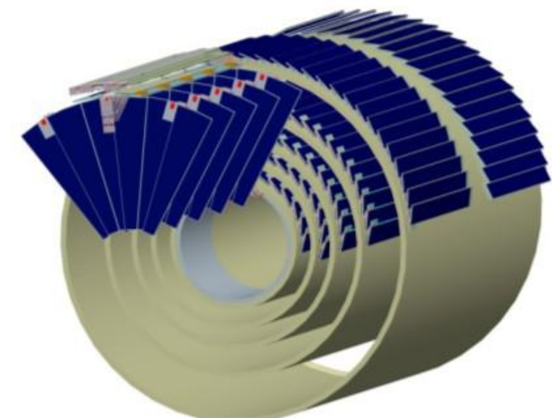
ATLAS Phase-II upgrade tracker

- Numerous challenges for silicon sensors on ATLAS Phase-II Upgrade
  - Higher granularity to keep same low occupancy
  - Higher radiation tolerance to deal with increased radiation environment
  - Novel powering solutions to power efficiently x7.5 more channels
  - Maintain low cable count to keep detector performance
  - Reduce cost per sensor to cover larger area (~ 200 m^2)
- Replacement of ATLAS Inner detector by an **all-silicon tracker**:

"LoI layout" for the Phase-II Silicon tracker

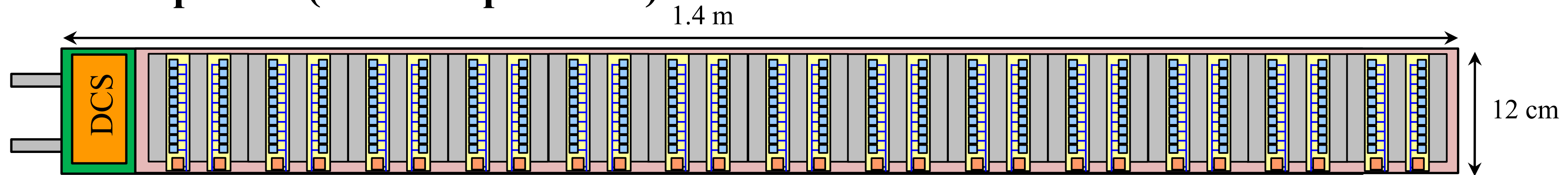


Strip detector
3 layers of short strips (2.5 cm) **staves**
2 layers of long strips (4.8 cm) **staves**
14 disks of endcap **petals**



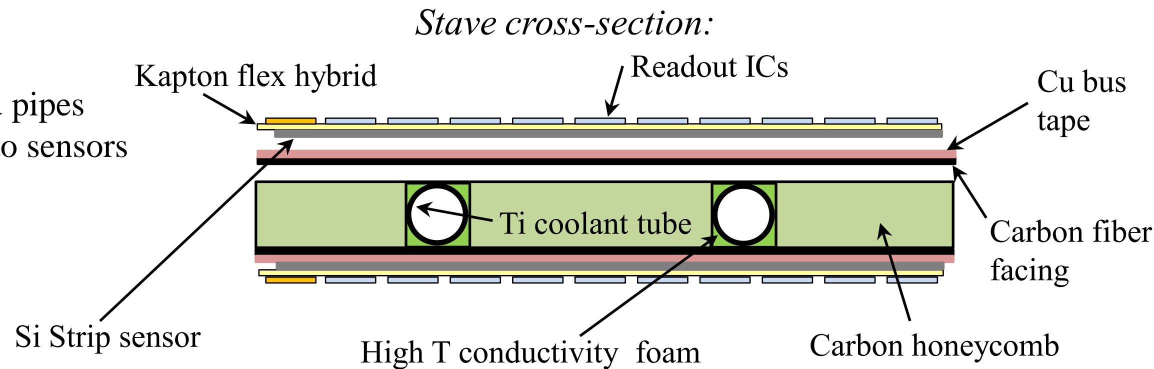
Stave concept for strip tracker

Barrel strip stave (short strip version):

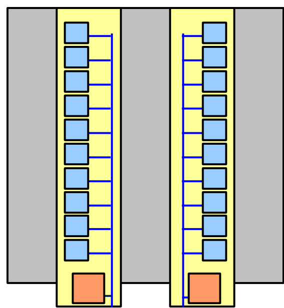


- Designed to minimize material
  - Shortened cooling paths
  - Module glued to stave core with embedded pipes
  - No substrate or connectors, hybrids glued to sensors
- Designed for large scale assembly
  - Simplified build procedure
- All components testable independently
- Aimed to be low-cost
  - Minimize specialist components

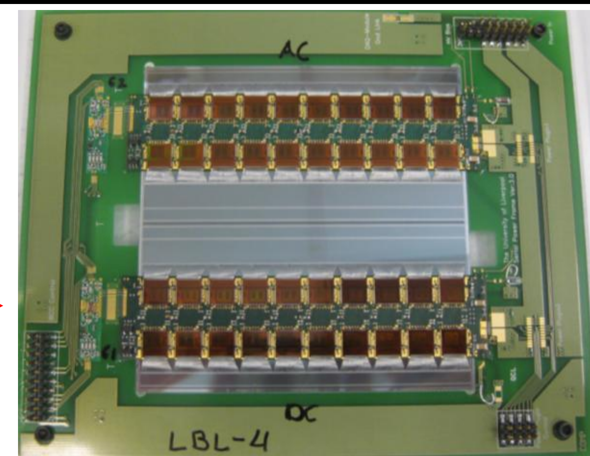
Stave cross-section:



Short strip module:



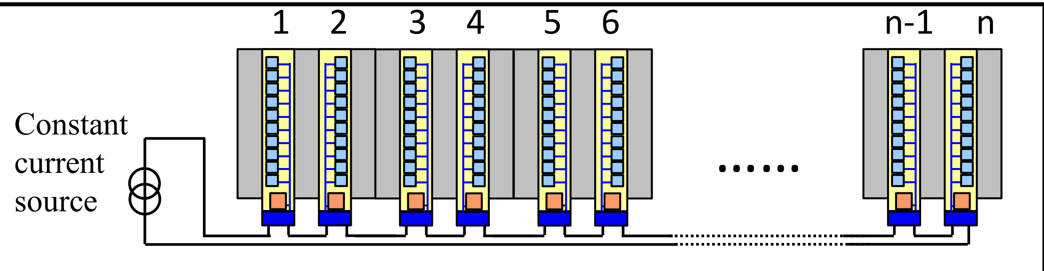
- 1 n-in-p strip sensor with 4 x2.5cm strips (5120 channels)
- 2 hybrids directly glued onto Si sensors
  - 10 ABCN130 ASICs (256 ch) + 1 HCC/hybrid
- Strips connected to FEE with wire bonds
- Binary readout
- Current prototypes: ABCN250 (128 ch/chip) + BCCs
  - More than 70 modules produced



Power and additional electrical components

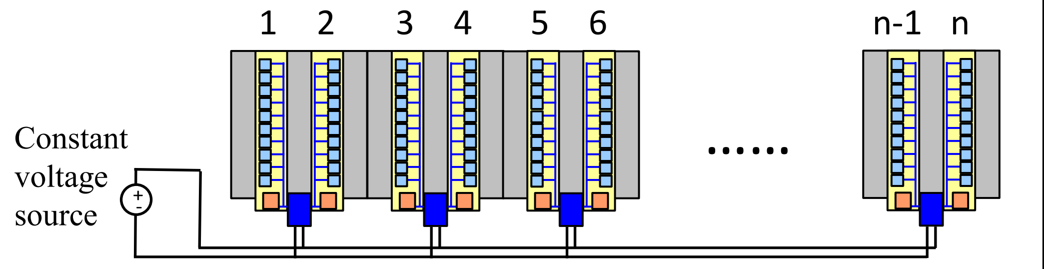
- LV: Two powering distributions under study for *n hybrids,* each with *current I*

  - **Serial powering**
    - Total current = I
    - Different GND levels per hybrid
    - AC coupling of data lines
    - Bypass protection required



  - **DC-DC powering**
    - Total current = $n \cdot (I/r^*)$
    - Switching system
    - Can be noisy
    - High mass

  *r = voltage conversion ratio

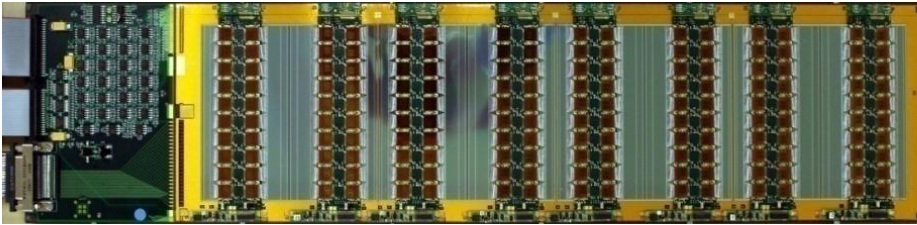


- HV: rad-hard switches for multiplexing under study and demonstrated for short staves recently

- Additional electrical components of the stavelet
  - **Bus tapes**: data and power traces, co-cured with carbon fiber facings
  - **End of Stave (EoS) boards**: multi-module readout and control

Stave prototypes

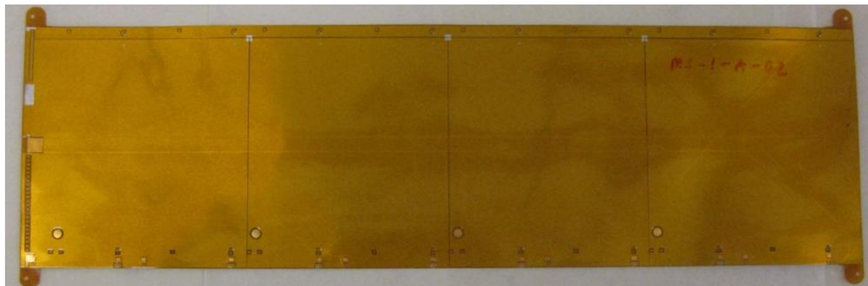
- "Stavelets": shortened short strip stave prototypes with 4 modules
  - Key test bed for electrical testing, powering, protection, G&S, …
  - Single-sided stavelets built and tested so far at RAL and LBNL, each with unique features
  - Full-lenght staves in construction



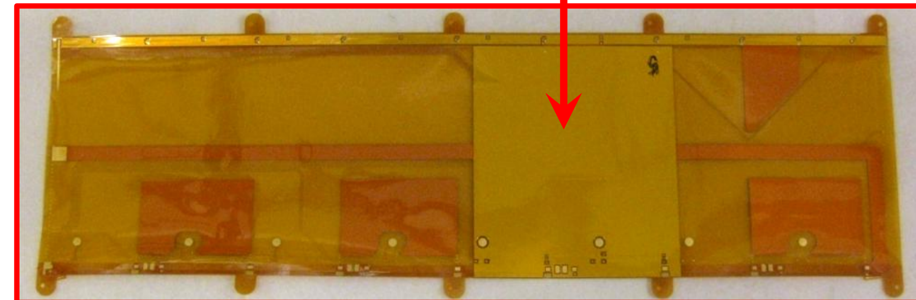
  - Double-sided, shieldless stavelet recently assembled at LBNL

Motivation and features of double-sided stavelet

- **Double-sided stavelet** prototype: one side DC-DC, other side serial
  - Proof of principle of double-sided stave concept for the first time
  - Test of both power distributions on a identical test bench
- **Shield-less bus tape**: Al shielding layer removed from tape; CF acts as effective shielding
  - Reduces the material budget of the tapes by ~ 50% (8-10% reduction overall stave)
  - Co-curing complexity greatly reduced (deformations become marginal)
  - Tape costs reduced
  - Shield left at one module position for comparison



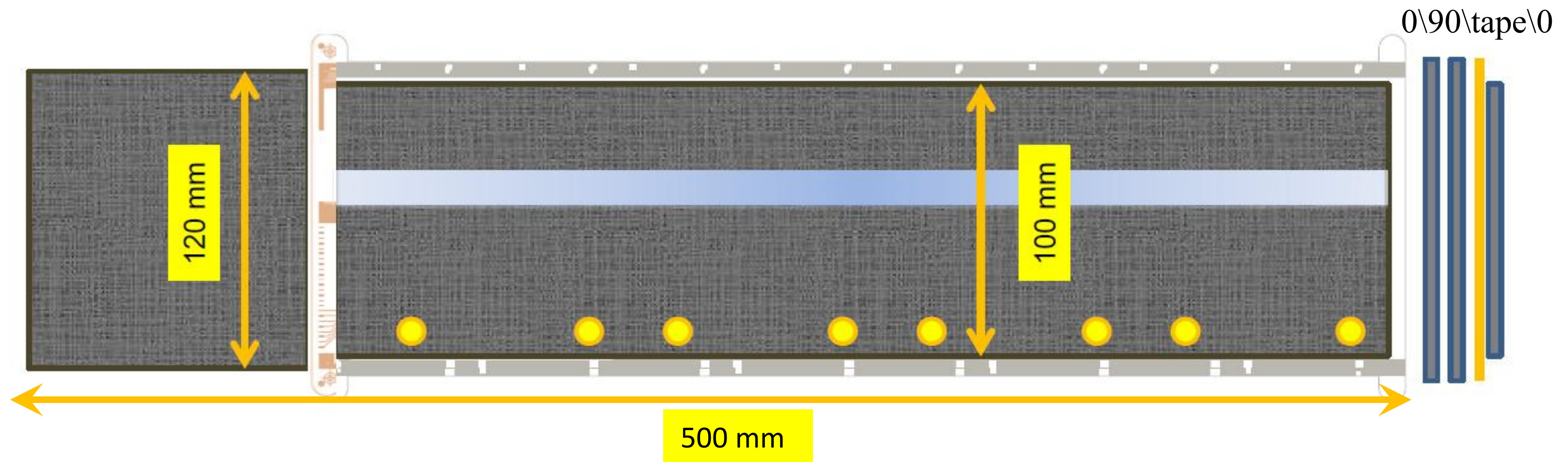
Baseline layout

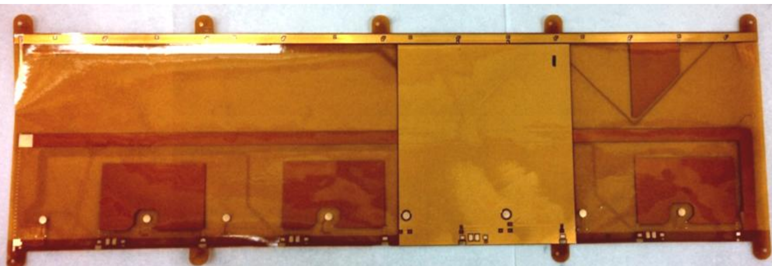


Shield-less tape

Tapes co-curing and core lamination

- Tapes co-cured in between CF layups
  - Last CF layer acts as shielding
  - Simplified co-curing procedure (co-cured on flat surface)



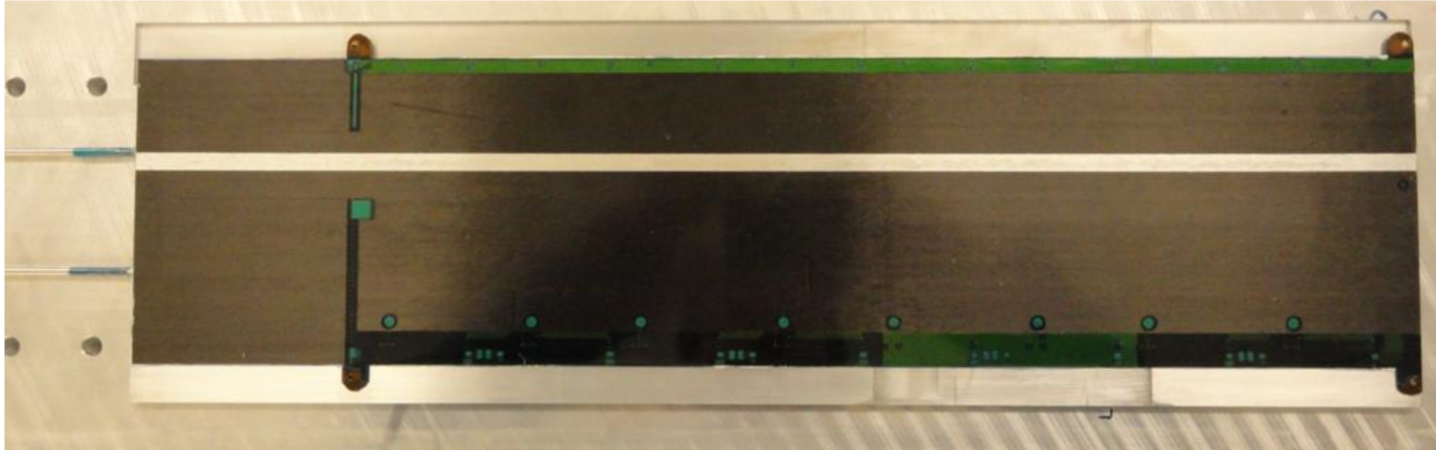


Shieldless core and assembly tools

Baseline design

Shieldless core and assembly tools

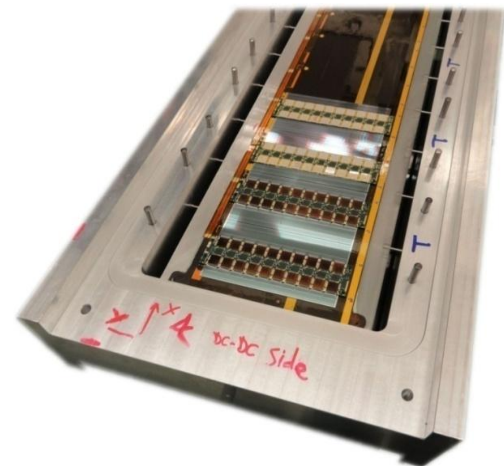
Shieldless core

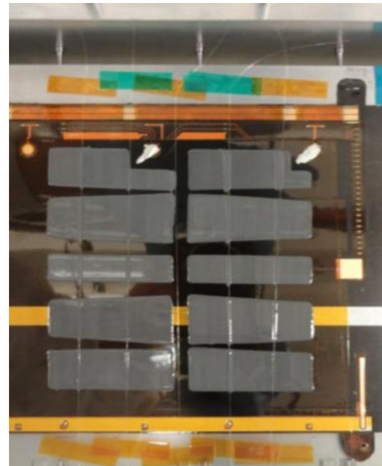


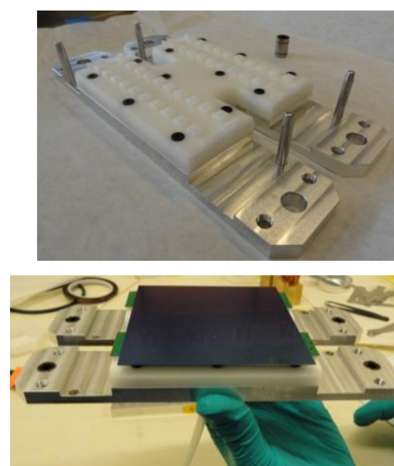
Shieldless core and assembly tools

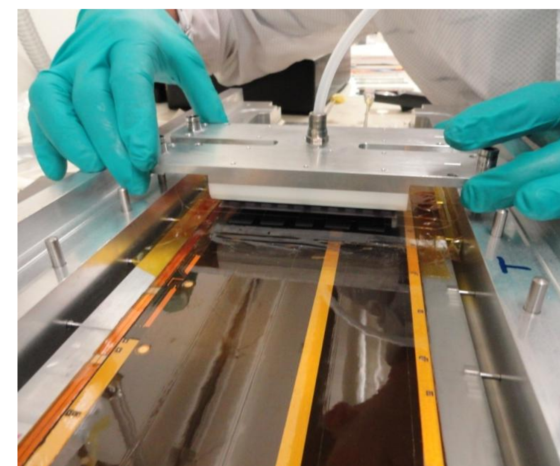
Shieldless core

- New precision mechanical tools developed for stavelet assembly
  - Allow module placement with **X-Y precision accuracy ~ 150 µm**, **glue thickness ~ 175 µm**



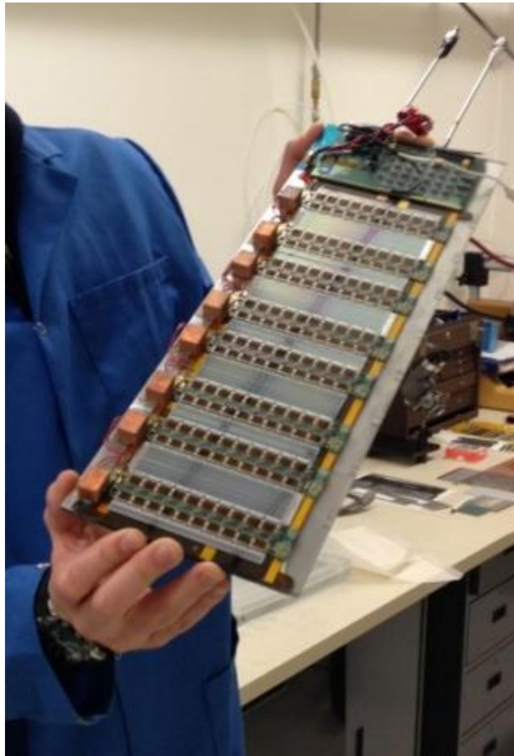




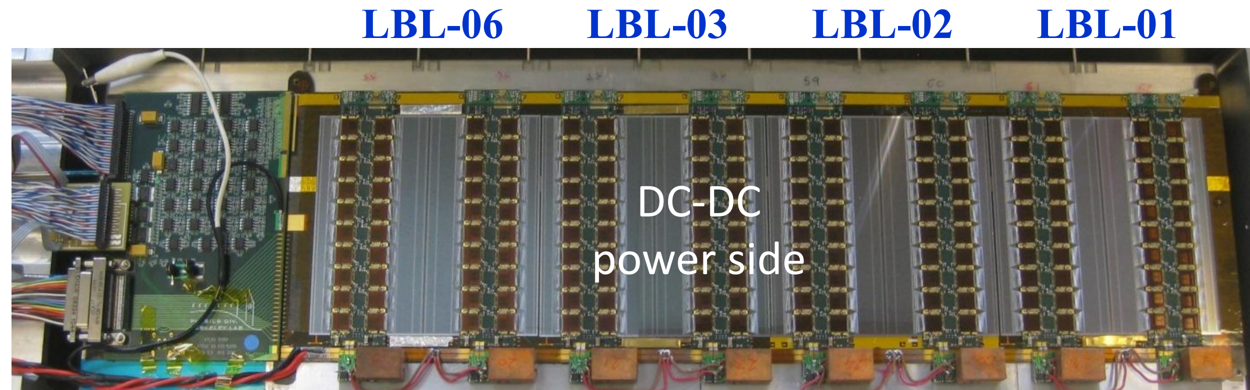


Shieldless stavelet

- Both sides fully loaded
  - Modules assembled at Berkeley and UC Santa Cruz



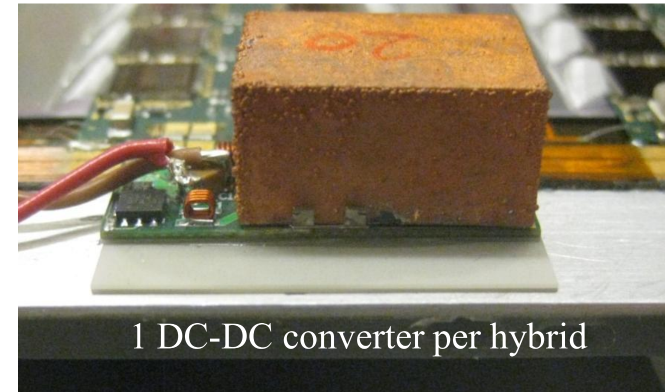
LBL-06 LBL-03 LBL-02 LBL-01



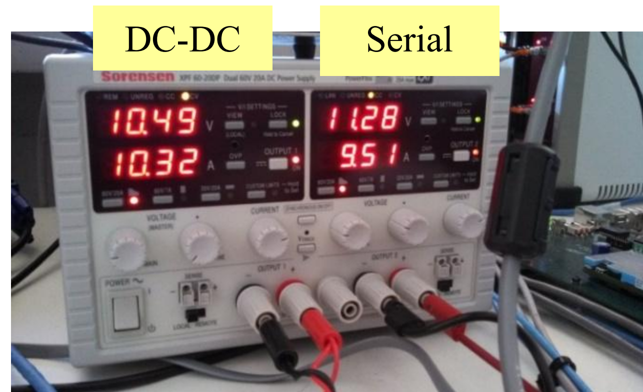
LBL-07 SC-03 SC-02 SC-01

Power components and numbers

- DC-DC power side
  - 1 DC-DC converter per hybrid
    - Constant voltage: 10.5 -11 V
- Serial power side
  - 1 Power Protection Board (PPB) per module
    - Allow slow control/fast response bypass of modules within the SP chain
    - Constant current 9.50 A
- Real time power during electrical tests:


1 DC-DC converter per hybrid

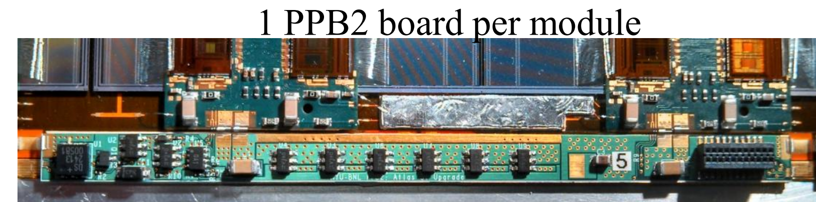
DC-DC | Serial



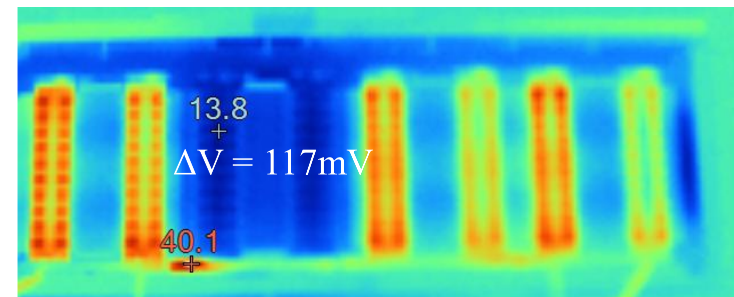
DC-DC:
V_{const} = (2.7 x 3.75) V
I_{tot} = (8 x 1.3) A

SP CoM:
V_{tot}= (4 x 2.8) V
I_{const} = (2 x 4.25) A

1 PPB2 board per module

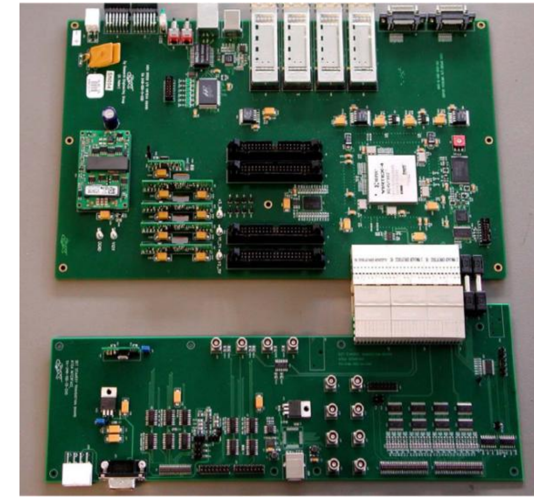


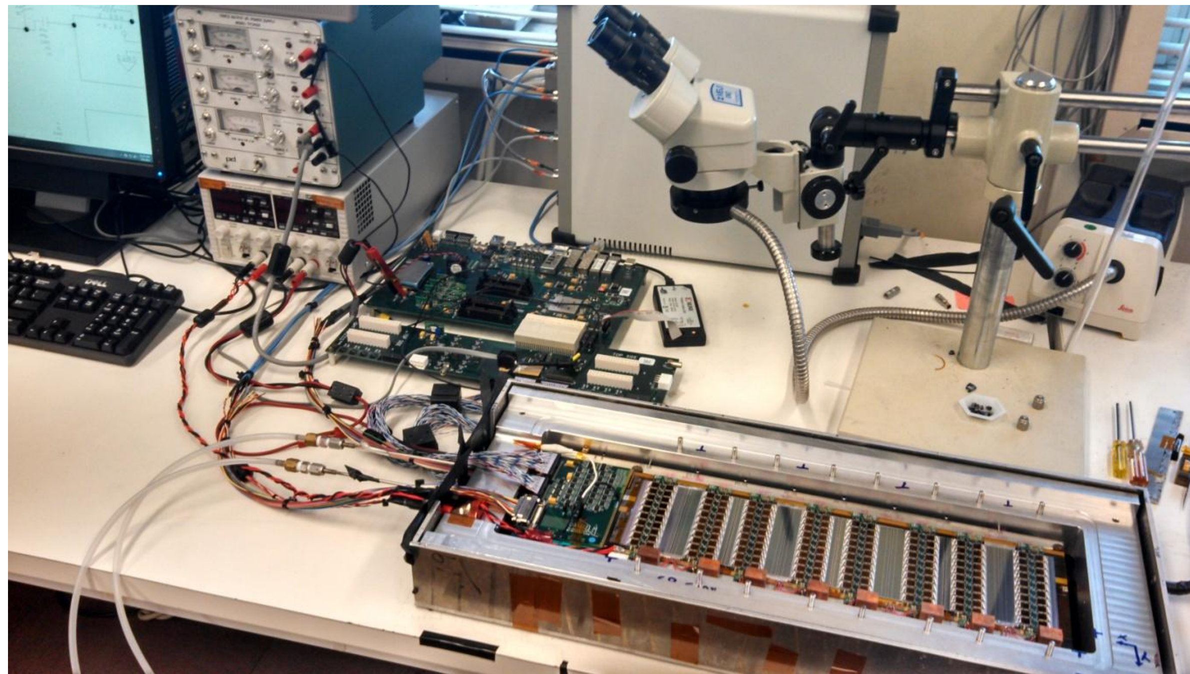
PPB2 slow control disables M2

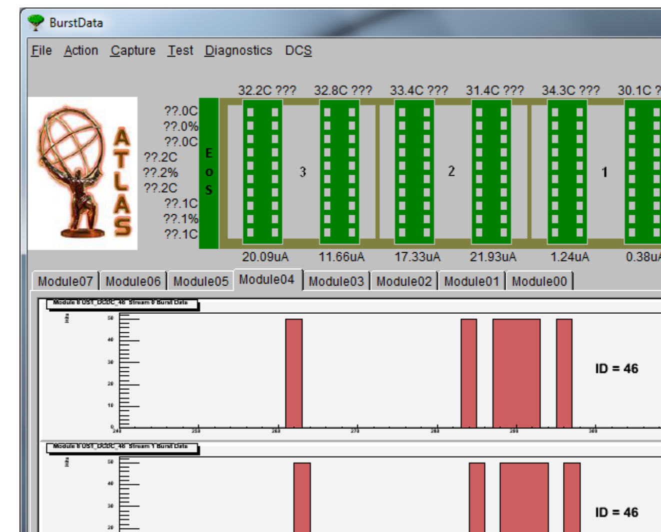


Electrical test setup

- Simultaneous readout of 8 modules (16 hybrids, ~ 41000 strips)
  - **DAQ**: Generic HSIO board (Virtex-4 FPGA)
  - Dedicated **firmware** and **software**
  - **LV**: Sorensen XPF 60-20DP dual output power supply
  - **HV**: Custom ATLAS SCT HV VME cards (2x4 channels)
  - **Water cooling** ~ 6°C and test box flushed with N_2



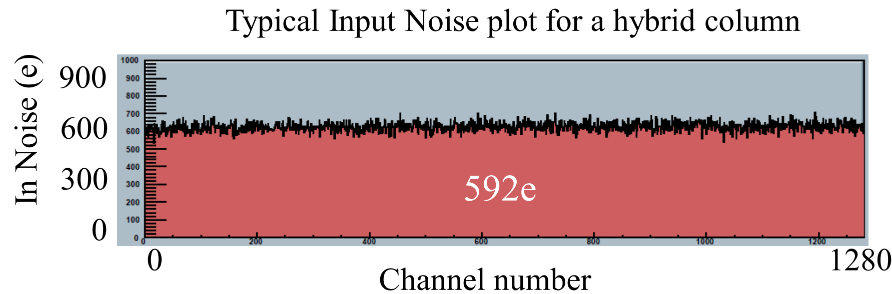




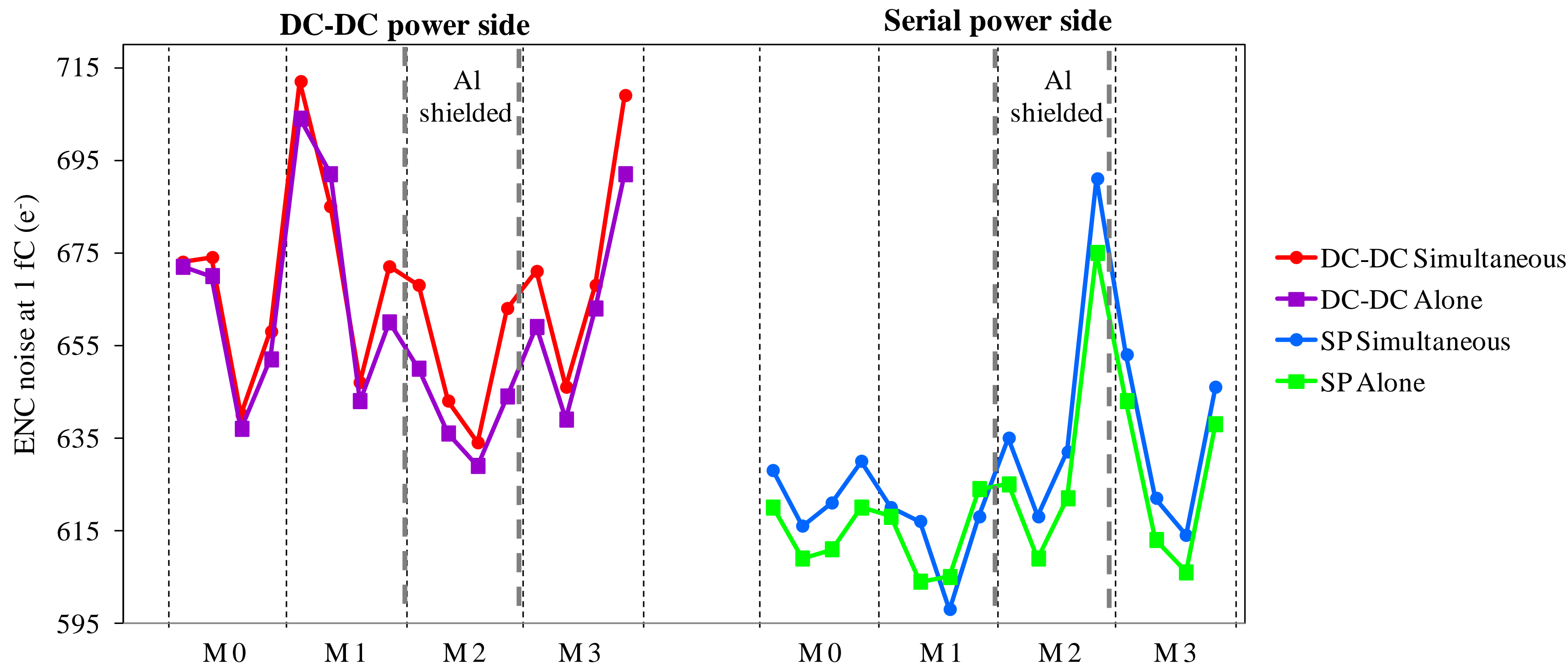
Thanks UK colleagues!

Results: electrical performances

- Electrical tests on stavelet
  - **ENC noise:**
    - Threshold scans at several input charges
    - Occupancy curve (s-curve) ⇒ response curve + output noise ⇒ Gain ⇒ **Input ENC noise**
    - Typical target value at 1fC input charge: **600-650 e^-** (S/N =10.42)



Results: ENC noise at 1 fC

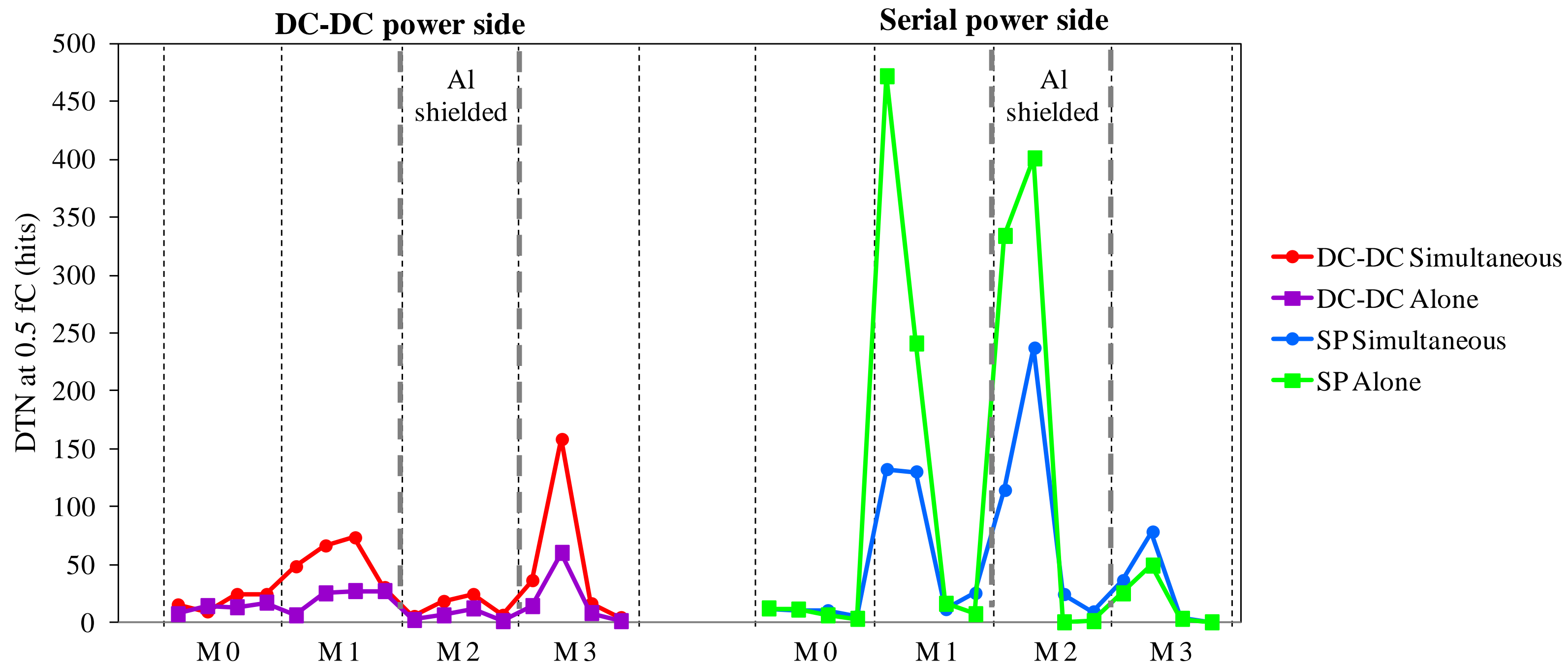


- Acceptable noise results for both sides running simultaneously and synchronous
  - Results consistent with previous prototypes
- Slight increase in ENC noise on both sides when running simultaneously (> 7.5e$^-$ avg)
  - Can be fully attributable to T increase (~ 1.5e$^-$/^{o}C)
- Consistently lower ENC noise by ~ 25-30 e$^-$ on serial power side
- Al shielded module shows no significant difference in either case

Results: electrical performances

- **Double trigger noise** tests:
  - Known issue for deadtimeless systems (simultaneous integration and readout): readout trigger signals may produce noise interference during charge integration
  - For a series of fixed thresholds, issue a trigger, readout and discard, wait for 132 cycles, issue a trigger, readout
  - The second trigger probes the occupancy as was integrated during the first trigger
  - Ideally, one should expect 0% occupancy (0 hits)
  - Results on a 30 CLK cycles interval centered in the ABCN pipeline length (132)
  - Threshold set at 3 different injected charge values (1, 0.75 and 0.5 fC)
  - NO charge injected

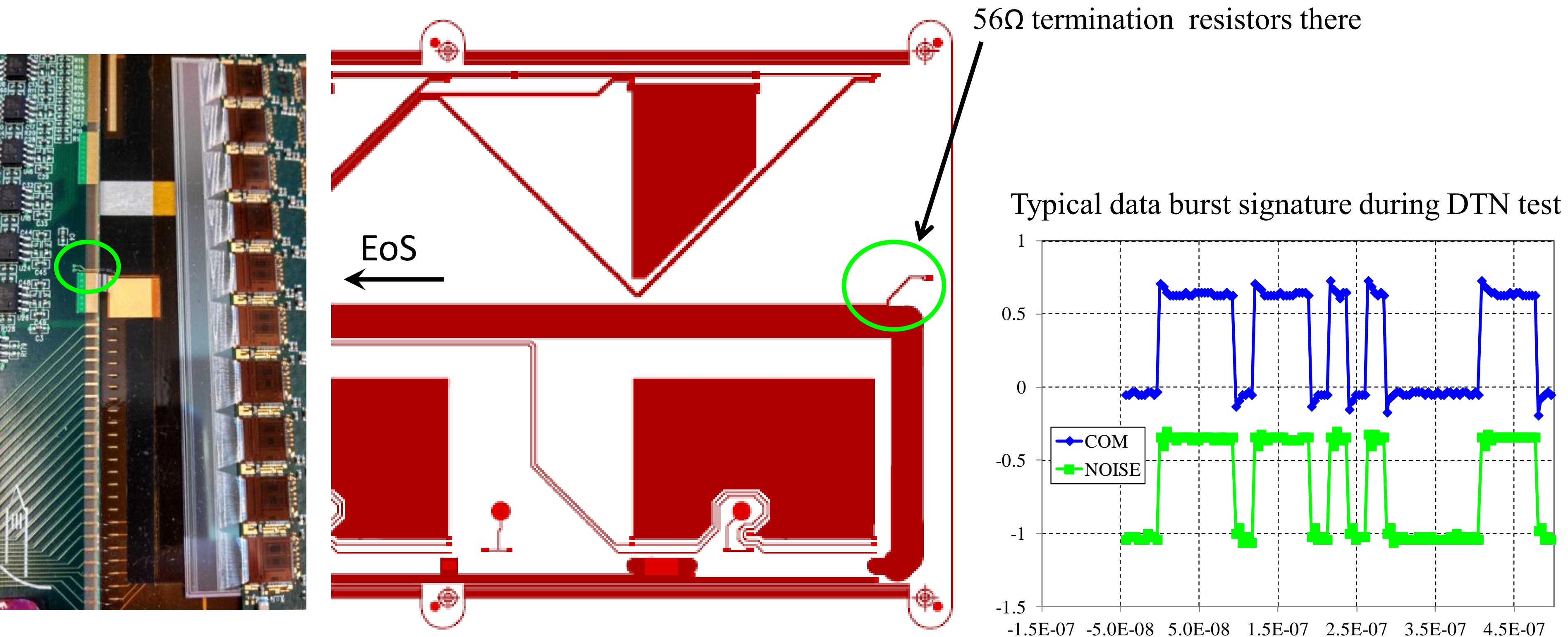
Results: DT noise at 0.5 fC



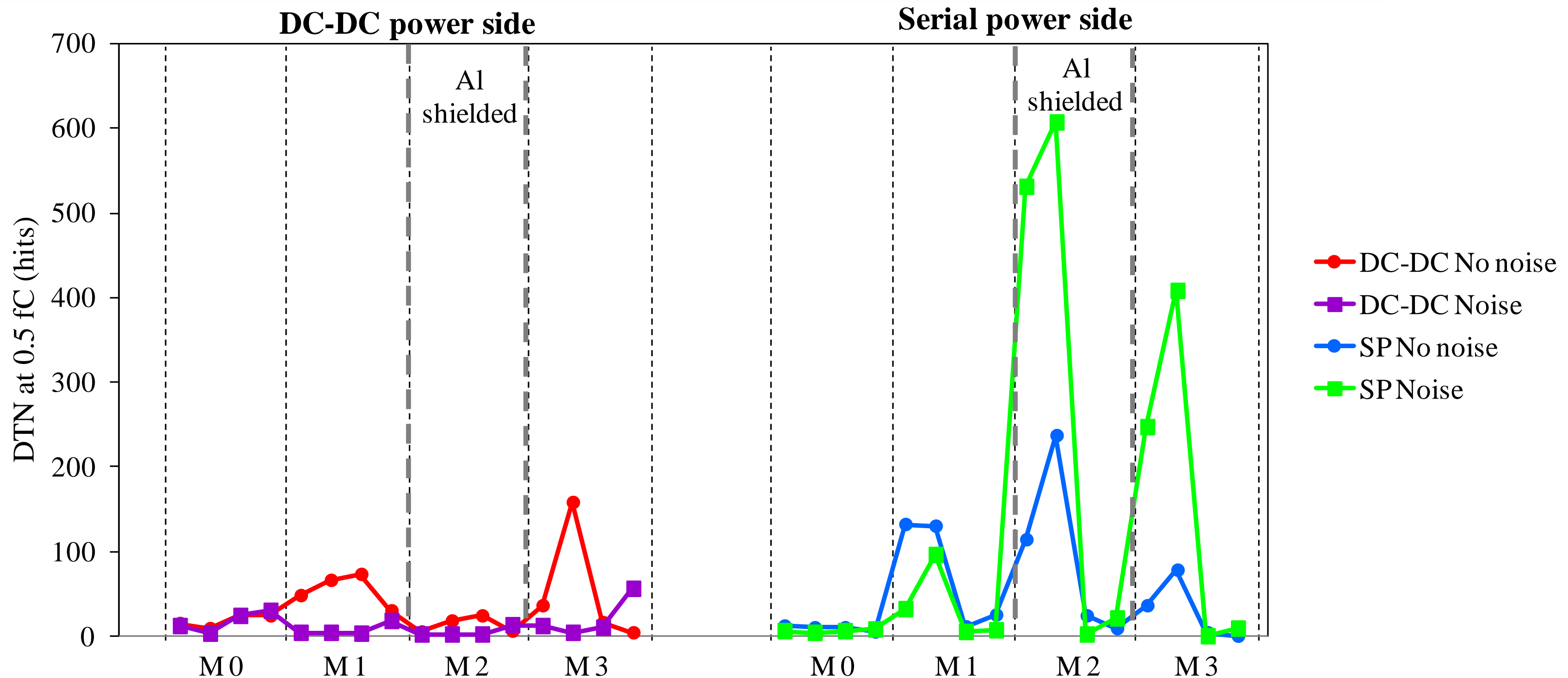
- DC-DC side: only 1 column with > 100 hits at 0.5 fC, clean at 1 and 0.75 fC
- SP side: 2 hybrids show DTN > 200 hits, clean at 1, 0.75 fC
- Lower, more stable DTN on DC-DC power side
  - DC-DC: Only 1 chip column above 100 hits
  - SP: 2 hybrids (4 chip columns) above 100 hits, results not completely reproducible
  - Worst case is shown here: related to CM noise developing along data lines
- Al shielded module shows no significant difference in either case

Noise injection on pulsing lines

- Noise pulsing lines were included in bus tape to artificially inject noise all along the stavelet
  - COM signals are rerouted synchronously through pulsing lines during tests
  - Allows an accurate comparison between shielded and shieldless modules
  - Tests the robustness of stavelet prototype



DTN at 0.5 fC after noise injection



- DC-DC side: Negligible effects of noise injection on DTN
- SP side: DTN on "ugly" hybrids gets worse with noise injection, unchanged in the rest
  - One of those hybrids is on the Al shielded module
- Not shown here:
  - DTN clean at 1 and 0.75 fC on both sides
  - Negligible effects on ENC noise on both sides
- **NO significant difference between shieldless and shielded modules**

Summary and conclusions

- Shieldless, double-sided stavelet prototype for strips built and tested:
  - Setup developed for the reliable readout of a double sided stavelet
  - Minimal degradation of noise performances in both cases when running both sides synchronously
  - Comparison between both powering distributions on an identical test bench:
    - Slightly better ENC results for SP
    - Slightly better DTN results for DC-DC
  - No difference between shielded and shieldless modules, even after aggressive noise injection tests

- **Double-sided stave concept for strip modules demonstrated**
- **Al screen on bus tape not required, can be replaced by CF layer**
  - Less material
  - Easier co-curing
  - Cheaper cable

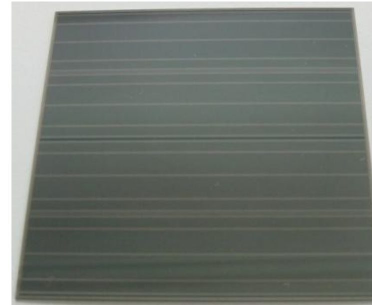
Backup

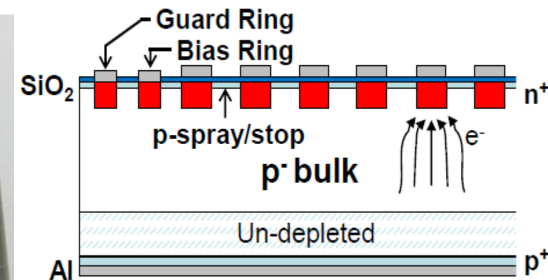
ATLAS strip collaboration

The ATLAS strips community

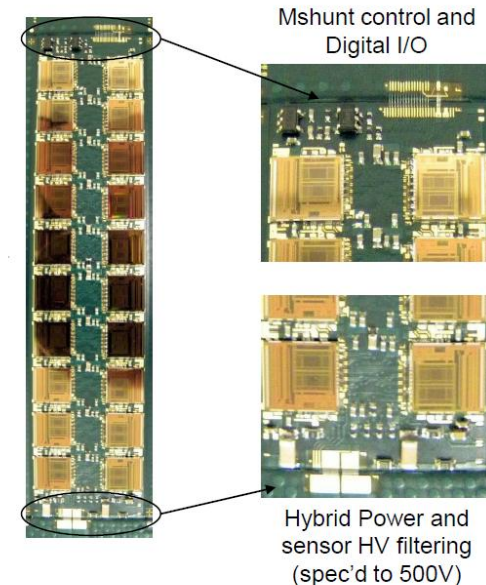
Strip module components

- **Silicon sensors**: n^+ strips in p-type substrate (n-in-p)
  - Collects electrons (as opposed to current p-in-n), depletes from segmented side, single-sided process
  - 9.75x9.75 cm^2 sensors fabricated on 6" wafers in collaboration with Hamamatsu Photonics
  - Barrel: rows of 1280 strips, 74.5 μm pitch, 2.5 cm long (short strips), 5 cm long (long strips), 40 mrad stereo-angle for 3D resolution implemented on layout
  - Meet electrical specifications, also after irradiation

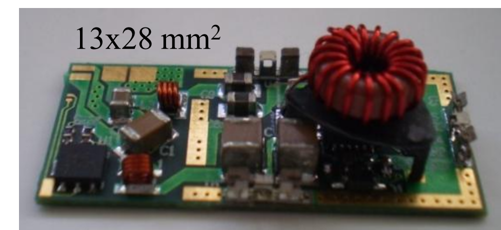




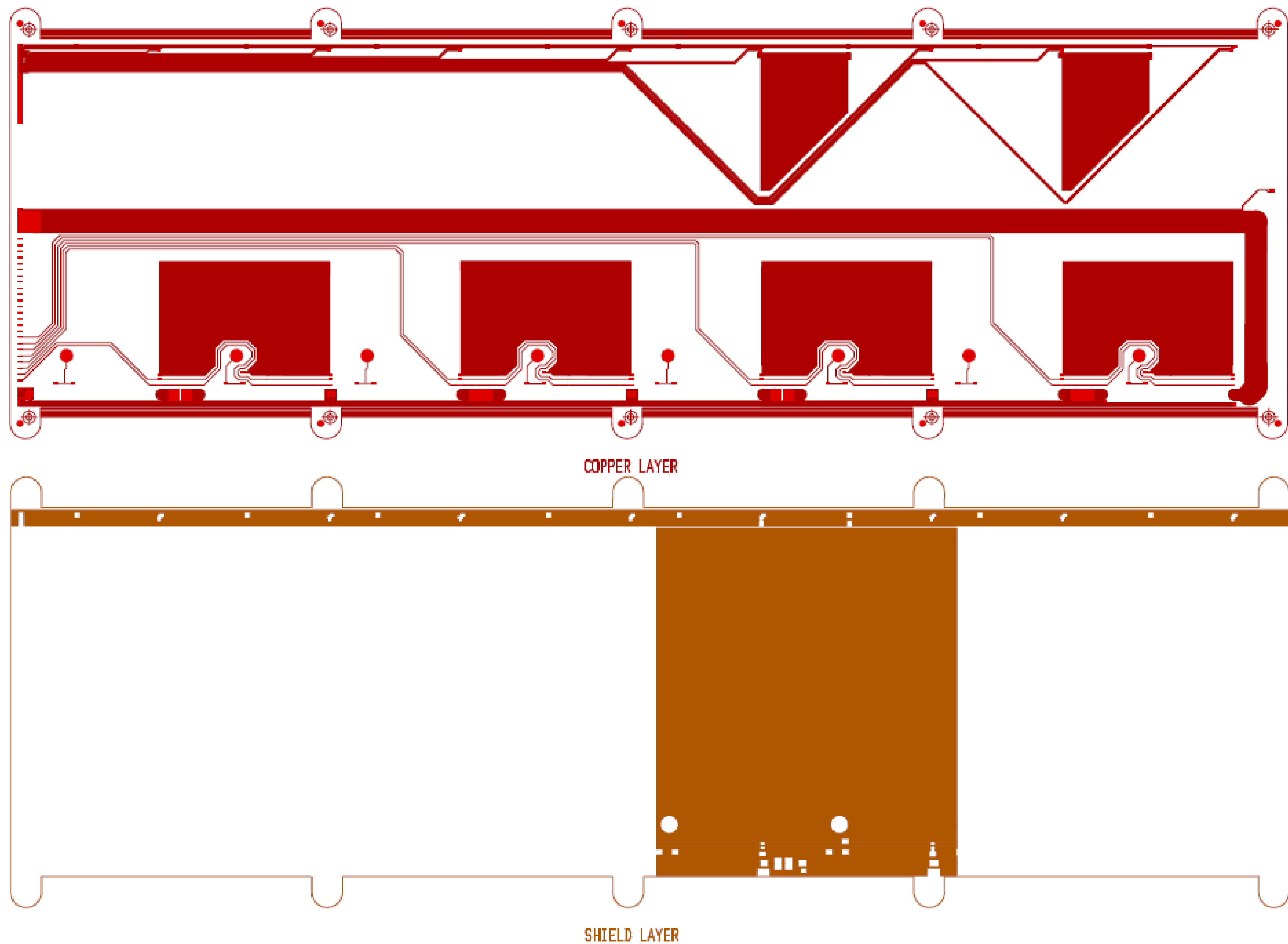
- **Readout and control electronics:** ABCN25 and BCCs (250 nm CMOS from IBM)
  - **ABCN**: 128 binary readout channels per ASIC, connected to sensor strips via wirebonds, mounted on **low-mass flex hybrids (**substrate-less, no connectors)
  - **BCCs**: Basic Control Chip process commands, generates 40-80 MHz CLK, handles hybrids addresses and 160Mb/s multiplexed data from each hybrid
  - Will be substituted by **ABCN-130** and **HCC** (130nm CMOS)



- **Power and protection circuitry**: Power Protection boards (SP), DC-DC converters (DC-DC)
  - **PPB**: fast response and slow-control bypass of modules within an SP chain
  - **Buck DC-DC converters**: custom low-mass inductor and shield + AMIS 4 ASIC (0.35μm LDMOS)

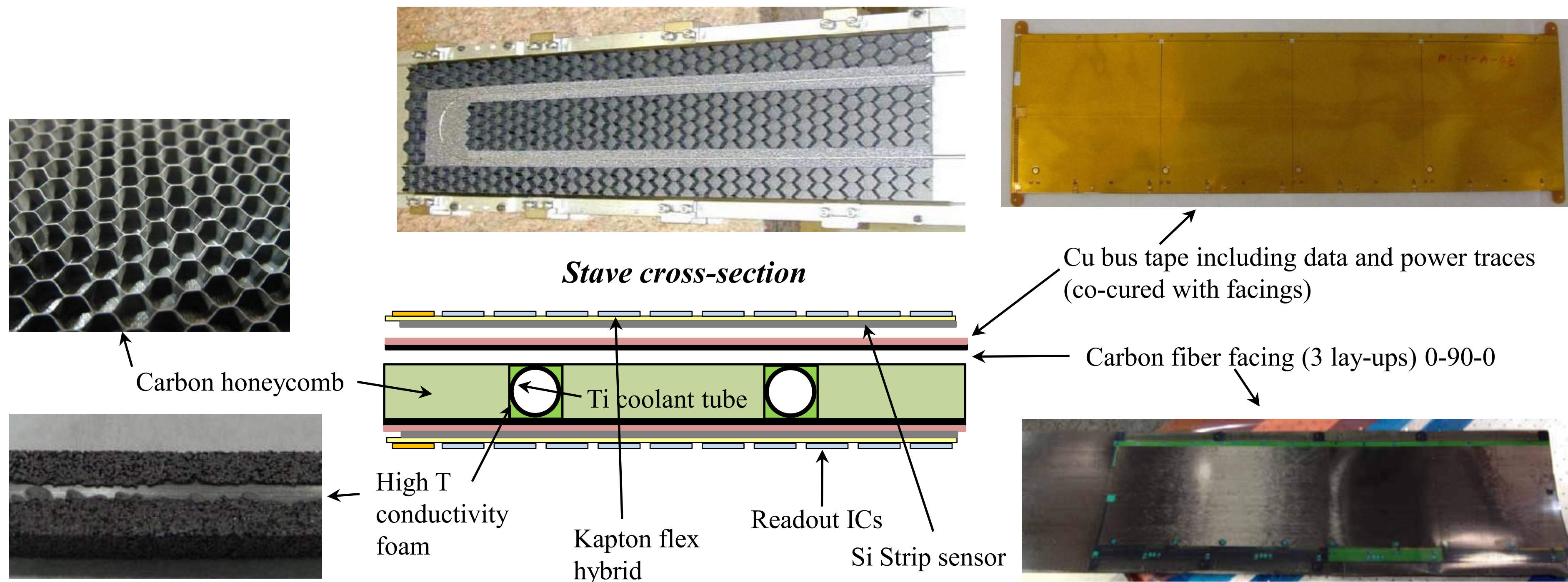


Shieldless tape



Stavelet core

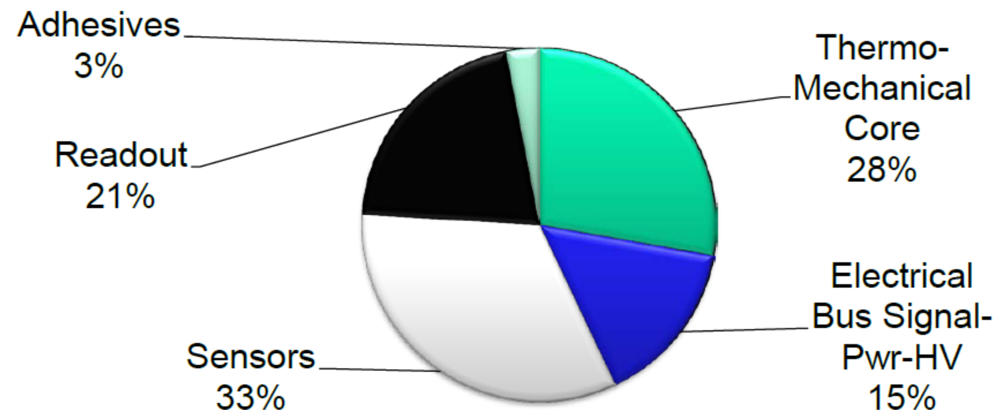
- Support structures (cores): low mass, embedded cooling pipes, good thermal performances, resistance to deformations, flat structure
  - Carbon composites: very flexible class of materials, reasonable Xo, good thermal properties, variable CTE
    - Carbon fiber "sheets" consist of filaments or woven layers impregnated with epoxy



Material budget

- Stave material estimates for 130 nm stave:
  - Based on as-built stavelets

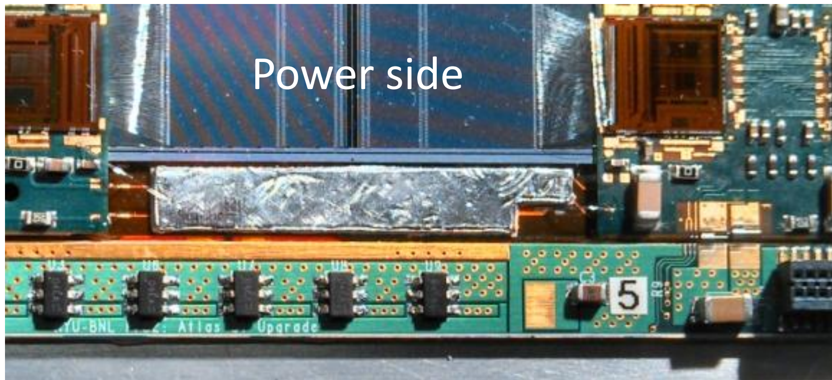
	%X0
Stave core	0.55%
Bus tapes	0.30%
Modules	1.07%
Module to stave adhesives	0.06%
TOTAL	**1.98%**



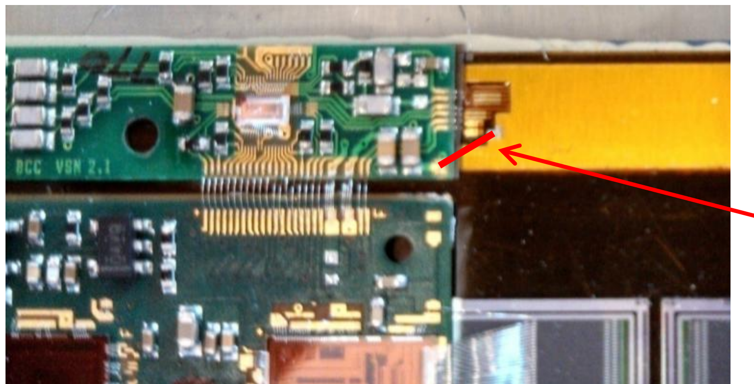
  - Titanium cooling tube: 2.2mm OD x 0.14mm wall
  - Tapes contribution are significantly reduced (~50%) by removing Al screen + one glue layer (overall 10% material reduction)
  - Sensor dominates module material (~ 63%) and overall stave material (~ 33%)
  - Power components will add 0.03 - 0.15 %X0, depending on power scheme (first approximation: changes in bus tape not considered)

Other details

- Low inductance GND reference links in between hybrids of the same module:
  - Shieldless tape, cannot use shield as low inductance reference in between hybrids
  - Metal referencing links on top of tape, BCC and power side independent of each other

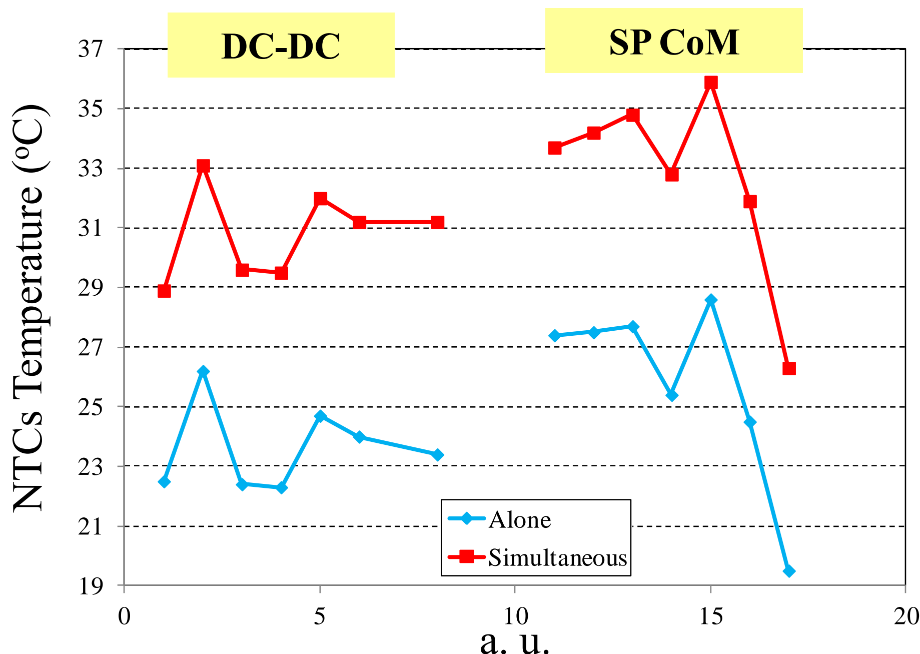


- CM removal capacitive links (100nF, 10 μF) between data shielding and BCC GNDs
  - Critical for SP CoM to obtain reasonable DTN results (learned from previous prototypes)

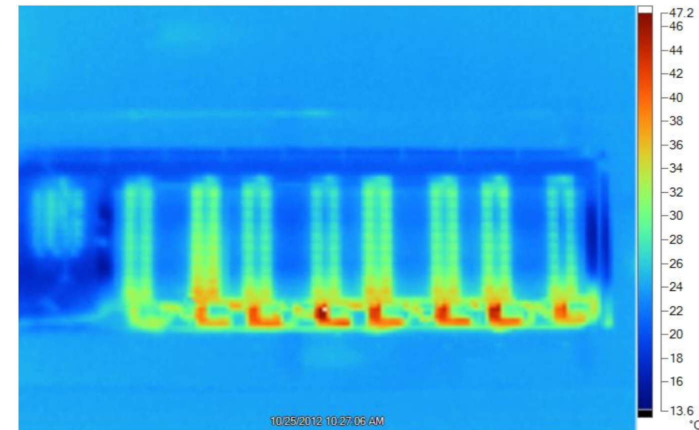


Results: Thermal performances

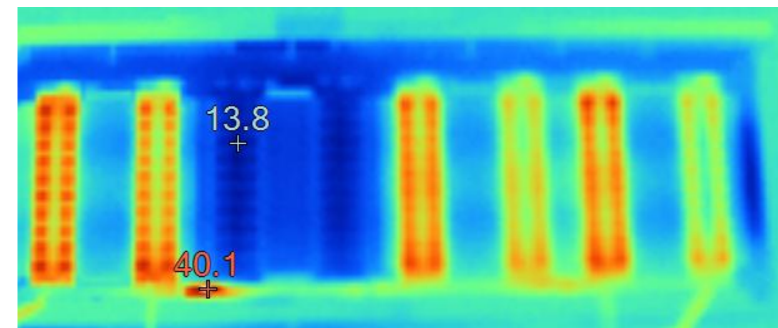
- > 200 Watts of dissipated power when both sides are running simultaneously
- Water cooling: chiller set at 3ºC, shielding box flooded with N_2 to avoid moisture
- Measurement of NTCs on hybrid and SHTs on cooling pipes
  - Highly dependent on glue thickness between hybrids and sensor
  - **7 ºC temperature increase when running both sides simultaneously**



DC-DC power



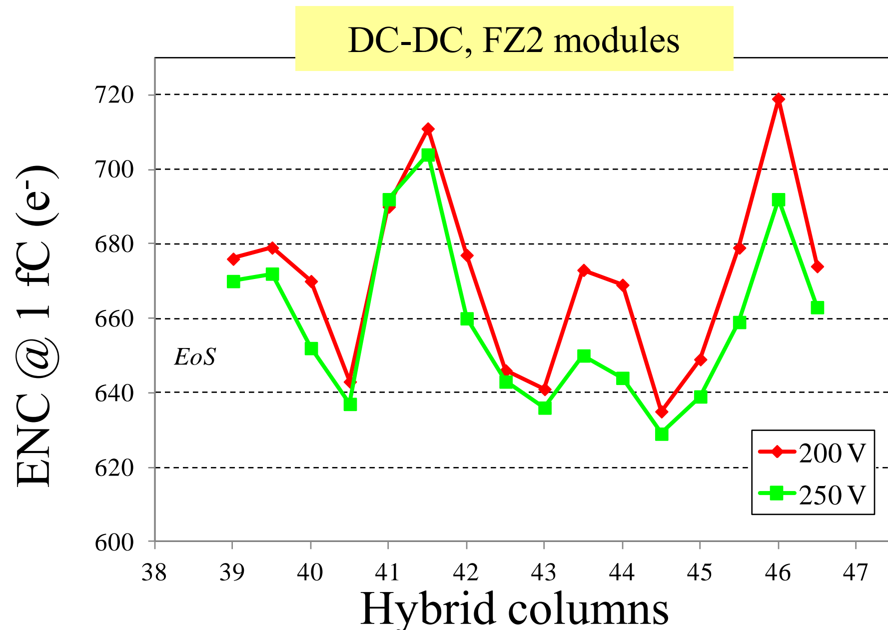
SP CoM with PPB2 slow control disabling M2

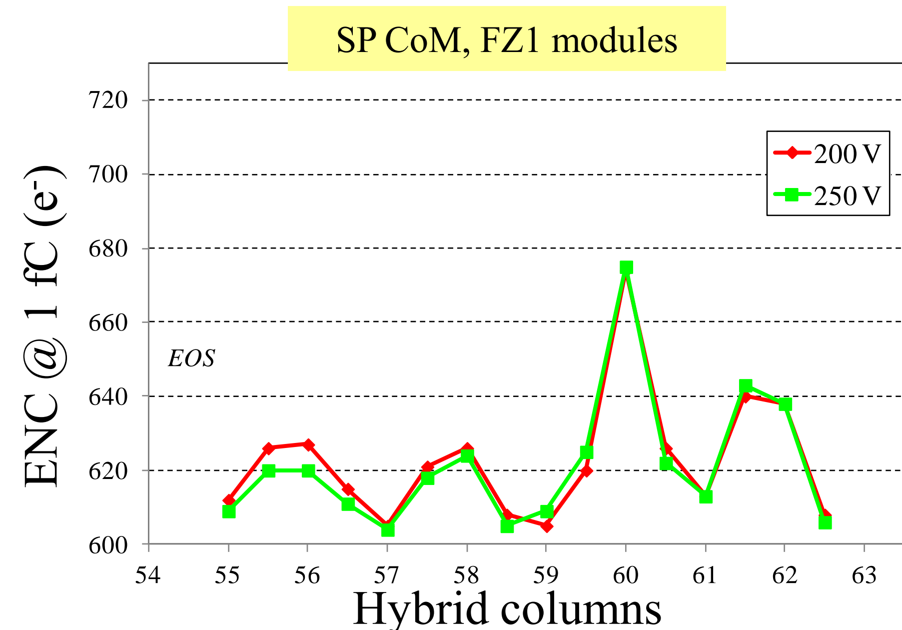


SHTs:
Each side alone: $T_{outlet} - T_{inlet}$ = **0.8 ºC**
Both sides simultaneous: $T_{outlet} - T_{inlet}$ = **5 ºC**

Results: ENC noise at 200 vs. 250 V

- DC-DC modules are Float-Zone 2 (FZ2) (grade B) sensors, I ~ 10-15 μA @ 200 V
- SP modules are FZ1 (grade A) modules, I < 0.5 μA @ 200 V
  - FZ2 modules showed improved noise results at 250 V in some cases at some module building sites
  - Test of each side independently at 200 and 250 V:





  - Significant differences (< 12e$^-$) for FZ2 modules, minimal (< 1e$^-$) for FZ1 modules
  - All results shown previously were obtained at 250 V in both sides
  - No (significant) further improvement for FZ2s at higher voltages