Scribe-Cleave-Passivate (SCP) Slim Edge Technology for Silicon Sensors

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with
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Acknowledgements:

1) Technical Guidance and Support by
Marc Christophersen*, Bernard F. Phlips*
(* Code 7654, U.S. Naval Research Laboratory

2) Our numerous collaborators from ATLAS and RD50
**Basic Idea:** To minimize ~1 mm wide inactive peripheral region. This is relevant for “tiling” (as opposed to “shingling”) of large-area detector composed of small sensors.

**Method:** To instrument the sidewall in a close proximity to active area, such that it’s resistive.
Conventional sensors have the bias voltage gradient in the guard rings region. To implement slim edges, we’d like to have the gradient on the sidewall => similar surface quality and passivation requirements.

Surface imperfections lead to additional current consumption => IV test as a measure of performance.
Method -- SCP Treatment

**Scribing**
- Diamond stylus
- Laser
- XeF₂ Etch
- DRIE Etch

**Cleaving**
- Tweezers (manual)
- Loomis Industries, LSD-100
- Dynatex, GTS-150

**Passivation**
- Native Oxide + Radiation
  - N-type
    - Native SiO₂ + UV light or high T
    - PECVD SiO₂
    - PECVD Si₃N₄
    - ALD “nanostack” of SiO₂ and Al₂O₃
  - P-type
    - ALD of Al₂O₃

All Treatment is post-processing & low-temp (Etch-scribing can be done during fabrication)

Basic requirement: 100 wafers (for rectangular side cleaving) with reasonably good alignment between sensor and lattice.
Examples with N-type Sensors

**XeF2 scribing + Nitride PECVD**

- Si SSD with 900\(\mu\)m dead edge
- Cut within 50 \(\mu\)m of Guard Ring
- Guard Ring Cut (!) 0 \(\mu\)m to Guard Ring
- Without guard ring

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Graphs showing current vs. bias with and without guard ring.

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Examples with P-type Sensors

Device A

14 µm

- diode edge
- cleaved edge

If you obtain
1. minimal damage at edge and
2. “right” sidewall surface charge
you don’t need guard ring(s)!

- slim edge
- no guard ring
- die level processing

Device B

- Si diode
- guard ring
- SiO₂

Processed device with alumina layer

Un-processed reference

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The initial trials started within the framework of ATLAS Planar Pixel Collaboration.

Last summer, the scribe-cleave-passivate (SCP) technology of fabricating slim edge sensors has been approved as RD50 project.

The participating institutions are interested in p- and n-type and 3D sensors.

We are currently actively working with CNM Barcelona, FBK Trento, MPI Muenchen, UNFN Bari, Ljubljana U., Glasgow U., and TU Dortmund on SCP application to their devices.

Note that the methods developed are rather generic, applicable to a wide variety of Si devices.
# RD50 Activity Matrix

<table>
<thead>
<tr>
<th>Institute</th>
<th>Contact Person</th>
<th>Sensors</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNM Barcelona</td>
<td>G. Pellegrini</td>
<td>3D diodes, strips, pixels</td>
<td>2nd round of tests (FEI3 and FEI4 pixel)</td>
</tr>
<tr>
<td>FBK Trento</td>
<td>G.-F. Dalla Betta</td>
<td>3D diodes, strips</td>
<td>2nd round of tests ongoing</td>
</tr>
<tr>
<td>MPI Muenchen</td>
<td>A. Macchiolo</td>
<td>P-type planar pixels</td>
<td>P-type strip devices sent; in progress</td>
</tr>
<tr>
<td>UNFN Bari</td>
<td>D. Creanza</td>
<td>N-type “SMART” detectors</td>
<td>First processed devices sent for evaluation; in progress</td>
</tr>
<tr>
<td>Ljubljana U.</td>
<td>G. Kramberger</td>
<td>P- and N- type</td>
<td>Devices sent; used in laser TCT studies of the field profile</td>
</tr>
<tr>
<td>Glasgow U.</td>
<td>R. Bates</td>
<td>P- and N- type</td>
<td>Sensors with SCP used in a precision X-ray scan of charge collection efficiency</td>
</tr>
<tr>
<td>TU Dortmund</td>
<td>T. Wittig</td>
<td>IBL-style n-on-n sensors</td>
<td>Initial tests done, Iterations with IBL sensors</td>
</tr>
<tr>
<td>Vilnius U.</td>
<td>J. Vaitkus</td>
<td>P- and N-type for passivation quality studies.</td>
<td>P- and N-type diodes sent; irradiated p-type strip devices to be sent.</td>
</tr>
</tbody>
</table>

**Ongoing Activities within RD50 Collaboration**

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Current Efforts

We had a lot of technical development, with different fabrication options explored. For details, see recent publications:

- M. Christophersen et al., "Alumina and Silicon Oxide/Nitride Sidewall Passivation for P- and N-Type Sensors", NIM A 699 (2013) 14

Recent work is focused on:

- **Technical development:**
  - Wafer-level processing
- **Device performance:**
  - CCE near the edge
  - Radiation hardness
Wafer-based Processing

A lot of processing steps are easily amenable to automation due to processing technology/machines. A key manual step we used so far is cleaving. It was done manually, with 2 tweezers. In parallel with making and evaluating test samples, we explored machine-based cleaving options for mass-production.
Wafer-based Processing

The latest tests with Dynatex machine are extremely promising:

a) 9-cm long narrow section is removed intact (it broke when being peeled off the blue tape). The removed piece is 680 um wide and 400 um thick!

b) 1.6 x 3.5 cm$^2$ sensor cleaved on 4 sides.

Cut-off from Glast/Fermi production.
Alternative Wafer Processing

Based on our studies, wafer cleaving provides the best performance due to low defect density on the sidewall. Nonetheless, a process modification is possible:

instead of Scribe-Cleave-Passivate,
one can do Cut-DamageRemoval-Passivate.

The cut here can be either laser through-cut or conventional saw cut. This might insure reliability of the singulation process, at the price of possibly higher currents. An option for difficult cases, e.g. with wrong lattice orientation.

Post-processed by G. Pellegrini et al.
<table>
<thead>
<tr>
<th>Sensor Type</th>
<th>Origin</th>
<th>Edge-Active area Distance [um]</th>
<th>Signal Readout</th>
<th>Beam</th>
<th>Ref</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-type strips</td>
<td>PPS (CIS)</td>
<td>~200</td>
<td>Binary (PTSM)</td>
<td>$^{90}$Sr</td>
<td>V. Fadeyev et al, Pixel 2012, NIM A in press</td>
</tr>
<tr>
<td>N-type strips</td>
<td>GLAST (HPK)</td>
<td>~200</td>
<td>Analog (ALiBaVa)</td>
<td>$^{90}$Sr</td>
<td>R. Mori et al. 2012 JINST 7 P05002</td>
</tr>
<tr>
<td>P-type strips</td>
<td>PPS (CIS)</td>
<td>150</td>
<td>Analog (ALiBaVa)</td>
<td>Focused X-ray</td>
<td>R. Bates et al., 2013 JINST 8 P01018</td>
</tr>
<tr>
<td>P-type 3D pixels</td>
<td>IBL (CNM)</td>
<td>50</td>
<td>FE-I3 &amp; FE-I4</td>
<td>CERN Test Beam</td>
<td>S. Grinstein et al., RESMDD12 G. Pellegrini et al., Pixel 2012, NIM A in press</td>
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</table>

In all cases CCE on the edge was within few % of CCE on other electrodes

⇒ Caveat: all un-irradiated devices.

New developments:
  o MPI study has device irradiation in progress.
  o Glasgow (R. Bates et al) are planning a follow up with irradiated devices.
P-type HPK (ATLAS07)
These sensors did not work after cleaving (initial trial without sidewall passivation). Breakdown at ~few Volts. There is an empirical evidence that the breakdown improves after irradiation.
We put these sensors in proton beam to see if they would indeed improve.
Leakage is initially dominated by the edge current, which is reduced with fluence. At $10^{14}$ neq, $I_{\text{edge}} < I_{\text{bulk}}$.

Comparison of expected and observed currents at 200 V

Observation on “SC only” P-type:
High fluence irradiation -> resistive edge!
N-type GLAST HPK Photo Diodes with SCP edge both nitrite and oxide passivation

Observations on N-type:
Low fluence (1e13, < inversion) edge isolation due to passivation (Nitrite/nanostack)
High fluence (>1e14, > inversion): resistive edge
…No dependence on type of passivation, leakage current close to bulk expectation

Expected current [uA] @ -5 C

- 13.3
- 1.33
- 0.16

Pre-rad
Irradiated 12 SCP processed p-type strip devices (CIS courtesy A. Macchiolo) at LANL (thanks S. Seidel). Results are inconclusive:

+ Breakdown voltages extended post-rad
+ High fluence devices (3/3 for $1e16 neq$, 3/3 for $1e15 neq$) show expected post-rad leakage current
- Lower fluence devices (1/3 for $1e13 neq$ and 1/3 for $1e14 neq$) show earlier breakdown!

A parallel investigation of the robustness of the passivation layer revealed a possible susceptibility to rough handling. There is no proof that this has skewed the irradiation results.

... was followed up at CERN irradiation run in 2012 with protons. Results were similar, indicating either continuous packaging issues, or a real problem at low fluences.
Observation on SCP P-type with neutrons:
3D neutron-irradiate sensors show approximate scaling with fluences:
no high currents for low fluences!
=> See vastly different fluence scaling. Either due to field geometry or non-ionizing dose.

3D Trento diodes scaled according to volume and measurement temperature
We are pursuing a method of making devices with reduced peripheral material ("slim edges"). This is an alternative to making "active edge" sensors, which typically requires very specialized processing.

A lot of fabrication aspects are figured out. Currently focusing technical developments on wafer-level processing.

The method rose a lot of interest in the community. We are collaborating with many RD50 groups on further development and application to their particular sensor designs.

Sensor sensitivity near the edge:
- Had multiple studies of CCE near the edge on un-irradiated sensors. So far no issues.
- Will be interesting to see results from irradiated devices: MPI and U. of Glasgow studies.

Radiation hardness of the passivation:
- N-type devices seem to be rad-hard. This is expected, since the properties of the sidewall after irradiation should be similar to the case of top surface on conventional sensors. (Same passivation, similar surface properties.)
- There appears to be an issue with rad hardness on p-type devices for fluences <10^{14} neq/cm^{2}.
- This has to be related to properties of dielectric (alumina) after irradiation. There is a project, lead by G. Pellegrini (CNM) to fabricate MOS-like structures with alumina to find more details about it.
- Studies of neutron-irradiated p-type 3D sensors are in progress. Preliminary data indicate no issues. This is either due to different field geometry or non-ionizing dose.
Back-Up Slides
Passivation Options

<table>
<thead>
<tr>
<th>N-type Si</th>
<th>P-type Si</th>
</tr>
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<tbody>
<tr>
<td>+ Si O2</td>
<td>– Al2 O3</td>
</tr>
<tr>
<td>or Si3 N4</td>
<td>– ALD deposition</td>
</tr>
<tr>
<td>+ PECVD deposition</td>
<td>–</td>
</tr>
<tr>
<td>or oxide growth</td>
<td>–</td>
</tr>
</tbody>
</table>

Surface passivation makes the sidewall resistive. N- and p-type devices require different technologies.

- For n-type devices one needs a passivation with *positive* interface charge. SiO$_2$ and Si$_3$N$_4$ layers works well.
- For p-type material a passivation with negative interface charge is necessary. We found that Al$_2$O$_3$ works in this case.
This is an optional step for the SCP process. A gaseous Xenon Difluoride (XeF₂) etch step can remove scribing damage: needed for Laser and diamond scribe).
Scribing Technologies: Diamond-, Laser-, and Etch-based

Diamond scribing

Laser scribing

Issues:

- Diamond scribing: surface chipping of existing passivation (=> to do again in future runs)
- Laser scribing: some degree of damage due to affected region of the sidewall
- XeF2 etching: cleaving by industrial machines is difficult

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Scribing Technologies: DRIE

DRIE-based trenching as scribing has a promised of being a “universal” production solution without shortcomings of the other methods.
Effect of Surface Termination – P-Type Si

• After all the handling, we need to remove a native oxide. That is done w/ HF and leads to the “H-termination”, which can’t be passivated with alumina $\text{Al}_2\text{O}_3$.
• Need to covert the H-termination into F-termination which in combination with alumina ALD should work. Know they chemistry!
• The hunt for an ideal surface termination for p-type Si is still on.
Progress with Passivation (N-type Diodes)

PECVD process has been developed by industry as a wafer process => Small height of the chamber in a typical machine.
This worked well for small size samples, that could be positioned vertically, or slanted. For large sensors this is not quite applicable => replace by ALD method.

Study with HPK Fermi/GLAST diodes.
The plain ALD SiO2 is worse than the best case of PECVD Si3N4. But a “nanostack” of ALD SiO2 (10 nm) and Al2O3 (50 nm) works well. Parameters are from G. Dingemans et al, J. Appl. Phys. 110, 093715 (2011); doi: 10.1063/1.3658246

Consistently low I and high B(break). Quite similar to the best case of PECVD nitride!
3. 2012 Proton Irradiation @CERN

A round of irradiations at SPS (huge help from G. Casse & M. Glaser):
- p-type diodes from ATLAS07 Test Structures
- n-type diodes from Fermi/GLAST Test Structures, with both PECVD nitride and ALD oxide
p-type ATLAS07 HPK Photo Diodes

Observation #4 on S-C-P p-type:
Leakage currents do not scale with fluence
low fluence (< 1e14): reduced edge performance
high fluence (>1e14): resistive edge
Progress with Passivation (N-type Diodes)

Performance dependence on the deposition temperature:
Can work in the T range that is safe for the finished devices!

Much improved leakage current and breakdown voltage with Si Nitride.