Nalu Scientific
Data Acquisition Systems

Nalu Scientific: Advanced Micro Electronics for Particle Physics

Isar Mostafanezhad, Ph.D.

Founder and CEO, Nalu Scientific, LLC

July 9, 2019, isar@naluscientific.com

Supported by DE-SC0019531, SC0019527, SC0015231, SC0017833

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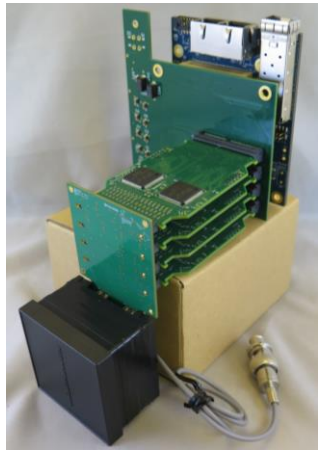
Waveform Digitizer SoCs for Single Photon Time of Flight Detection: Compact, Low Cost, Low Power

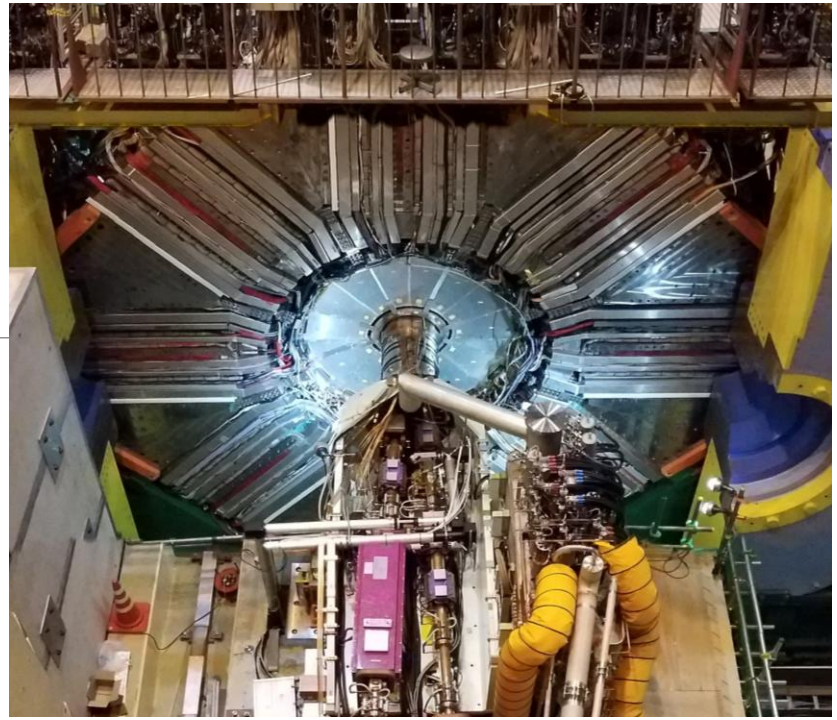
1. Various Front-end Chips:

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP
- Low cost
- User friendly



2. Integration:

- SiPM
- PMT
- LAPPD
- Antenna arrays



3a. Main application: Particle collider experiments (Belle II at KEK in Japan)

3b. Other applications:

- Beam diagnostics
- Plasma/Fusion diagnostics
- Lidar
- Medical imaging

About Nalu Scientific

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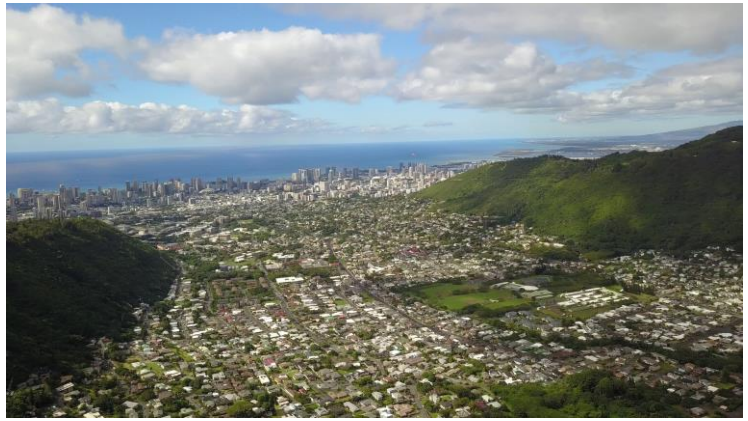

Integrated Circuits Design
- Analog + digital System-on-Chip (SoC)
- Digital implementation

Hardware Design
- Field Programmable Gate Arrays (FPGA)
- Complex multi-layer Printed Circuit Board (PCBs)

Expertise in:
- Time of Flight (ToF) measurements
- Fast timing
- Radiation detection
- Readout electronics for Particle Physics

Team

Isar M.
Founder and CEO
UH PhD EE
3x Entrepreneur

Luca M.
Senior Engineer
PhD EE, 20+ yrs
IC Design Lead

Dean U.
Senior Engineer
30+ yrs experience
Digital IC Design

Ryan P.
Senior RF Engineer
10+ yrs experience
High Frequency Design

Ben R.
Staff Physicist
PhD Phys
Particle Physics Guru

Chris C.
Design Engineer
BS CE
Agile R&D

Angela A.
Office Manager
Admin Guru

Marcus L.
SW/PM

Kenneth L.
EE

+ 3 Postdocs and 3 PhD candidates at University of Hawaii

Advisors

Kevin H.
Strategic Business

Jeremy F.
IP & Legal

Shawn U.
Gov. Relations

Rozi R.
Technology Analysis

Craig O.
Vertical Market Analysis

Prof. Gary V.
UH Subcontract

Ryan O.
Media Consultant

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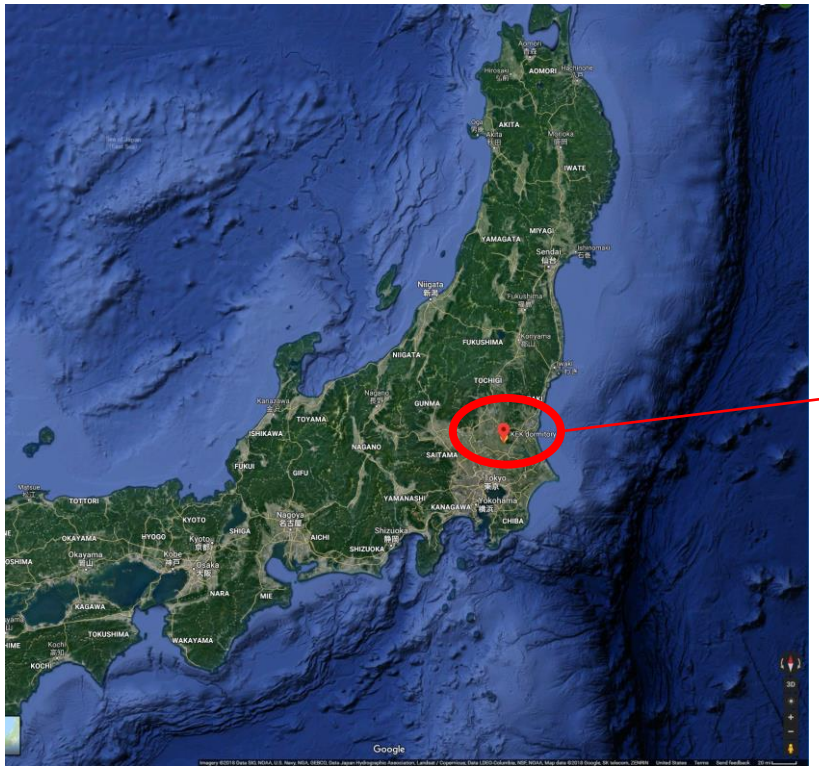
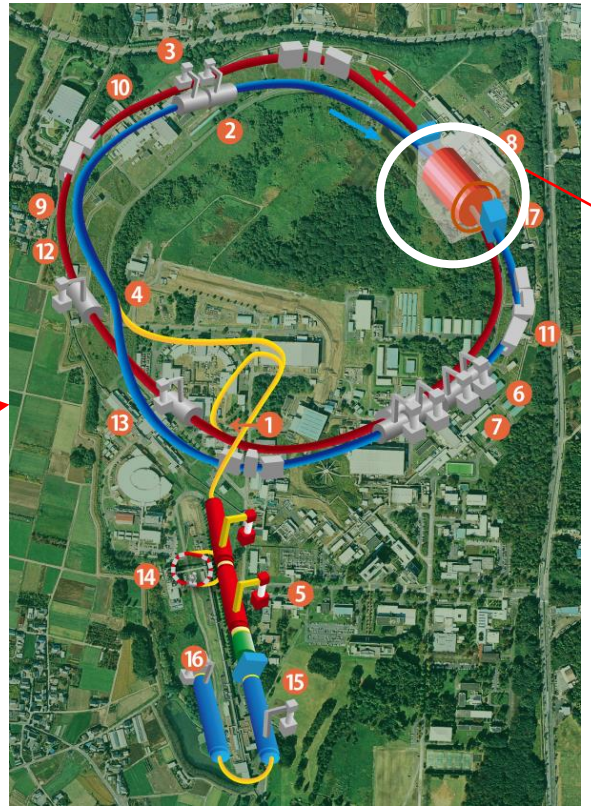
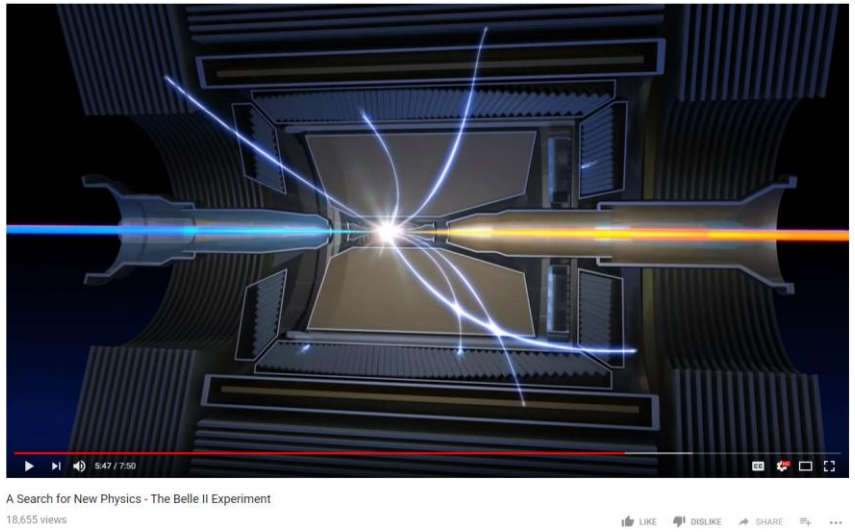
Where did we start?
A Search for New Physics – The Belle II Experiment



Tsubuka City
Located 60 mi north of Tokyo



High Energy Accelerator Research Facility (KEK) in Tsukuba



Interaction point inside the electron/positron collider

Some History:

Belle II Upgrade is a 26 Country, 900+ member Collaboration

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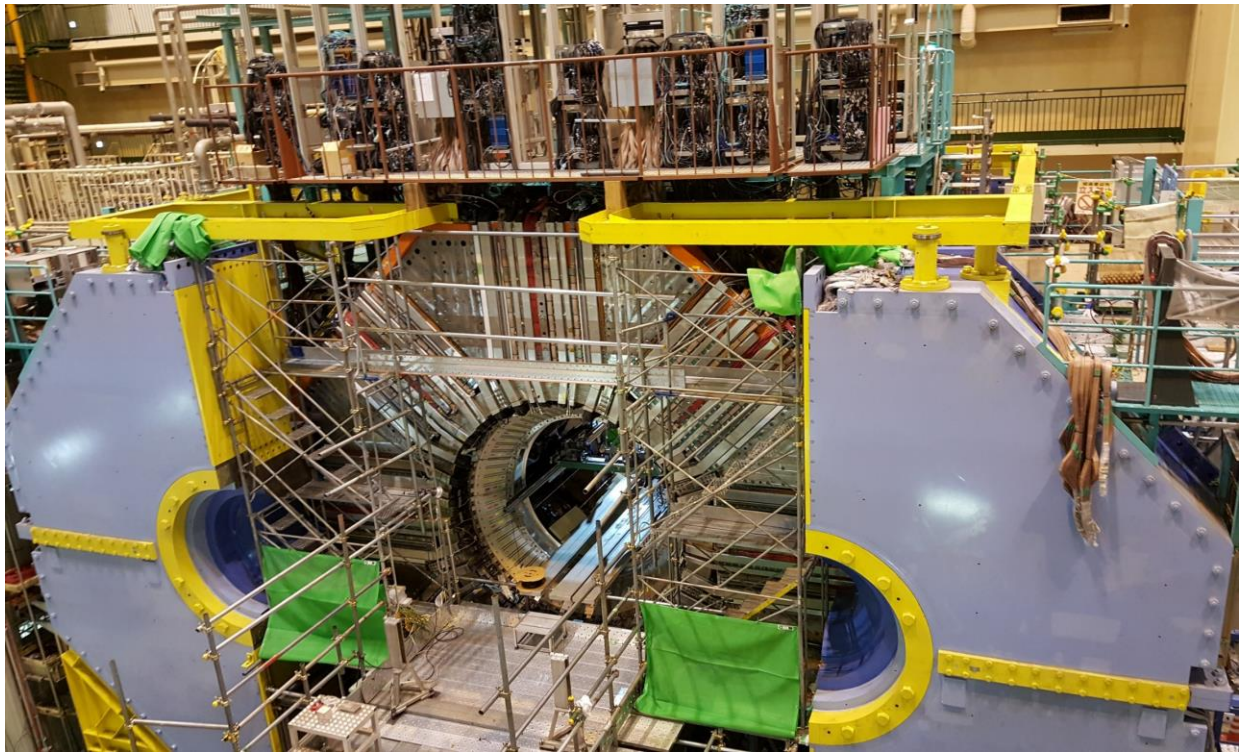
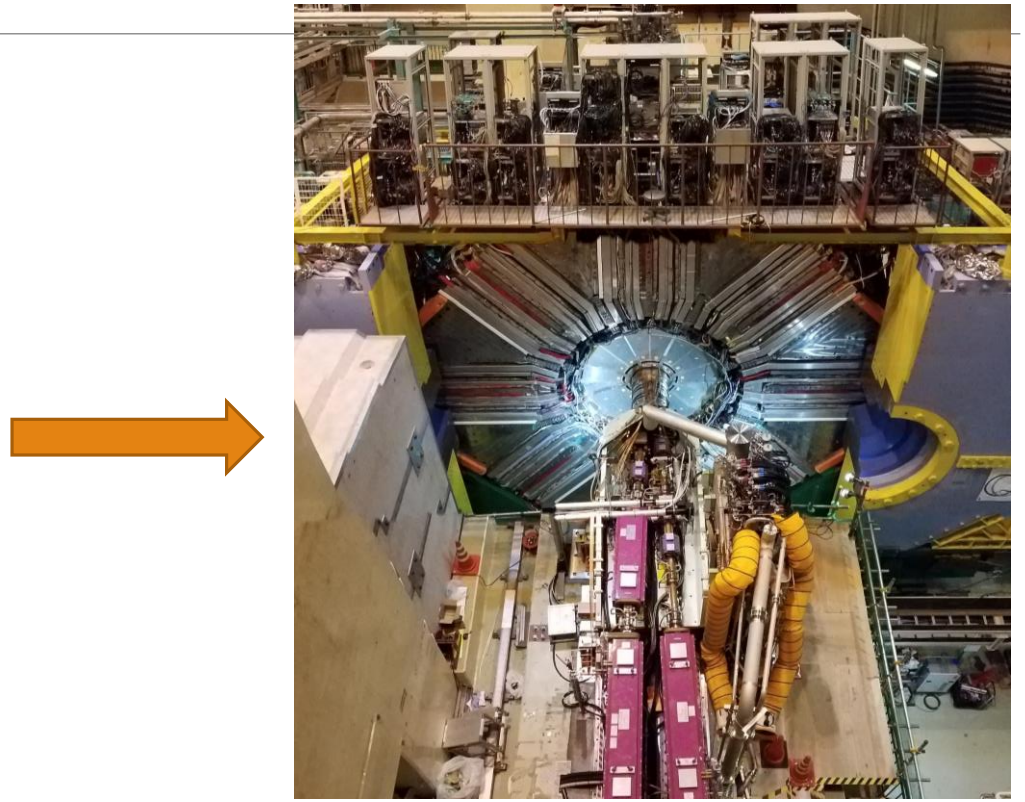
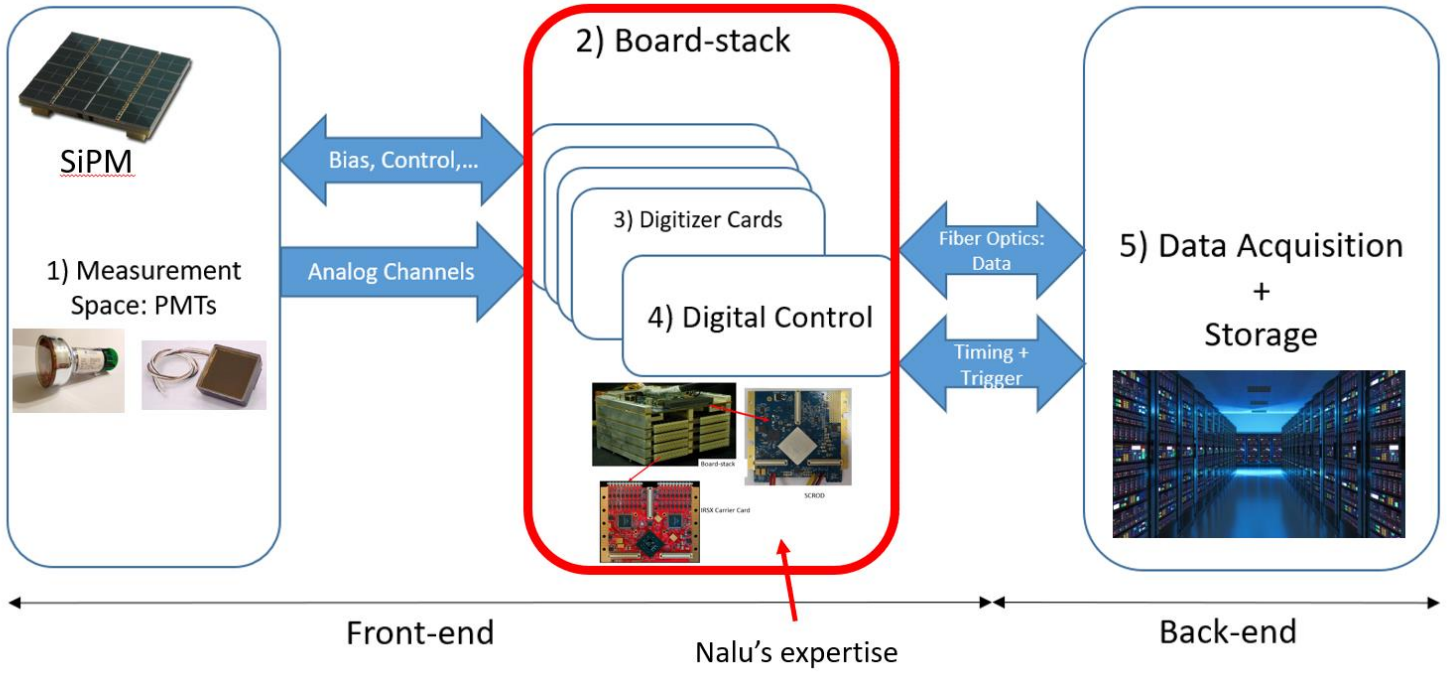




2015 **2018**

Belle II: e+ e- experiment at 40x luminosity of Belle -> Detector needs to operate at severe beam background

Lesson 1:
How does a Particle Physics Experiment Work?



Lesson 2:
Opportunities

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Next gen Particle Physics electronics need to be:

- Radiation hard
- High performance
- Low cost, low power
- And **user friendly**

Solution: New System-on-Chip Integrated Circuit Design

Opportunity: Not many commercial options available

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Benefits of Higher Integration - SoC

- **Analog memory:**
  - Sampling always on (1-10 Gsa/s), but at low power
  - Digitize only Region of Interest (ROI)
  - Long analog buffer -> suitable for large experiments
- **Digital processing:**
  - Per channel cost reduction by a factor of 4
  - Relax thermal design by 40% reduction in power dissipation
  - Trigger time-stamping at the front-end
  - Eliminating the need for costly high-end FPGAs
  - User friendly: substantially reducing the FPGA firmware development labor
  - Reduced complexity and design and cabling effort/cost for the front-end boards

Analog/Mixed signal design

+

Digital/Synthesized logic

=

System-on-Chip (SoC)

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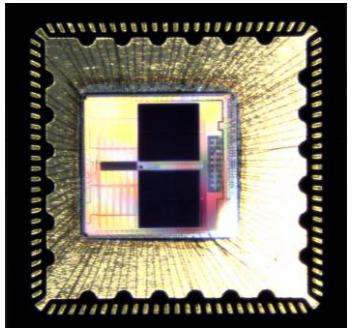
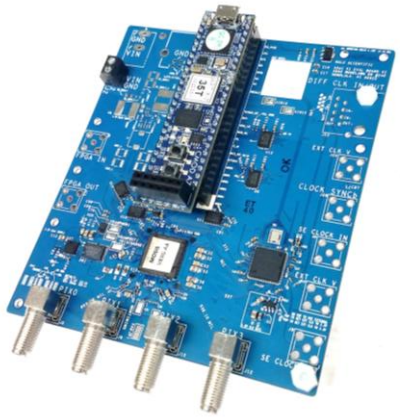
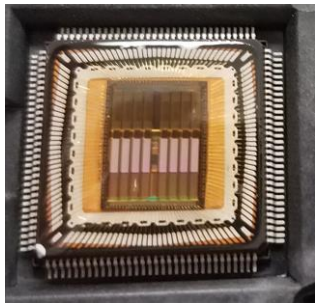
Funded SBIR Programs

- **Various event based digitizers (US DOE):**
  - ASoC: High speed event based digitizer (4GSa/s, 80mW/ch, 4 channels)
    - Phase I, II SBIR: Feb 2016-Nov 2019, Grant: DE-SC0015231
  - AARDVARC: High speed event based digitizer (14GSa/s, 80mW/ch, 4 channels)
    - Phase I, II SBIR: May 2017-Aug 2020, Grant: DE-SC0017833
  - SiREAD: High channel count digitizer (1GSa/s, 32 channels, 20mW/ch)
    - Phase I: Feb 2017-Nov 2017
  - AODS: Very compact digitizer with high dynamic range
    - Phase I: Feb 2019-Nov 2019, Grant: DE-SC0019531





- **Advanced Fast Diagnostics Tools (US DOE):**
  - **TR-BHM: Time Resolved Beam Halo Monitor for accelerator beam diagnostics**
    - Phase I: Feb 2019- Nov 2019, Grant: DE - SC0019527
  - **UPAC: Ultrafast Pixel Array Camera for fusion energy plasma diagnostics**
    - Phase I: July 2019- June 2020, Grant: DE-SC0019790



- **Lidar (NASA)**
  - SWELL: Single-photon-sensitive Waveform Enhanced and Lightweight Lidar
    - Phase I: July 2019- Dec 2019 (tentative – award pending contract negotiation)

Nalu Scientific SBIR Project: ASoC

Compact, high performance waveform digitizer

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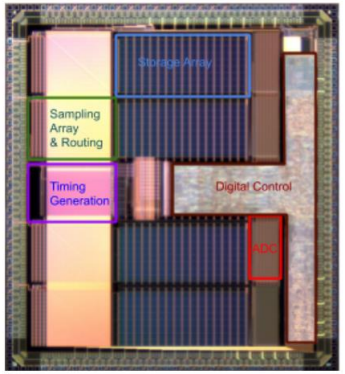
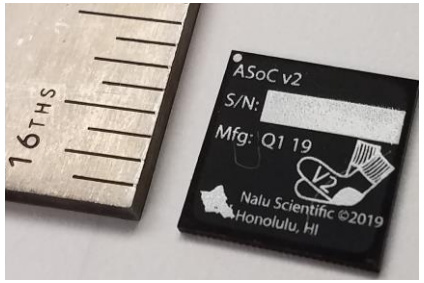


Fabricated

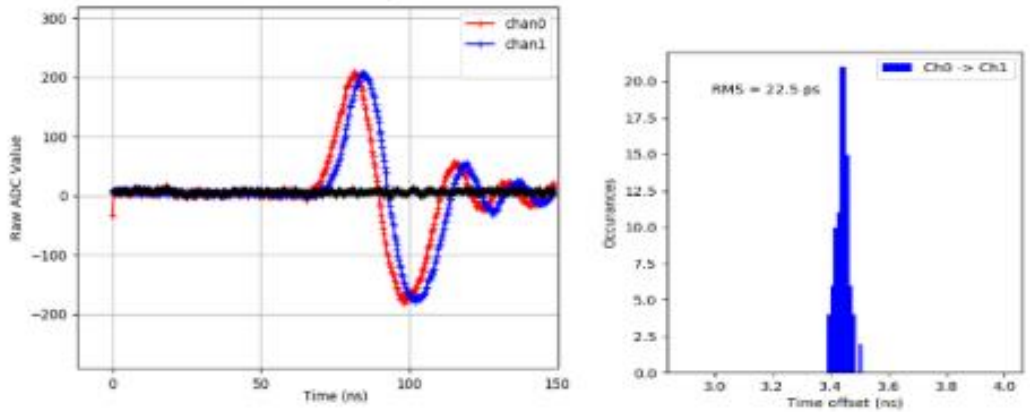


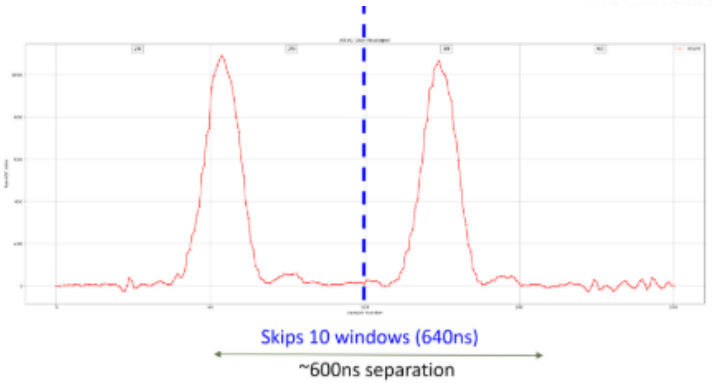
Parameter	Spec (measured)
Sample rate	2.4-3.2GSa/s
Number of Channels	4
Sampling Depth	16kSa/channel
Signal Range	0-2.5V
Resolution	12 bits*
Supply Voltage	2.5V
RMS noise	~1 mV
Digital Clock frequency	25MHz
Timing resolution	<25ps**
Power	140mW/channel
Analog Bandwidth	950MHz

Key Contribution:

- High performance digitizer: 3+ Gsa/s
- Highly integrated
- Commercially available
- 5mm x 5mm die size

Live demo at IEEE NSS-MIC 2018





All chips, are designed with commercial grade tools and licenses and can be sold once commercialized.

AARDVARC V2 under test

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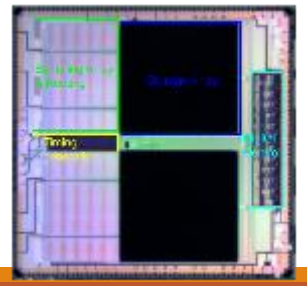
- AARDVARC V2 fabricated and packaged
- Test board V2 designed, fabricated and assembled
- Lower cost FPGA dev card identified and purchased (x5)
- Test firmware V2 developed
- New software and GUI designed and implemented

AARDVARC Parameter	Specification (measured)
Process node	130 nm
Channels	4
Sampling Rate	10-14.5GSa/s*
Storage Samples/ch	32768
Analog BW	>1GHz**
Dynamic Range	1.0 V**
Time accuracy	<5 ps***
Readout	Parallel/Fast Serial
ADC bits	12
Power/ch	80 mW*



AARDVARC Test card

Xilinx A7 FPGA dev card

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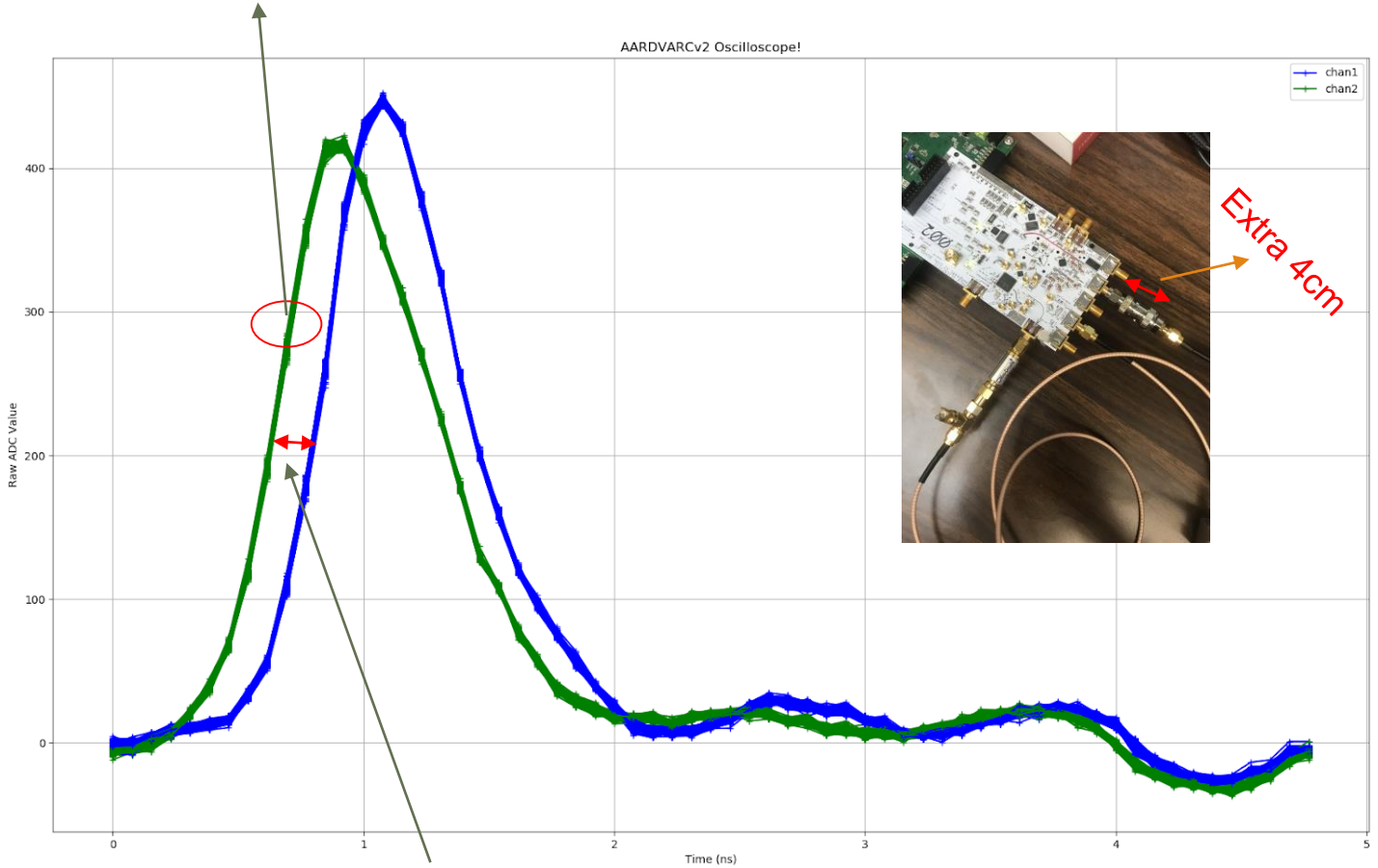
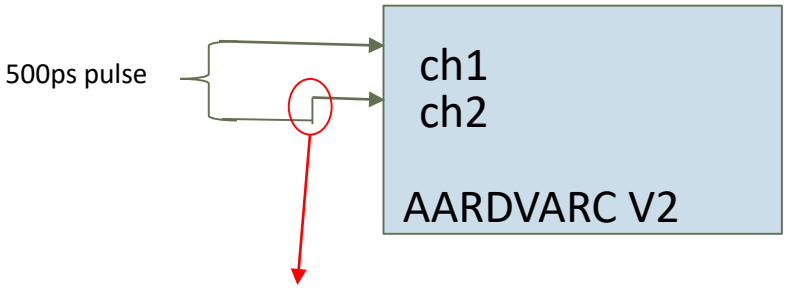
Overlayed 250 events showing very small timing jitter



Two pulses in two channels in 250 events

Pulses created by shunting Si5341 square wave output

Difference in timing created by adding a right angle connector to cable



Delay caused by an extra SMA connector ~ 140ps (1-2 Samples at 13 GSa/s)
Jitter measured at ~1-2ps
More results to be shown in conferences in the next 2-3 months

Note: the pulse gen is synced with ASIC sampling clock.

Synergies: LAPPD

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In June 2019 we measured LAPPD pulses using ASoC and AARDVARC chips. We are still analyzing the data.

SiREAD Electronics Evaluation

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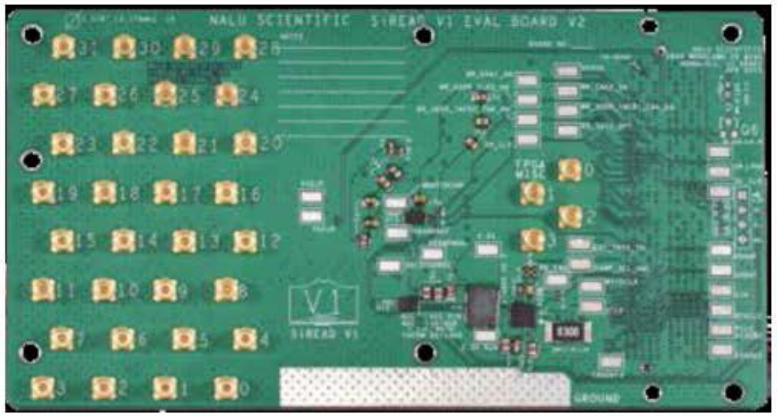
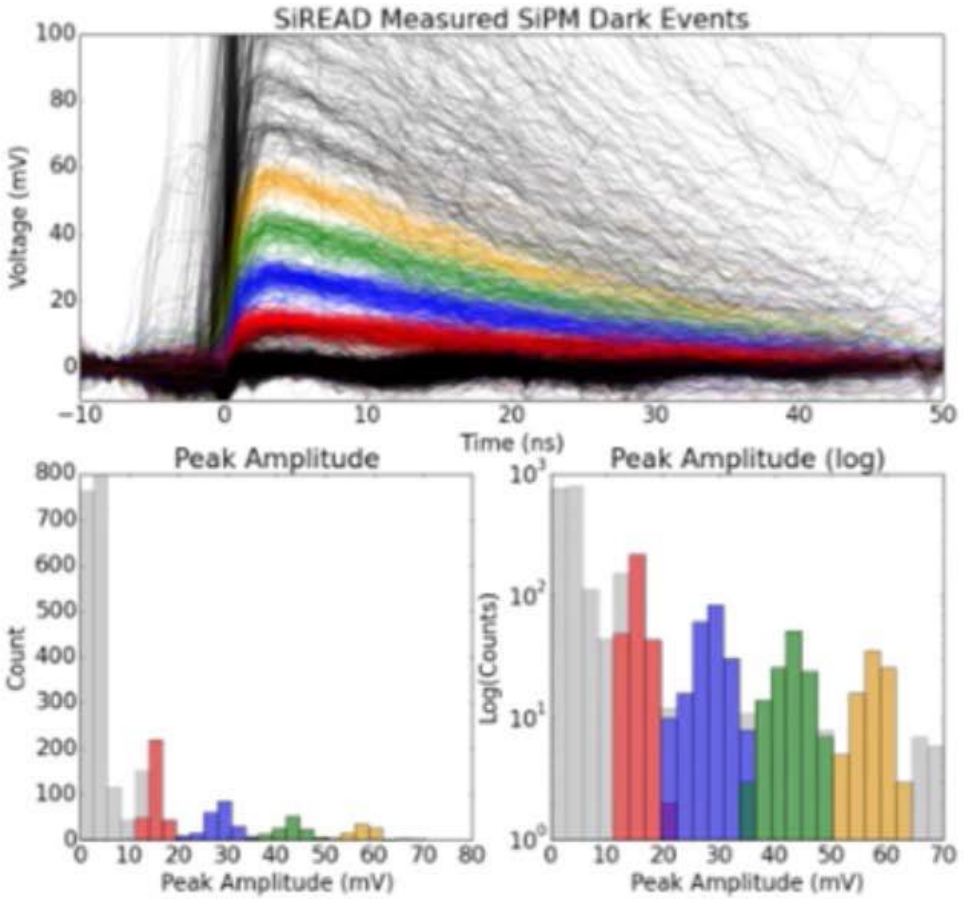
Micrograph of the fabricated prototype SiREAD and chip on the evaluation PCB

High channel count evaluation PCB for SiREAD with 32 dedicated MMCX connectors





Superimposed dark count waveforms recorded from a SiPM using the SiREAD operating at 1 Gsa/s

MaPMT Readout

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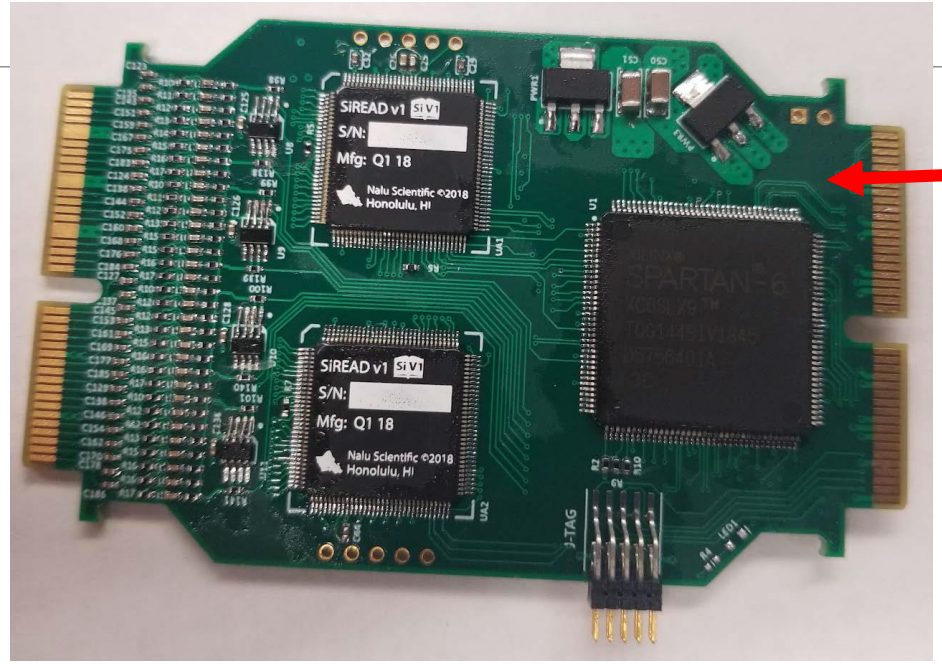
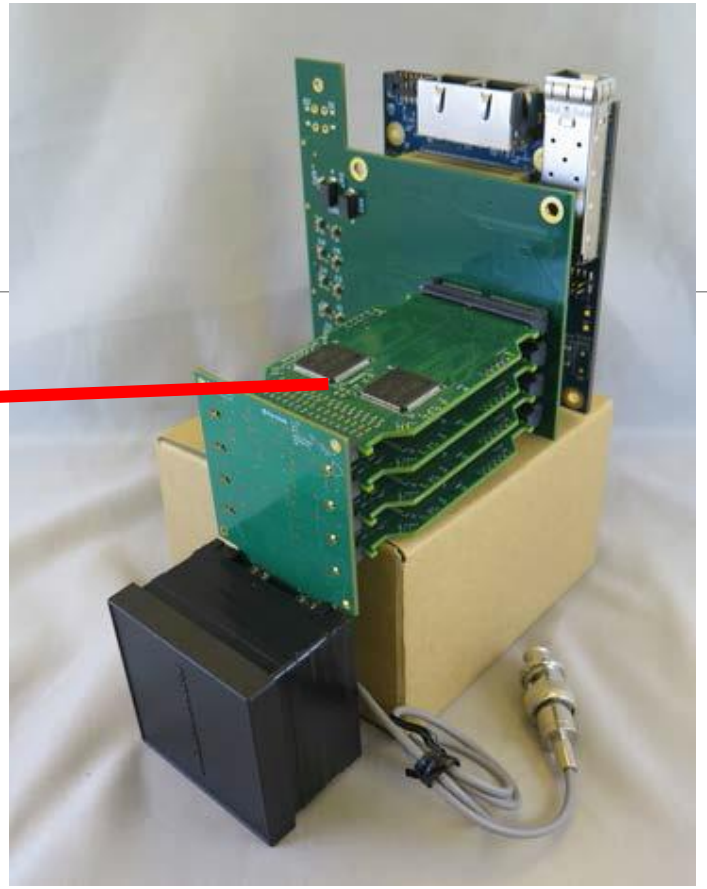
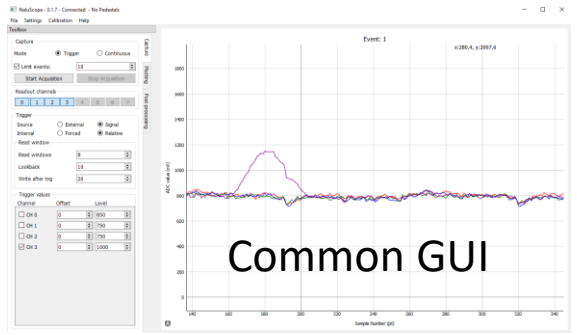


Photograph of the 64 channel SiREAD based (2x SiREAD rev.1) readout card as a building block for the 256 MA-PMT readout.



Photograph of the first generation of 256-anode 2" PMT readout for use with mRICH prototype in the Fermilab beam test facility.



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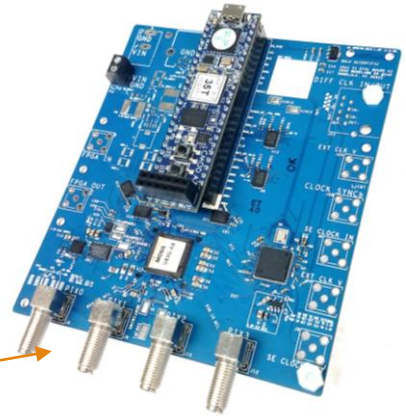
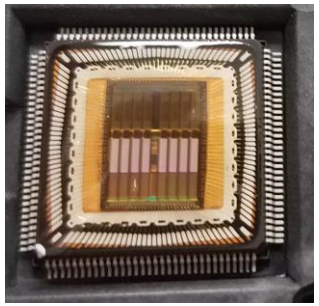
Current SoC-ASIC Projects

Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	32k	8	35	Rev 2 avail
SiREAD	1-3	0.6	4k	64	80-120	Rev 1 avail
AARDVARC	6-10	2.5	32k	4-8	4-8	Rev 2 avail
AOD	1-2	1	8k	1-4	100-200	Nov 2019



- **ASoC**: Analog to digital converter System-on-Chip
- **SiREAD**: SiPM specialized readout chip with bias and control
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
- **AODS:** Low density digitizer with High Dynamic Range (HDR) option



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Acknowledgements

US Department of Energy

Hawaii Technology Development Corporation (HTDC)

University of Hawaii Department of Physics

Incom, Inc.

Funding and Collaboration

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FY16-20

- ✓ **$3.7M Secured by Nalu**
  - ✓ 7x SBIR Phase I
  - ✓ 2x SBIR Phase II
  - ✓ Various matching grants
  - ✓ Misc. contracts

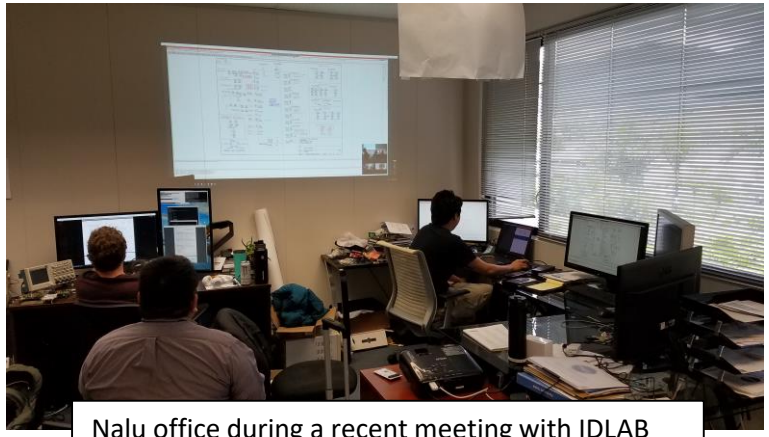
FY16-20

- ✓ **$425k Sponsored Research**
  - ✓ University of Hawaii
  - ✓ 4x post docs
  - ✓ 4x graduate students
  - ✓ Misc. materials and supplies

1x MS and 2x PhDs had their first jobs at Nalu Scientific.

FY19-20

- ✓ **New possibilities:**
  - ✓ New tech-dev based on UH capabilities
  - ✓ Local testing at UH
  - ✓ Workforce development
  - ✓ Hiring more UH grads
  - ✓ US-JAPAN Collaboration



Nalu office during a recent meeting with IDLAB

Why Hawaii?

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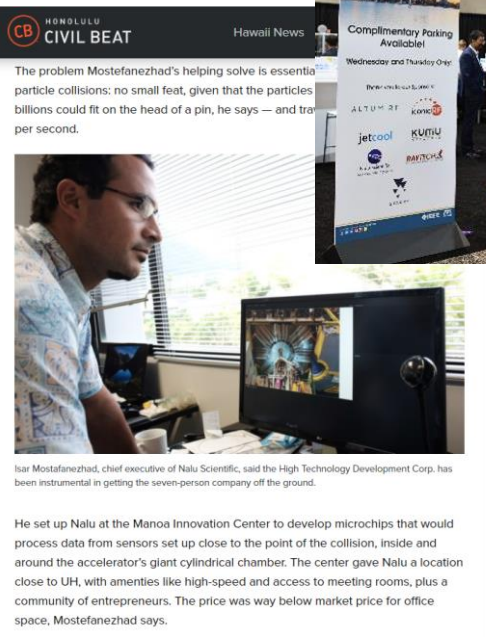
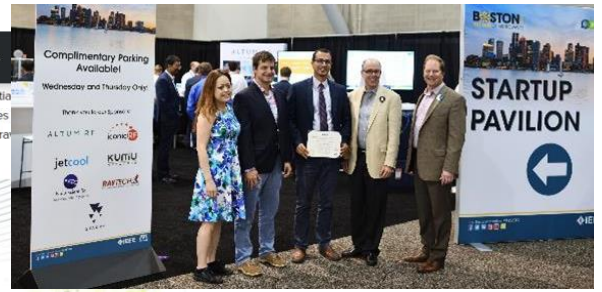
Strategic location!
- Continental US
- Asia

University of Hawaii
- Collaboration
- Workforce
- Facilities
- World class faculty

Greater impact on State
- Economical (high paying jobs)
- Technological
- “Hawaii Brand”
- Reverse the brain drain
- Lots of resources available


APS meeting on Big Island Oct 2018





Startup Pavilion at IMS2019

Good Media Coverage

In the news and events

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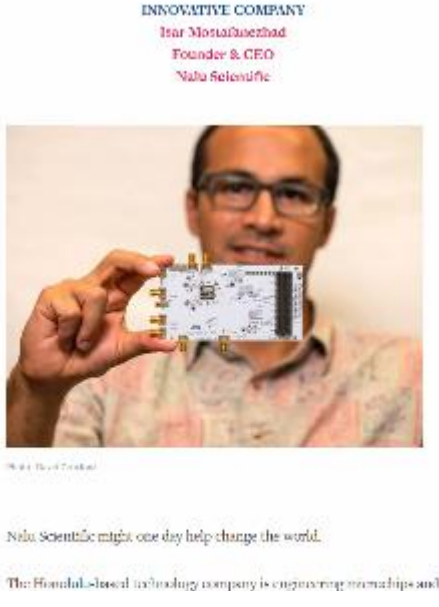
Booth and AARDVARC Live demo at US-Japan Particle Physics Symposium in Honolulu (April 2019)

Pacific Biz News 40 under 40

Next Top Startup Pitch Competition
Runner up - IMS2019 - Boston



Hawaii Biz Magazine
Most Innovative Small Biz of the year

IEEE Young Professionals Panel
IMS2019 - Boston

IPAC 2019 booth- Melbourne

Hawaii Congressman Ed Case visit