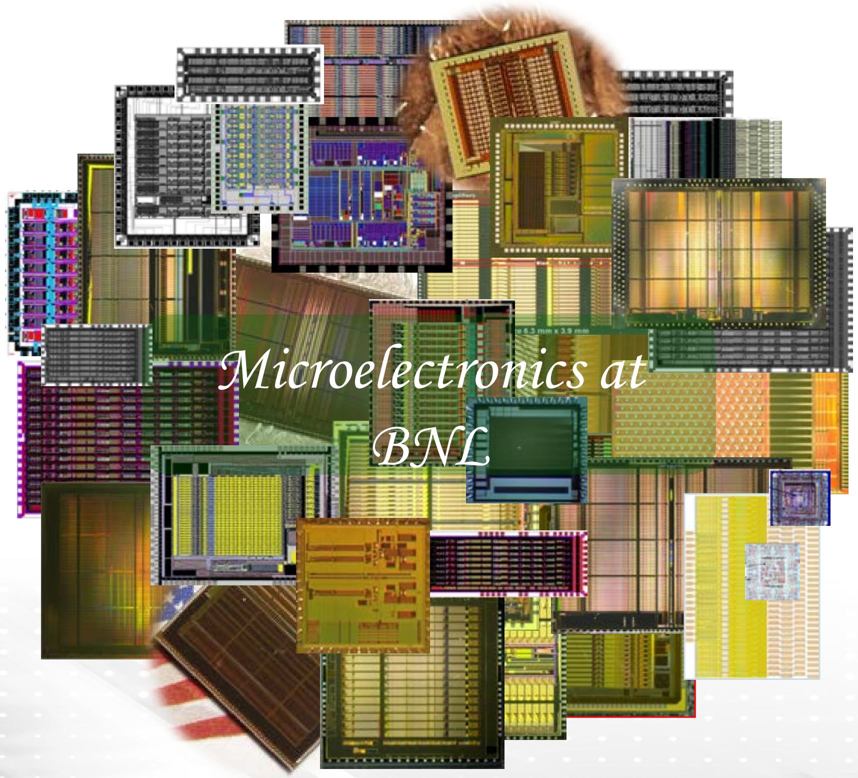
BNL ASICs: Waveform Sampling, and Charge Processing

Shaorui Li

Microelectronics at BNL

- Since early '90, microelectronics at BNL successfully developed **over 50 state-of-the-art ASICs** with a wide range of impact and is especially renowned on:
  - **Low-noise low-power** front-end optimized for ***high charge-, spatial-, and timing-resolutions;***
  - **Cold electronics** (enabling HEP large-scale cryogenic detectors);
  - **High functionality ASICs** (> 100,000 transistors per channel including analog front-end, mixed-signal ADCs, and digital processing for ATLAS upgrade).

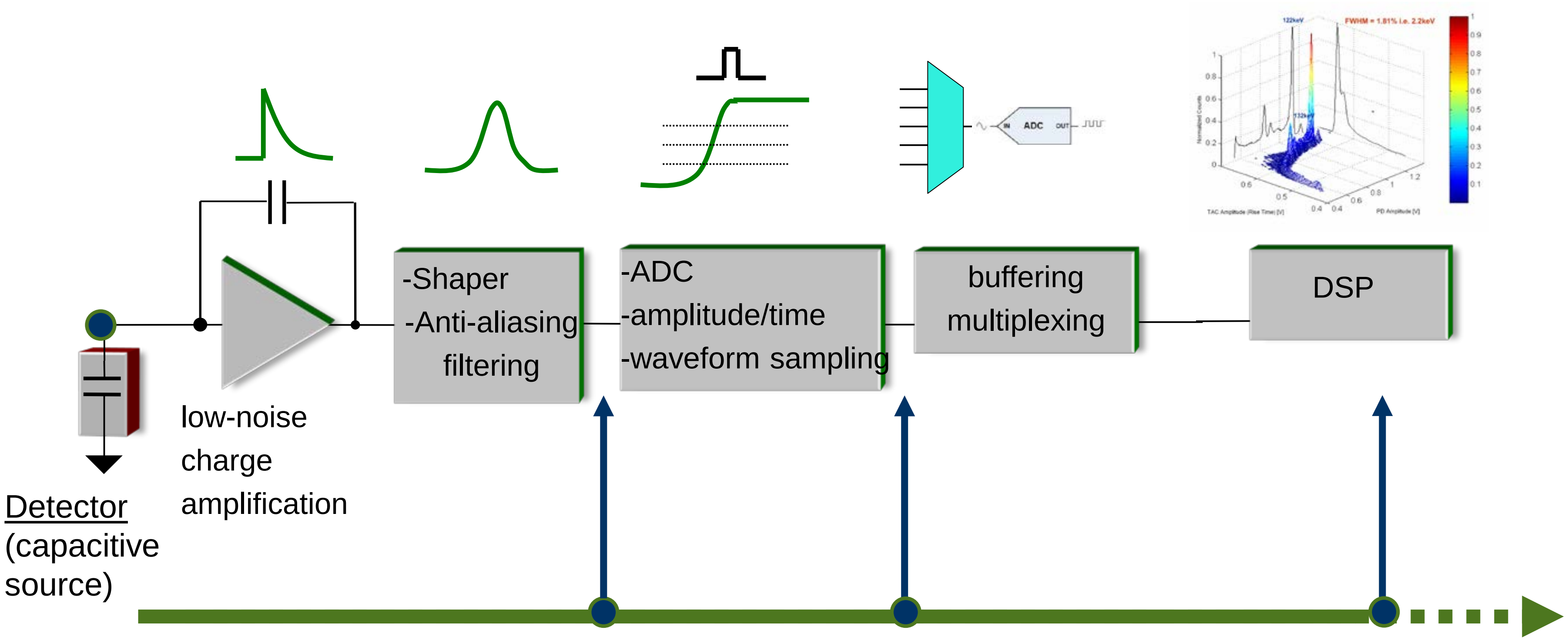


A **major challenge** is how to efficiently respond to the increase in **demand**, **functionality** and **complexity**

Review of ASICs Developed at BNL

Year	ASIC Families	Collaborator	Publications	Impact areas
1996-1999	ATLAS family	ATLAS	*	Particle Physics
1996-1999	RHIC family	RHIC	*	Nuclear Physics
1997-2001	CreV family	eV Products	*	Nonproliferation, Medical Imaging
2000-2004	HERMES family	NSLS	*	Energy Sciences, Light Sources, Medical Imaging
2001-2009	PDD family	eV Products	*	Energy Sciences, Light Sources
2002-2003	CPG1 ASIC	LANL	*	Nonproliferation
2003-2004	LEGS TPC ASIC	Physics	*	Nuclear & Particle Physics
2005-2008	CPG2 ASIC	eV Products	*	Nonproliferation
2005-2007	SNS He^3 ASIC	ORNL	*	Energy Sciences
2005-2007	Multiwindow ASIC	eV Products	*	Nonproliferation, Medical Imaging
2005-2008	RATCAP ASIC	Medical	*	Medical Imaging, Neuroscience
2006-2011	H3D family	DoD, UMich	*	Nonproliferation, Medical Imaging
2006-2016	Compton Imager ASIC	NRL, NASA	*	Nonproliferation, Energy Sciences
2006-2010	LUNAR family	NSLS, NASA	*	Energy Sciences, Light Sources
2010-	DUNE front-end ASIC	Physics	*	Particle Physics
2011-	DUNE ADC ASIC	Physics	*	Particle Physics
2011-	ATLAS VMM family	Physics	*	Particle & Nuclear Physics
2014-	MARS family	NSLS	*	Energy Sciences, Light Sources
2014-	HEXID 2D family	NSLS, NASA, SBU, WUSTL, RMD	*	Energy Sciences, Light Sources
2015-	Ge family	LBNL, LANL	*	Particle Physics, Energy Sciences, Nonproliferation
2015-	H3DD family	DoD		Nonproliferation, Particle & Nuclear Physics
2015-	ATLAS HLC ASIC	Physics	*	Particle Physics
2016-	SAR ADC ASIC	Physics		Particle Physics, Energy Sciences
2016-	LDO regulator	Physics		Particle Physics, Energy Sciences

Developing Front-End Readout ASICs:
Increased Functionality and Complexity



Detector
(capacitive
source)

low-noise
charge
amplification

-Shaper
-Anti-aliasing
filtering

-ADC
-amplitude/time
-waveform sampling

buffering
multiplexing

DSP

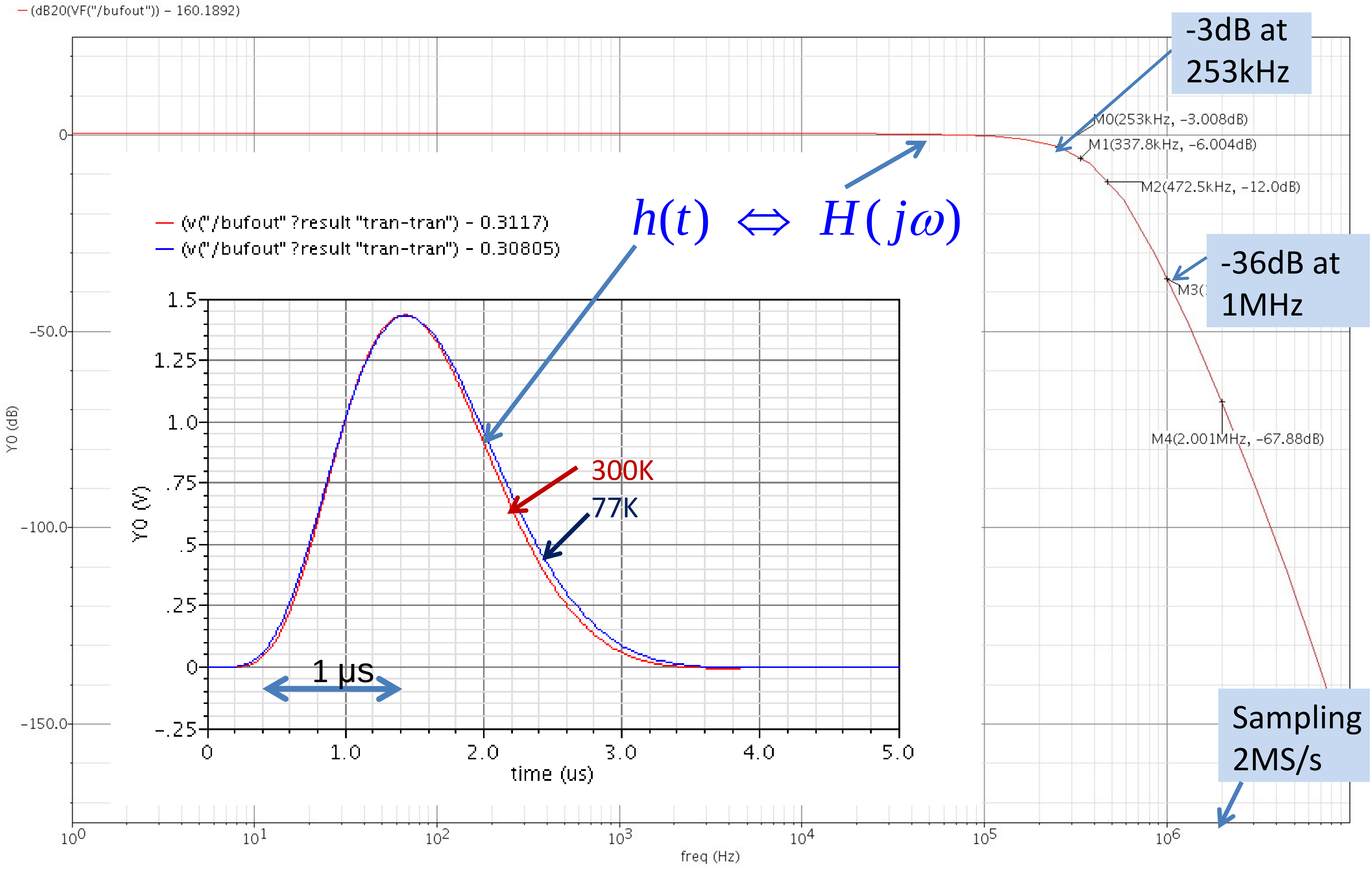
year 2000
- 250 nm technology
- 16,000 transistors
- 16 channels
- analog

year 2010
- 180 nm technology at cryo temp.
- ~ 1M transistors
- ~ 100 channels
- analog and mixed-signal

year 2011
- 130/65 nm technology
- >> 1M transistors
- >> 100 channels

LAr ASIC Anti-aliasing filter: bandwidth, Nyquist rate, sampling frequency

Oversampling: $M = f_N/f_{NR} = f_S/4f_{3db}$ = Nyquist frequency/Nyquist rate


-3dB at 253kHz

-36dB at 1MHz

Sampling 2MS/s

$h(t) \Leftrightarrow H(j\omega)$

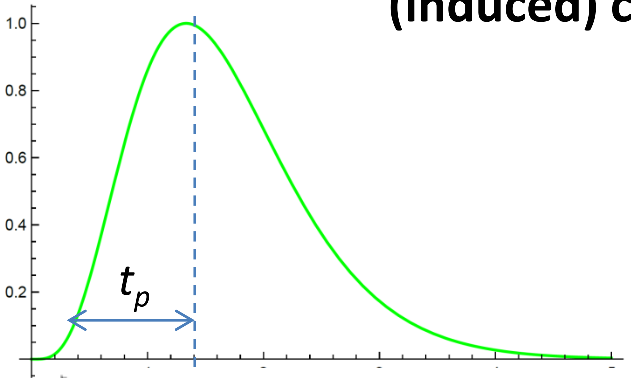
300K

77K

1 µs

Sampling, Waveform Reconstruction and Charge (area) Measurement of (induced) current *i(t)=qδ(t)* , *from the samples*

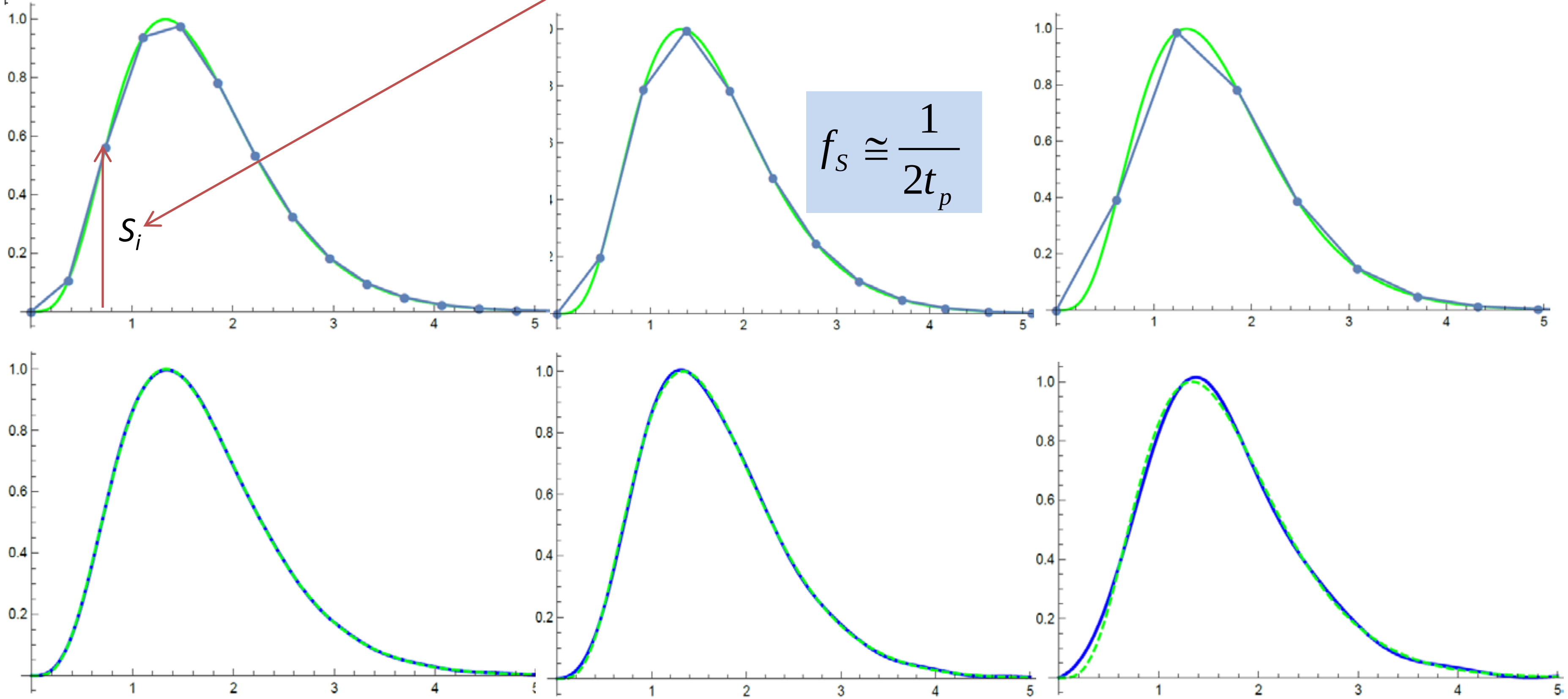
[Courtesy: V. Radeka]



M=$f_S/f_{NR}= f_S/4f_{3db}$ = sampling frequency/(4 x bandwidth)

$$\Delta q/q = \left[\sum S_i - \int h(t)\,dt\right] \Big/ \int h(t)\,dt$$ = charge(area) error

Waveform interpolating function = ***sinx/x*** used with each sample to reconstruct the waveforms (bottom row)



$$f_S \cong \frac{1}{2t_p}$$

M=2.5 $\Delta q/q = 0.0011\%$

M=2 $\Delta q/q = 0.0850\%$

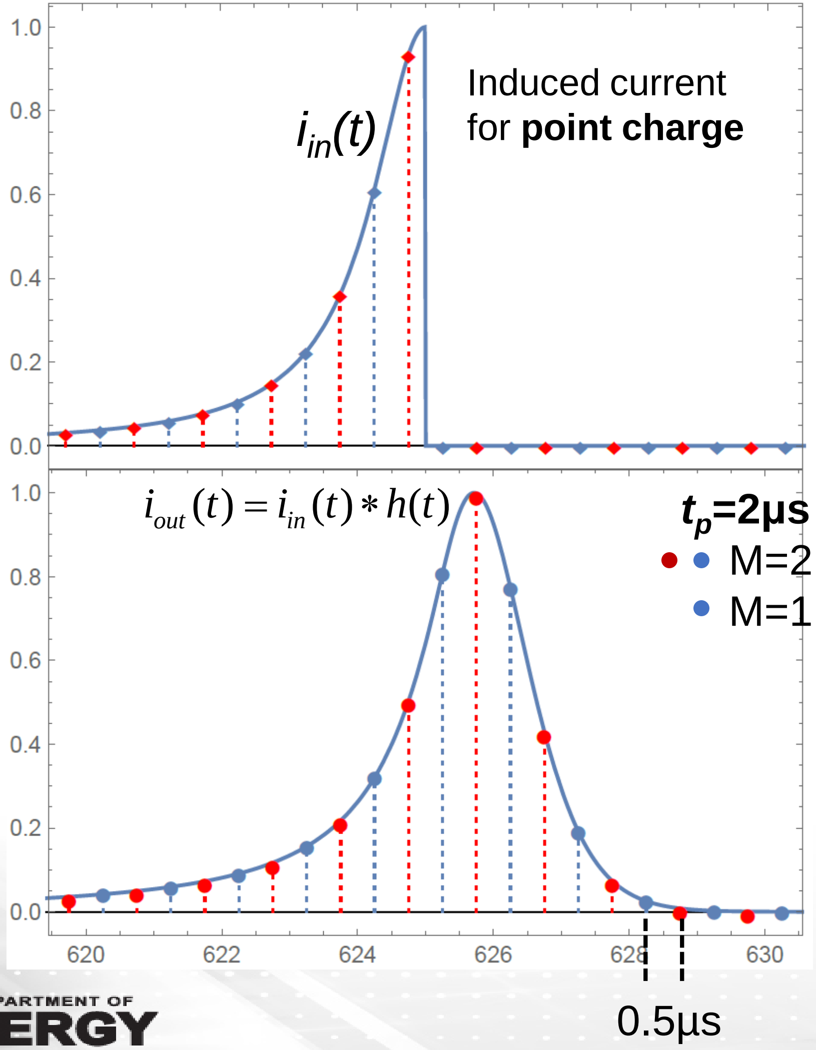
M=1.5 $\Delta q/q = 0.3683\%$

Accuracy of charge information in the samples vs oversampling

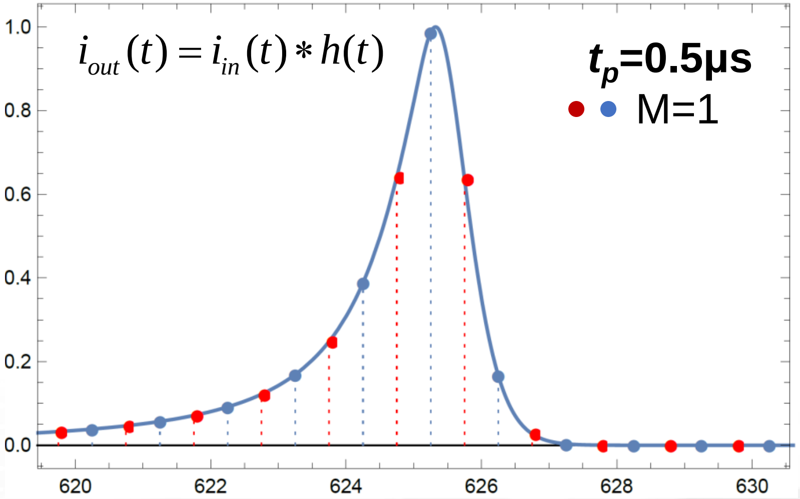
Oversampling $M = f_S / f_N = f_S / 2f_{3db}$ = sampling frequency/Nyquist frequency

[Courtesy: V. Radeka]

$$\Delta q / q = \left[\sum i_{out(i)} - \int i_{out}(t)\, dt \right] \Big/ \int i_{out}(t)\, dt$$ = charge(area) error

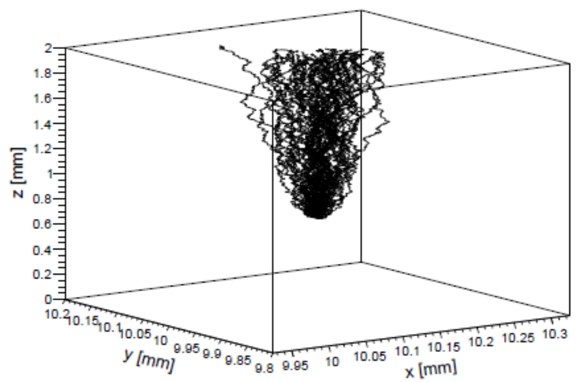


The ***sampling frequency*** is **2MS/s** for both **t_p=0.5µs** and **t_p=1µs (1MS/s** for every other sample at **t_p=1µs).** The ***Nyquist rate*** is ~**500 kHz** at **1 µs** peaking time and ~**1MHz** at **0.5 µs**. The sum of samples ***area error*** is less than **~0.1%** in all cases, and less than **~0.03%** for M=2 (**t_p=1µs and 2MS/s).**

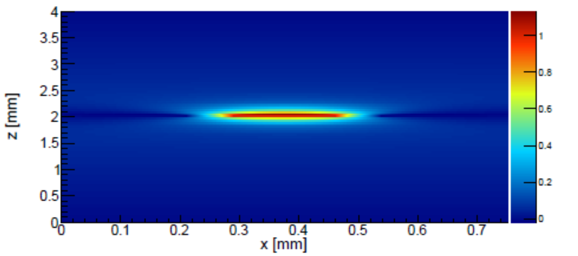


Example: Induced Current & Charge Simulations in GEANT4 w/ Laplace Solver

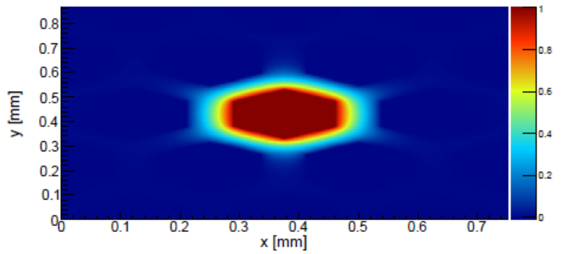
[Tang & Kislat_WUSTL]



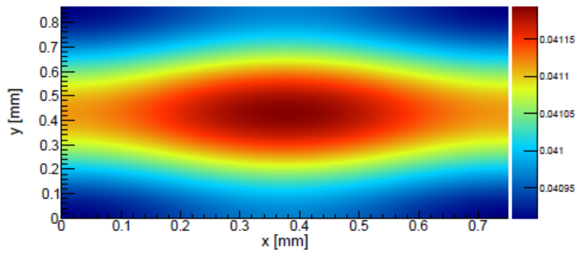
Vertical slice through center pixels

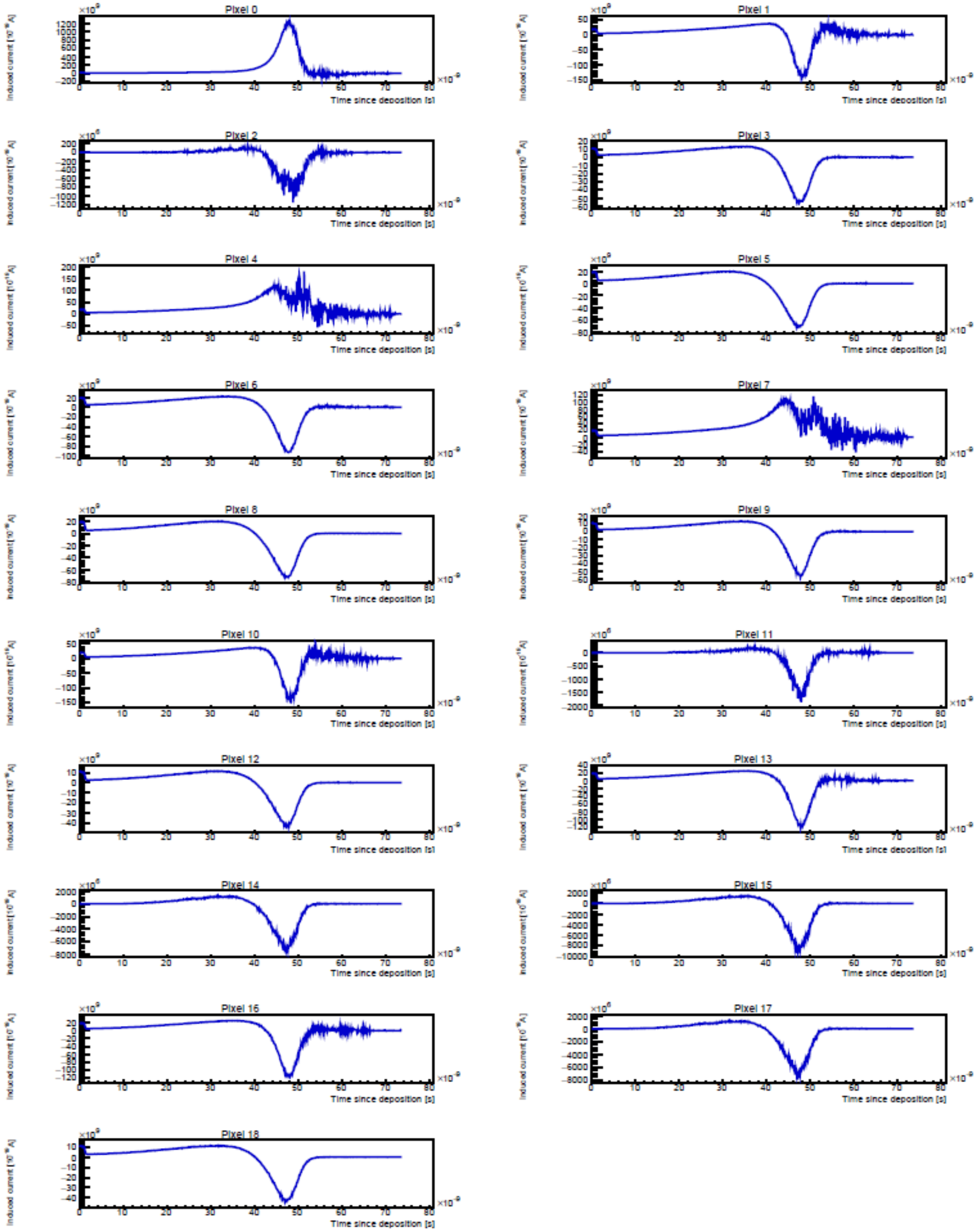


Horizontal sice through anode

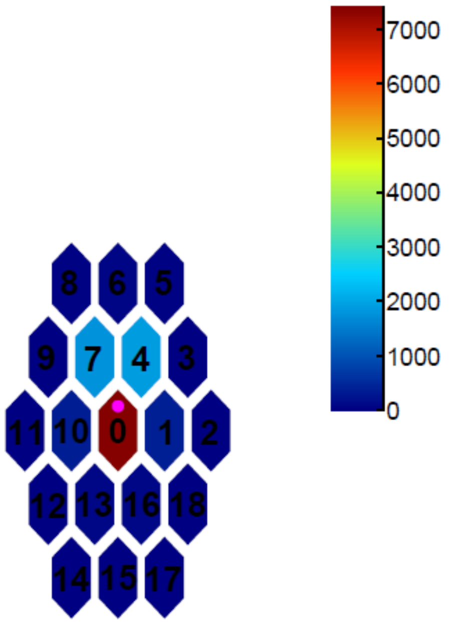


Horizontal slice halfway to anode



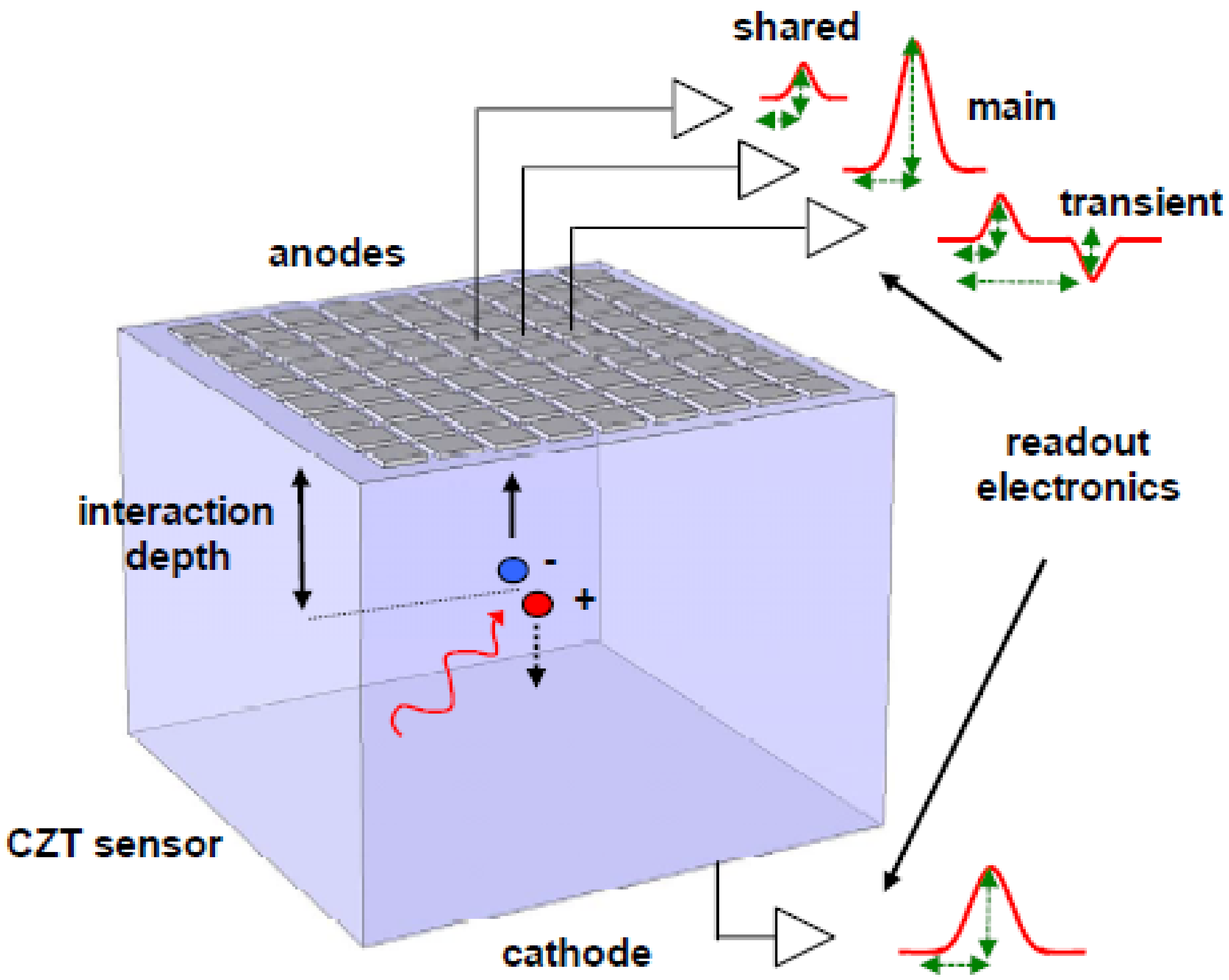


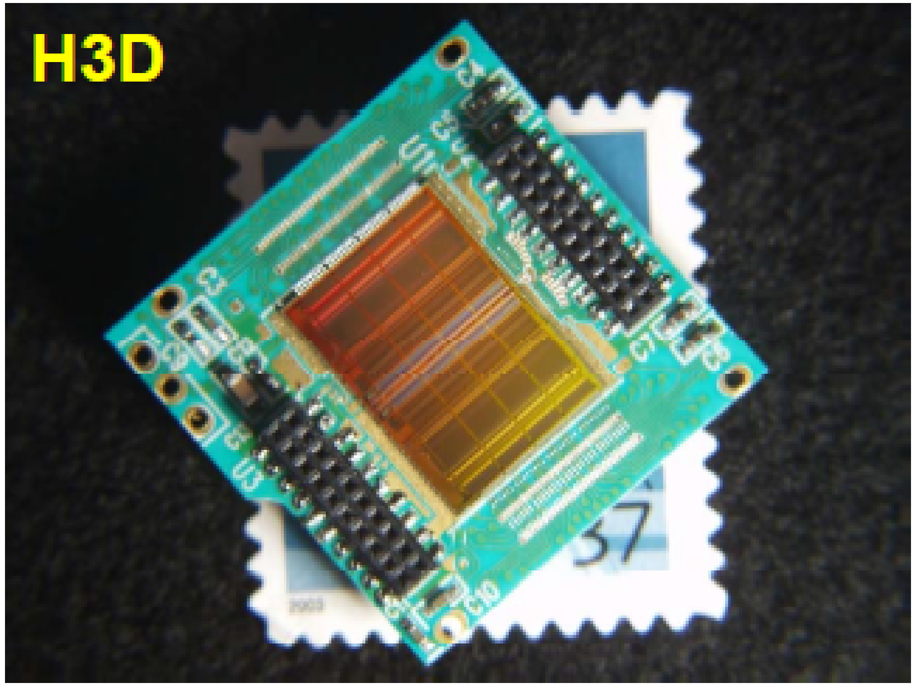
8.0 keV event 0



Si detector @ 60um pitch, 300nm thickness

Analog 3D PSD Technique - H3D ASIC

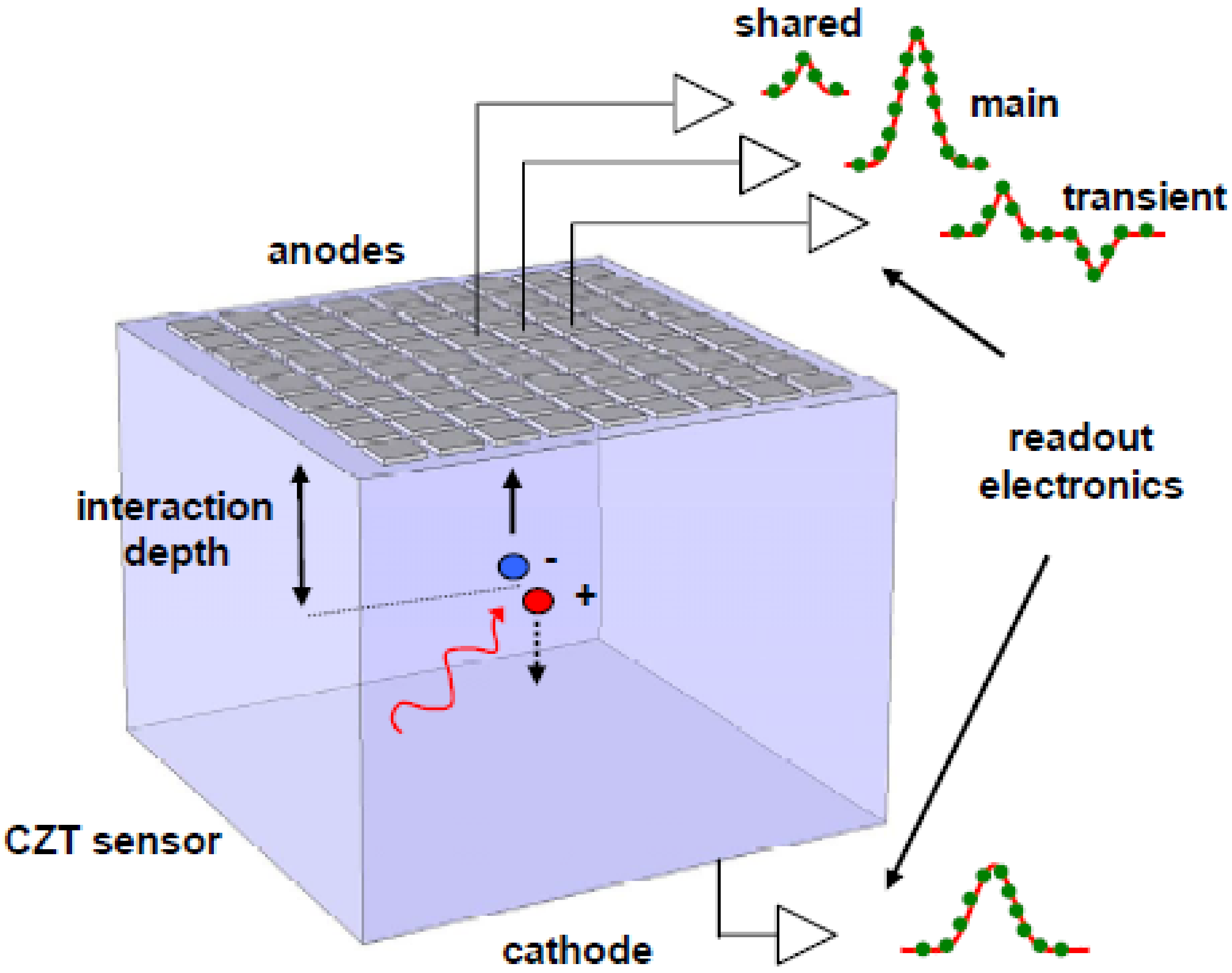


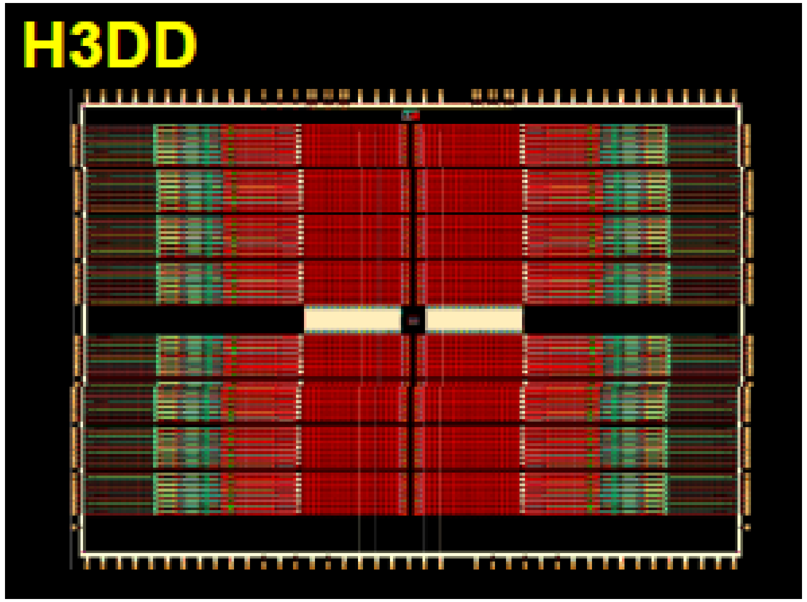


- H3D ASIC measures peak amplitude and relative timing on each signal *(Prof. Z. He)*

[G. De Geronimo_TNS2008]

Digital 3D PSD Technique - H3DD ASIC



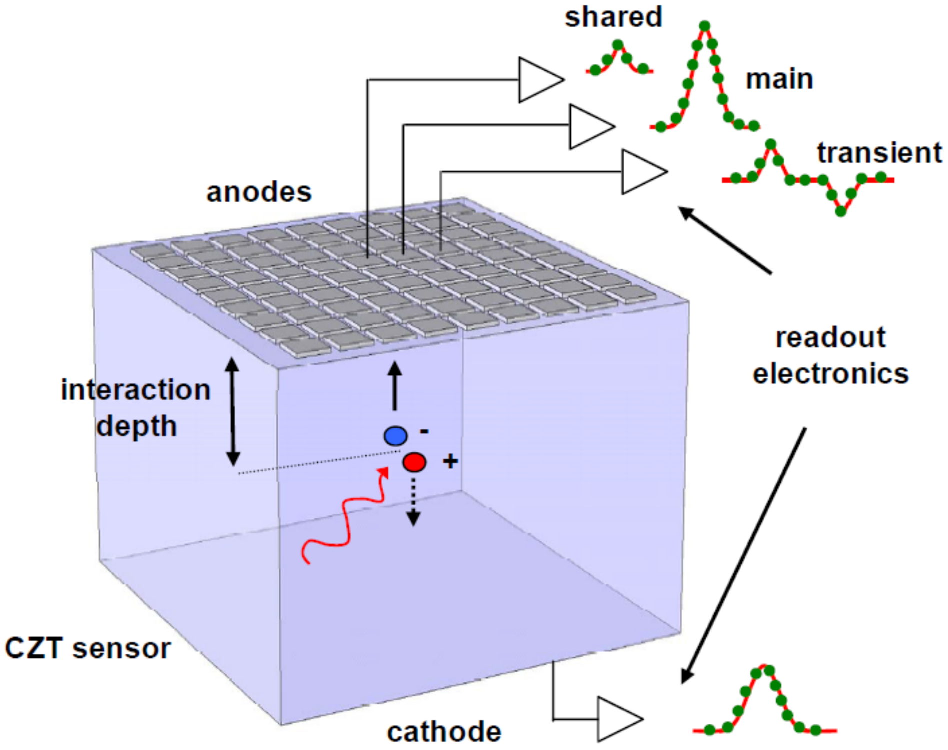


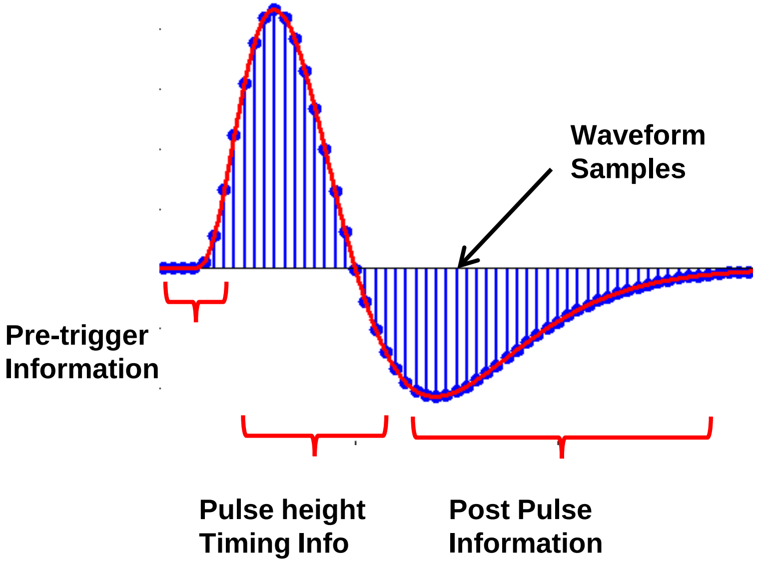
- H3DD ASIC measures **whole waveform** on each signal
- Waveforms are analyzed with powerful signal processing techniques, thus achieving **higher resolution** *(Prof. Z. He)*

[G. De Geronimo_Sept. 2016]

Digital 3D PSD technique – H3DD ASIC

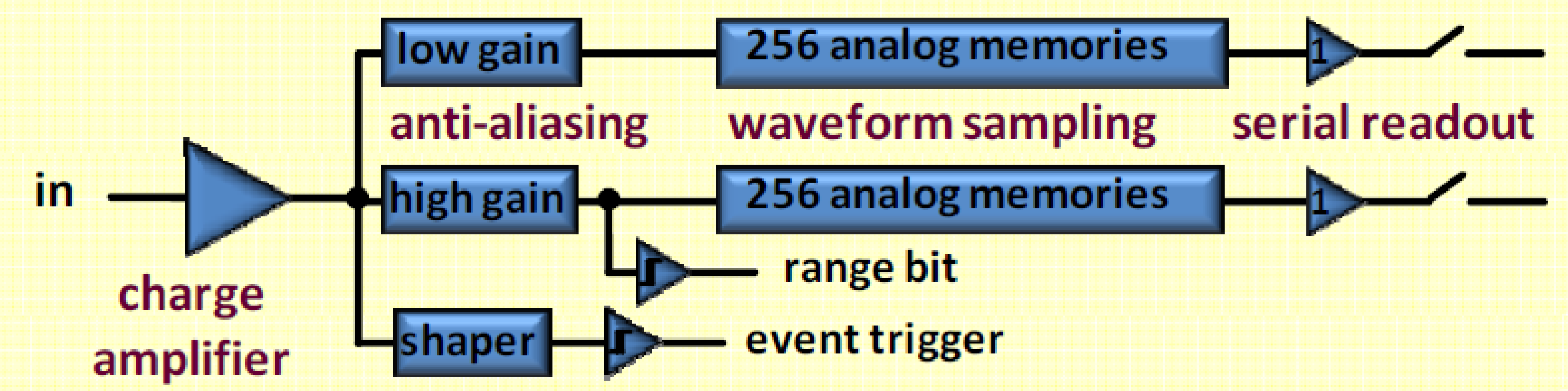
[A. D’Andragora_Apr. 2018]





•H3DD ASIC measures whole waveform on each signal
•Waveform is digitally sampled and stored
•Advanced algorithms can extract information from the stored data
↓
•Waveforms can be analyzed with powerful signal processing techniques, thus achieving higher resolution

H3DD Channel Architecture

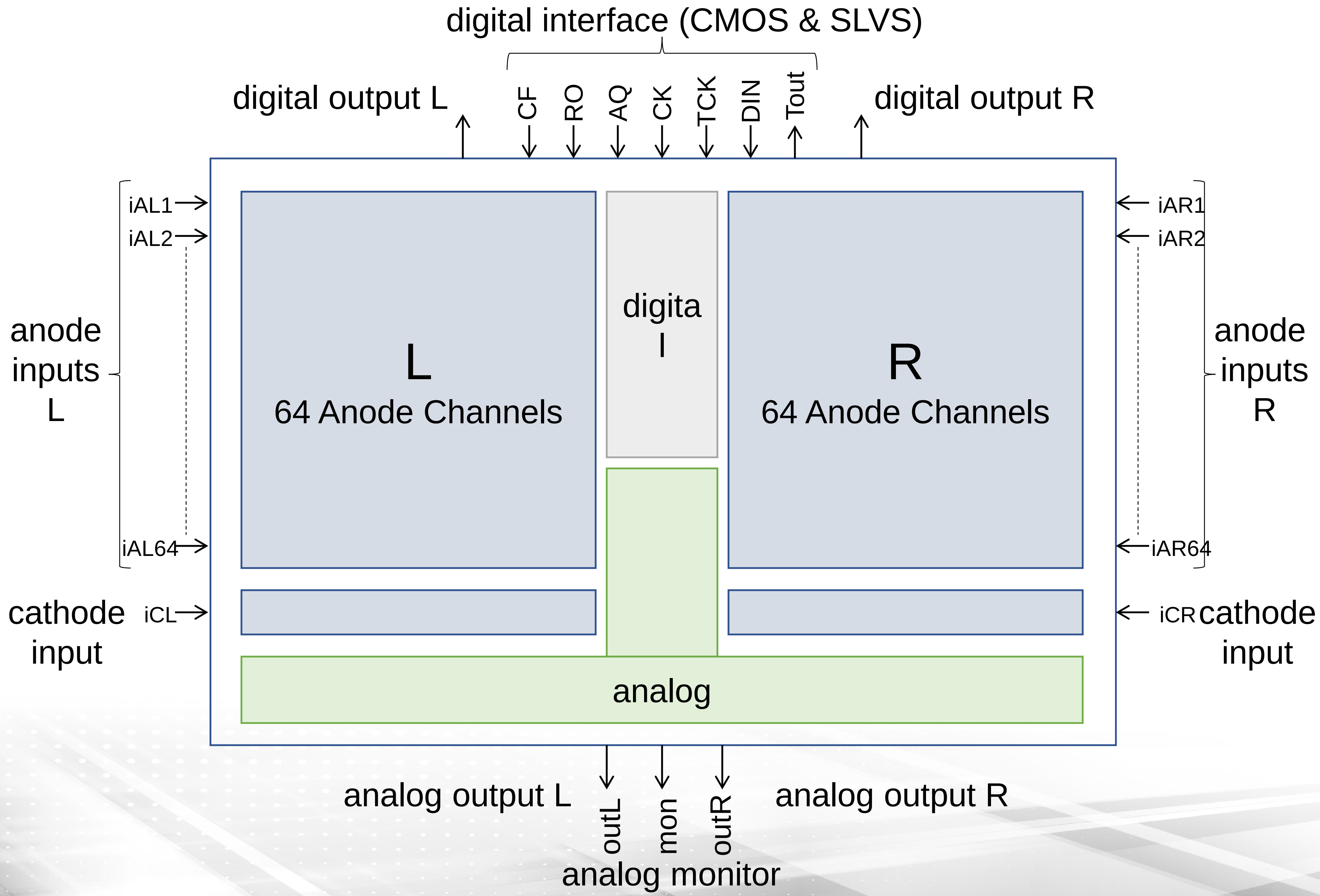


- energy resolution < **1 keV**
- energy range up to **9 MeV**
- dynamic range up to **10,000**
    - from dual-gain architecture
- programmable gain
- programmable anti-aliasing filter
- low-noise event discrimination

- high-resolution waveform sampling
- record depth up to **256** samples
- programmable **pre-** and **post-trigger**
- sampling rate up to **200 MS/s**
- readout rate up to 100 MS/s
- multiple trigger and readout modes
- power dissipation **~1.7 mW/channel**

[G. De Geronimo_Sept. 2016]

ASIC Architecture



digital interface (CMOS & SLVS)

digital output L

CF
RO
AQ
CK
TCK
DIN
Tout

digital output R

anode inputs L

iAL1
iAL2
iAL64

L
64 Anode Channels

digita l

R
64 Anode Channels

iAR1
iAR2
iAR64

anode inputs R

cathode input

iCL

iCR

cathode input

analog

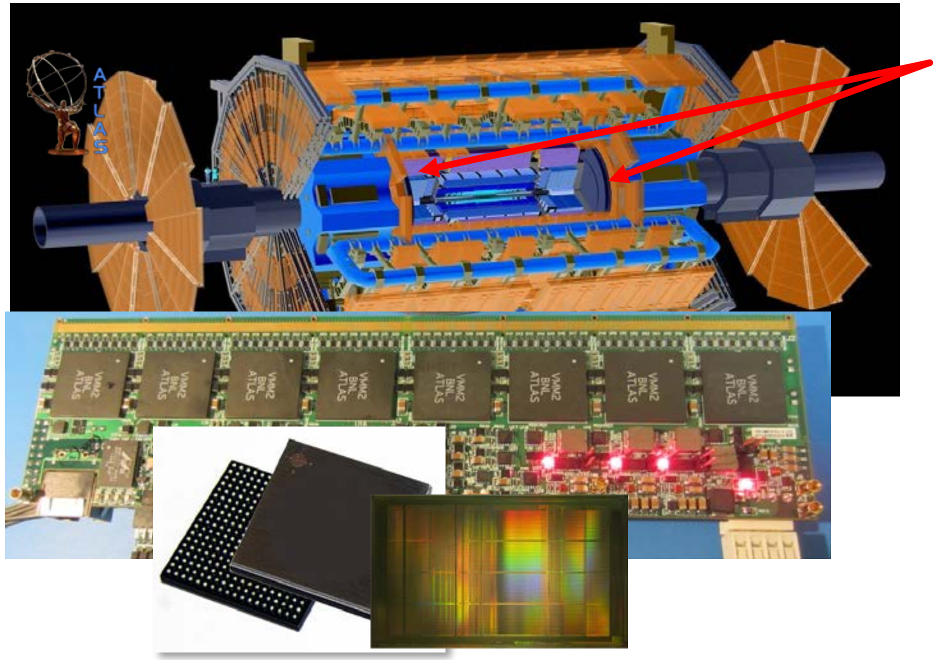
analog output L

outL
mon
outR

analog output R

analog monitor

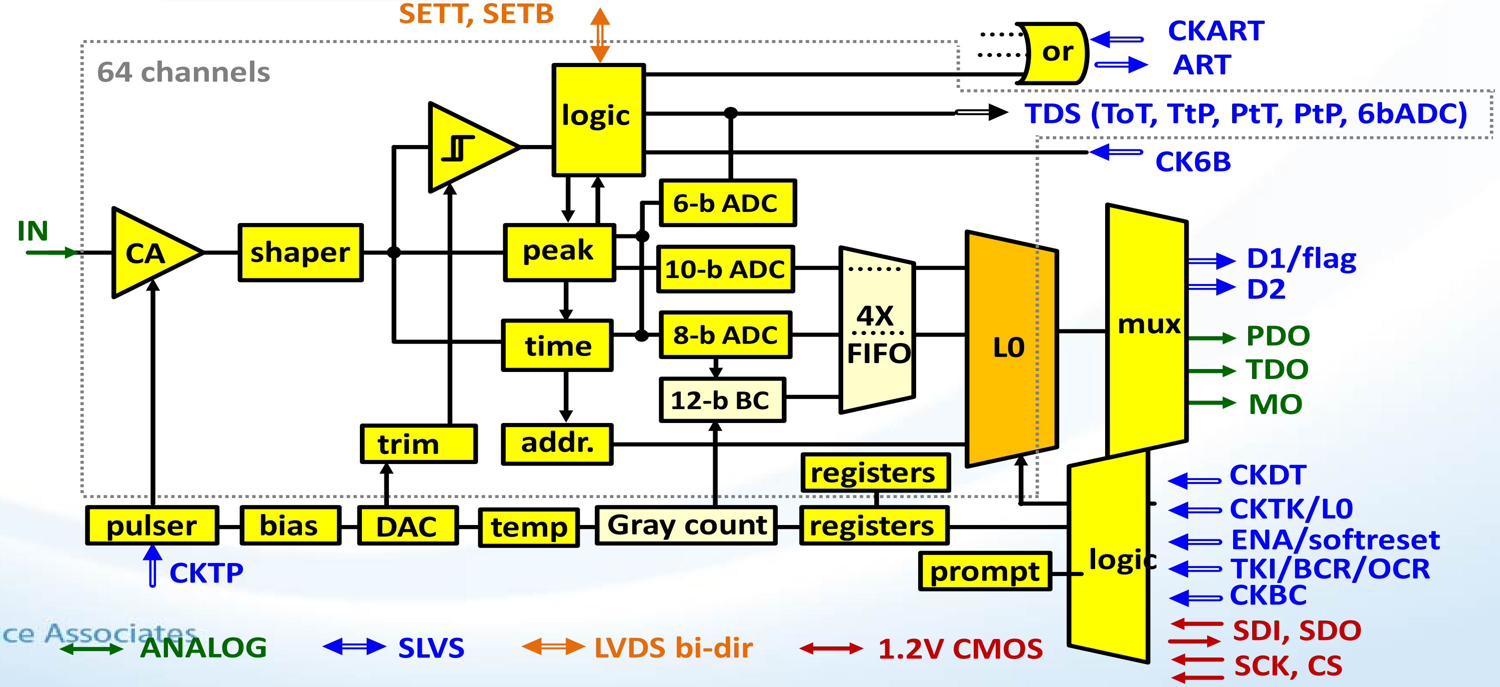
FE-SOC: ASIC for ATLAS Muon Spectrometer



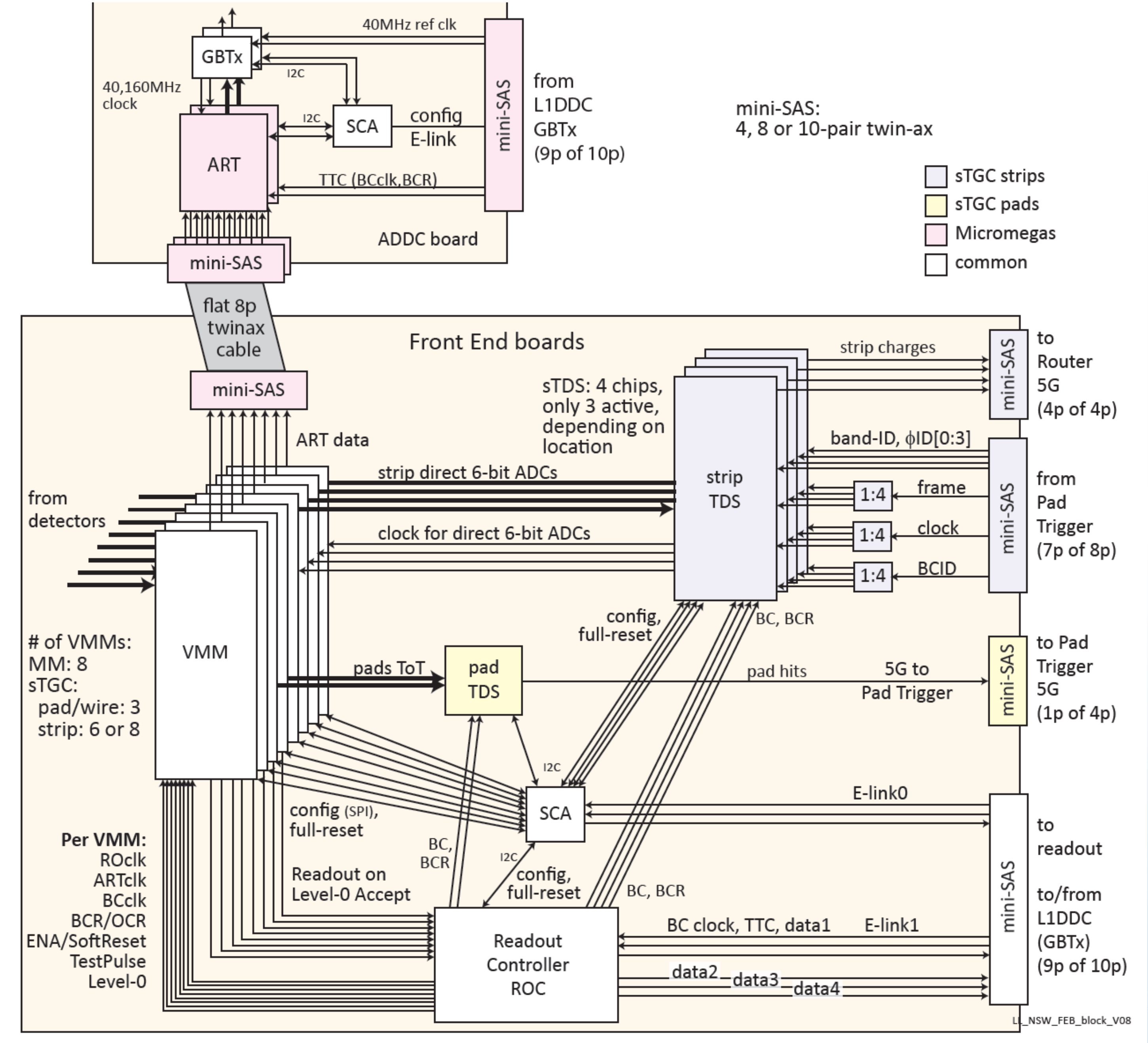
New Small Wheels: 2.3M channels,
2pC @ < **1fC** rms, 100ns @ < **1ns** rms, 30pF-**2nF**

- 64 channels: low-noise amplification, peak, timing, discrimination, **3 ADCs**, timestamp, FIFO, **L0 handling (on-chip DSP)**
- real-time address, sub-hysteresis, direct outputs, fully digital interface
- CMOS 130nm, 13.5 mm x 8.4 mm,
- **transistor count/ch.: > 100,000**

G. De Geronimo et al., TNS June 2013



Overall DAQ System of the VMM



VMM3a digital mode:

- 38 bit data (2 serial lines): 1b flag, 1b thr (hit/neighbor), 6b addr, 10b peak, 20b time (8b TAC + 12b memory)
- max. event rate: 4MHz/ch (~250ns: conversion time 200ns+), 64-deep latency FIFO for 16us hits (250ns *64)
- readout time per ch: 19b * 6.25 ns = 120ns
- two serial lines at 160MHz with Double Date Rate => 640 Mb/s

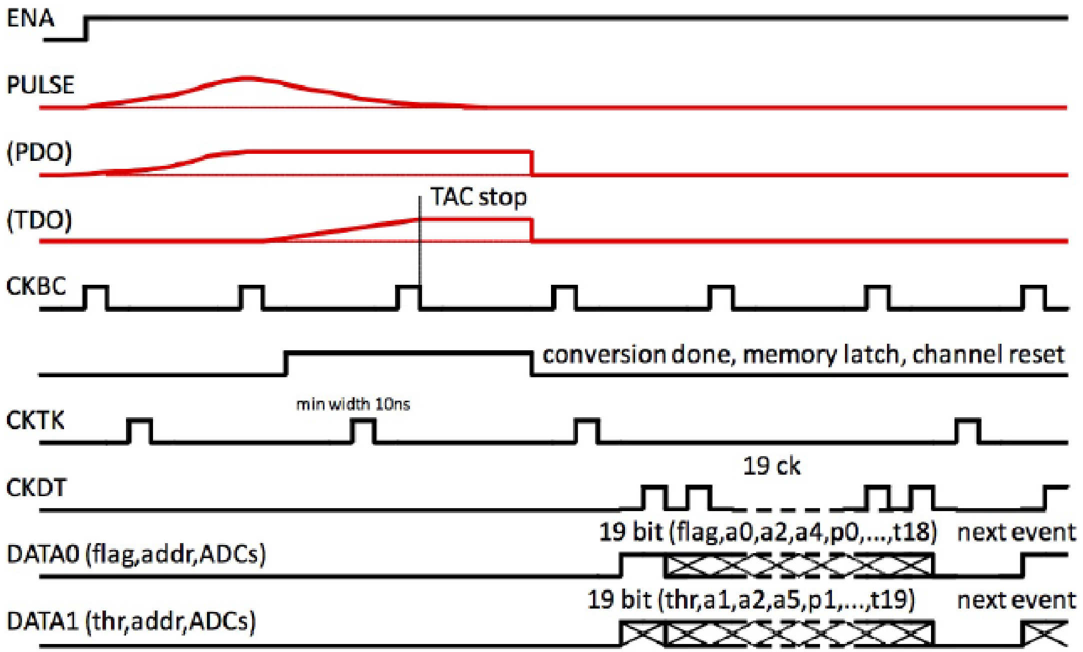
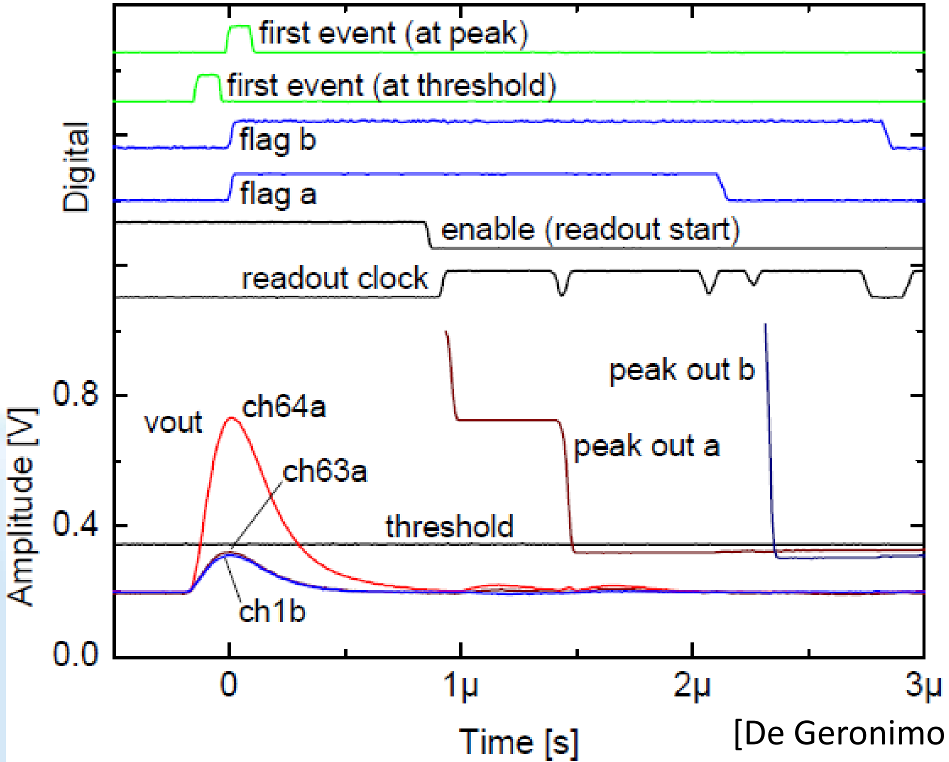
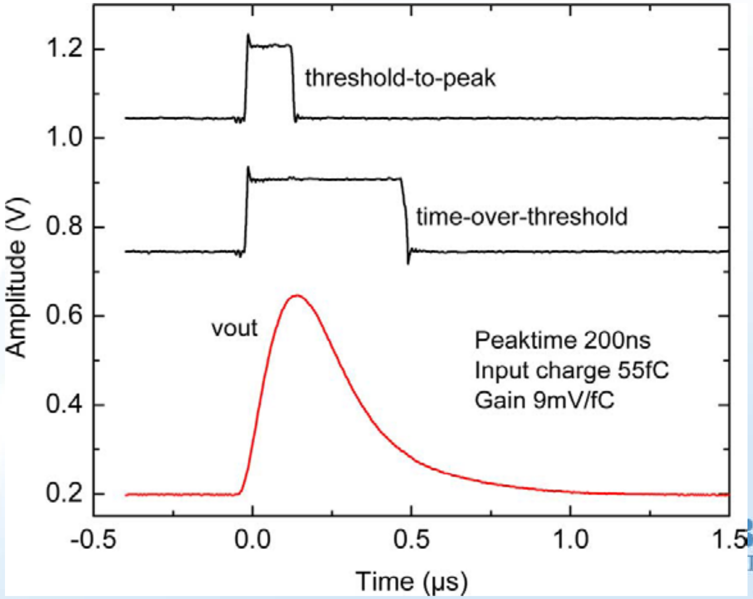


Figure 11: Data Readout with ADCs (continuous mode, 1 bit/ck).



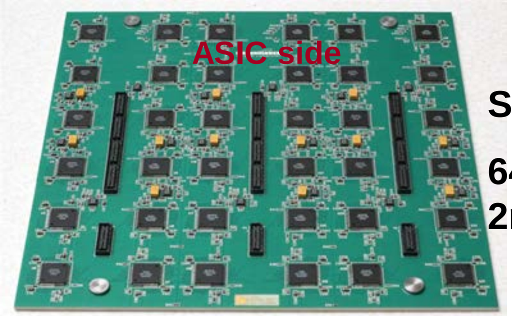
[De Geronimo et al_VMM1_TNS2013]



Two-Dimensional, Pad Detector for Neutron Scattering

$^3He + n \rightarrow {}^3H + p$ +764keV (~ 5 fC, or ~ 30k electrons)

24 cm × 24 cm anode pad board, with 5mm × 5mm pads → 2304 pixels

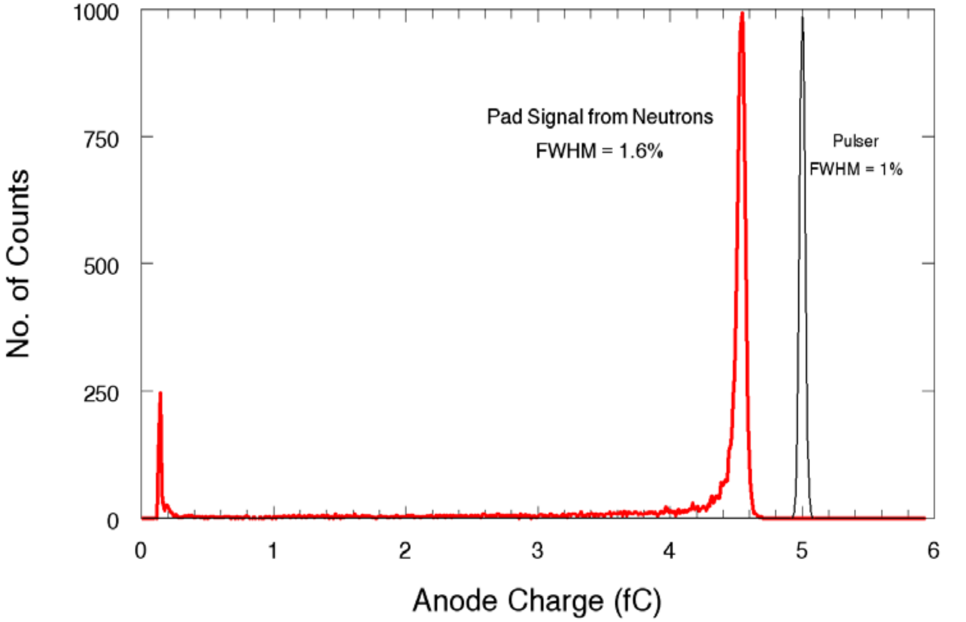


SNS ASIC

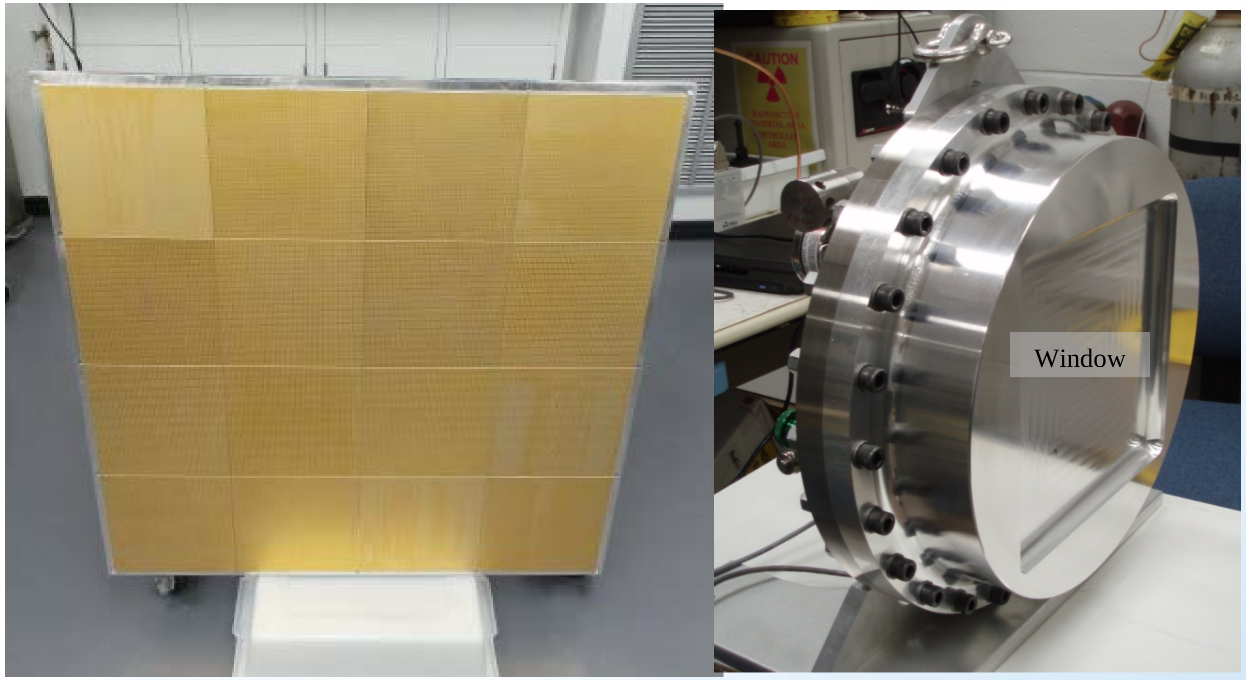
64 channel 2mW/ch

Neutron beam, ~ 1 mm^2, over pad# 20-53

2 μs shaping, 3 bar ^3He / 2 bar C_3H_8



Array of 4 × 4 pad boards, comprising 37 k independent channels. Operation in ionization mode, i.e. unity gas gain, would not be not feasible without ASICs



1 m × 1 m Detector for ANSTO

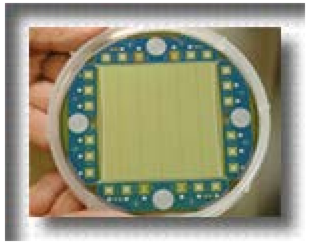
G. De Geronimo et al., TNS 54 (2007)

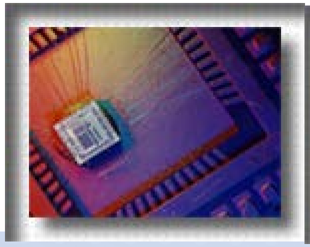
Instrumentation Division at BNL

Staff:

Approximately 45 total. About 14 scientists, 12 engineers, 11 technical.

Core Competencies:



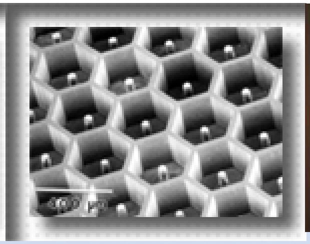


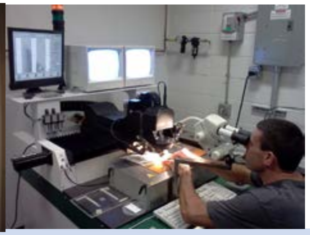
Semiconductor Detectors: Silicon X- and gamma-ray detectors, silicon charged particle detectors, Si CCDs, germanium X- and gamma-ray detectors.

Gas and Noble Liquid Detectors: Micropattern gas detectors, noble liquid TPCs, noble liquid calorimetry, ^{3}He based thermal neutron detectors.

Electronics: Low Noise ASICs, rad-hard electronics, digital signal processing, special printed circuit boards, high-density interconnect laboratory.

Lasers and Optics: Ultra-short photon and electron sources and



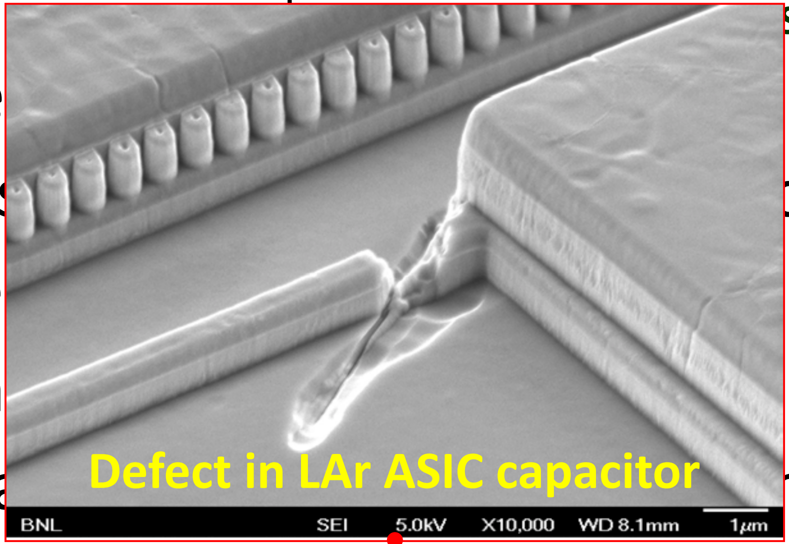


Mission:
To develop state-of-the art instrumentation required for experimental research programs.

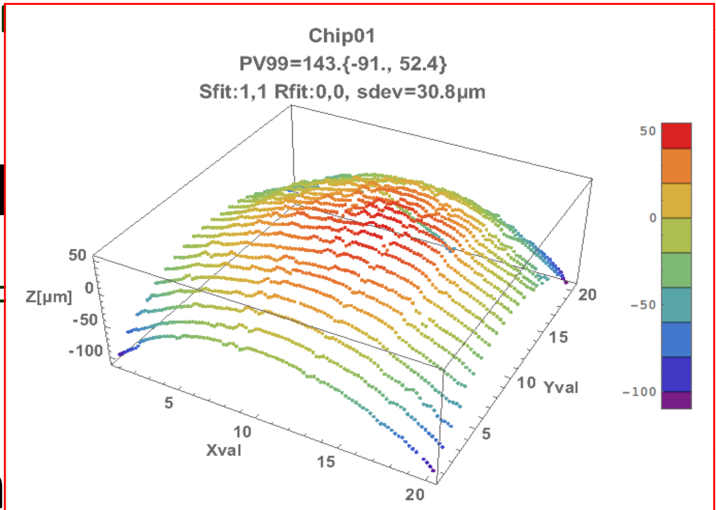
Backup Slides

Resources

ASIC design
- **Mietek Dabrowski (Cryo FE, ATLAS FE)**
- **Shaorui Li (HEXID, Cryo FE, GE, LUNAR)**
- **Yuan Mei (SAR_ADC)**
- **Emerson Vernon (AVG, MARS, H3D)**
- **Wenbin Hou (SBU PhD, NCI, LDO_REG)**
- **S .)**



Defect in LAr ASIC capacitor



BGA package curvature in VMM

Scie

Sens d

Inte P

Prin

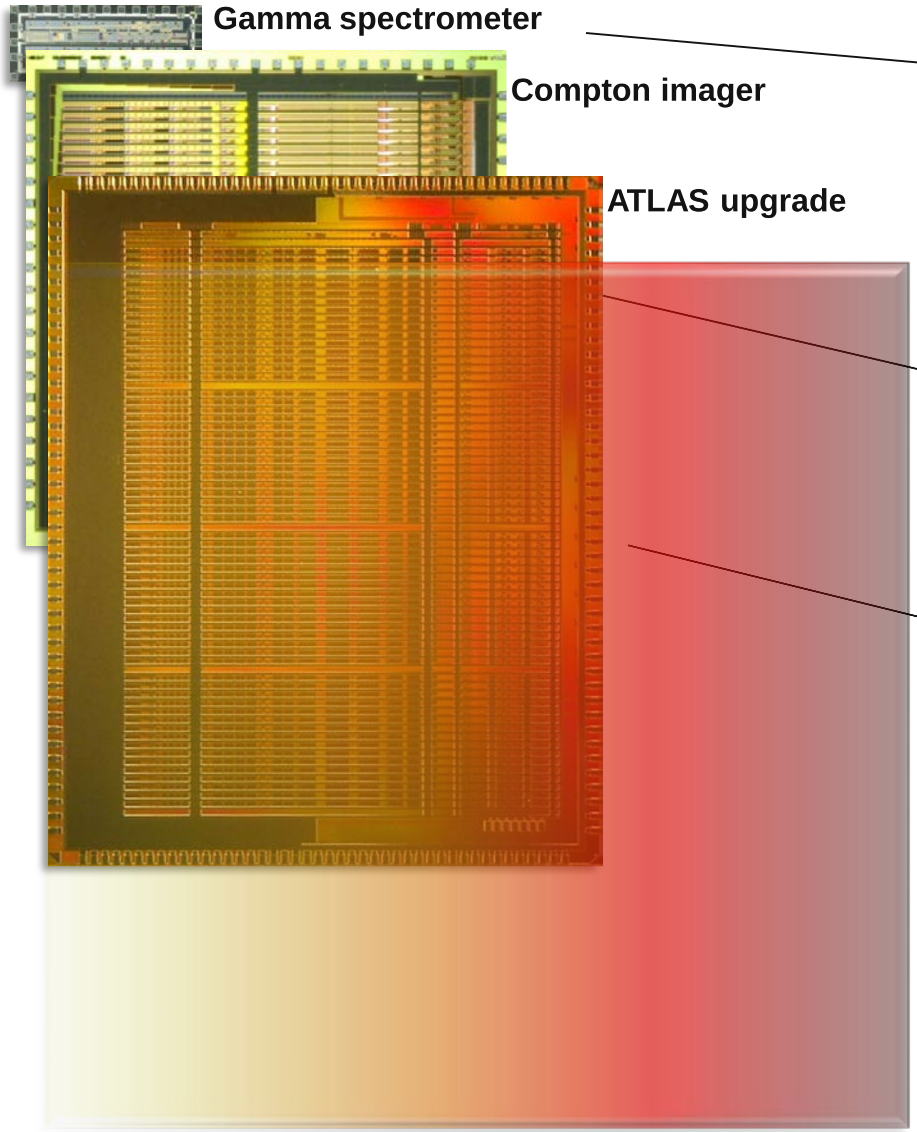
Data n

CAD tools and compuing A. Kandasamy

SEM laboratory, Optical metrology J. Warren, P. Takacs

- Developed in close collaboration with detector scientists from different fields

Design Complexity



~ year 2001
tech. CMOS 500nm, 3.3V
~ 10k transistors, ~ 2mm^2
preamplifier/filter

1-2 designers

3-4 designers

~ 2006
250nm, 2.5V
~ 100k transistors, ~ 25mm^2
+ discrim/peak-det/mux

Public-Domain CAD tools

Industry-Standard CAD tools *(Cadence, Mentor)*

~ 2011
130nm, 1.2V
~ 1M transistors, ~ 50mm^2
+ time-det/tots/mux/ART

5-6 designers

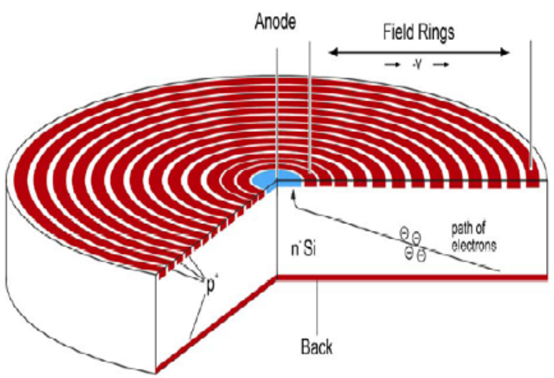
2016 to 2020
< 65nm, < 1.2V
> 10M transistors, > 100mm^2
+ ADCs/DSP/SOC/EOC

DSP=Digital Signal Processing
SOC=System on Chip
EOC=Experiment on Chip

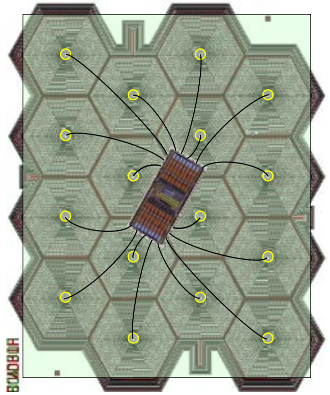
> 8 designers

~ 1-2 new designs/year, ~ 3-4 revisions/year

ASIC for Radiation-Hard High-Resolution X-ray Spectrometers



[Rehak & Gatti _1983]



16 x 20mm² SDD pixels

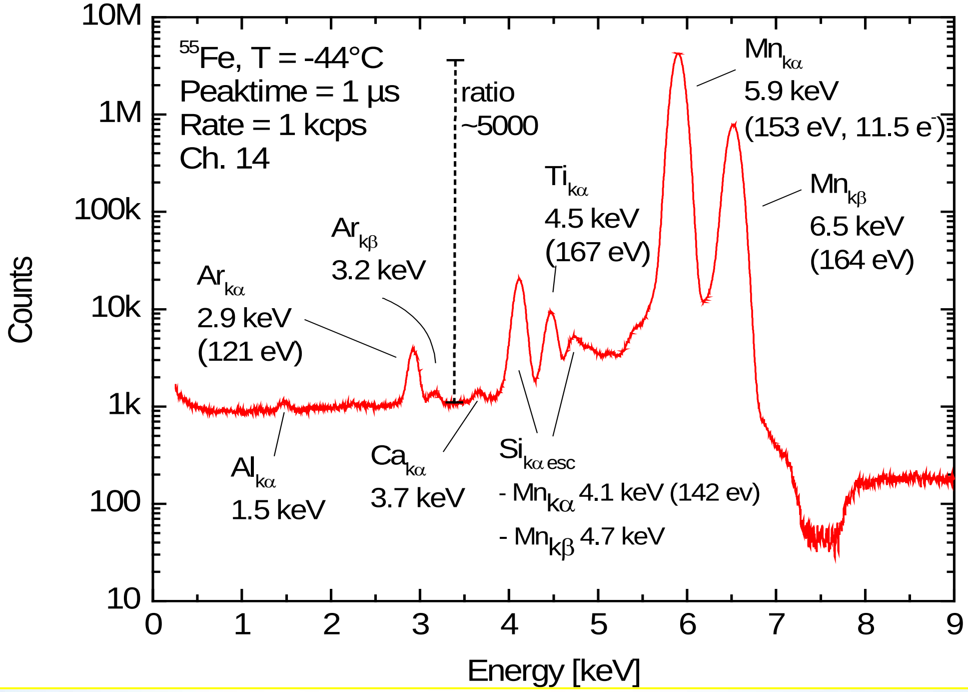
Improving Radiation Resistance:

- Radiation degradation due to leakage current of NMOS↑

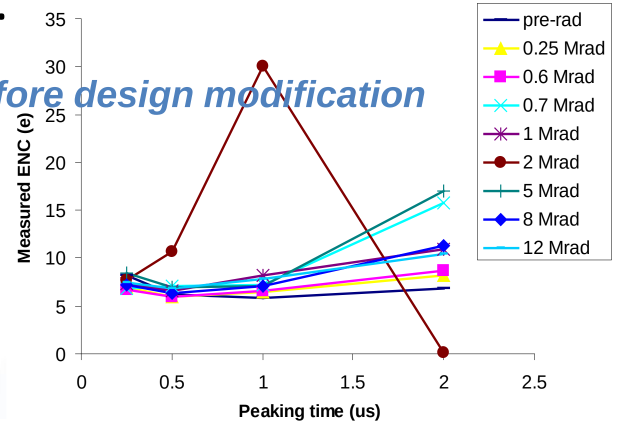
-ENC degradation: peak at around 2 Mrad

-Modified design to improve radiation resistance: replacing NMOS switch with PMOS switch; insert PMOS switch between NMOS current source and charge amp. input; increase device length; gate-enclosed layout.

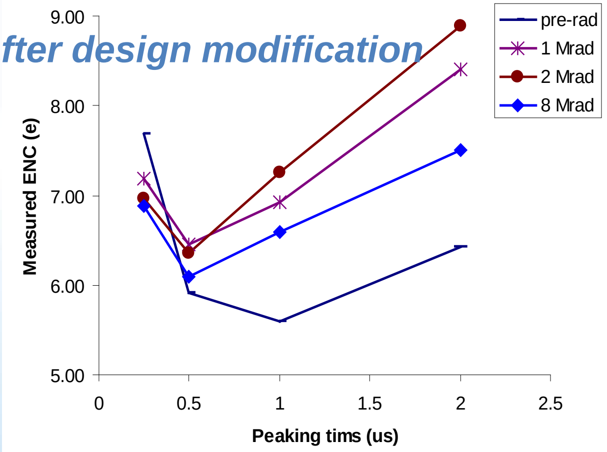
~11 e⁻ resolution (93 eV) with 20 mm² SDD pixel



ENC before design modification



ENC after design modification

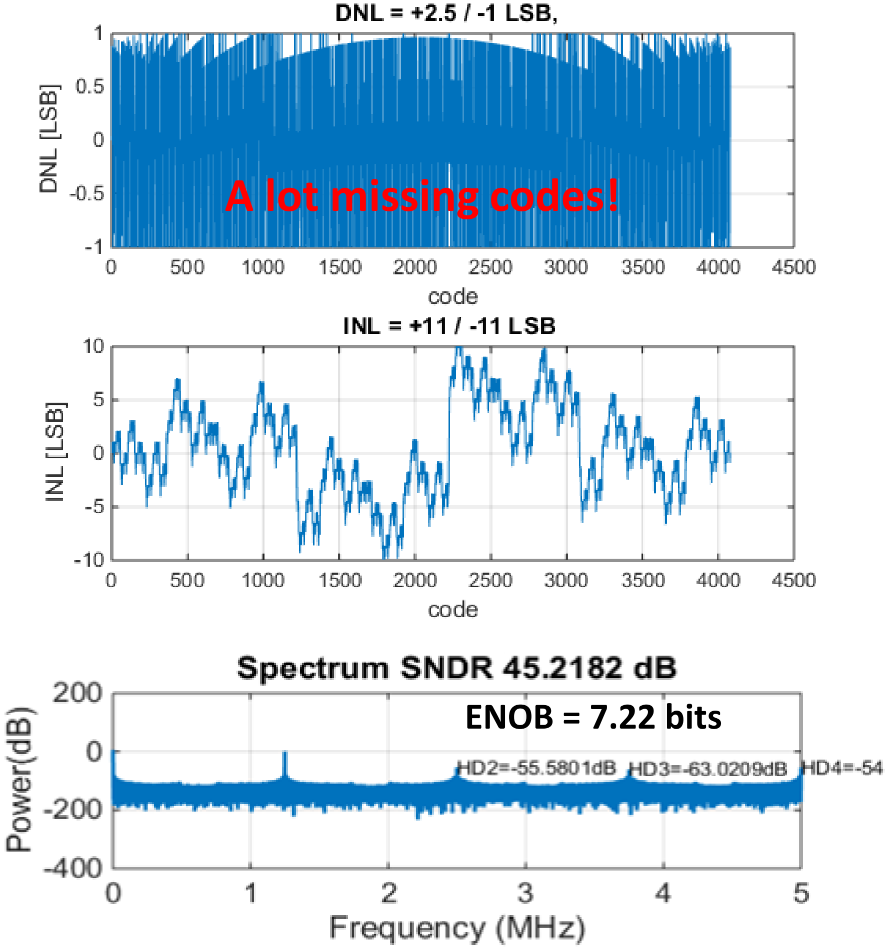


[S. Li & G. De Geronimo, IEEE TNS 2013]

12-bit 2MS/s SAR (Successive Approximation Register) ADC [Y. Mei_FEE2017]

- Both linearity (INL/DNL) and resolution (ENOB) are improved with *digital calibration* scheme!

Without Calibration


DNL = +2.5 / -1 LSB,

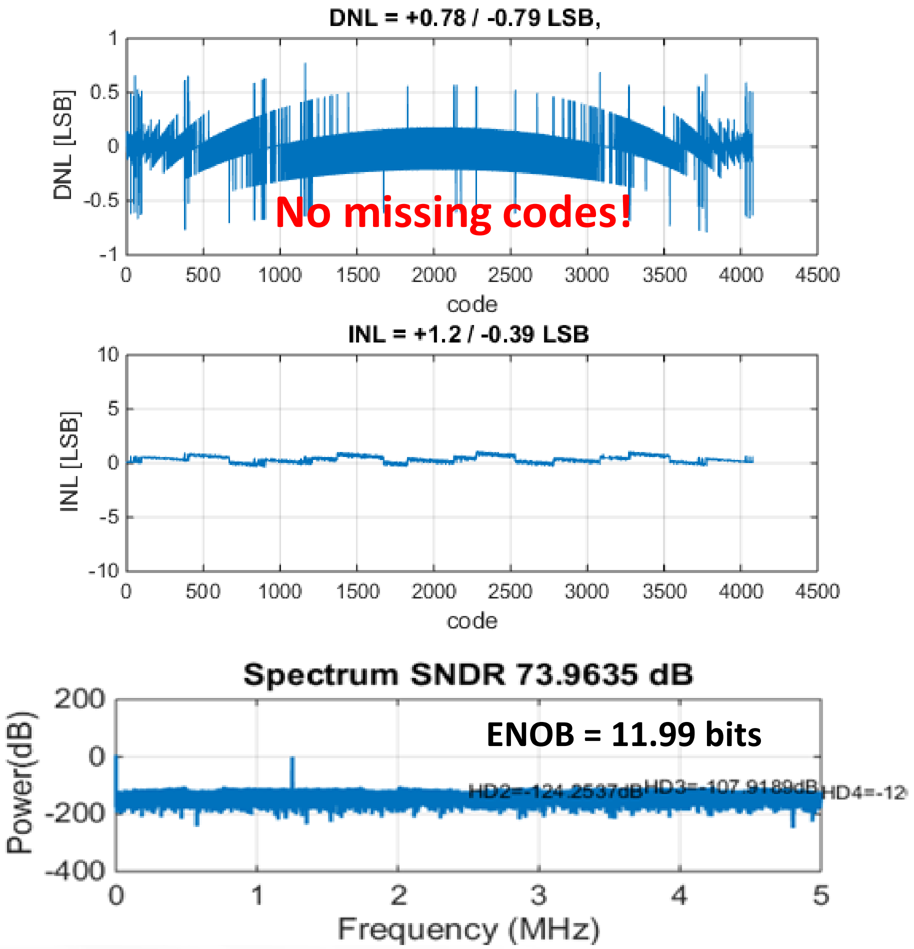
A lot missing codes!

INL = +11 / -11 LSB

Spectrum SNDR 45.2182 dB

ENOB = 7.22 bits

With Calibration

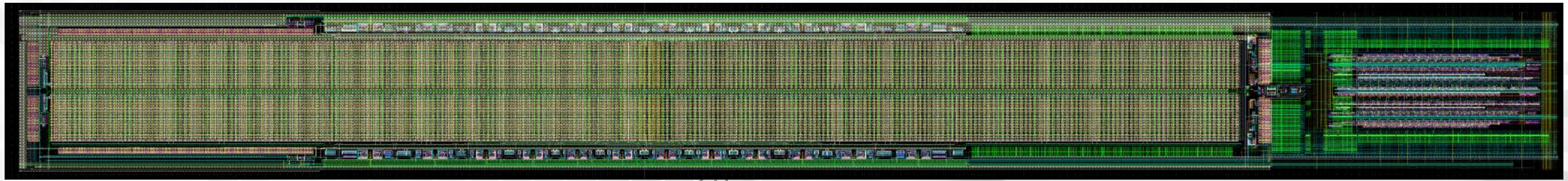

DNL = +0.78 / -0.79 LSB,

No missing codes!

INL = +1.2 / -0.39 LSB

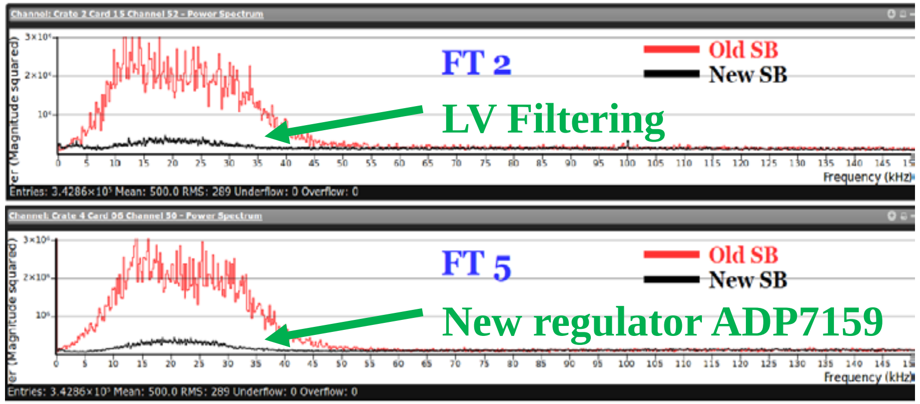
Spectrum SNDR 73.9635 dB

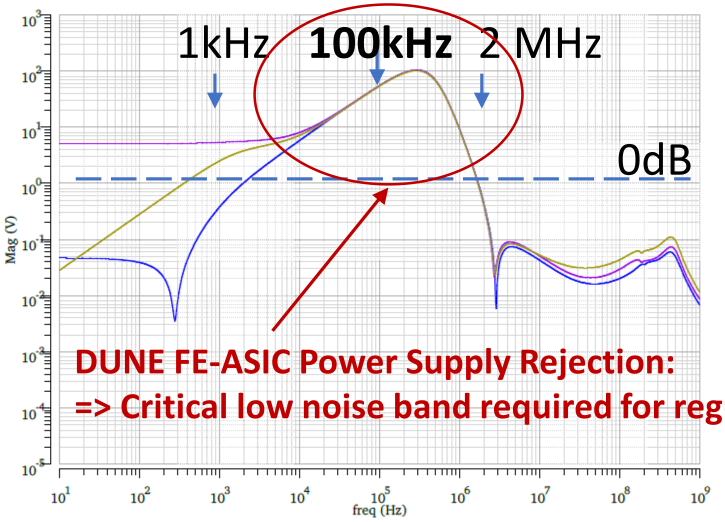
ENOB = 11.99 bits



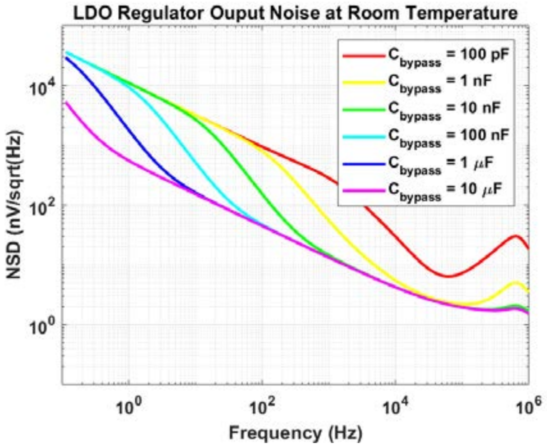
Ultra-Low-Noise LDO Regulator in 65 nm for Cryogenic FE ASIC [W. Hou_NSS2018]

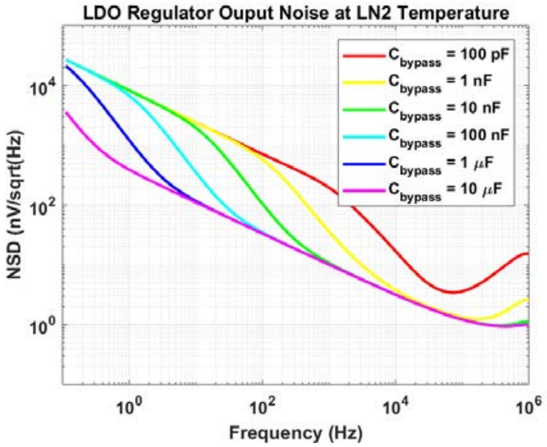
- Front-end ASICs may suffer of limited power-supply rejection, especially at frequencies corresponding to the shaper time constants.





DUNE FE-ASIC Power Supply Rejection:
=> Critical low noise band required for regulator

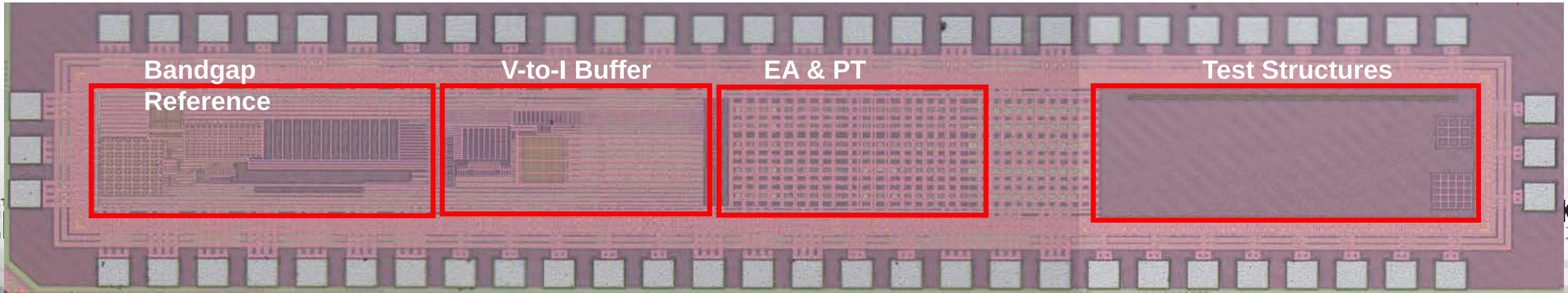




SIMULATED LDO PERFORMANCE

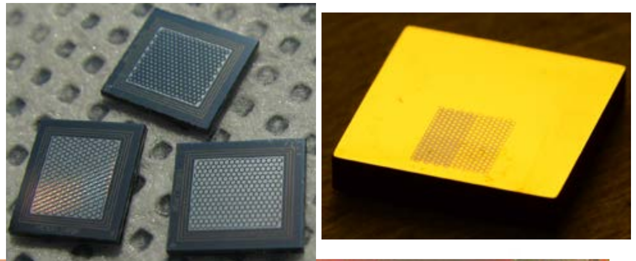
	Room Temp (300K)	Cryogenic Temp (77K)
Nominal output*	1.175 V	1.156 V
Current Efficiency	98.4%	98.6%
Power Efficiency	77.08%	75.99%
Phase Margin	80°	58°
PSR at 10 Hz	43.8 dB	51.8 dB
PSR at 100 KHz	51.8 dB	54.5 dB
Output RMS Noise	1.49 μV	0.987 μV

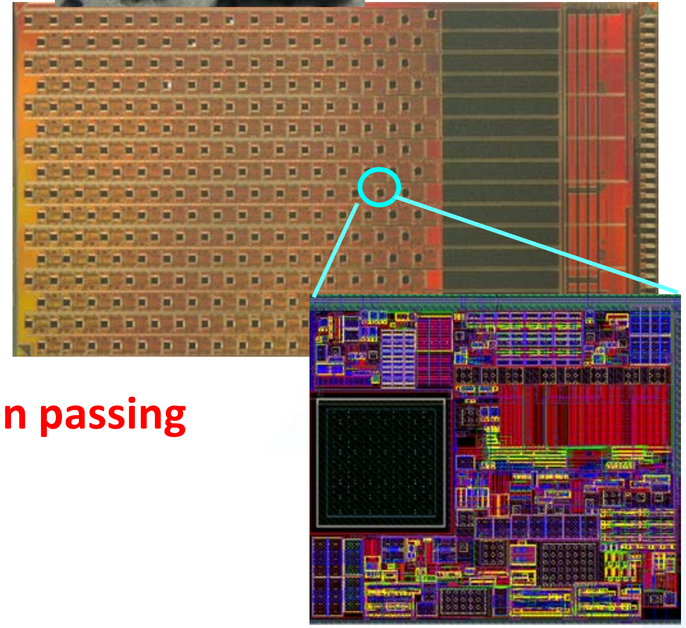
* Note that the output current is 150 mA and the load capacitance is 50 μF in all of the performance simulation in this table.



2-D ASIC Hi-Resolution X-ray Imager

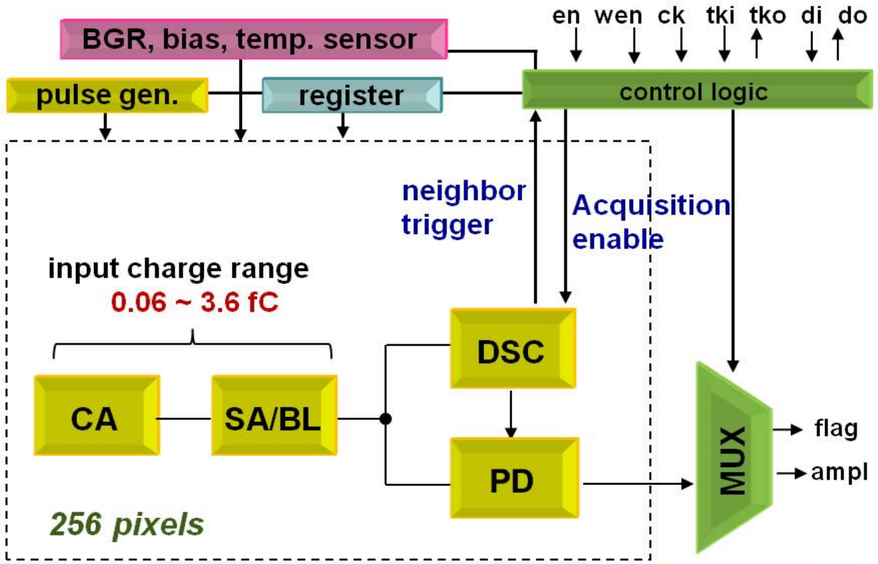
- ~700,000 transistors in CMOS 130nm technology (1.2 V supply)
- 256 hexagonal channels at 250 µm pitch
- 3-side abuttable, with 33 I/O pins only on the right side
- Each channel includes:
  - -low-noise charge amplifier (adjustable gain: 0.25, 0.5, 1 V/fC)
  - -shaper (adjustable peaking time: 125, 250, 500, and 1000 ns)
  - -baseline stabilizer
  - -discriminator and peak-detector
- ~0.6 mW/channel
- Simulated ENC: ~ 11 electrons (@ 60 fF det. cap. & 6pA leakage per pixel)

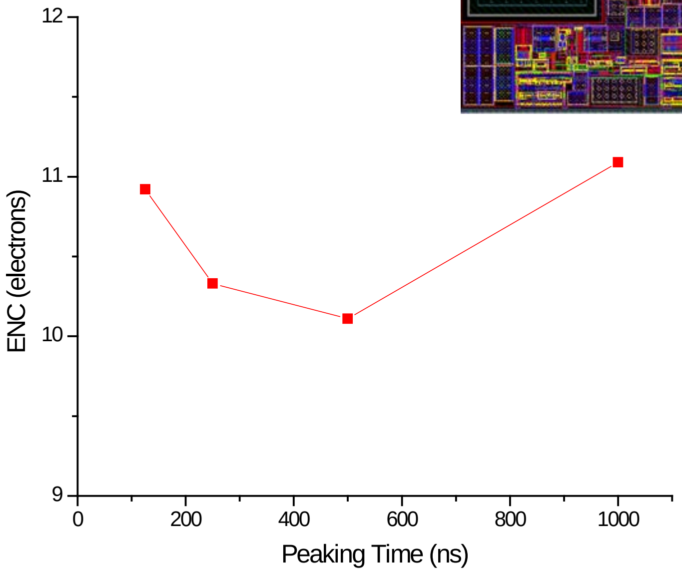




⇒Limited area for low-noise low-power readout chain

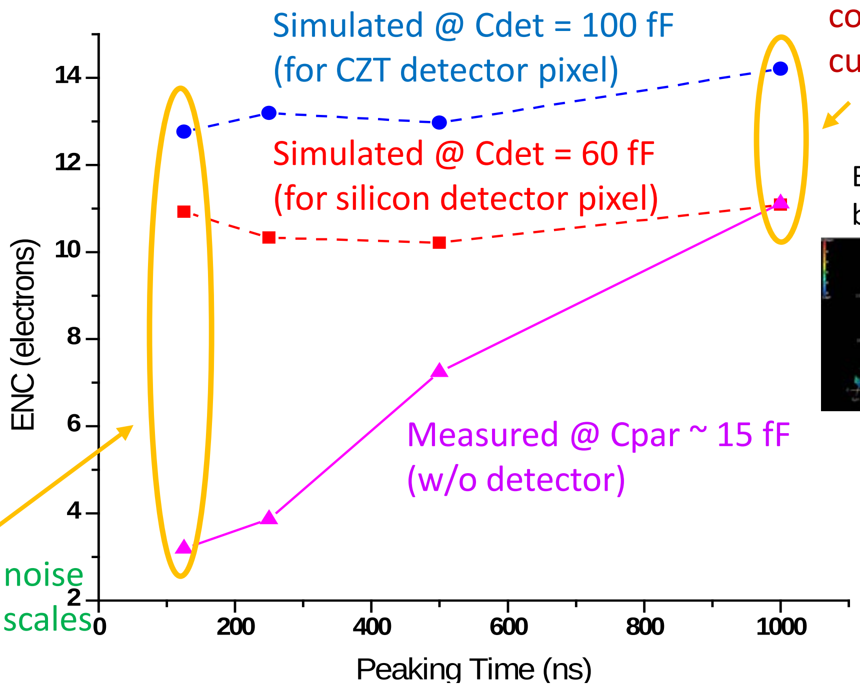
⇒No direct address control of each pixel, relying on token passing





[S. Li & G. De Geronimo, NSS 2017]

Simulated and Measured ENC versus Peaking Time

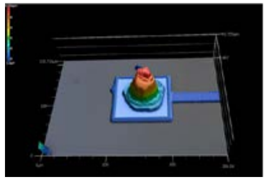


Higher measured parallel noise contribution from leakage current than simulated.

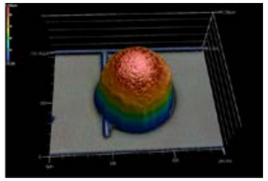
White series noise contribution scales with Cin

[Li & De Geronimo_NSS 2017]

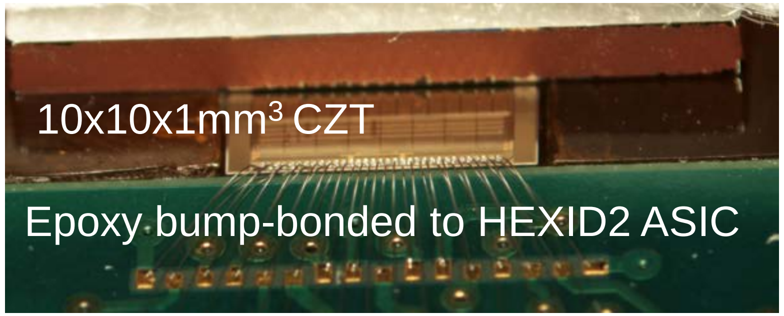
BNL gold-stud bump ~60 µm



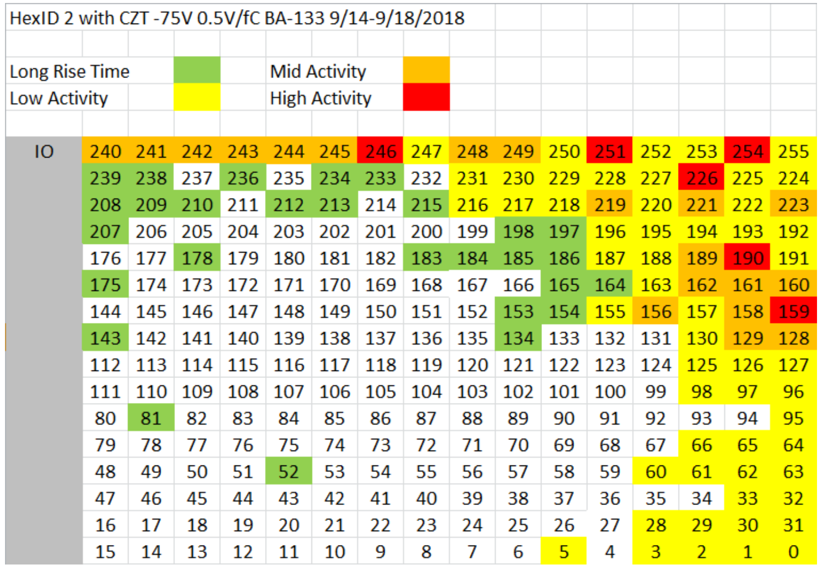
IBM bump ~100 µm




Si det. gold-stud bump-bonded to HEXID2 ASIC at BNL


10x10x1mm^3 CZT

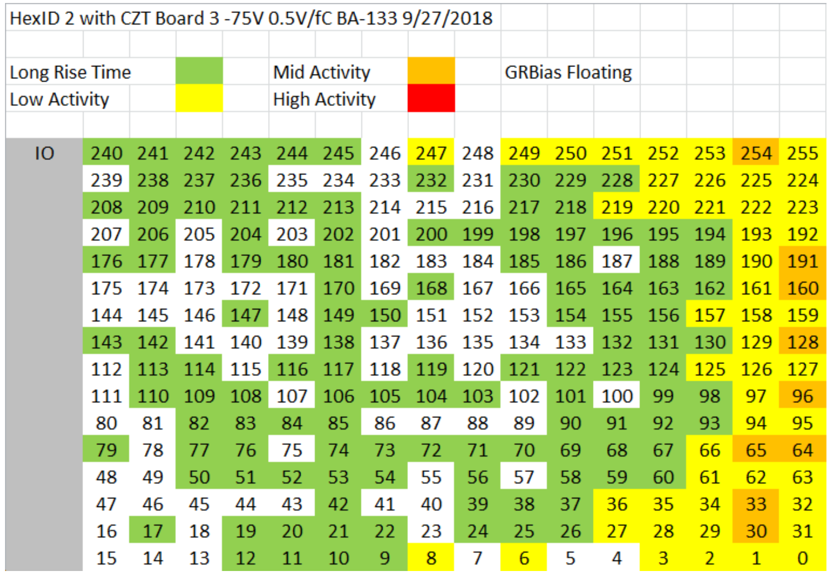
Epoxy bump-bonded to HEXID2 ASIC



HexID 2 with CZT -75V 0.5V/fC BA-133 9/14-9/18/2018

Long Rise Time 🟩 Mid Activity 🟧
Low Activity 🟨 High Activity 🟥

IO	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
	239	238	237	236	235	234	233	232	231	230	229	228	227	226	225	224
	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
	207	206	205	204	203	202	201	200	199	198	197	196	195	194	193	192
	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
	175	174	173	172	171	170	169	168	167	166	165	164	163	162	161	160
	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
	143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128
	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0



HexID 2 with CZT Board 3 -75V 0.5V/fC BA-133 9/27/2018

Long Rise Time 🟩 Mid Activity 🟧 GRBias Floating
Low Activity 🟨 High Activity 🟥

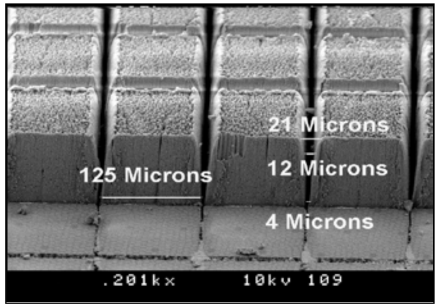
IO	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
	239	238	237	236	235	234	233	232	231	230	229	228	227	226	225	224
	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
	207	206	205	204	203	202	201	200	199	198	197	196	195	194	193	192
	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
	175	174	173	172	171	170	169	168	167	166	165	164	163	162	161	160
	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
	143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128
	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ASIC for Pixelated-Scintillator-Based X-Ray Detectors

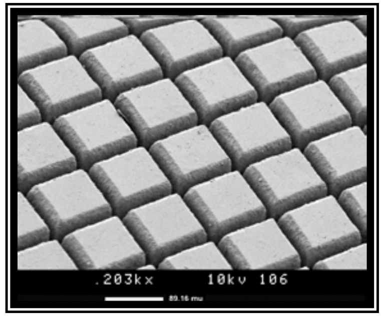
[Li & De Geronimo_NSS 2018]

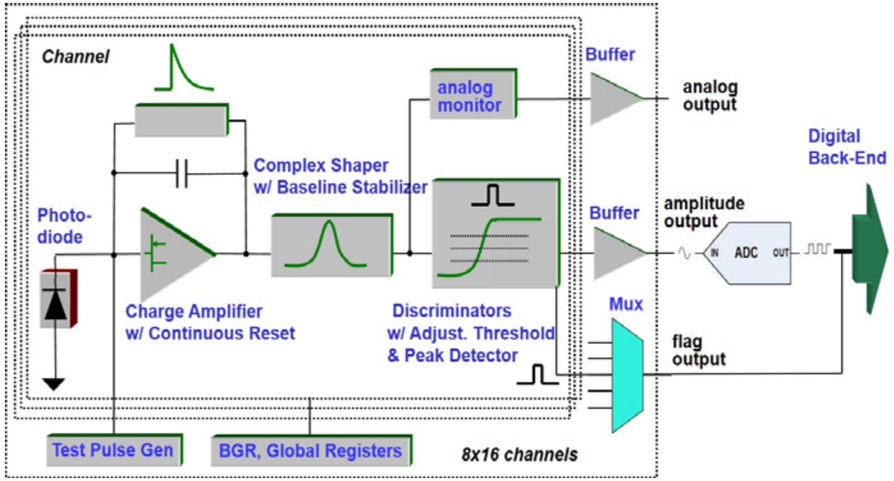
Pixelated Micro-Columnar Films Scintillator (RMD Inc.):

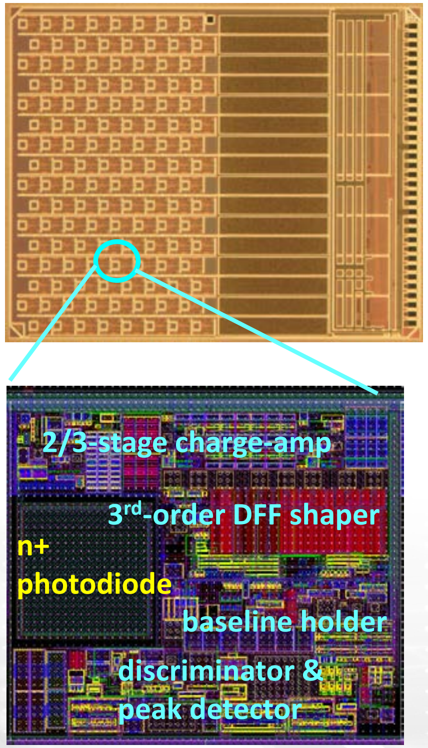
CsI:Tl:
125 µm pitch and 140 µm thick

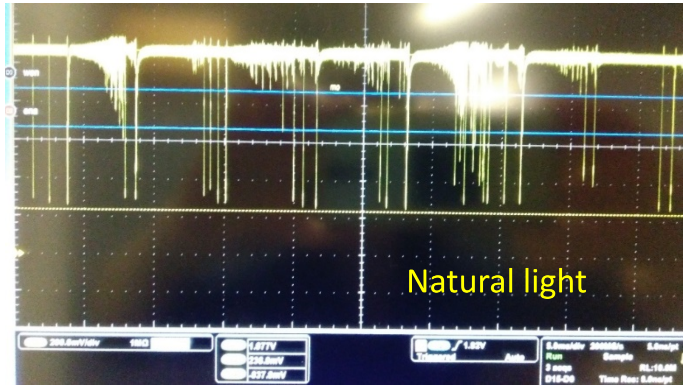


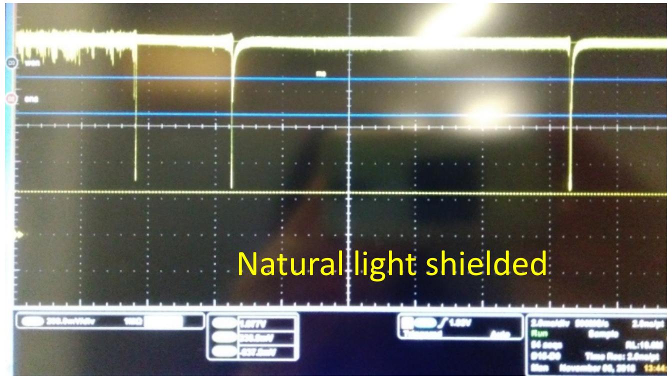
Lu_2O_3:Eu:
100 µm pitch and 1 mm thick

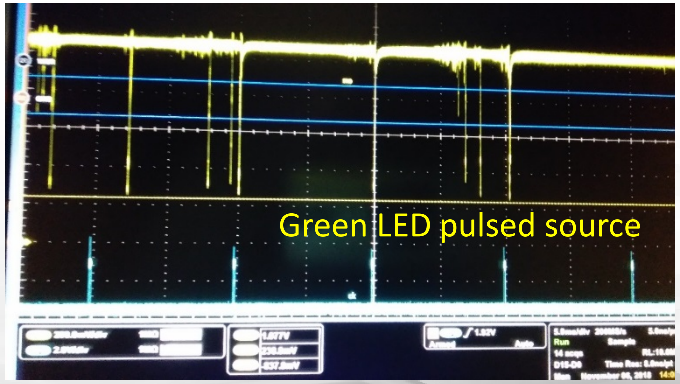


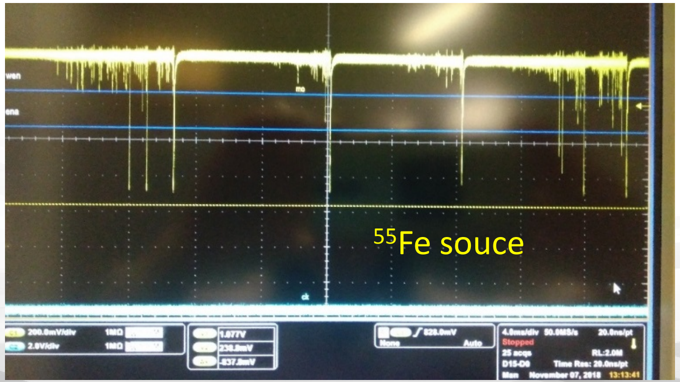




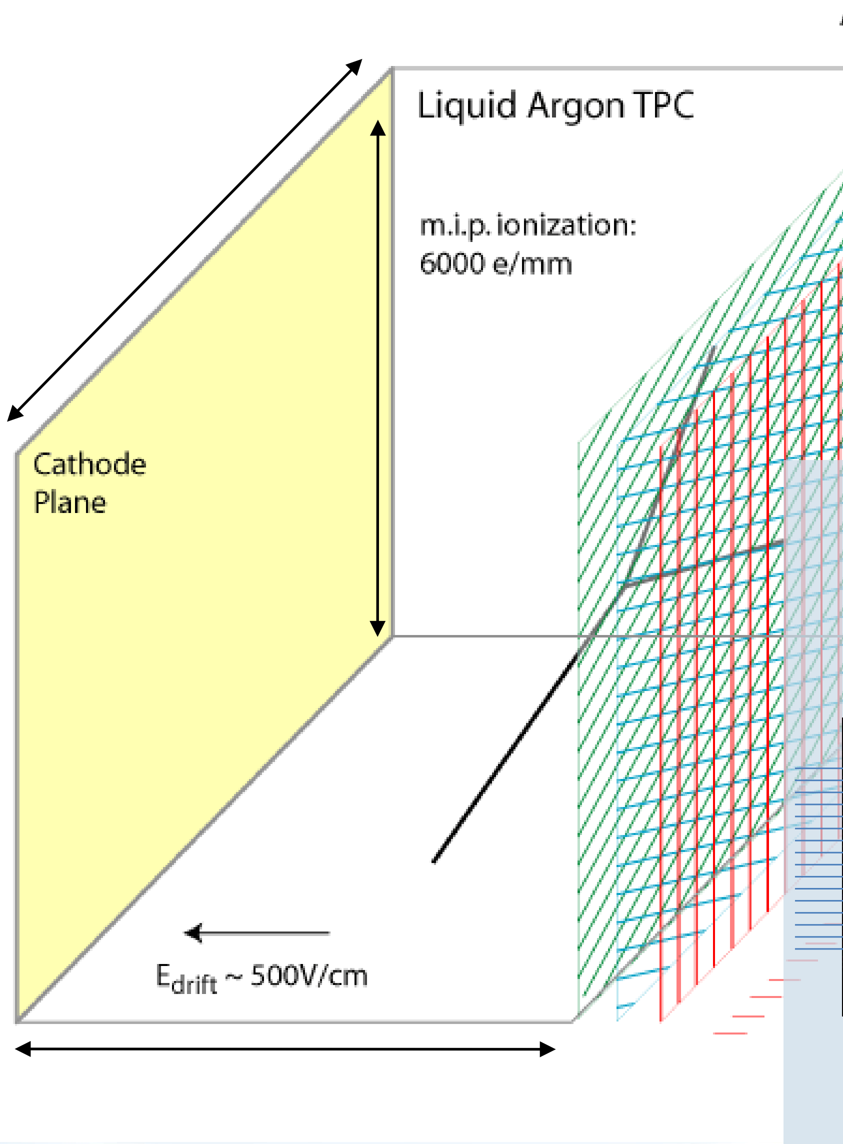








Cryogenic ASICs (μBooNE, ProtoDune, SBND, DUNE)



G. De Geronimo et al., IEEE TNS 58 2011

Up to 600,000 sensing wires

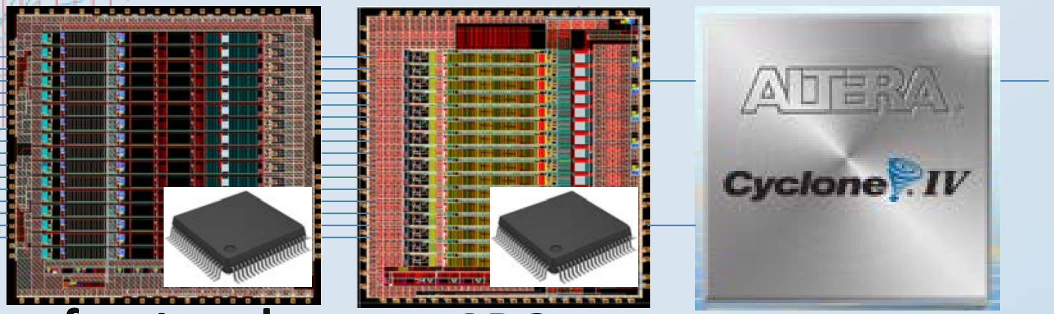
Low-noise and multiplexing

⇩

- **submerged in LAr (88K)**
- **lifetime > 30 years**

Cryogenic electronics

voltage regulation



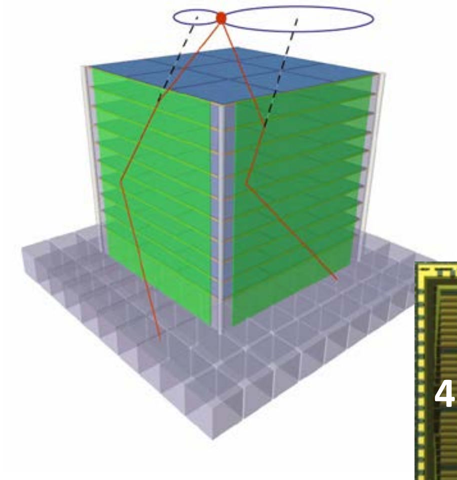
front-end **ADC** **multiplexing**

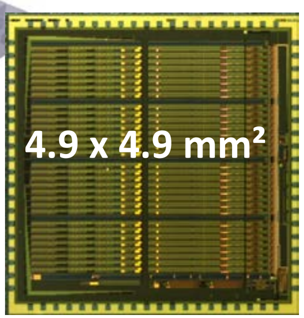
R&D on cryogenic characterization & lifetime

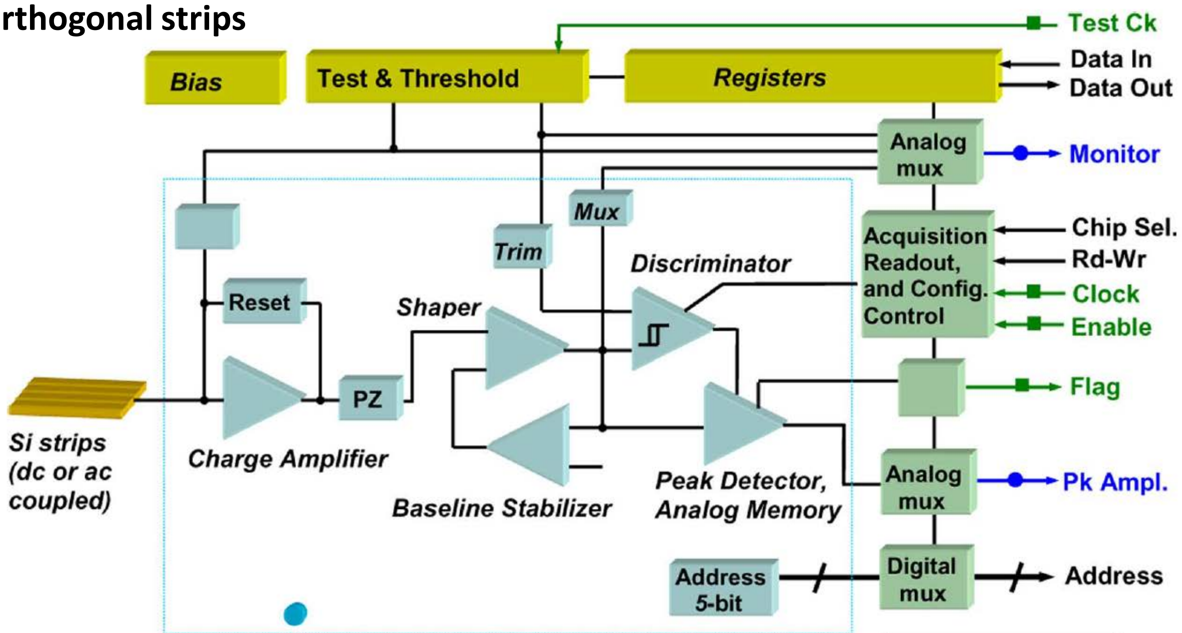
Compton Imager ASIC for NRL

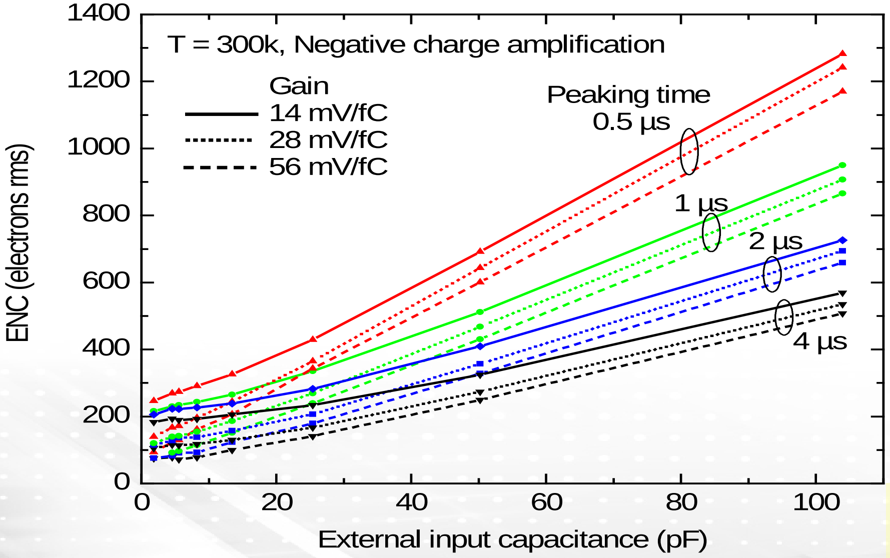
Layers of 1x1 m², 2 mm thick Si double-sided orthogonal strips

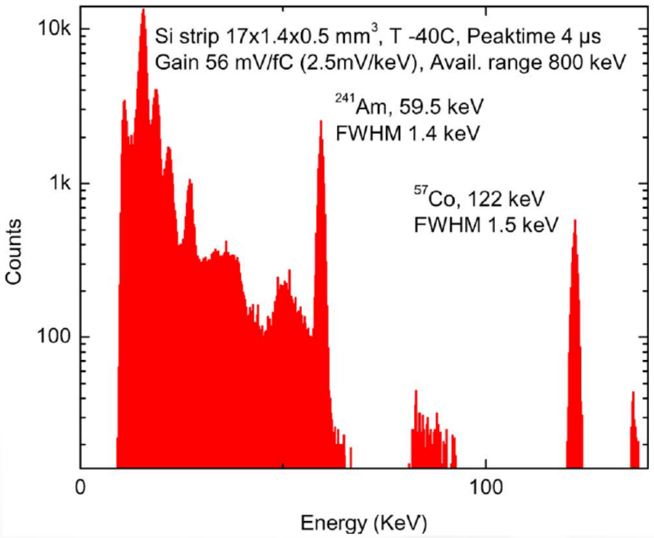
Total strip length 30 cm (≈ 30pF)











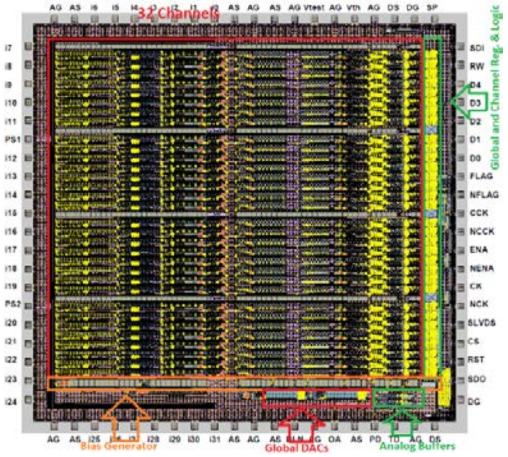
< 1.8 keV FWHM up to 800 keV

G. De Geronimo et al., TNS 55 (2008), collaboration with NRL

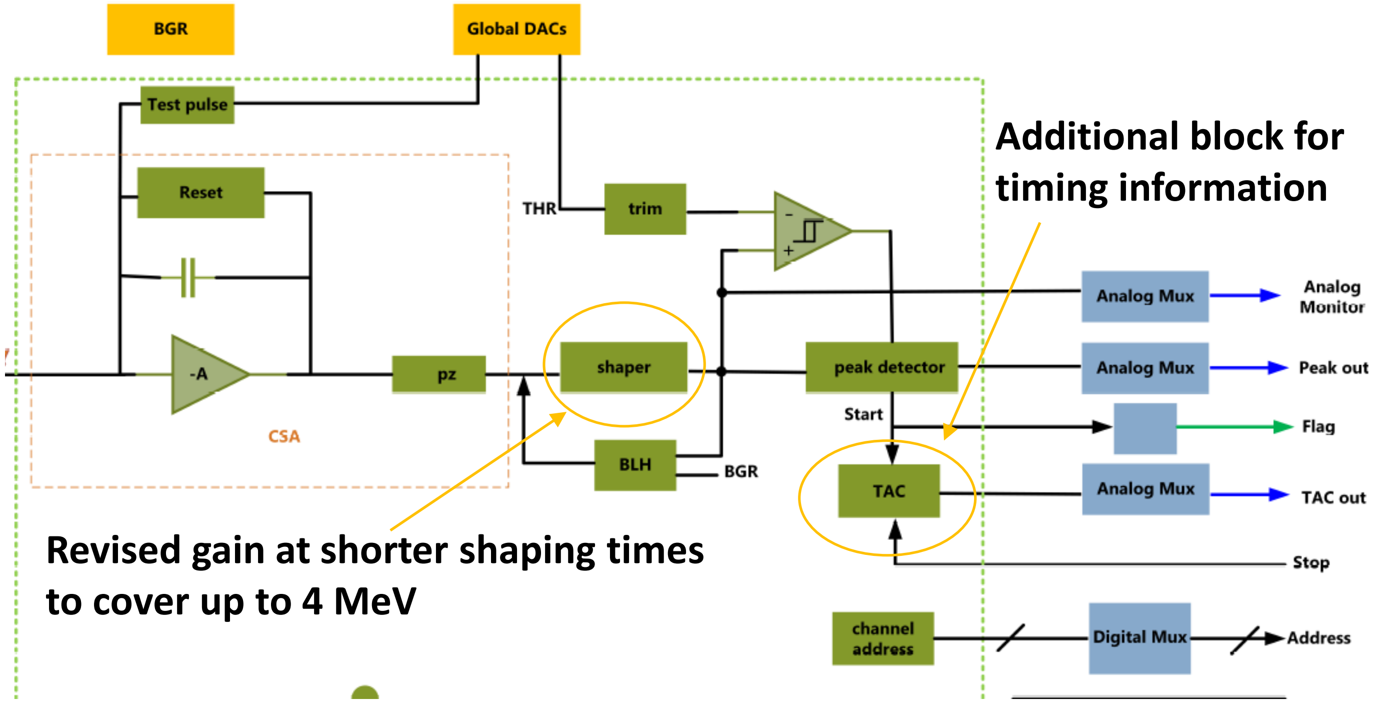
- *adopted by NASA/WUSL for CZT sensors for x-ray astrophysics*
- *adopted by NASA/SWRI for Heavy Ion Sensor (HIS) solar orbiter*
- *adopted by CERN for MicroMegas characterization*

Revised ASIC for HPGe Strip Detectors [by W. Hou & G. De Geronimo]

HPGe Strip Detectors to cover high energy range (up to 4 MeV) with timing resolution

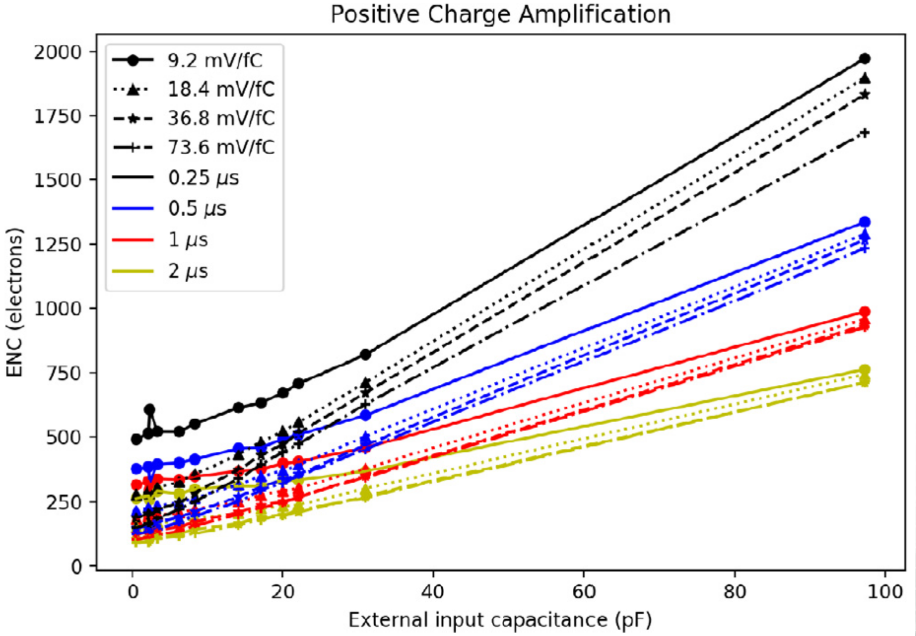


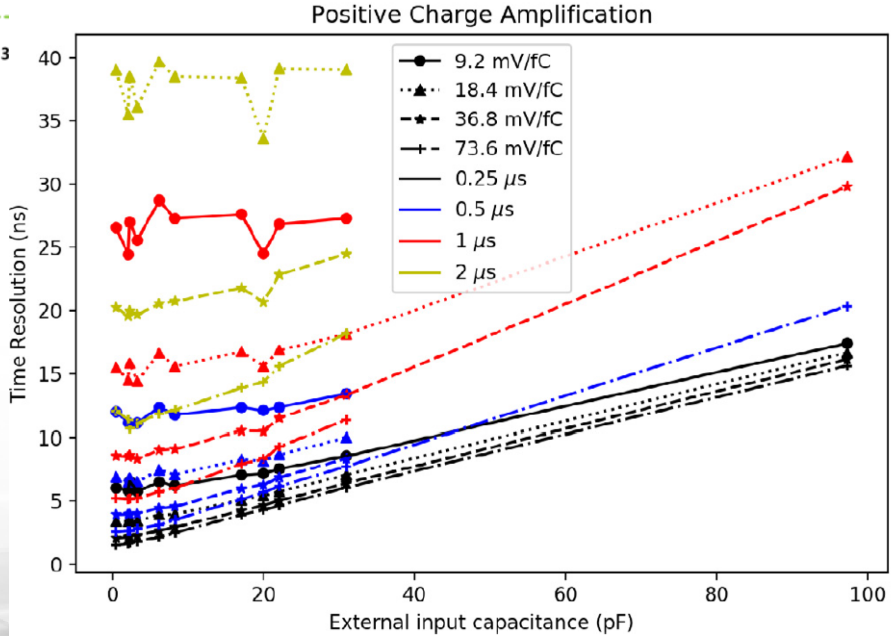
E. A. Wulf et al., NIMA (2018)



Additional block for timing information

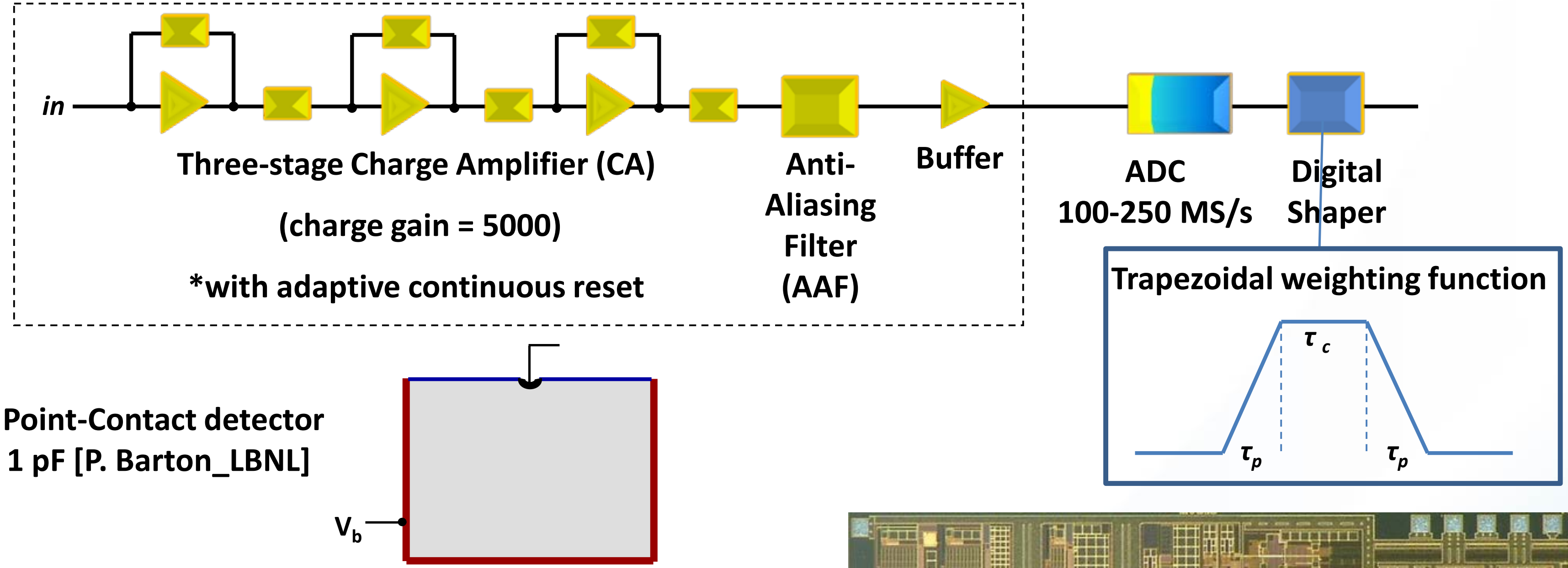
Revised gain at shorter shaping times to cover up to 4 MeV





Very Low Noise ASIC for Germanium Point-Contact Detector in LAr

- **Large gain** (~5000) of charge amplifier to lower noise contributions from later stages
- **Adaptive continuous reset** successfully avoid dead-time and switching noise in charge amplifier, and automatically adjusts to detector leakage current.
- **Large bandwidth** of anti-alias filter (AAF) to preserve 50ns pulse rise time



Three-stage Charge Amplifier (CA)

(charge gain = 5000)

***with adaptive continuous reset**

Anti-Aliasing Filter (AAF)

Buffer

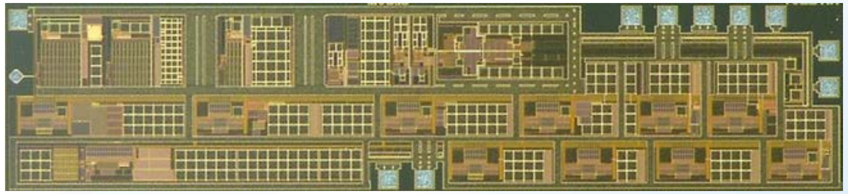
ADC 100-250 MS/s

Digital Shaper

Trapezoidal weighting function

Ge Point-Contact detector
C < 1 pF [P. Barton_LBNL]

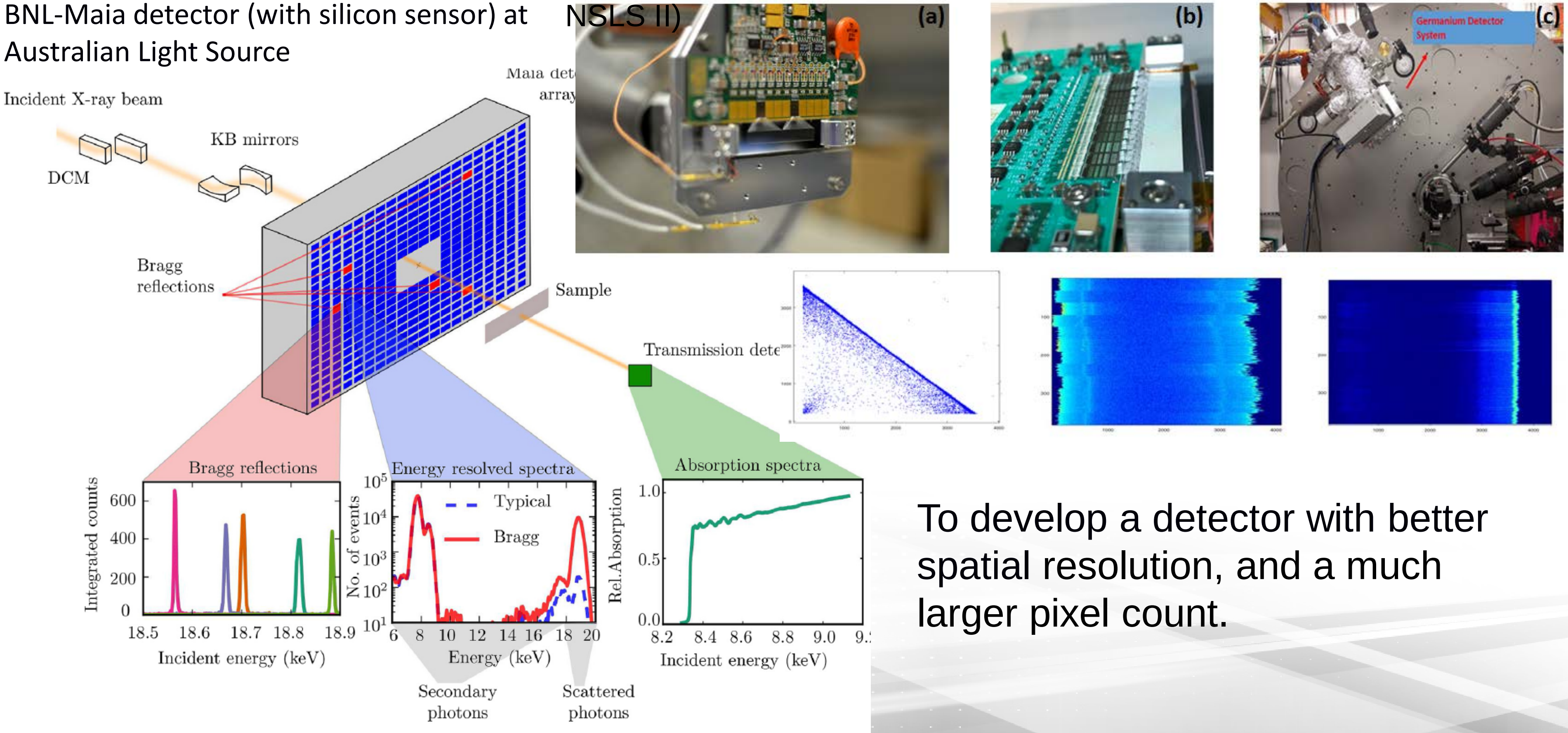
Cdet (fF)	ENC_total (e-)	ENC _m1&lk (e-)	ENC_m1-1/f (e-)
200 (possible load)	5.3	4.8 (~82%)	4.5 (~71%)
100 (target load)	**3.9**	3.5 (~78%)	3.2 (~65%)
1 (**without load)**	**2.6**	2.1 (~68%)	1.9 (~48%)



[S. Li & G. De Geronimo, IEEE NSS 2017]

Germanium Hyperspectral Imaging Detector with Cold Electronics

- Develop a detector capable of recording the position and energy of a detected x-ray, with energies from a few keV to over 100keV.
- Need to design and characterize readout electronics capable of operation at a temperature of around 100K (-200C!) for germanium to provide excellent energy resolution. The goal of this proposal is to fabricate a monolithic Ge pixel array sensor and also develop a prototype cold ASIC.



BNL-Maia detector (with silicon sensor) at Australian Light Source

Ge strip detector system at the X-ray powder diffraction beamline (BNL NSLS II)

To develop a detector with better spatial resolution, and a much larger pixel count.

2/26/2019