Front-end electronics for EIC - PID

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Near-term and next-generation Readout

- In order to permit development of detector prototypes, strategy has been to use existing electronics, while in parallel working toward readout suitable to the final requirements
- Building upon lessons learned from the development of photosensor readout for the Belle II upgrade (picosecond timing, low-cost, large muon system) and CTA SCT cameras (\$1.40/channel)
- ASIC development important, but firmware and support have been the most critical issues
- UH has partnered with Nalu Scientific team to develop commercial variants (with functional extensions), and to provide engineering support
- Developing front-end readout compatible of numerous back-end control and acquisition options

Electronics – Specifics

Requirements

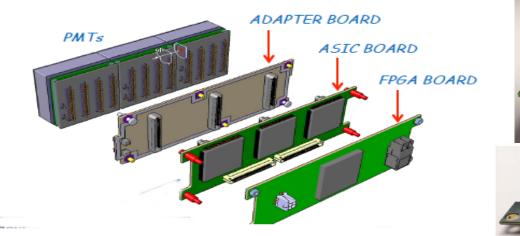
- Need to read out several photosensors (MaPMTs, MCP-PMTs, and SiPMs) with similar sensor and pixel size (16x16 array of 3 mm pixels)
 - DIRC also requires good timing (<100 ps)
- Goal is to have common front end electronics with good timing that can be used for all sensors and detectors (mRICH, dRICH, DIRC)

Implementation

- The Maroc-based CLAS12 front end has been adapted to 3 mm pixels and already used for the first two mRICH beam tests (next slide)
 - Maroc is not a universal long-term solution due to its poor timing
- After initial studies using TARGETX chips, the front end have now switched to the SiREAD ASIC. This can be used for all EIC PID detectors and sensors.

Electronics – Maroc (used for previous mRICH beam tests)

CLAS12 RICH electronics





SSP Fiber-Optic DAQ

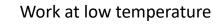


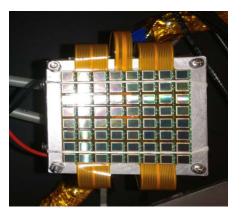
FPGA Board

SiPMs

- Mass production technology
- Photon counting
- Excellent time resolution
- Compatible with magnetic field
- ✓ High dark rate
- Low radiation tolerance







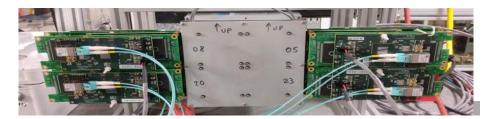
Readout Electronics Development

Goal:

- Develop an integrated suite of readout electronics for the different photosensors used for all the Cherenkov detectors and prototypes.
- Provide a reference readout system for prototypes performance assessment
- Developed a generic DAQ system compatible with the Consortium needs
- Test applications with various sensors (including SiPMs)

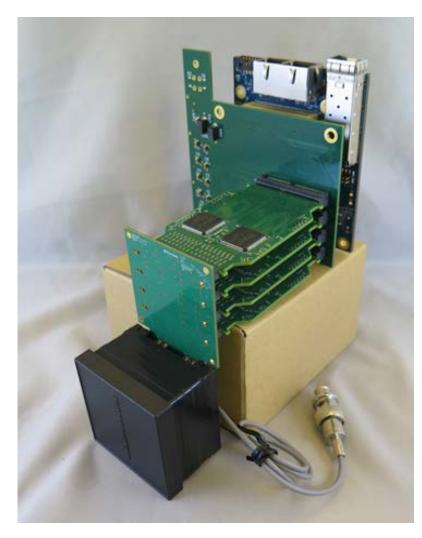
FY 20 Activities:

- Moving from the TARGETX (Belle-II) to the new SiREAD chip
- Development of pulsed laser test benches for detailed characterization









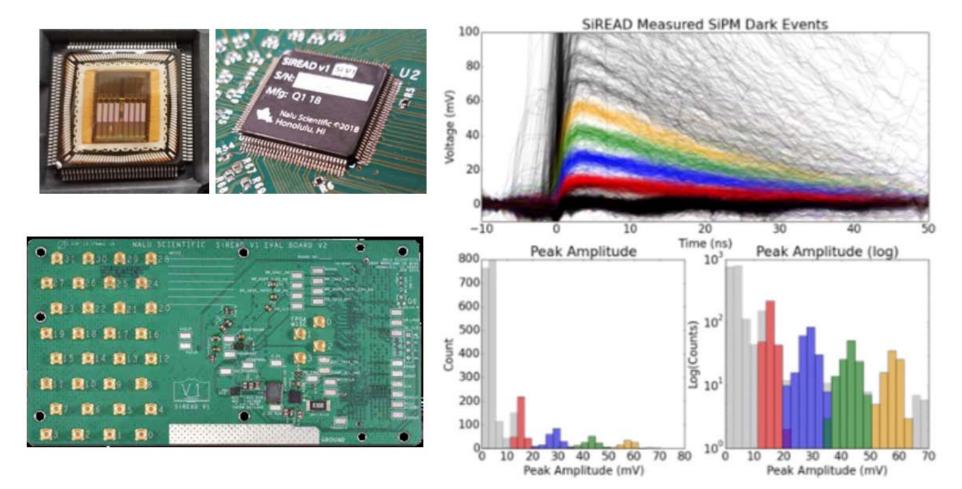
Photograph of the first generation of 256-anode 2" PMT readout for use with mRICH prototype in the Fermilab beam test facility.

MA PMT Readout



Photograph of the 64 channel SiREAD based (2x SiREAD rev.1) readout card as a building block for the 256 MA-PMT readout.

SiREAD Performance



 Micrograph of the fabricated prototype SiREAD (top left). Prototype SiREAD on the evaluation PCB (top middle). Superimposed dark count waveforms recorded from a SiPM using the SiREAD operating at 1 Gsa/s (right). High channel count evaluation PCB for SiREAD with 32 dedicated MMCX connectors (bottom left).

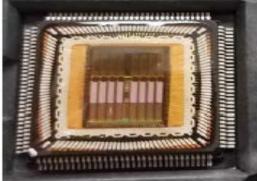
Nalu's SoC-ASIC Portfolio

Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	32k	8	35	Rev 2 avail
SIREAD	1-3	0.6	4k	64	80-120	Rev 1 avail
AARDVARC	6-10	2.5	32k	4-8	4-8	Rev 2 avail
AODS	1-2	1	8k	1-4	100-200	Nov 2019

- ASoC: Analog to digital converter System-on-Chip
 - Rev 1 under test Funded Phase II Eval card available
- SiREAD: SiPM specialized readout chip with bias and control
 - Rev 1 under test
- AARDVARC: Variable rate readout chip for fast timing and low deadtime
 - Rev 1 under test Funded Phase II

All chips, are designed with commercial grade tools and licenses and can be sold once commercialized.





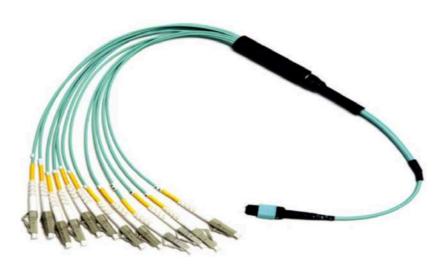




HW/FW Development

- Need for robust firmware development (lesson from Belle II)
- Nalu Scientific team provides in-house FW development, with institutional memory
- UH provides comprehensive bench, environment and picosecond laser/photosensor testing
- UH hiring new post doc (December timescale)
- Immediate push is to get SiREAD version of 256 anode PMT readout working; evaluate performance; design more compact version

Back-end Electronics (INFN/JLab)



Optical ethernet (2.5 Gbps)

Small setups: TCP/IP Optical bridge / PC Desktop

Full experiment: SSP protocol SSP board / VSX crate

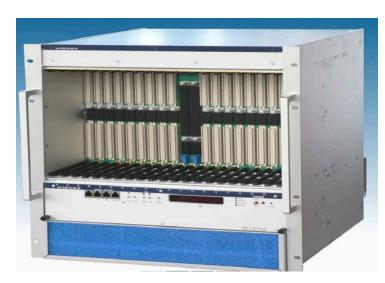
Next: SSP + Ethernet Switches

Optical bridge / PC Desktop Few FPGA units ~ 500 channels





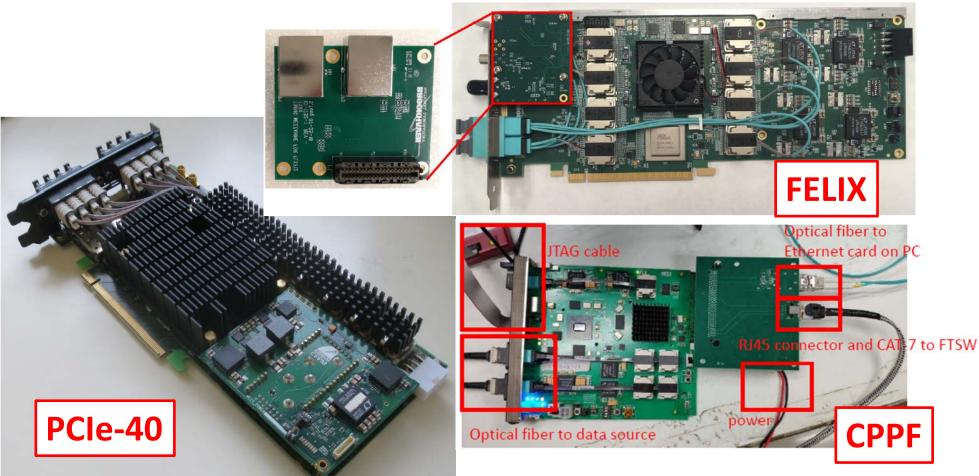
SSP board / VSX crate ~ 50 k channels

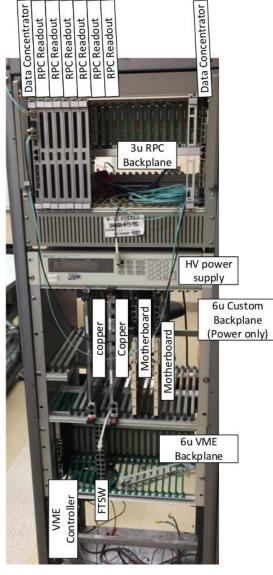




Backend Control/Readout

- Current: JLAB and Belle2link readout as baseline
- Experience with Bellell DAQ upgrade





R&D Requirements to achieve TDR Readiness by 2023

- FY2020: complete SiREAD-based MA-PMT readout (firmware)
- FY2021-22: Readouts for prototype beamtests
 - 3 permanent development stations (1 per detector) with a full readout chain for at least 1 sensor
 - > 1 set-up to read out up to 12 sensors (256 channels each) for (DIRC) test beams
- FY2023: DAQ readout demonstrator (with proposed back-end)
- One full-time DAQ/readout Postdoc
- Yearly contract with Nalu Scientific for engineering support

R&D Resource Requirements

Front-end

Item	FY2020	FY2021	FY2022	FY2023	Total	Comment
DAQ/readout postdoc	25	65	67	68	225	Projected salary escalation (partial in FY2020)
Hardware development	10	35	105	25	175	Prototypes in 2021, 2023; 2022 large build
Testing (student) labor			55		55	For production build for beamtests
Nalu subcontract		50	80	50	180	Firmware and engineering services
Beamtest support			30		30	Including DAQ team travel
Totals	35	150	337	143	665	

Back-end

FY	20- 1	20- 2	20- 3	20- 4	21- 1	21- 2	21- 3	21- 4	22- 1	22- 2	22- 3	22- 4	23- 1	23- 2	23- 3	23- 4	Tot	INFN
Post-doc (Back-end)				20				50				50		30			150	
Travel (Test-beam)				4			4	6			6	4				4	28	
Back-end				10				50				30				20	110	
Total personal				24				60				60				34	178	
Total material				10				50				30				20	110	