Front-end electronics for EIC - PID

Marco Contalbrigo – INFN Ferrara
Isar Mostafanezhad - Nalu Scientific
Gary Varner – University of Hawaii
Near-term and next-generation Readout

• In order to permit development of detector prototypes, strategy has been to use existing electronics, while in parallel working toward readout suitable to the final requirements

• Building upon lessons learned from the development of photosensor readout for the Belle II upgrade (picosecond timing, low-cost, large muon system) and CTA SCT cameras ($1.40/channel)

• ASIC development important, but firmware and support have been the most critical issues

• UH has partnered with Nalu Scientific team to develop commercial variants (with functional extensions), and to provide engineering support

• Developing front-end readout compatible of numerous back-end control and acquisition options
Electronics – Specifics

Requirements

- Need to read out several photosensors (MaPMTs, MCP-PMTs, and SiPMs) with similar sensor and pixel size (16x16 array of 3 mm pixels)
  - DIRC also requires good timing (<100 ps)
- Goal is to have common front end electronics with good timing that can be used for all sensors and detectors (mRICH, dRICH, DIRC)

Implementation

- The Maroc-based CLAS12 front end has been adapted to 3 mm pixels and already used for the first two mRICH beam tests (next slide)
  - Maroc is not a universal long-term solution due to its poor timing
- After initial studies using TARGETX chips, the front end have now switched to the SiREAD ASIC. This can be used for all EIC PID detectors and sensors.
Electronics – Maroc (used for previous mRICH beam tests)

CLAS12 RICH electronics

SiPMs

✓ Mass production technology
✓ Photon counting
✓ Excellent time resolution
✓ Compatible with magnetic field
✓ High dark rate
✓ Low radiation tolerance

Work at low temperature
Readout Electronics Development

**Goal:**

- Develop an integrated suite of readout electronics for the different photosensors used for all the Cherenkov detectors and prototypes.
- Provide a reference readout system for prototypes performance assessment
- Developed a generic DAQ system compatible with the Consortium needs
- Test applications with various sensors (including SiPMs)

**FY 20 Activities:**

- Moving from the TARGETX (Belle-II) to the new SiREAD chip
- Development of pulsed laser test benches for detailed characterization
MA PMT Readout

Photograph of the first generation of 256-anode 2" PMT readout for use with mRICH prototype in the Fermilab beam test facility.

Photograph of the 64 channel SiREAD based (2x SiREAD rev.1) readout card as a building block for the 256 MA-PMT readout.
SiREAD Performance

• Micrograph of the fabricated prototype SiREAD (top left). Prototype SiREAD on the evaluation PCB (top middle). Superimposed dark count waveforms recorded from a SiPM using the SiREAD operating at 1 Gsa/s (right). High channel count evaluation PCB for SiREAD with 32 dedicated MMCX connectors (bottom left).
Nalu’s SoC-ASIC Portfolio

<table>
<thead>
<tr>
<th>Project</th>
<th>Sampling Frequency (GHz)</th>
<th>Input BW (GHz)</th>
<th>Buffer Length (Samples)</th>
<th>Number of Channels</th>
<th>Timing Resolution (ps)</th>
<th>Available Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASoC</td>
<td>3.5</td>
<td>0.8</td>
<td>32k</td>
<td>8</td>
<td>35</td>
<td>Rev 2 avail</td>
</tr>
<tr>
<td>SiREAD</td>
<td>1-3</td>
<td>0.6</td>
<td>4k</td>
<td>64</td>
<td>80-120</td>
<td>Rev 1 avail</td>
</tr>
<tr>
<td>AARDVARC</td>
<td>6-10</td>
<td>2.5</td>
<td>32k</td>
<td>4-8</td>
<td>4-8</td>
<td>Rev 2 avail</td>
</tr>
<tr>
<td>AODS</td>
<td>1-2</td>
<td>1</td>
<td>8k</td>
<td>1-4</td>
<td>100-200</td>
<td>Nov 2019</td>
</tr>
</tbody>
</table>

- **ASoC**: Analog to digital converter System-on-Chip
  - Rev 1 under test – **Funded Phase II - Eval card available**
- **SiREAD**: SiPM specialized readout chip with bias and control
  - Rev 1 under test
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
  - Rev 1 under test – **Funded Phase II**

All chips are designed with commercial grade tools and licenses and can be sold once commercialized.
HW/FW Development

• Need for robust firmware development (lesson from Belle II)

• Nalu Scientific team provides in-house FW development, with institutional memory

• UH provides comprehensive bench, environment and picosecond laser/photosensor testing

• UH hiring new post doc (December timescale)

• Immediate push is to get SiREAD version of 256 anode PMT readout working; evaluate performance; design more compact version
Optical ethernet (2.5 Gbps)

Small setups:
TCP/IP
Optical bridge / PC Desktop

Full experiment:
SSP protocol
SSP board / VSX crate

Next:
SSP + Ethernet Switches

Optical bridge / PC Desktop
Few FPGA units ~ 500 channels

SSP board / VSX crate
~ 50 k channels
Backend Control/Readout

• Current: JLAB and BelleII link readout as baseline
• Experience with BelleII DAQ upgrade
R&D Requirements to achieve TDR Readiness by 2023

• FY2020: complete SiREAD-based MA-PMT readout (firmware)
• FY2021-22: Readouts for prototype beamtests
  ➢ 3 permanent development stations (1 per detector) with a full readout chain for at least 1 sensor
  ➢ 1 set-up to read out up to 12 sensors (256 channels each) for (DIRC) test beams
• FY2023: DAQ readout demonstrator (with proposed back-end)
• One full-time DAQ/readout Postdoc
• Yearly contract with Nalu Scientific for engineering support
# R&D Resource Requirements

## Front-end

<table>
<thead>
<tr>
<th>Item</th>
<th>FY2020</th>
<th>FY2021</th>
<th>FY2022</th>
<th>FY2023</th>
<th>Total</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAQ/readout postdoc</td>
<td>25</td>
<td>65</td>
<td>67</td>
<td>68</td>
<td>225</td>
<td>Projected salary escalation (partial in FY2020)</td>
</tr>
<tr>
<td>Hardware development</td>
<td>10</td>
<td>35</td>
<td>105</td>
<td>25</td>
<td>175</td>
<td>Prototypes in 2021, 2023; 2022 large build</td>
</tr>
<tr>
<td>Testing (student) labor</td>
<td></td>
<td>55</td>
<td></td>
<td>55</td>
<td></td>
<td>For production build for beamtests</td>
</tr>
<tr>
<td>Nalu subcontract</td>
<td>50</td>
<td>80</td>
<td>50</td>
<td></td>
<td>180</td>
<td>Firmware and engineering services</td>
</tr>
<tr>
<td>Beamtest support</td>
<td></td>
<td>30</td>
<td></td>
<td>30</td>
<td></td>
<td>Including DAQ team travel</td>
</tr>
<tr>
<td>Totals</td>
<td>35</td>
<td>150</td>
<td>337</td>
<td>143</td>
<td>665</td>
<td></td>
</tr>
</tbody>
</table>

## Back-end

<table>
<thead>
<tr>
<th>FY</th>
<th>20-1</th>
<th>20-2</th>
<th>20-3</th>
<th>21-1</th>
<th>21-2</th>
<th>21-3</th>
<th>22-1</th>
<th>22-2</th>
<th>22-3</th>
<th>23-1</th>
<th>23-2</th>
<th>23-3</th>
<th>23-4</th>
<th>Tot</th>
<th>INFN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Post-doc (Back-end)</td>
<td>20</td>
<td></td>
<td></td>
<td>50</td>
<td></td>
<td>50</td>
<td></td>
<td>50</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>Travel (Test-beam)</td>
<td>4</td>
<td></td>
<td></td>
<td>4</td>
<td></td>
<td>6</td>
<td></td>
<td>6</td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td>4</td>
<td>28</td>
</tr>
<tr>
<td>Back-end</td>
<td>10</td>
<td></td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>110</td>
</tr>
<tr>
<td>Total personal</td>
<td></td>
<td>24</td>
<td></td>
<td>60</td>
<td></td>
<td>60</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>34</td>
<td>178</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total material</td>
<td></td>
<td>10</td>
<td></td>
<td>50</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>110</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>