Contribution ID: **270** Type: **Talk**

Staggered Dslash Performance on Intel Xeon Phi Architecture

Monday, 23 June 2014 18:10 (20 minutes)

The conjugate gradient algorithm is among the most essential and time consuming parts of lattice calculations with staggered quarks. We test the performance of dslash, the key step in the CG algorithm, on the Intel Xeon Phi, also known as the many integrated cores (MIC) architecture, with different parallelization strategies using MPI,OpenMP, and the vector processing units (VPUs).

Primary author: Ms LI, Ruizi (Indiana University)

Co-author: Prof. GOTTLIEB, Steven (Indiana University)

Presenter: Ms LI, Ruizi (Indiana University)

Session Classification: Algorithms and Machines

Track Classification: Algorithms and Machines