UNIVERSITY OF BIRMINGHAM

EIC Silicon Vertex and Tracking: Technology survey

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on behalf of eRD18 (University of Birmingham), eRD16 (LBNL);

with inputs from RAL CMOS sensor group, BNL Instrumentation Division

1st EIC Yellow Report Workshop, 19 -21 March 2020

Outline

- **EIC Silicon Vertex and Tracking Detector**
- Survey of silicon technology options
- Selected technologies
  - Depleted MAPS
  - 65 nm MAPS
- Conclusion

Introduction

- The results presented in this talk are based on the work carried out in the past four years by eRD18 and eRD16 with continuous support, review and feedback by the DOE's nationally administered EIC detector R&D program
  - Work has covered over the years technology surveys, technology evaluation with testing of existing prototypes, and detector layout simulations
  - The EIC detector R&D committee formed by experts in different detector technologies provided peer-reviewed assessment of the work every six months
  - https://wiki.bnl.gov/conferences/index.php/EIC_R%25D

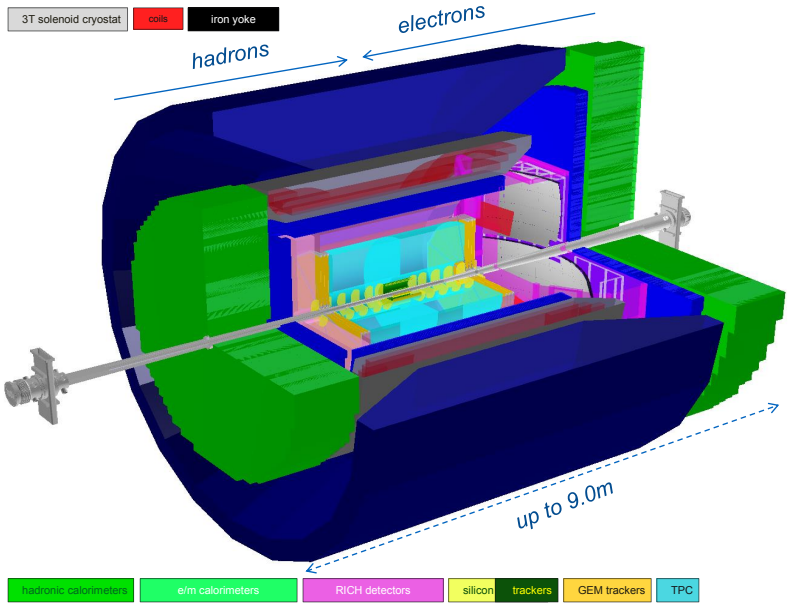
- Inputs to this talk are also provided by the EIC Detector Requirements and R&D Handbook

EIC Tracking Detector

- All EIC detector concepts proposed so far are equipped with Si vertex and tracking detectors in central and forward regions
  - Surrounded by a tracker made of gaseous detectors (see Kondo's talk)

Example: BeAST detector Si vtx & tracking
Based on ALICE ITS upgrade
2 inner + 2 outer barrel layers
2 x 7 disks
20 μm pixel pitch
0.3% X/X_0 per layer

A. Kiselev, EIC UG meeting 2016, EIC R&D meeting 2016, EIC tracking workshop 2018



- An all-silicon tracker concepts is also considered as an option to design a more compact tracking detector

EIC Silicon Vertex and Tracking Detector

- A silicon vertex and tracking detector at the EIC has to fulfil three tasks (see EIC Detector Requirements and R&D Handbook)
  - Determine primary vertices with high precision
  - Allow the measurement of secondary vertices for heavy-flavor decays
  - Low-pT tracking

- Fulfilling these tasks defines two fundamental requirements for the selection of the technology: high granularity and low material budget
  - Spatial resolution = ~5 µm
  - Material budget = < 0.3% X/X0 per layer

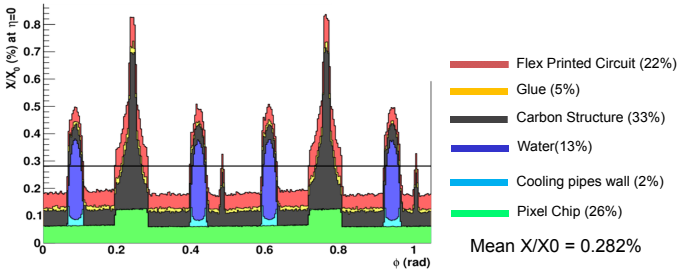
(confirmed in simulations by eRD16 and eRD18)

- Consider also readout requirements for the EIC
  - 50 – 500 kHz interaction frequency → integration time down to 2 µs
  - 112.6 MHz bunch-crossing frequency → < 9 ns time resolution (optional)

Low material budget = low power

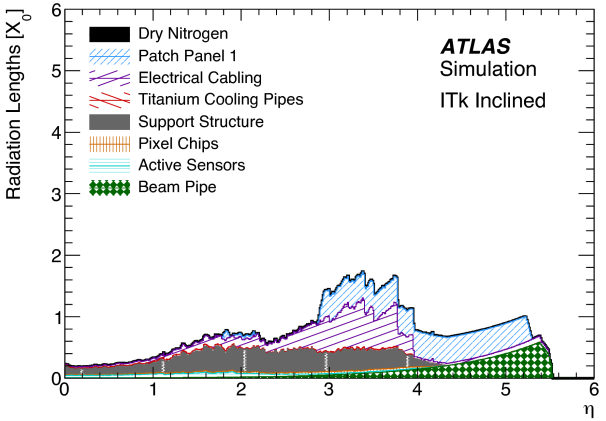
- The material budget of silicon vertex and tracking detectors is dominated by support structures, cooling and services, not silicon
- The detector feature that needs to be optimised for low material budget is the power consumption
- A low power front-end chip requires a low sensor capacitance

ALICE ITS inner layers



J. Phys. G: Nucl. Part. Phys. 41 (2014) 087002

ATLAS ITK



https://cds.cern.ch/record/2257755?ln=en

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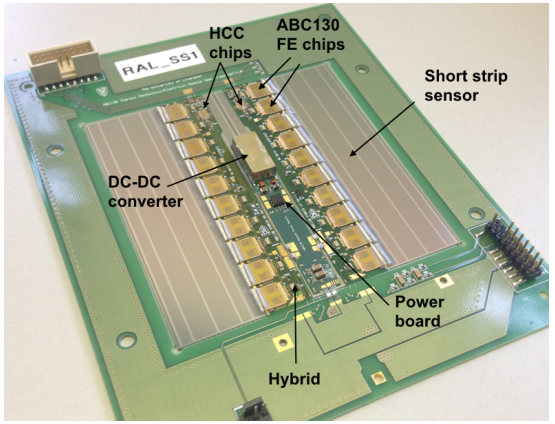
Strip detectors and hybrid pixels

https://cds.cern.ch/record/2257755?ln=en
https://cds.cern.ch/record/2285585/

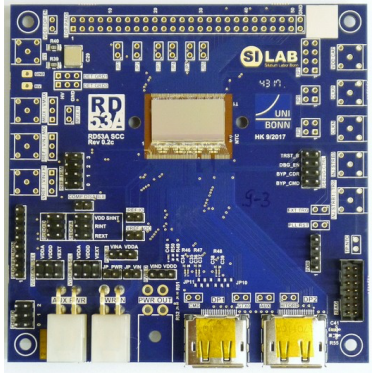
ATLAS ITk strip module



- Technologies designed for high radiation levels (1-10e15 1 MeV n_{eq}/cm^2, 50 – 500 Mrad) and particle rates (> 1 MHz/mm^2)
  - Used by vertex and tracking detectors of ATLAS and CMS at the LHC and upgrades

- Latest developments for HL-LHC have much improved granularity and material budget over earlier generations, but…
  - Pixel pitch 50x50, 25x100 μm^2 (limited by bump bonding technology)
  - Material budget < 2% X/X_0
  - Large sensor capacitance limits low power development even when relaxing radiation and rate requirements

RD53 chip



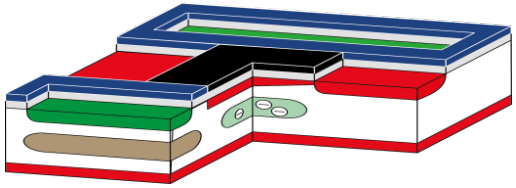
https://www.hep1.physik.uni-bonn.de/research/

These technologies are not suitable for the EIC as they cannot provide the required fine granularity and low material budget

DEPFET sensor

J. Ninkovic,
https://indico.cern.ch/event/722363/contributions/3031258/

- Concept: sensor with integrated first stage amplification



Thin & small pixel: vertex, low E electron detectors (TEM)

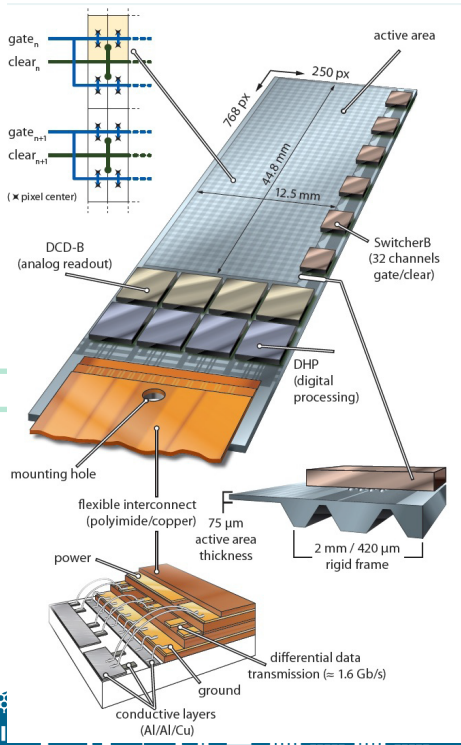
pixel size: 20μm…75μm
read out time per row: 25ns-100ns
Noise: ≈100 el ENC
thin detectors: 30μm…75μm → still large signal: 40nA/μm for MIP

- Example: Belle-II vertex detector, PXD
  - Readout chips on sensor side and end of stave
  - Rolling shutter readout architecture

Requirements:

• Single point resolution	**~10 μm**
• Radiation	**~20 Mrad (10 years)**
• Material budget	**0.2 % X_0/layer**
• Frame time	**20 μs**

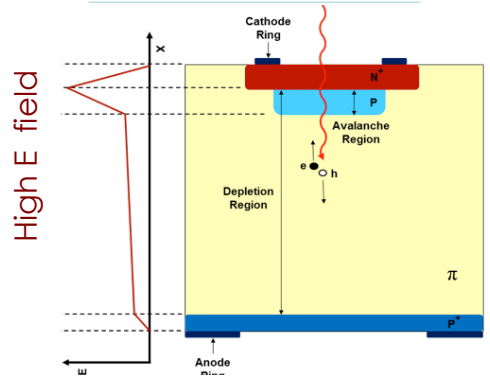
PXD module



This technology is the rightball park, but rolling shutter readout is too slow for the EIC (interaction frequency up to 500 kHz)

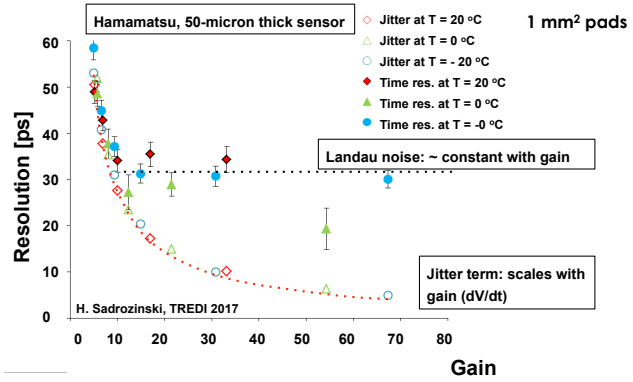
Low Gain Avalanche Detectors

R. Arcidiacono, https://indico.cern.ch/event/722363/contributions/3031252/



- LGAD silicon sensor with an additional gain layer that allows to reach time resolution in the order of tens of ps

- State-of-the-art LGAD Developed for ATLAS and CMS timing detectors at HL-LHC
  - "Pixel" pitch > 1 mm
  - Power consumption = 300-400 mW/cm^2



- Ongoing developments to reduce pitch to few hundred μm, still far from EIC requirements
- Power consumption difficult to lower because of large sensor capacitance and required ps time resolution

This technology is not suitable for the EIC Si vertex and tracking detector

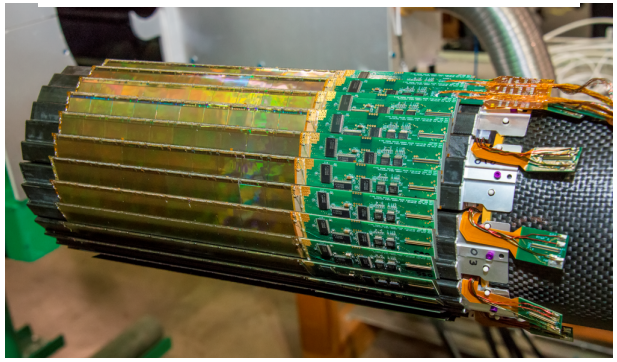
MAPS

P. Riedler, https://indico.cern.ch/event/632608/
G. Aglieri Rinella, NIMA 845 (2017) 583 - 587

- MAPS contain sensor and electronics in the same silicon substrate
- State-of-the-art MAPS detectors
  - MIMOSA sensor at STAR HFT
  - ALPIDE sensor at ALICE ITS
- MAPS key features
  - Small pixel pitch, < 30 μm
  - Low power, < 150 mW/cm^2
  - Low material budget, < 0.4% X/X_0 per layer
  - Moderate radiation hardness, < few 10^{13} 1MeV n_{eq}/cm^2, < few Mrad

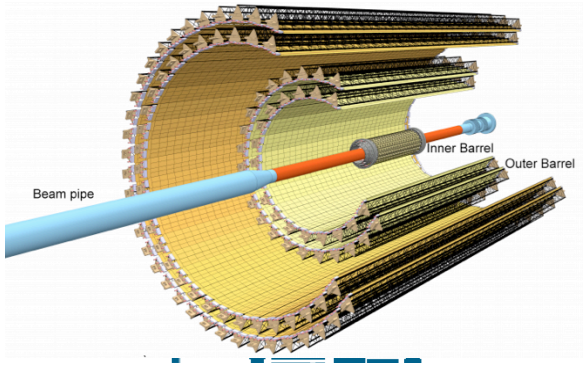
This technology is compatible with EIC requirements

STAR Heavy Flavour Tracker (HFT) at RHIC



G. Contin, NIMA 907 (2018) 60 - 80

ALICE Inner Tracking System (ITS) Upgrade at LHC



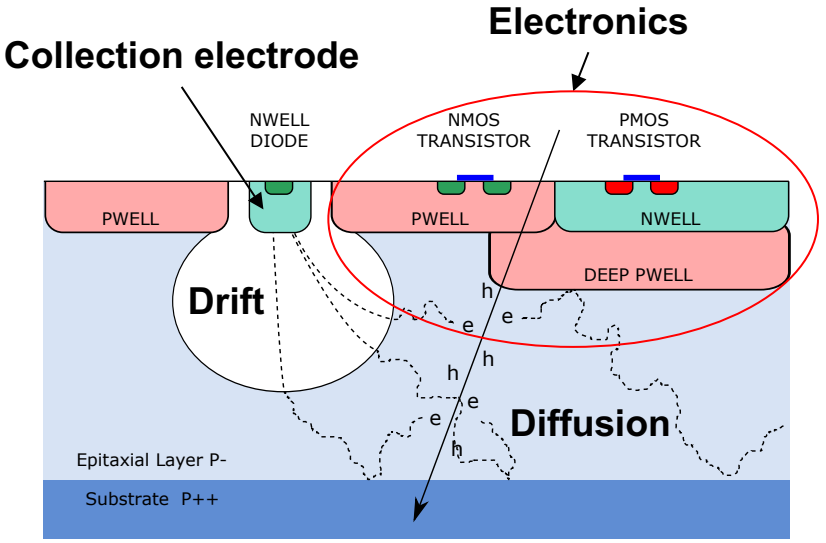
J. Phys. G: Nucl. Part. Phys. 41 (2014) 087002

ALPIDE sensor

- Current baseline for EIC Si vertex and tracking detector simulations
- 180 nm TowerJazz CMOS Imaging Sensor process
- Innovation with respect to traditional MAPS: partially depleted epi-layer
  - Charge collection in part by drift
- Small collection electrode = low detector capacitance → low power
  - And also low noise, low crosstalk, fast readout

ALPIDE sensor
28 x 28 μm^2 pixel pitch
10 μs integration time
Power density < 35 mW cm^{-2}
50 kHz interaction rate (Pb-Pb)
200 kHz interaction rate (pp)

ALICE- ITS
Inner layer thickness = 0.3% X/X_0
Outer layer thickness = 0.8% X/X_0



J. Phys. G: Nucl. Part. Phys. 41 (2014) 087002

G. Aglieri Rinella, NIMA 845 (2017) 583 - 587

Towards an EIC specific silicon sensor

- Excerpt from the EIC Detector Requirements and R&D Handbook– With respect to the ALPIDE…

> *"The EIC would certainly benefit in **improvements in the integration time** as well as in a further reduction of the energy consumption and material budget going towards **0.1-0.2% radiation length per layer**. Timing-wise the ultimate goal of this technology would be to **time stamp the bunch crossings** where the primary interaction occurred. […] Concerning spatial resolution the simulations indicate that a pixel size of **20 microns** must be sufficient."*

  - Spatial resolution = ~5 μm
  - Material budget = < 0.3% X/X0 per layer
  - Integration time = 2 μs
  - Optional: time resolution = < 9 ns

Explore recent MAPS developments:
DMAPS and 65nm MAPS

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  - 65 nm MAPS
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Recent MAPS developments: Depleted MAPS

- Developed in the context of the ATLAS Inner Tracker Pixel Upgrade, effort started more than 5 years ago
  - Main focus on radiation hardness and time resolution
  - *Reminder: EIC needs high granularity and low material budget!*

- HV/HR-CMOS technologies considered: TJ, LFoundry, AMS

- Advantage: charge collection by drift achieved via full depletion of the substrate
  - Larger signal, improved S/N
  - Faster and more complete charge collection

  ] Beneficial for improved spatial and time resolution

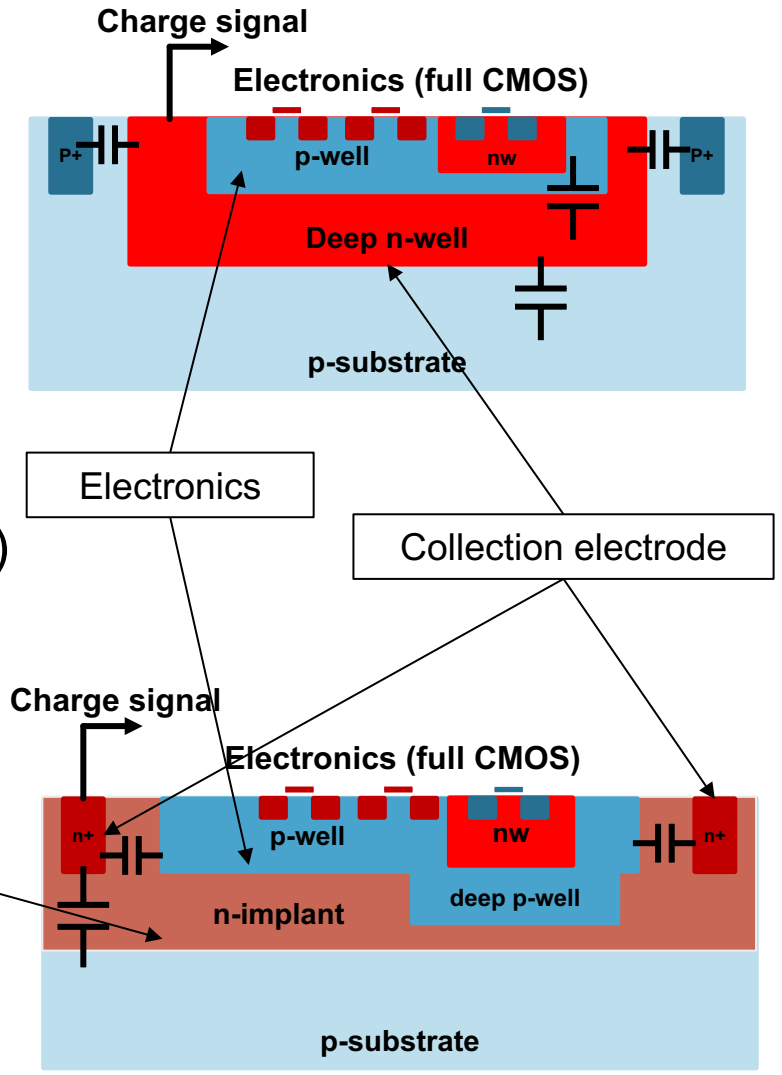
  - Improved radiation hardness (not relevant for the EIC)

Depleted MAPS layout

- Large collection electrode
  - Electronics inside large collection node
  - Uniform electric field in the substrate
  - Large capacitance (hundreds of fF)
  - LFoundry, AMS

- Small collection electrode (as in ALPIDE)
  - Electronics outside the collection node
  - Small capacitance (few fF)
  - Full depletion with extra deep planar junction in the substrate
  - TJ 180 nm modified CIS process

Obvious technology option to consider for the EIC

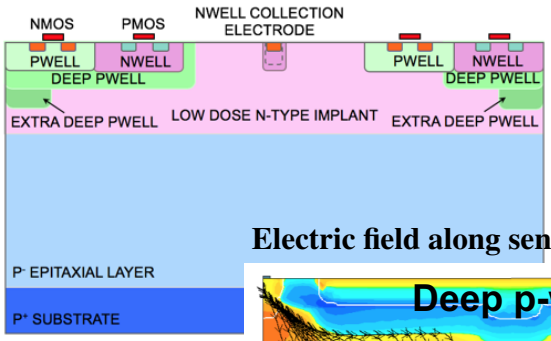


TJ 180 nm modified CIS process

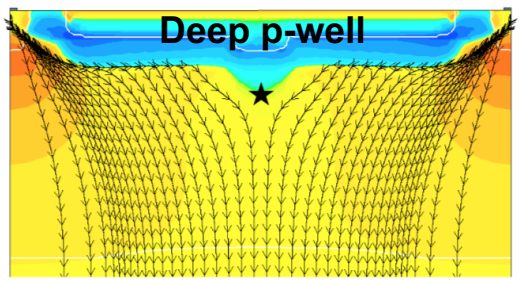
H. Pernegger et al 2017 JINST 12 P06008
W. Snoeys et al NIMA 817 (2017)
M. Munker *et al* 2019 JINST 14 C05013

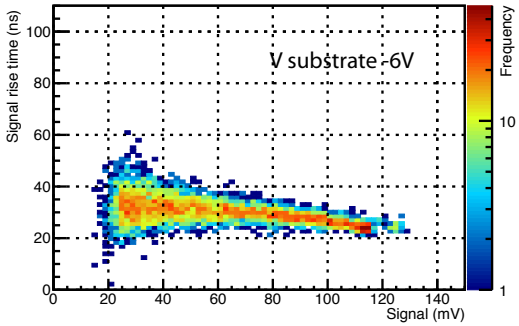
- Deep planar junction to achieve depletion under electronics p-well
- Demonstrated improved charge collection properties with respect to standard TJ 180 nm process
- Sensor layout design further optimised at the edge of the pixel to achieve uniform sensor response over the entire pixel

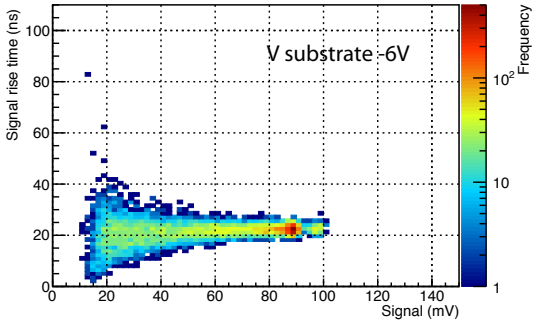
Example of sensor layout design

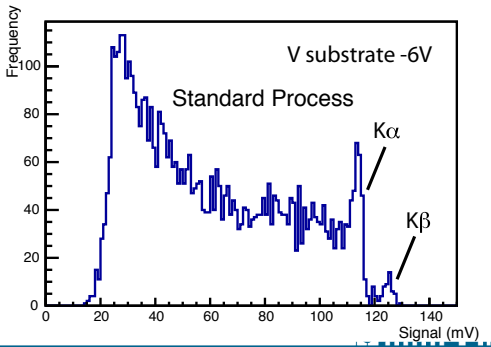


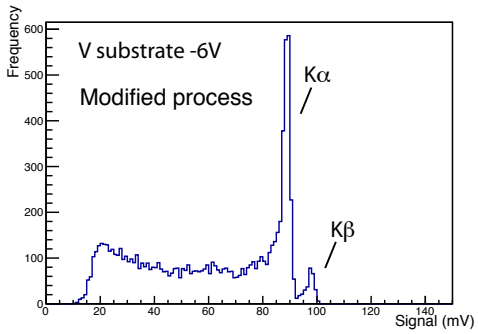
Electric field along sensor depth:











DMAPS in TJ 180 nm modified CIS process

- MALTA and TJ-Monopix for ATLAS ITk pixel at HL-LHC
  - Very compact and low power FE design (for the specific application)
  - Two different digital readout architectures explored to cope with the rates and required time resolution, asynchronous and column-drain
    - Asynchronous architecture: no clock propagated to the pixel matrix in order to reduce the digital power consumption
  - Successfully meet requirements for operation at the HL-LHC

	ALPIDE	MALTA	TJ-MONOPIX
Experiment	ALICE ITS (inner/outer layers)	ATLAS ITk pixel Phase II (outermost layer)	
Technology	TJ 180 nm CIS	TJ 180 nm CIS modified	
Substrate resistivity [kOhm cm]	> 1 (epi-layer 18-25 um)		
Collection electrode	small	small	small
Detector capacitance [fF]	<5		
Chip size [cm x cm]	1.5 x 3	2 x 2	1 x 2
Pixel size [um x um]	28 x 28	36.4 x 36.4	36 x 40
Integration time [ns]	4×10^3	<100	
Time resolution [ns]	2×10^3	< 5	< 25
Particle rate [kHz/mm^2]	10	10^3	
Readout architecture	Asynchronous		Synchronous, column drain
Analogue power [mW/cm^2]	5.4	~ 70	
Digital power [mW/cm^2]	31.5/14.8	N/A	N/A
Total power [mW/cm^2]	36.9/20.2	N/A	N/A
NIEL [1MeV n_{eq}/cm^2]	1.7×10^{13}	$> 1.0 \times 10^{15}$	
TID [Mrad]	2.7	100	

G. Aglieri Rinella, NIMA 845 (2017) 583 - 587
R. Cardella et al 2019 JINST 14 C06019
M. Dyndal et al 2020 JINST 15 P02005
I. Berdalvic, PhD thesis
I. Caicedo et al 2019 JINST 14 C06006
K. Moustaks et al NIMA 936 (2019) 604-607

Conclusion of DMAPS technology survey

- The most suitable technology for an EIC DMAPS sensor is the TJ 180 nm modified CIS process

- Existing DMAPS prototypes in this technology have features that are approaching EIC requirements
  - Power consumption, especially digital, should be assessed based on EIC requirements (integration time, time resolution, radiation and rates)
  - Pixel pitch however is too large

- To use this technology, a new design based on an optimisation of existing prototypes is needed
  - A feasibility study evaluating low power front-end architectures for 20 μm pixels has been carried out by eRD18 in collaboration with RAL CMOS sensor group; report to be released to YR Tracking WG soon

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Recent MAPS development: MAPS sensors in 65 nm

- The ALICE ITS3 project aims at developing a new generation MAPS sensor with extremely low mass for the LHC Run4 (HL-LHC)
  - Talk from Vito Marzari at the 2019 EIC Users Group meeting in Paris

- It is very interesting for an EIC detector in many ways
  - Detector specifications & timeline compatible with those of the EIC
  - Innovative development suited to an EIC starting in approx. 10 years
  - Large effort at CERN
  - Non-ALICE members welcome to contribute to the R&D to develop and use the technology for other applications

ALICE ITS3 sensor

- Chosen technology: TJ 65 nm process
  - Backup technology: TJ 180 nm CIS
- Specifications meet (or even exceed) the EIC requirements

ALICE

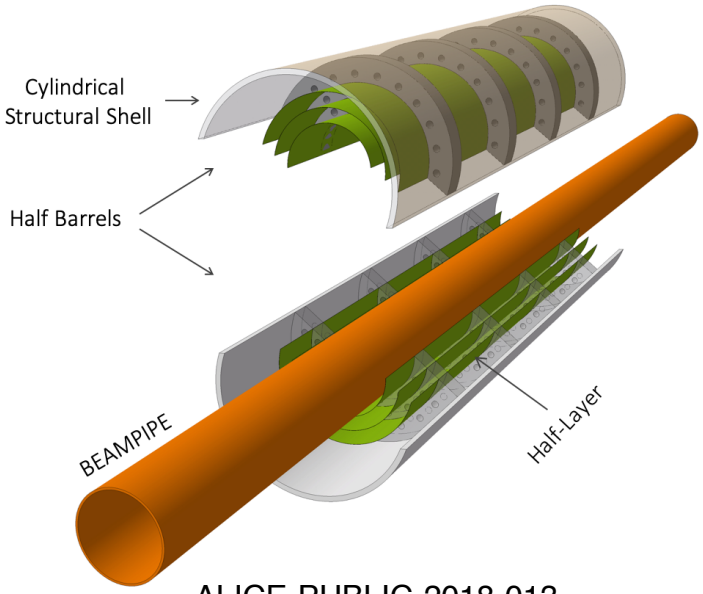
Specifications

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

M. Mager | ITS3 kickoff | 04.12.2019 |

ALICE ITS3 detector

- At system level, an aggressive R&D programme is starting to develop a system with < 0.05% X/X_0



ALICE-PUBLIC-2018-013
https://cds.cern.ch/record/2644611

- Low power design
  - Cooling can be done by convection through a forced airflow between the layers

- Wafer scale sensor using stitching technology, thinned and bent around the beam pipe, each layer half barrel is a single stitched sensor
  - Power and data distribution on-chip, no need for flexible PCB, interconnections outside the active area
  - Mechanical support outside acceptance

Comments on the ALICE ITS3 development

- The ALICE ITS3 specifications are a good match to the EIC requirements

- Joining this development would allow the EIC community to leverage on
  - A larger effort to develop a sensor for the EIC silicon vertex and tracking detector
  - An aggressive R&D programme into lightweight services, mechanics and cooling

This seems the most appropriate way forward

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Preliminary EIC sensor specifications

	EIC Sensor	
Detector	**Vertex and Tracking**	
Technology	TJ 65 nm Backup: TJ CIS 180 nm	
Substrate Resistivity [kohm cm]	1 or higher	
Collection Electrode	Small	
Detector Capacitance [fF]	<5	
Chip size [cm x cm]	Full reticule or stitched	
Pixel size [µm x µm]	20 x 20	
Integration Time [µs]	2	
Timing Resolution [ns]	< 9 (optional)	
Particle Rate [kHz/mm^2]	**TBD**	
Readout Architecture	Asynchronous	
Power [mW/cm^2]	< 20	
NIEL [1MeV neq/cm^2]	10^{10}	[1]
TID [Mrad]	< 10	[1]
Noise [electrons]	< 50	
Fake Hit Rate [hits/s]	< 10^{-5}/evt/pix	[2]
Interface Requirements	**TBD**	

[1] From EIC white paper
[2] ALPIDE specification

Conclusion and next steps

- The technology of choice for the EIC Si vertex and tracking detector is MAPS

- Two possible technology variants have been identified
  - DMAPS in TJ 180 nm modified CIS technology
  - New generation MAPS TJ 65 nm

Based on the technology options presented in these slides, it appears that the best path forward to arrive at an EIC Si vertex and tracking detector with the required performance is to join the ITS3 effort and contribute to integrating the EIC requirements into the ITS3 sensor design

See Leo's talk (next on agenda) for more details on how we can do this…

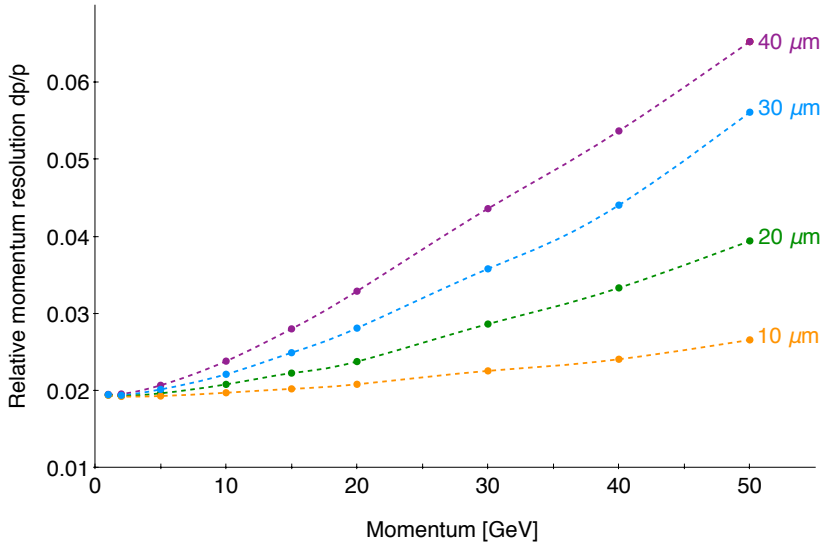
Backup

eRD16: Simulation results – disks, pixel pitch

- Ernst Sichtermann, simulation of disks arrays in forward regions
  - Increased pixel size in the disk-arrays at large-z is not desirable
  - https://wiki.bnl.gov/conferences/images/8/89/ErnstSichtermann.pdf

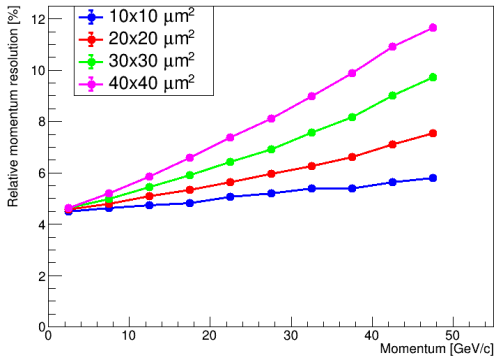
eRD16 - EIC R&D Simulations

- E.g. scan of pixel-size,

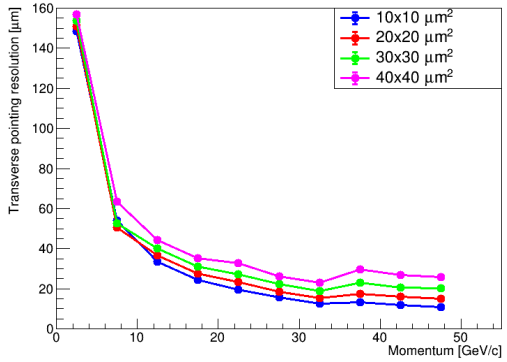


eRD18: Simulation results – disks, pixel pitch

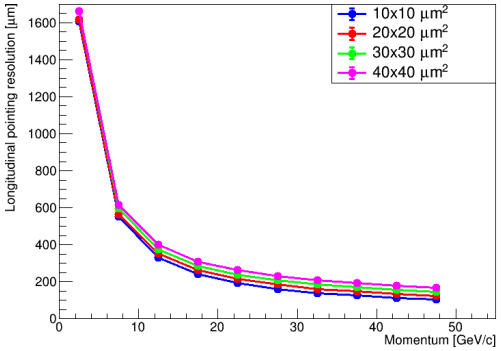
- H. Wennlof, simulation of disks arrays in forward regions
  - https://indico.bnl.gov/event/7689/contributions/35412/attachments/26828/40846/Simulation_report_Feb2020.pdf



(a) Relative momentum resolution.



(b) Transverse pointing resolution.



(c) Longitudinal pointing resolution.