Kickoff meeting held at CERN on December 4, 2019 for “ALICE ITS Upgrade in LS3”

Lawrence Berkeley National Laboratory

https://indico.cern.ch/event/860914/

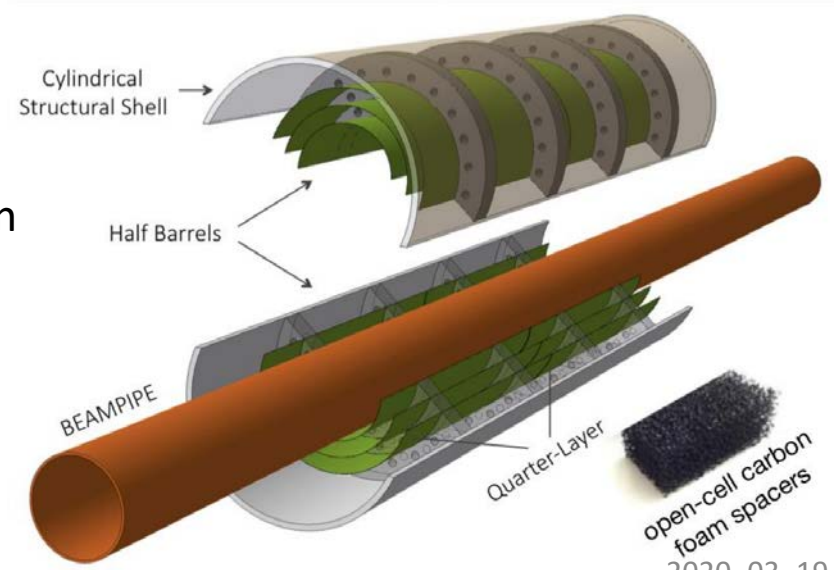
The most relevant efforts in this Letter of Intent (endorsed by the LHCC in September 2019) include:

- Silicon R&D for next generation MAPS sensor (with significant improvements)

coupled with

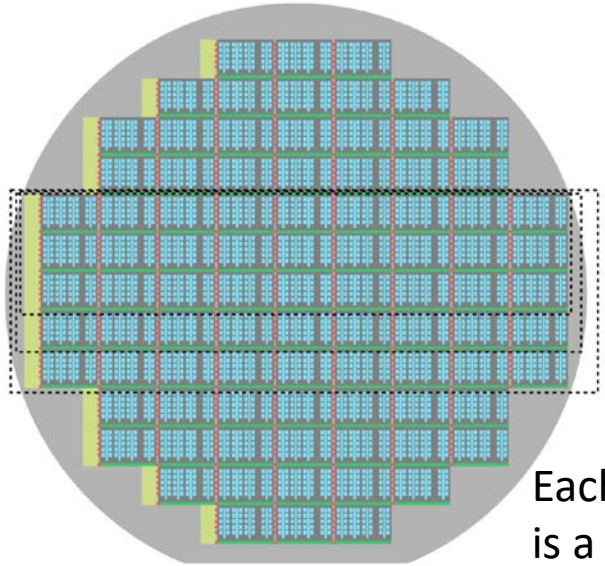
- R&D into extremely low X/X0 cylindrical vertex detection with “bent” silicon

“bent” silicon Detector concept



X/X0 ~ 0.05%

“stitched” silicon



Each layer half barrel is a single stitched sensor

New sensor design – compared to existing ALPIDE

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Specifications

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

M. Mager | ITS3 kickoff | 04.12.2019 |

Sensor development milestones

Table 3: Planned chip submissions.

	Milestone	Description	Production[a]	Date
MS CD-1	1	**Technology test structures** single pixels, transistors, small memory cell array for studying the radiation hardness of the technology	MPW	Q4 2019
MS CD-2	2	**Pixel test vehicle** optimization of pixel and diode geometries	MPW	Q3 2020
MS CD-3	3	**Large area prototype** basic blocks: pixel matrix, periphery, output serial links exercising of stitching different parts	ER	Q4 2021
MS CD-4	4	**Full-scale prototype** prototype of final chip with all functionality	ER	Q4 2022
MS CD-5	5	**Final Chip** possible minor adjustments wrt milestone 4	ER	Q4 2023

[a] MPW: multi-project wafer run, ER: engineering run

Pre – COVID-19

R&D Milestone 1

Validation of 65nm CMOS technology (Q2 2020)

Organization of effort for ITS3

ITS3-WP1: Physics studies, Simulation and Reconstruction alice-its3-wp1@cern.ch

- Physics performance studies
- Detector functional requirements
- Detector model and simulation
- Reconstruction

ITS3-WP2: Pixel chip design alice-its3-wp2@cern.ch

- Test structures and validation of the technology
- Optimization of the pixel layout
- Large area building block prototypes
- Full scale prototypes
- Final chip

ITS3-WP3: Pixel chip characterization alice-its3-wp3@cern.ch

- Development of hardware and software for the pixel chip characterization
- Laboratory, Beam and Radiation tests
- Pixel chip device simulation

Organization of effort for ITS3

ITS3-WP4: Pixel sensor thinning, bending and interconnection alice-its3-wp4@cern.ch

- Tests with existing material (ALPIDE wafers)
- Tests with 300 mm dummy wafers
- Test with full-scale prototypes
- Mechanical, electrical and functional validation of the procedures

ITS3-WP5: Mechanics and cooling alice-its3-wp5@cern.ch

- Selection and characterization of carbon materials (structural and thermal properties)
- Development and production of support structures
- Development, production and validation of the Engineering Module based on dummy chips
- Development, production and validation of the Qualification Module based on prototype chips
- Production of the Final Module based on final chips

An EIC effort will require additional effort in R&D

EIC – WP6: Discs based on ITS3 sensors
EIC – WP7: Long staves based on ITS3 sensors
EIC – WP8: Support and cooling for discs and staves
+?

Towards an EIC silicon consortium

- As already stated, we consider joining the CERN based ITS3 silicon effort as the most likely path so success for developing a sensor that meets the EIC requirements.

- I have already approached the ITS3 management team and they are quite supportive of having and EIC based contingent in the contributor base. As was described before, the ITS3 project is set up from the beginning to include non - ITS/ALICE/CERN members. A MOU that codifies this is being formed in WP2.

- There are existing institutions like LBNL, Bari, Trieste, Wuhan and others that are already part of ITS/ALICE who have demonstrated interest in using ITS3 developed sensors for EIC.

- Other institutions such like Birmingham, RAL, BNL instrumentation, IMPCAS etc. are not part of ALICE/CERN but have a strong interest in an EIC sensor and extensive silicon experience.

- **We are in the process of forming a consortium of institutions to join the ITS3 effort as the primary development for an EIC based sensor. I will be meeting again with ALICE/ITS3 management next week to expand on our plans and get basic information. Any group that feels that they can contribute and is interested in joining this consortium, please get in touch with me.**