DE LA RECHERCHE À L'INDUSTRIE

Cylindrical Micromegas Tracker and more...

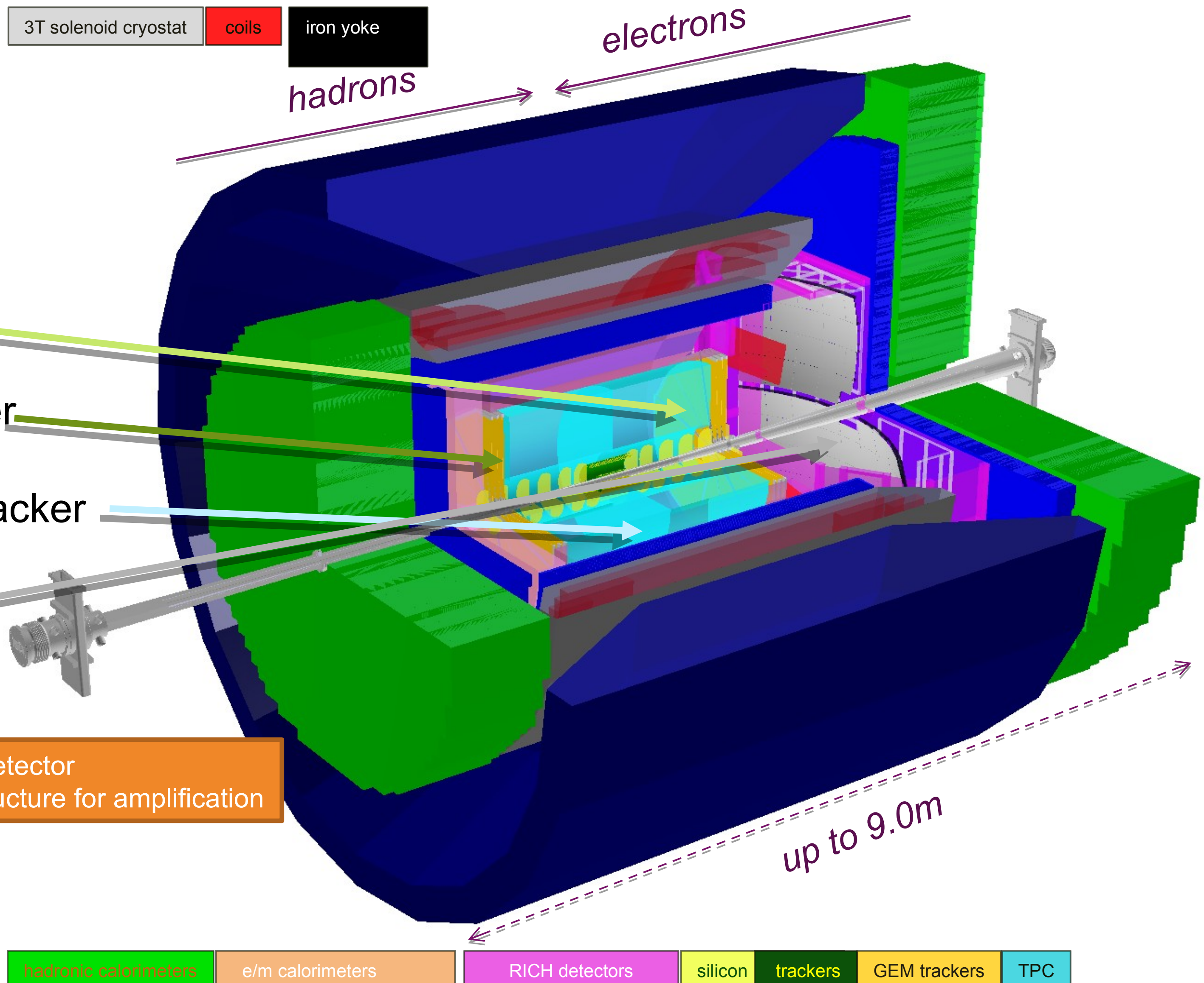
F.Bossù for DPhN and DEDIP

EIC YR meeting – Tracking WG
19 March 2020

MPGDs in an EIC Detector

MPGDs @ EIC :

- TPC readout
- Large Planar tracker
- Large Cylindrical tracker
- RICH readout

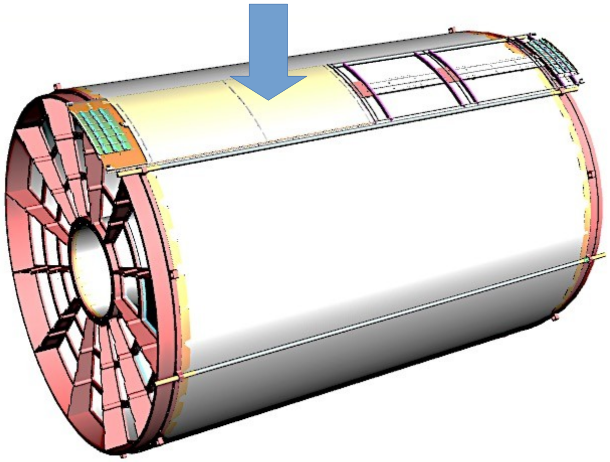


MPGD = Micro-Pattern Gas Detector
=> Gas detector with small structure for amplification

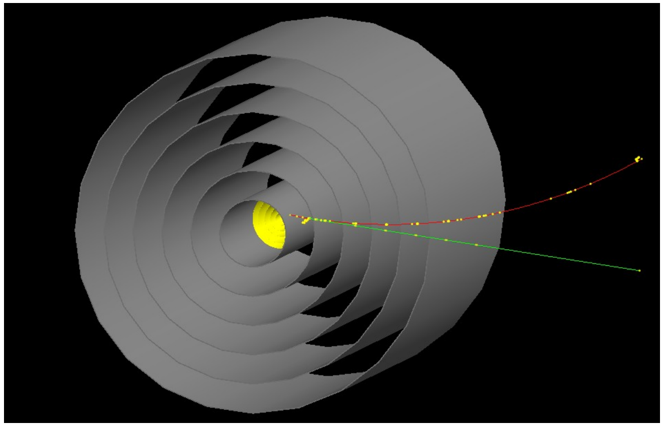
MPGD Cylindrical tracker

- Two options

- External/Internal layers to a TPC to help track matching with calorimetry and particle identification detectors
- Must fit in very narrow space
- Good spatial resolution
- Possibly, good timing resolution



- Full tracker, i.e. several concentric layers of MPGDs
- Layers can be cylindrical for a compact designs
- Must work in high particle rates and high magnetic fields



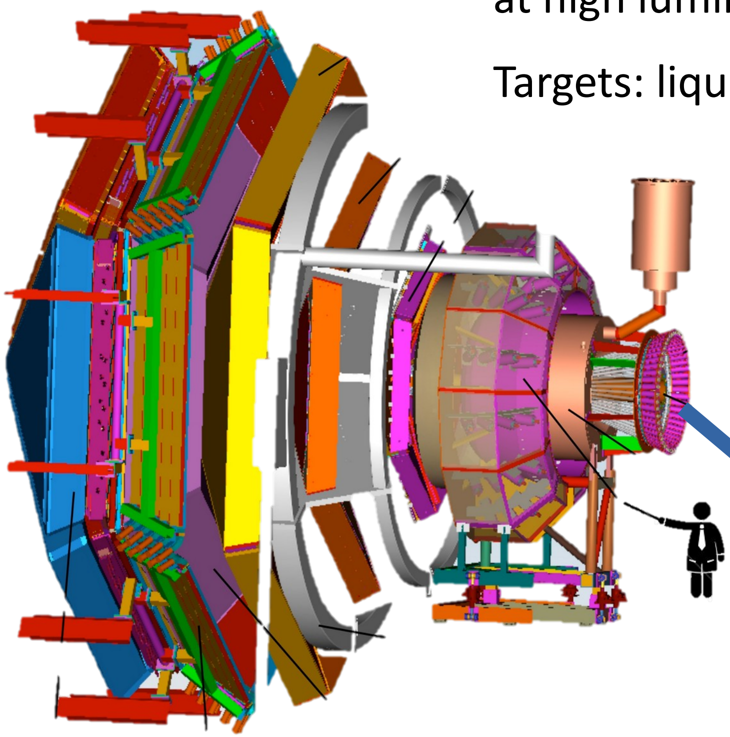
- For both solutions, low X/X0 is mandatory
- The technology must be affordable and reliable for large surfaces

Experience with a cylindrical MM trackers

CLAS12 Experiment at Jefferson lab

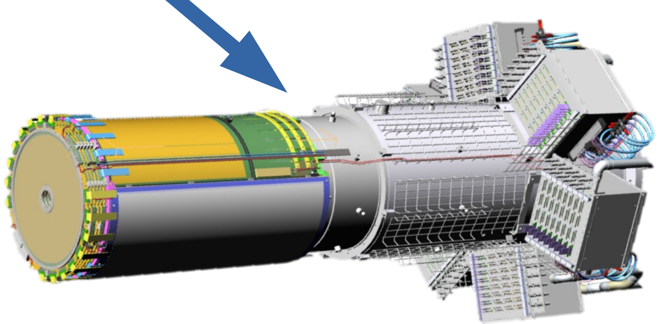
Study of the nucleon structure with ~11 GeV electron beam at high luminosity (10^{35} cm^{-2}s^{-1})

Targets: liquid hydrogen, liquid deuterium and other nuclei



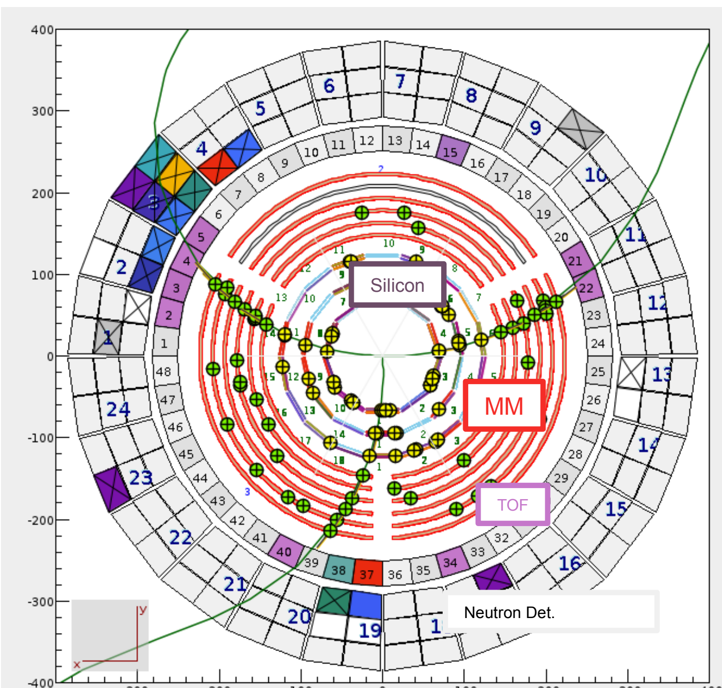
Micromegas Vertex Tracker (MVT) :

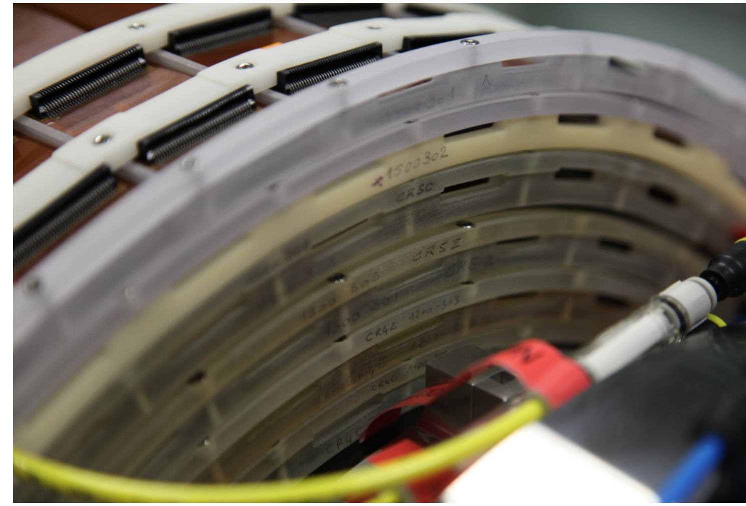
- Inserted in the 5T solenoid
- Used in combination with the Silicon Vertex Tracker (SVT)

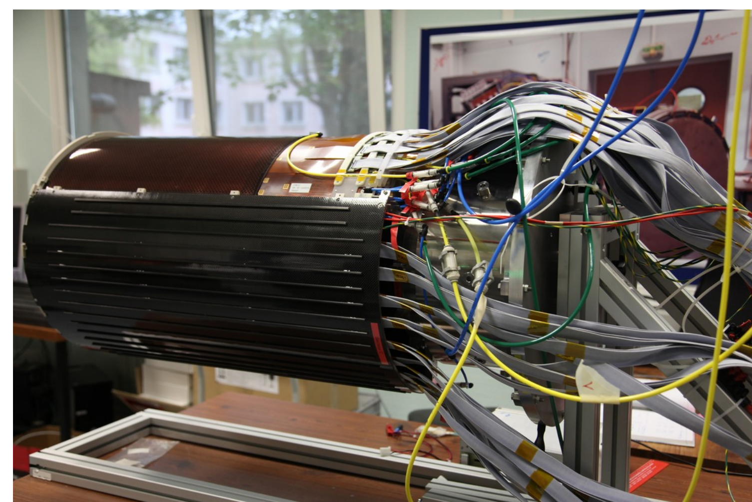


CLAS12 Micromegas Vertex Tracker

- 4 m² of curved Micromegas detectors
- DREAM based Front-End Electronics ~ 20k ch.
- Low momentum particles => Light Detectors ~0.3% of X0
- Limited space of ~10 cm for 6 layers (small radius ~12 cm)
- High magnetic field (5T)
- 6 Layers with different R (18 detectors total)
- Up to 30 MHz of particle rate







DREAM Front-End Electronics

Versatile FE readout electronics developed at Saclay primarily for CLAS12, and widely used by various experiments

Sustains trigger rates of 50 kHz and beyond; Low dead time operation with concurrent sampling and readout

Off-detector architecture with up to ~2m micro-coaxial cables and tolerant to 1.5 T magnetic field

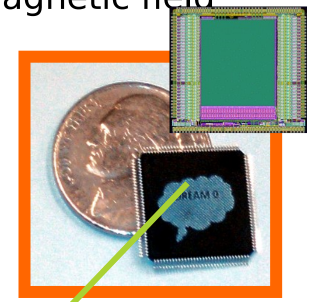
Based on an in-house developed 64-channel Dream ASIC

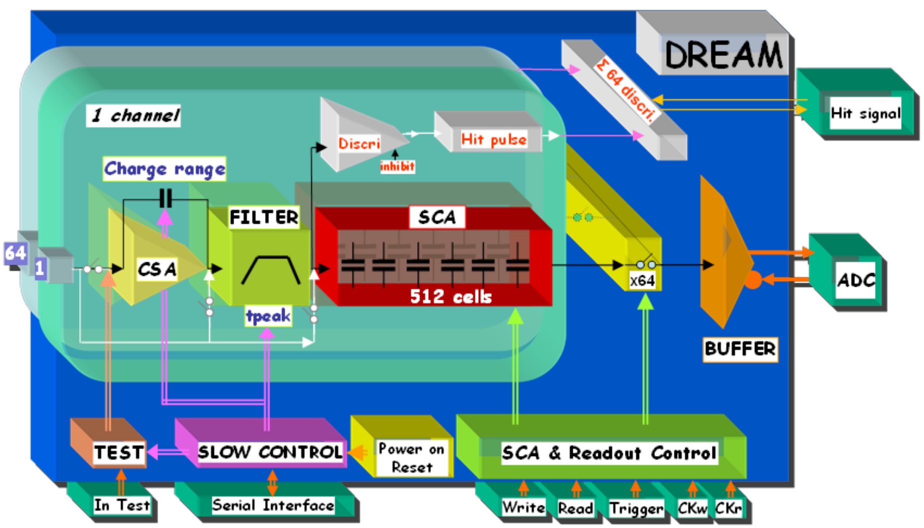
High input capacitance friendly: O(100pF) level

Sampling frequency up to 50 MHz

Adjustable peaking time from 70 ns to 1 μs

Adjustable gain/dynamic range from 50 fC to 600 f

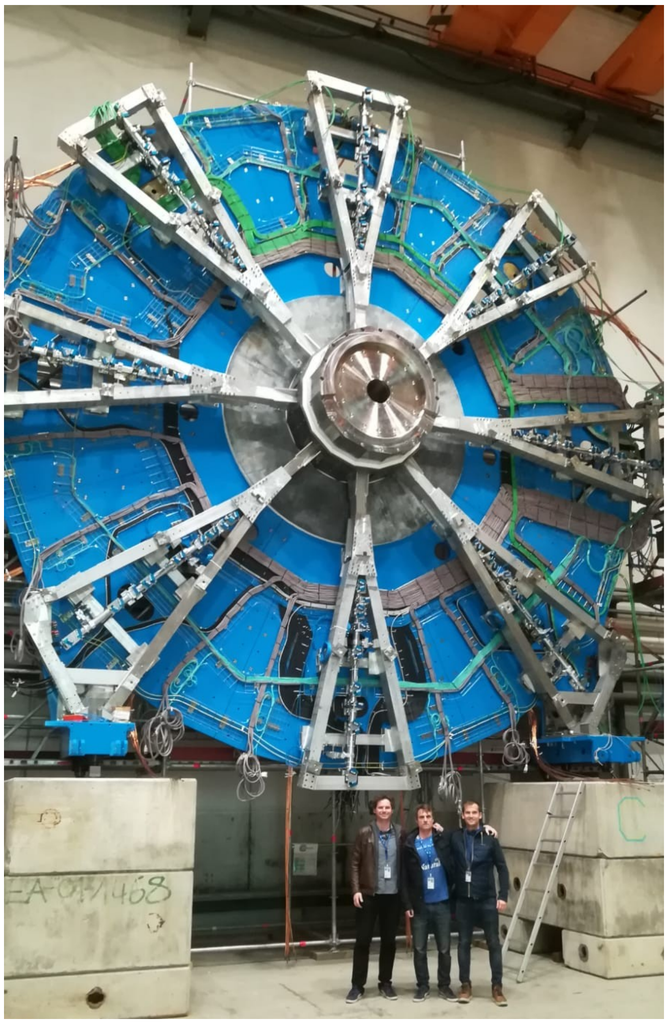


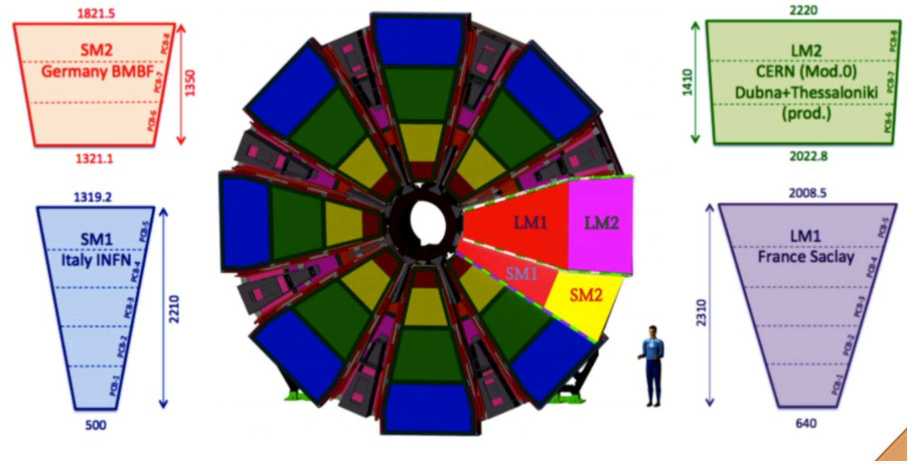


512-channels Front-End Unit

Large planar detectors

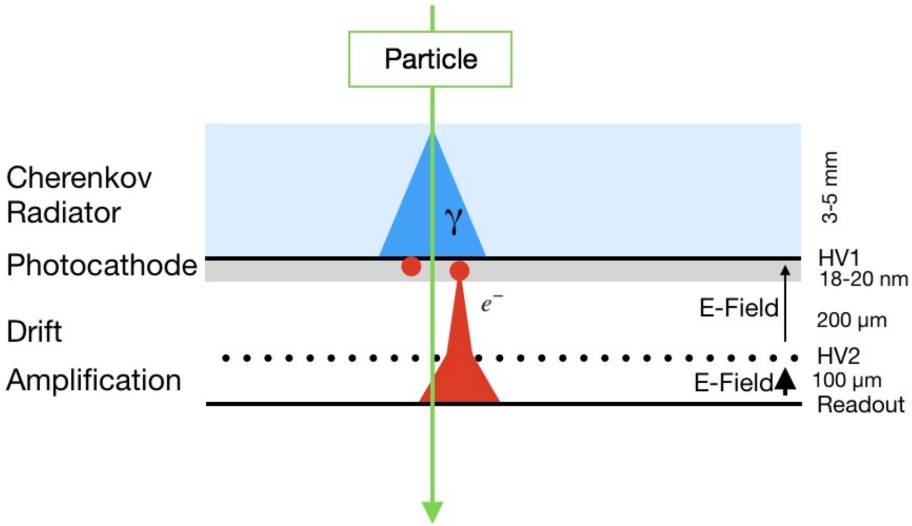
ATLAS NEW SMALL WHEEL

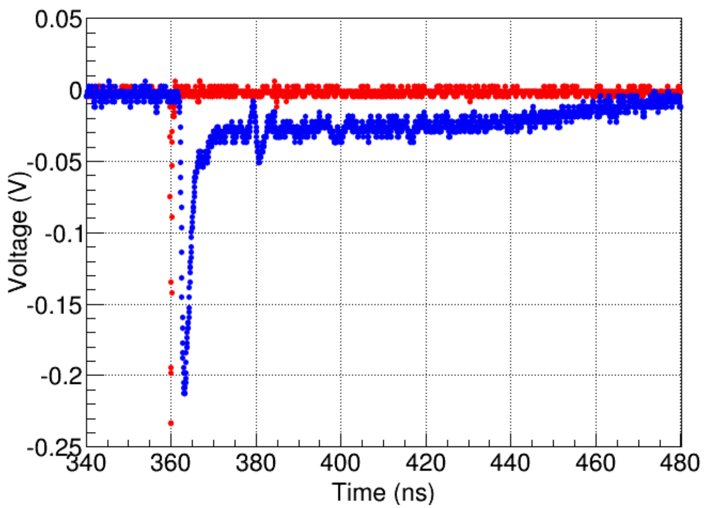




- Total of 1200m2 of resistive Micromegas
- 2.3x2m no dead area detectors ~16m2 of active area of detector
- 60um resolution, 100um mechanical precision
- Max rate 15kHz/cm^2
- Resistive technology, high-rate oriented, will be part of the trigger system
- Saclay main contributor
- Large dedicated clean room for assembling and testing

The “PICOSEC” Micromegas concept





https://doi.org/10.1088%2F1742-6596%2F1312%2F1%2F012012

- A particle produces Cerenkov light.
- Photons produce electrons in the photocathode.
- Electrons are amplified by a two stage Micromegas detector.
- Two signal components:
  - Fast: ***electron peak*** (~1 ns). -> Timing features.
  - Slow: ***ion tail*** (~100 ns).

Small drift gap (200 nm):

- Pre-amplification possible
- Limited direct ionization
- Reduced diffusion impact

Cerenkov radiator:

- Photoelectrons emitted simultaneously by the photocathode (fixed distance from the mesh)

Aiming at:

- **single photoelectron time jitter ~100 ps**
- **produce sufficient photoelectrons to reach timing response ~40 ps.**

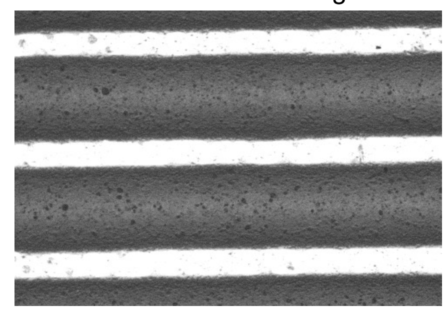
MPGD WORKSHOP AT SACLAY

120 m² of clean room for Micromegas bulk and resistive layer manufacturing.

Bulk process: addition of a mesh on PCB by photolithography
- Maximum detector size: 600 x 700 mm².
- Amplification gap from 50 to 292 µm
- Mesh woven (18 µm wires) or thin mesh (down to 5 µm)
- PCB with strip, XY strip, pixel,…
- Production : ~ 150 bulk in 2019
- R&D : thins mesh, curved bulk, segmented mesh, double mesh….

Double face micromegas

Resistive screen printing on various surface
- Maximum size: 600 x 600 mm²
- Resistive value: from 10 KOhm/sq, to 10 Gohm/sq
- Possibility of neutral on conductive paste
- Substrate: Kapton, glass, FR4
- Production: ~ 100 resistive substrate in 2019
- R&D : mixture for ad hoc resistive value, segmented resistive,…



Resist strip of 500 µm

contact stephan.aune@cea.fr

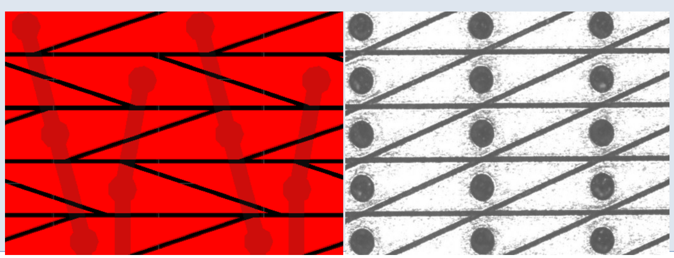
Bulk lab

Resist lab

2D READOUT AND LOW-IBF

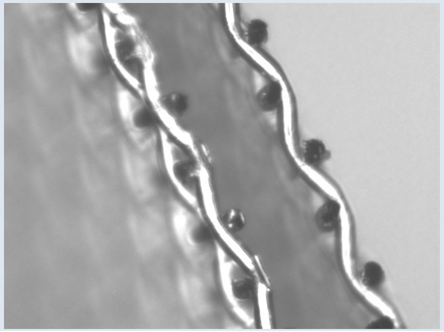
ZigZag 2D read out

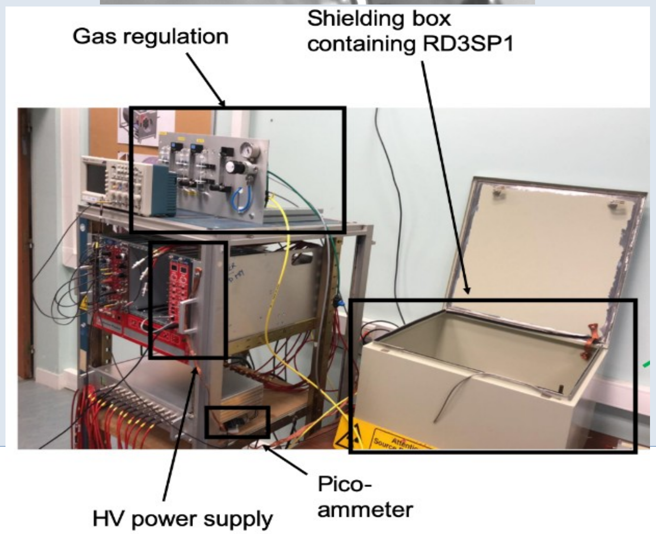
- R&D on laser etching for read out of MPGD detector
- 1D ZigZag: better then 100um res with 2mm strips
- MM, GEM and uRWELL read by the DREAM electronics
- 2D read-out with better than 200um resolution
- Development within an LDRD
- M. Revolle's PhD subject



Low-IBF for TPC

- Micromegas based solutions for
- low-IBF read-out planes for TPC
- A. Glaenzer's PhD subject





Summary

- Micromegas are a mature technology that can be an **affordable**, **low material budget** solution for **large area** detectors
- For **compact detector designs**, the central region can be equipped with cylindrical Micromegas tiles
- Ongoing R&D efforts aims at improving the patterns for better spatial resolution both in 1D and 2D read-out configurations
- Coupling a few mm Cerenkov radiator with Micromegas (PICOSEC) might be a solution also for fast timing tracking detectors
- CEA-Saclay new workshop allows for fast prototyping and production
- FEE ASIC design in parallel with detector prototyping (see backups for other examples of ASIC developments)

Backups

AGET front-end chip

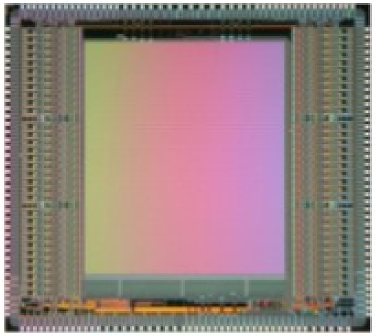
Irfu

Specifications

Parameter	Value
Polarity of detector signal	Negative or Positive
Channels number	64
External Preamplifier	Yes; access to the filter or SCA input (external CSA)
Charge measurement	
Input dynamic range	120 fC, 240 fC, 1 pC, 10 pC
Gain	Adjustable per channel
Output dynamic range	2V p-p (differential)
I.N.L	< 2%
Resolution	< 850 e- (Gain: 120fC; Peaking Time: 200ns; Cinput < 30 pF)
Sampling	
Peaking time	50 ns to 1 µs (16 values)
SCA time bin number	512 or 2 x 256 cells
Sampling Frequency	1 MHz to 100 MHz
Multiplicity	
Multiplicity signal	Analog "OR" of 64 discriminator outputs
Input dynamic range	5% or 17.5% of input channel input charge range
I.N.L	< 5%
Threshold value	7-bit DAC [(3-bit + polarity bit) common DAC + 4-bit DAC/channel]
Readout	
Readout frequency	25 MHz
Channel Readout mode	Hit, selected or all
SCA Readout mode	1 to 512 cells
Test	
calibration	1 channel among 64; 1 external test capacitor
test	1 channel among 64; internal test capacitor (1 among 4)
functional	1 to 64(68) channels; 1 internal test capacitor per channel
Counting rate	< 1 kHz
Power consumption	< 10 mW / channel @ 3.3V

Layout & package

- Technology: AMS CMOS 0.35 µm
- Surface: 8,5 x 7,6 mm² [7,8 x 7,4 mm²]
- Number de transistors:# 700 000 [500 000]
- Package: LQFP 160 (28 x 28 x 1.4 mm)
- 2014: end of test production (700 + 2500)



Also to mention **ASTRE** chip :

- derivative from AGET
- peaking times 70 ns to 8 µs
- space grade (HARPO project)
- produced and tested at low quantities

SAMPIC: Architecture

- **16 single-ended channels:**
  - Self triggerable (or Central OR Trigger, or External Trigger)
  - Independent channels
  - 64 analog sampling cells/ch
  - One 11-bit ADC/ cell (total : 64 x 16 = 1024 on-chip ADCs)
- **One common 12-bit Gray counter** (@160MHz) for coarse timestamping.
- **One common servo-controlled DLL**: (from 1 to 10 GS/s) used for medium precision timing & analog sampling
- **One common 11-bit Gray counter** running @ 1.3GHz and used for the massively parallel Wilkinson analog to digital conversion.
- **12-bit LVDS readout bus** (potentially running up to 400 MHz)
- **SPI Link** for Slow Control configuration

- Techno: AMS CMOS 0.18µ
- Size: 7 mm2
- Prototyping cost: only 10 k€
- Package: 128-pin QFP, pitch of 0.4mm