EIC R&D at the University of Birmingham

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Kick-off meeting of the EIC-YR Tracking Detectors Working Group

13 February 2020

Birmingham Instrumentation Laboratory - BILPA

- The **Birmingham Instrumentation Laboratory for Particle Physics and Applications** (BILPA) has been established in 2016 through a University funded initiative aimed at consolidating and expanding its capabilities in **semiconductor detector systems R&D and production**

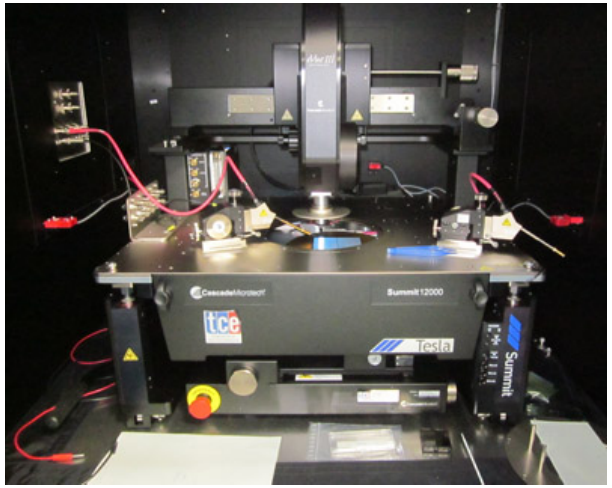
- The laboratory consists of **200 m^2 of open-plan cleanroom** space (ISO5 and ISO7) and is designed to accommodate work in three main areas
  - Detector development for the High-Luminosity upgrade of the LHC (**HL-LHC**)
  - **Generic R&D on semiconductor detectors** for future international collider experiments
  - **Medical application** of particle physics technology

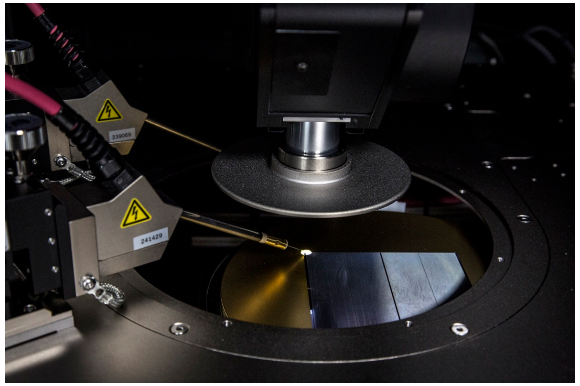
- This facility is complemented by a **high intensity irradiation line** at Birmingham MC40 cyclotron

- More info at http://www.ep.ph.bham.ac.uk/general/SiliconLab/index.html

BILPA and irradiation facility

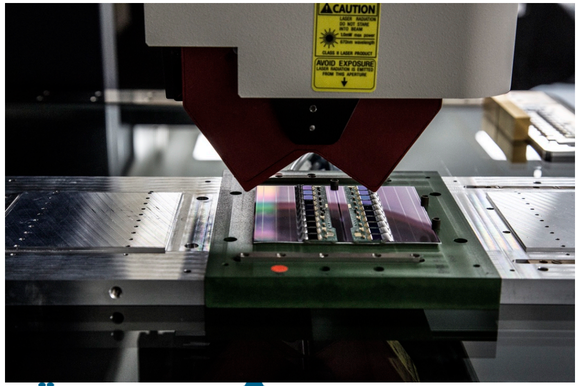
Panoramic view of the ISO5 clean room





Cascade Tesla Semi-automatic Probe station

Metrology on a ITk strip module with a OGP SmartScope Flash 500



BILPA R&D programme

- ATLAS Inner Tracker (ITk) upgrade at the HL-LHC
  - The UK will deliver 50% of the ITk strip barrel (~ 6000 modules)
  - Birmingham is one of two **hybrid production** sites, and one of five **module production** sites in the UK
  - The Birmingham irradiation facility is the only proton irradiation site for **strip sensor QA**

- Generic R&D on semiconductor detectors for future international collider experiments
  - **Reconfigurable MAPS** in radiation-hard Technology for outer tracking and digital electromagnetic calorimetry at an FCC facility (**DECAL sensor**)
  - EU funded AIDA2020 generic R&D on **depleted MAPS** (within the ATLAS ITk pixel effort)
  - Precision Central **Silicon Tracking & Vertexing for the EIC**
  - Development of radiation tolerant Low Gain Avalanche Devices (**LGAD**) for fast timing application
  - **RD50 R&D** for radiation-hard novel silicon technologies (DMAPS and LGAD)

- **Medical application** of particle physics technology
  - See backup slide

eRD18: Precision Central Silicon Vertex & Tracking for the EIC

- UoB is working on the development of a detailed concept for a **central silicon vertex and tracking detector** for a future EIC experiment, exploring the potential advantages of depleted MAPS (**DMAPS**) technologies
  - This project has been **running since 2016** with continuous support from the EIC Detector R&D Programme
  - Close **collaboration with eRD16 (Berkeley)**: Forward/Backward Tracking at EIC using MAPS Detectors

- The project focuses on the development of an **EIC specific sensor** and **conceptual design** of the silicon vertex and tracking detector
  - **WP1: Sensor Development**
    - Exploit on-going R&D in Birmingham into DMAPS to investigate potential solutions for the EIC
  - **WP2: Silicon Detector Layout Investigations**
    - Study performance requirements in terms of numbers of layers, layout and spatial resolution of the pixel hits

WP1: summary of activities

- **Technology investigations**
  - Most suitable technologies for an EIC Si vertex & tracking detector: MAPS or DMAPS sensors
  - eRD18 investigated in particular the benefits of using **DMAPS technologies (i.e. HV/HR CMOS)**
  - DMAPS technology for EIC identified and fully characterised: TJ 180nm modified CIS process
    - https://wiki.bnl.gov/conferences/images/9/9a/ERD18_TJ-Summary-Jun19.pdf
    - https://doi.org/10.1016/j.nima.2019.163381

- **Feasibility study** into an EIC specific sensor
  - Carried out in collaboration with **RAL CMOS sensor group**
  - Preliminary set of **specifications for an EIC specific sensor** compiled
  - Investigate options for the pixel design and readout architecture that would match the requirements for a tracking and vertex detector at an EIC, with the added capability to **time stamp individual bunch crossings**
  - A suitable **low power pixel design architecture** has been identified
  - See talk here: https://wiki.bnl.gov/conferences/images/6/65/ERD18ReportJan20v0.1.pdf

WP1: EIC sensor specifications

- A set of requirements for an EIC specific sensor has been compiled based on technology investigations and detector layout simulations
- The time stamping option might require a dedicated sensor to be used in an outer layer
  - Required pixel size and power consumption might be prohibitive for vertex and tracking
- Note: **these specifications are by no means restricted to DMAPS technologies**, and capture the requirements for an EIC sensor independently of the used technology (MAPS or DMAPS)

Detector	Vertex and Tracking	Added time stamping
Technology	TJ or similar	
Substrate Resistivity [kohm cm]	1	
Collection Electrode	Small	
Detector Capacitance [fF]	<5	
Chip size [cm x cm]	Full reticule	
Pixel size [µm x µm]	20 x 20	max 350 x 350
Integration Time [ns]	2000	
Timing Resolution [ns]	*OPTIONAL* *< 9 (eRHIC)* *< 1 (JLEIC)*	< 9 (eRHIC) < 1 (JLEIC)
Particle Rate [kHz/mm^2]	**TBD**	
Readout Architecture	Asynchronous	**TBD**
Power [mW/cm^2]	<35	<200
NIEL [1MeV neq/cm^2]	10^{10}	
TID [Mrad]	< 10	
Noise [electrons]	< 50	
Fake Hit Rate [hits/s]	< 10^{-5}/evt/pix	
Interface Requirements	**TBD**	

WP2: summary of activities

- **Basic layout simulations** based on EICRoot: completed
  - Baseline performance plots for a Si+TPC and all silicon tracker design
  - A report is being prepared and can be circulated to this WG

- **Physics performance** simulations: ready to start
  - G4E framework installed and running (thanks for Yulia & Dmitry)
  - Ready to start heavy flavour physics simulations
  - Inform the Detector/Physics Working Group input into the EIC Detector Yellow Report

Emerging alternative technology: ALICE ITS3 MAPS

- See Leo Greiner's talk at the MIT meeting
  https://www.jlab.org/indico/event/348/session/5/material/0/0.pdf

- The ALICE ITS3 project aims at developing a **new generation MAPS** sensor with **extremely low mass** for the LHC Run4 (HL-LHC)

- It is very interesting for an EIC detector in many ways
  - Detector **specifications & timeline** compatible with those of the EIC
  - **Innovative development** suited to an EIC starting in approx. 10 years
  - **Large effort at CERN**
  - **Non-ALICE members welcomed** to contribute to the R&D to develop the technology for other applications

ALICE ITS3

Kickoff meeting held at CERN on December 4, 2019 for “ALICE ITS Upgrade in LS3”

https://indico.cern.ch/event/860914/

The most relevant efforts in this Letter of Intent (endorsed by the LHCC in September 2019) include:

- Silicon R&D for next generation MAPS sensor (with significant improvements)

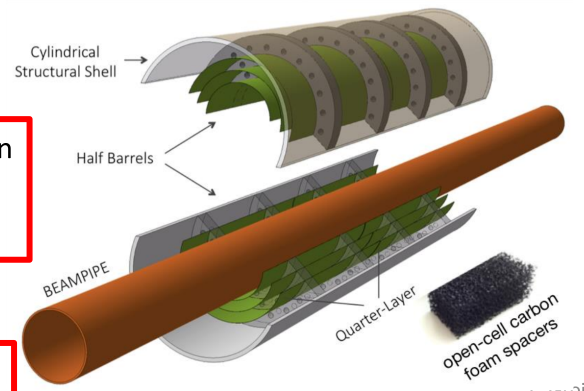
coupled with

- R&D into extremely low X/X0 cylindrical vertex detection with “bent” silicon

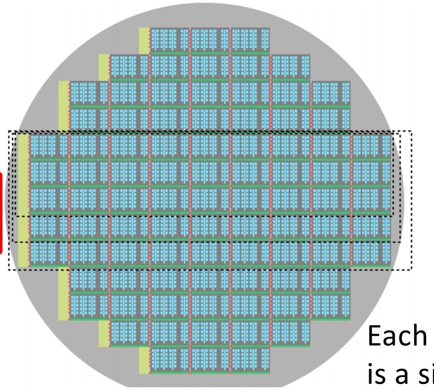
Much of this has already been presented by my colleague Vito Manzari at 2019 EIC User Group Meeting, 22-26 July 2019 Paris

“bent” silicon Detector concept

X/X0 ~ 0.05%



“stitched” silicon



Each layer half barrel is a single stitched sensor

L. Greiner (LBNL) - 2019_12_12 2

ALICE ITS3 sensor

- The ALICE ITS3 specifications meet or even exceed the EIC requirements

ALICE

Specifications

Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

M. Mager | ITS3 kickoff | 04.12.2019 |

Conclusion

- The BILPA clean rooms are equipped for R&D and production of semiconductor vertex and tracking detectors

- Birmingham has been working on the conceptual design of a silicon vertex and tracking detector for the EIC for more than four years now
  - Collaboration with eRD16 (Berkeley) and RAL CMOS sensor design group
  - Two possible technologies for an EIC sensor have been identified
    - TJ 180nm CIS process modified for full depletion (DMAPS) – study completed
    - New generation 65nm ALICE ITS3 sensor (MAPS)
  - A preliminary set of specifications for an EIC sensor have been defined
  - Options for pixel FE design have been simulated
  - More detailed results can be presented at the next meeting of this WG

- Next steps: commence work on ITS3 sensor technology to design the EIC silicon vertex and tracking detector

eRD18 reports and talks

- https://wiki.bnl.gov/conferences/images/0/05/BhamEICProposal-15Jun.pdf
- https://wiki.bnl.gov/conferences/images/3/32/BhamEICProposal.pdf
- https://wiki.bnl.gov/conferences/images/7/7d/ERD18_ReportJan17.pdf
- https://wiki.bnl.gov/conferences/images/e/e3/ERD18UpdateJan17.pdf
- https://wiki.bnl.gov/conferences/images/f/fd/ERD18_ReportJun17.pdf
- https://wiki.bnl.gov/conferences/images/1/1d/ERD18ReportJuly17v3.pdf
- https://wiki.bnl.gov/conferences/images/7/72/ERD18_ProgressReport_Jan2018.pdf
- https://wiki.bnl.gov/conferences/images/7/78/ERD18ReportJan18v1.pdf
- https://wiki.bnl.gov/conferences/images/d/dc/ERD18-Report-FY19Proposal-Jun18.pdf
- https://wiki.bnl.gov/conferences/images/9/97/ERD18-FY18Report-FY19Proposal_v2.pdf
- https://wiki.bnl.gov/conferences/images/c/c0/ERD18ReportDec18.pdf
- https://wiki.bnl.gov/conferences/images/c/c5/PeterJones.pdf
- https://wiki.bnl.gov/conferences/images/5/59/ERD18_Report-FY20Proposal-Jun19.pdf
- https://wiki.bnl.gov/conferences/images/8/87/ERD18ReportJul19v1.pdf
- https://wiki.bnl.gov/conferences/images/3/30/ERD18_Jan-2020.pdf
- https://wiki.bnl.gov/conferences/images/6/65/ERD18ReportJan20v0.1.pdf

- Summary on DMAPS technology investigations:
  - https://wiki.bnl.gov/conferences/images/9/9a/ERD18_TJ-Summary-Jun19.pdf
  - https://doi.org/10.1016/j.nima.2019.163381

BACKUP

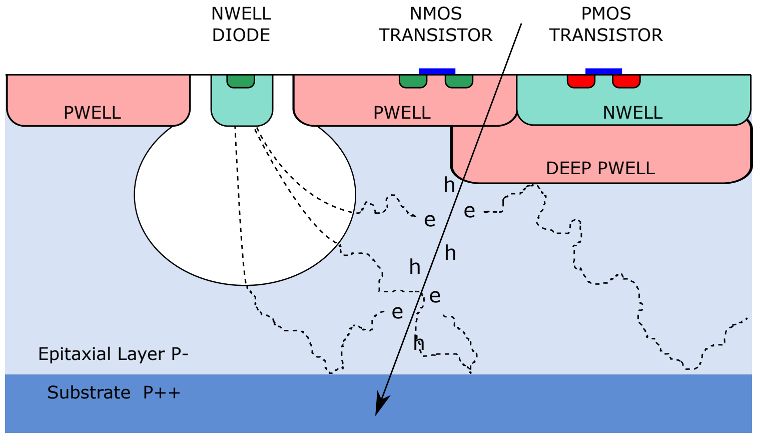
BILPA – Medical applications

- PRaVDA (Proton Radiotherapy Verification and Dosimetry Applications international consortium) using both large format CMOS and silicon strip with proposed future use of DMAPS for tracking
- ENLIGHT (CERN led hadron therapy consortium)
- STFC Network+ in Advanced Radiotherapy
- STFC+NPL Enhancement of the UK Primary Standard for Absorbed Dose for Proton Radiotherapy (DMAPS combined with NPL and RAL Microelectronics)
- Fast proton therapy verification with tracking detectors and calorimeters
- In-situ dose monitoring with prompt gamma rays at end of range
- MonteCarlo tools for medical applications

WP1: starting considerations and baseline

- Science drivers define the requirements for an EIC silicon vertex and tracking detector
  - Open heavy flavour decays – **high position resolution**
  - Precision tracking of high Q^2 scattered electrons – **low mass**

- Baseline: ALICE ITS **ALPIDE** sensor (state-of-the-art **MAPS**)
  - Partially depleted; charge **collection in part by drift**
  - Small collection electrode = **low detector capacitance** → low power, low noise, low crosstalk, fast readout



0.18 μm CMOS Tower Jazz
28 x 28 μm² pixel pitch
< 2 μs time resolution
Power density **< 50 mW cm^{-2}**
50 kHz interaction rate (Pb-Pb)
200 kHz interaction rate (pp)

Inner layer thickness = **0.3% X_0**
Outer layer thickness = 0.8% X_0

TID: 2.7 Mrad
NIEL: 1.7 x 10^{13} 1 MeV n_{eq} cm^{-2}

WP1: Towards an EIC-specific sensor

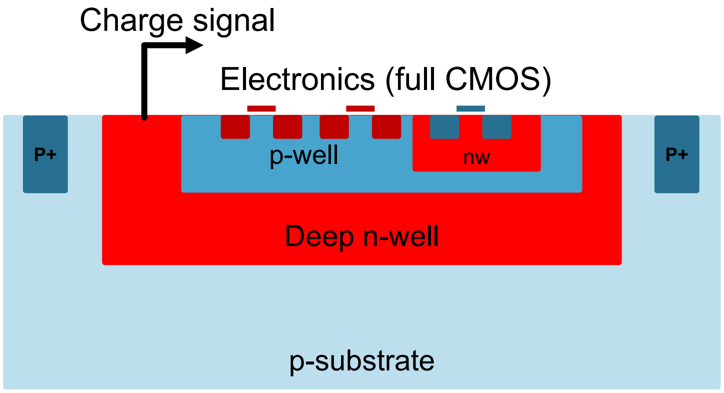
- Excerpt from EIC Detector Requirements and R&D Handbook

> *"The EIC would certainly benefit in **improvements in the integration time** as well as in a **further reduction of the energy consumption and material budget** going towards 0.1-0.2% radiation length per layer. Timing-wise the **ultimate goal of this technology would be to time stamp the bunch crossings** where the primary interaction occurred. […] Concerning spatial resolution the simulations indicate that **a pixel size of 20 microns** must be sufficient."*
>
> Electron-Ion Collider Detector Requirements and R&D Handbook, v4

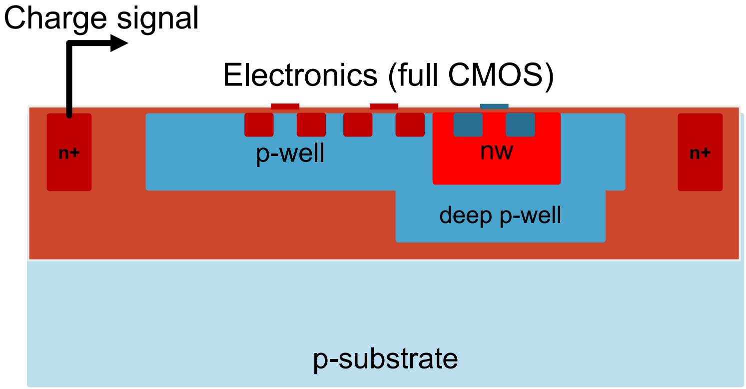
- Aim for **improved spatial resolution**
  - Smaller pixels, low power/mass (and careful mechanical design)
- Consider **readout requirements** for the EIC
  - Integration time and time-stamping capability
- eRD18 explored DMAPS technologies to match the required improvements
  - **Note**: at the time this work started in 2016 DMAPS were the evolution of MAPS
  - MAPS may now have an evolution of their own (see later slides on ITS3)

WP1: Depleted MAPS

- Main advantage is **charge collection by drift**
  - Achieved by full depletion of the substrate (**HV/HR CMOS**)
  - Faster and more complete charge collection
  - Less charge sharing between pixels
  - (also improved radiation hardness)



- Two approaches achieve to full depletion
  - Implement a **large collection electrode**
    - Approach followed in almost all technologies (for example: LFoundry, AMS)
    - Disadvantage: large capacitance
  - Introduce a **deep planar junction (only in TJ modified process)**
    - Advantage: small collection electrode (few μm^2)



WP1: survey of DMAPS technology

- This work was presented in July 2018 – **needs updating!**
  - https://wiki.bnl.gov/conferences/images/d/dc/ERD18-Report-FY19Proposal-Jun18.pdf
- State-of-the-art DMAPS prototypes, mainly developed for application at the HL-LHC, optimised for high particle fluences, radiation hardness and fast readout

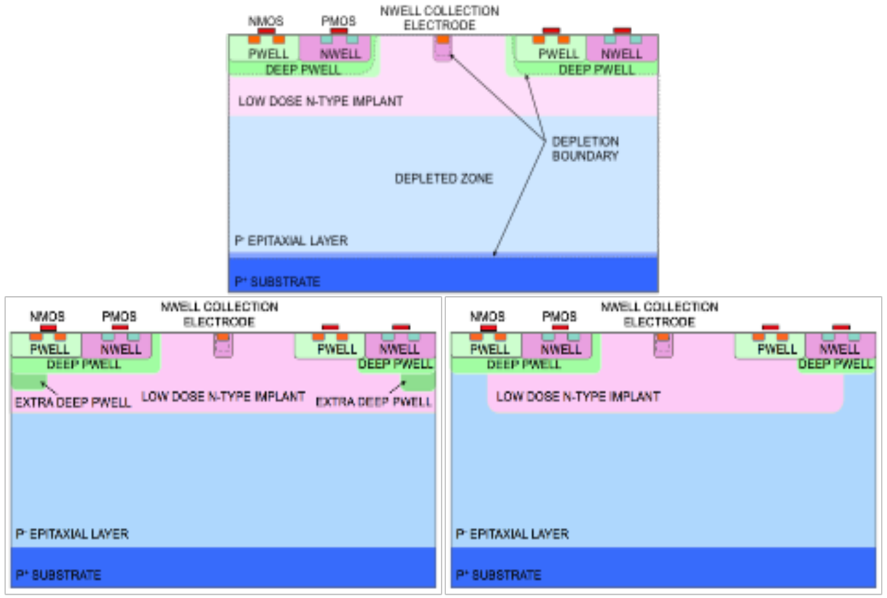
DMAPS

	ALPIDE	MALTA	TJ-MONOPIX	LF_MONOPIX	ATLASpix_Simple
Experiment	ALICE ITS	ATLAS ITk pixel Phase II (outermost layers only)			
Technology	TJ 180 nm	Modified TJ 180 nm		LF 150 nm	AMS 180 nm
Substrate resistivity [kOhm cm]	> 1 (epi-layer 18-25 um)			> 2	0.08 - 1
Collection electrode	small	small	small	large	large
Detector capacitance [fF]	<5			Up to 400	
Chip size [cm x cm]	1.5 x 3	2 x 2	1 x 2	1 x 1	0.325 x 1.6
Pixel size [um x um]	28 x 28	36.4 x 36.4	36 x 40	50 x 250	40 x 130
Integration time [ns]	4×10^3	<25			
Particle rate [kHz/mm^2]	10	10^3			
Readout architecture	Asynchronous		Synchronous, column drain		
Analogue power [mW/cm^2]	5.4	< 120	~ 110	~ 300	N/A
Digital power [mW/cm^2]	31.5/14.8	N/A	N/A	N/A	N/A
Total power [mW/cm^2]	36.9/20.2	N/A	N/A	N/A	N/A
NIEL [1MeV n_{eq}/cm^2]	1.7×10^{13}	1.0×10^{15}			
TID [Mrad]	2.7	50			

- A DMAPS sensor for the EIC would benefit from having a **small collection electrode** → small pixel pitch, low power analogue FE design
- The **TJ 180 nm modified** process is the only one providing **full depletion with a small collection electrode**

WP1: TJ 180 nm CIS process modified

- Developed by CERN-TJ collaboration for HL-LHC tracker upgrades
  - Deep planar junction allows full depletion with small collection electrode
  - Various sensor variants exists for optimised charge collection



- eRD18 studied the performance of this technology with various prototypes in lab and test beams
- More complete and faster charge collection wrt standard TJ process (i.e. ALPIDE) demonstrated
- Results are summarised here
  - https://wiki.bnl.gov/conferences/images/9/9a/ERD18_TJ-Summary-Jun19.pdf
  - https://doi.org/10.1016/j.nima.2019.163381

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