## EIC "Readout and DAQ" working group

Kick-off meeting February 17<sup>th</sup>, 2020

## Remarks concerning DAQ and trigger

Strongly depends on the kind of detector to read / physics to measure / background rates. Some general questions can be worked on now.

- Triggered or triggerless DAQ?
  - Identify pro/cons for each strategy focus on general arguments rather than technical/economical details. Possibly
    provide experimental data (or at least simulations) to support these arguments.
    - Technical/economical reasons are important, but all numbers will be very different when the EIC will be built.
  - Event definition and construction?
    - Are we ok with the paradigm "1 trigger == 1 event" in the triggered case?
    - Do we save "events" in the triggerless case, or just time-stamped hits / reconstructed quantities?
  - Effect on the physics to be measured / strategies to validate the trigger?
- DAQ
  - Do we need a new DAQ infrastructure or can we adapt/reuse existing systems? *Depends on answer to question before.*
  - $\circ$  Complexity of trigger/filter decision?  $\rightarrow$  How many trigger/filter levels?
  - How to implement online software filtering (relevant for triggerless system and for a L3 software trigger level)?
    - Interconnection with the reconstruction software is critical
  - How to simulate the trigger / filtering?

## Remarks concerning DAQ and trigger

More technical issues:

- Triggered case:
  - Size of the analog array? Digitization rate? *Depends on the input rate / number of channels*
  - Time available for trigger decision, i.e. front-end maximum latency?
  - How to distribute timing to FE?
- Triggerless case:
  - Digitization rate? Size of the memory buffer? *Depends on the input rate / number of channels*
  - Identify existing chips / readout solutions compatible with a triggerless architecture, do we need something new?
  - How to distribute timing to FE and associate it to the streamed data?