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***Electronics/DAQ sub working group for the
EIC yellow report***

1st meeting

Damien Neyret

CEA Saclay IRFU/DPhN

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Introduction to the Electronics/DAQ subWG

Motivations and methods

Bring peoples from different laboratories together to imagine realistic scenarios for the readout electronics and DAQ system of the future EIC experiments

Strong links to build with:

- detector WG → What detector we will have to read ? Expected signal flux ?
- physics and simulation WG → What signal to read ? What background to reject ? Which rate for each ?

12 to 18 months to produce ~15 pages for the yellow report

SubWG meeting every ~2 weeks

All opinions, all ideas will be always welcome ! (but please bring arguments to defend them...)

WG conveners

Andrea Celentano

Physicist at INFN-Genova

Worked on

- JLab Hall-B CLAS/CLAS12 experiments (trigger validation)
- JLab HPS experiment (ECal gain monitoring system)
- JLab BDx experiment (trigger and DAQ responsible)

Damien Neyret

Physicist at CEA Saclay IRFU/DPhN (Gif sur Yvette, France)

Worked on

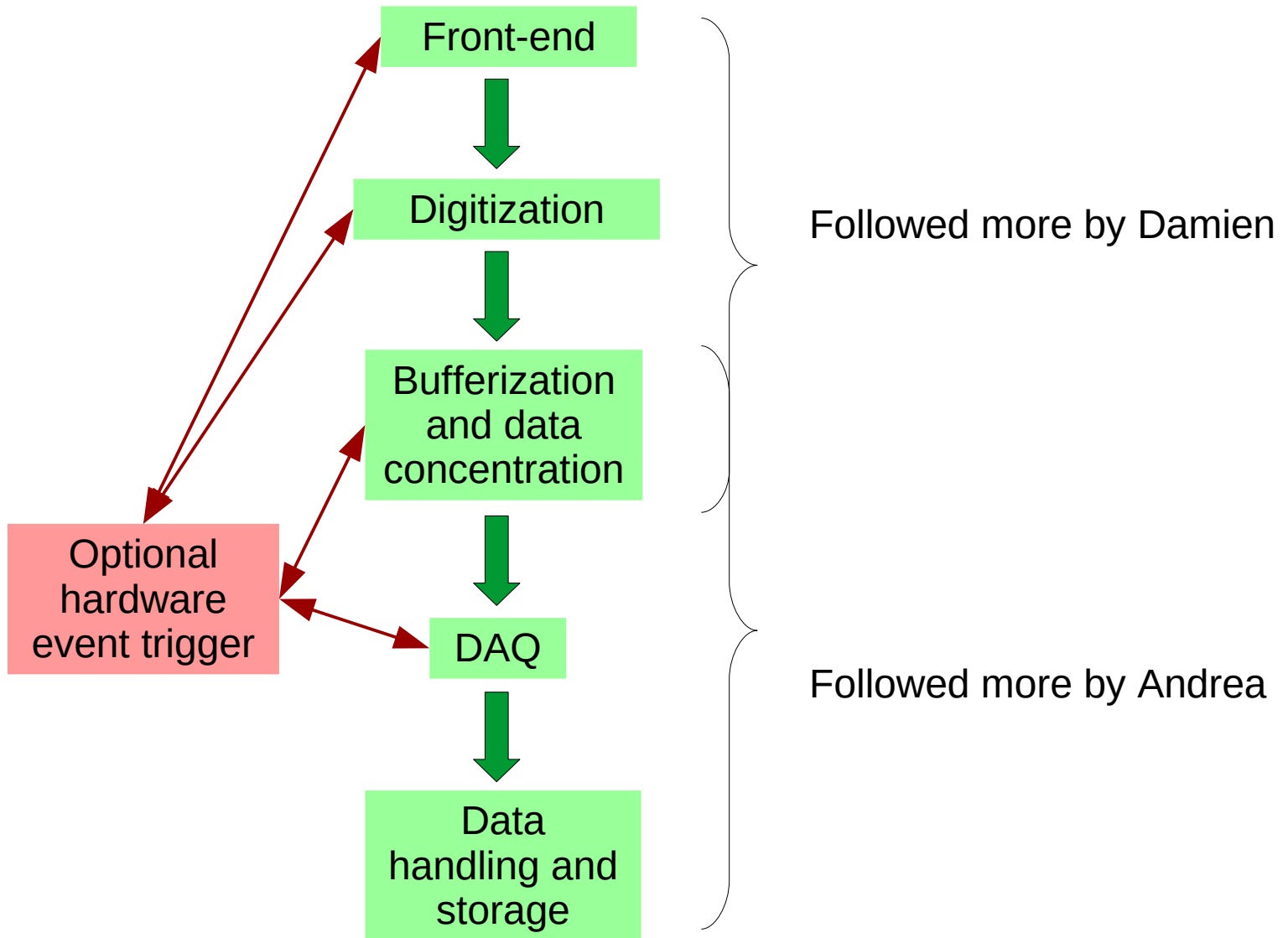
- JLab Hall A electron beam polarimeter (photon calorimeter + read-out/DAQ)
- Compass experiment at Cern (Micromegas and hybrid gaseous detectors, drift chambers, SFE16 and APV front-ends, DAQ system, data reconstruction)
- PandaX-III experiment at Jinping underground lab, China (Micromegas Microbulk detectors, AGET read-out, simulations)

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Topics covered by the subWG



Remarks on front-end part

Strongly depends of kind of detector to read

Amplitude and shape of the signals

Detector capacitance

Number of channels

Measurement to be done: amplitude, timing, position (barycenter of channels)

What resolution for each kind of measurement ? What peaking time ?

What context: particle fluxes, electronics occupancy, electronics noise level

First steps to reach

Overview on kind of detectors to read → contacts to take with detector WG

Present state of the art on read-out electronics: existing chips for each kind of detectors, foreseen evolutions

Projects on future read-out chips ?

Digitization and bufferization

Depends of scheme on software or hardware trigger (cf Andrea's talk)

Storage of analog signal and delayed digitization, or on-line digitization ?
Sampling rate ? Time to wait for trigger decisions ? Time between consecutive triggers ?
Size of buffers ? Digitization rates ?

First steps to reach

Evaluation on hardware vs software trigger systems
List of needs in term of rates, event sizes, data fluxes, etc...

Hardware aspects

ADC and TDC chips ? usage of FPGA as digitizers ?
Case of front-end chips with integrated digitization ?
Etc...

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Spares

