

# sTGC project summary

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BNL

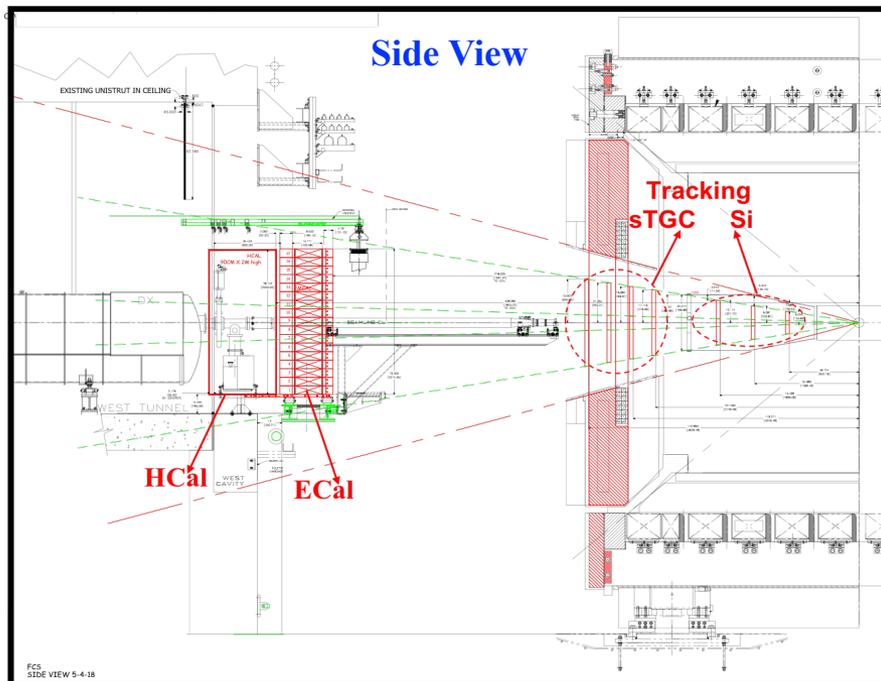
Introduction

The project

The prototype performance at STAR

Summary

# STAR forward upgrade for $2.5 < \eta < 4$



Calorimetry:  
Electromagnetic and Hadronic

Tracking:  
Silicon detectors and  
small-strip Thin Gap Chambers (sTGC)

pp, pA and AA data taking in FY2021/22 and  
parallel with sPHENIX data taking period

**AA physics at 200 GeV for 2023-2025:**  
**Constrain 3D hydro evolution**  
**Temperature dependent  $\eta/s$**   
**Rapidity dependent vorticity**

**Successful cost and schedule review on  
Nov 19, 2018, BNL**

# Key Performance Requirements

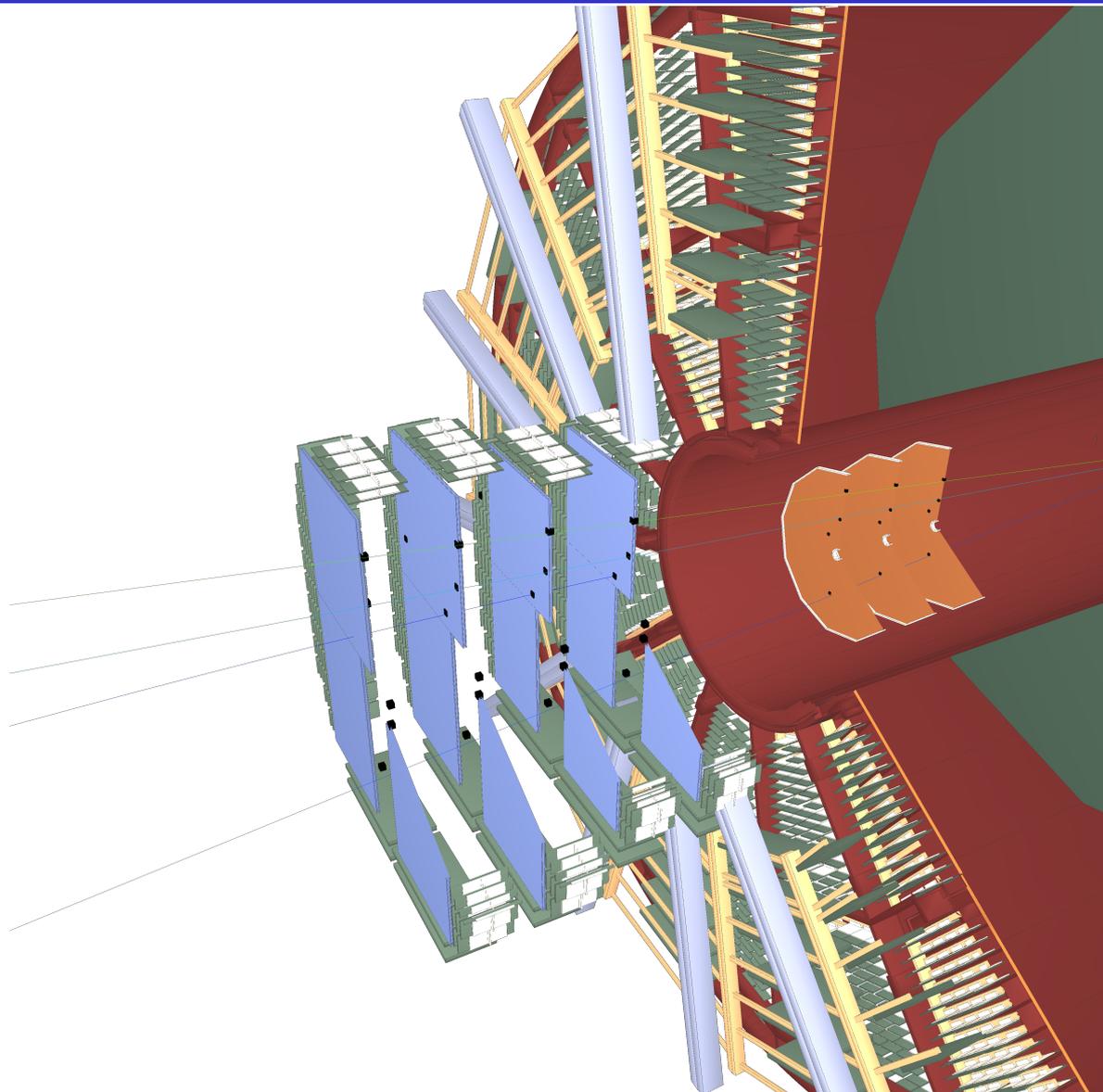
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**Charged sign separation for cold QCD physics**

**Momentum resolution 20-30% for peripheral heavy ion physics**

<b>Detector</b>	<b>pp and pA</b>	<b>AA</b>
<b>ECal</b>	$\sim 10\%/\sqrt{E}$	$\sim 20\%/\sqrt{E}$
<b>HCal</b>	$\sim 50\%/\sqrt{E} + 10\%$	---
<b>Tracking</b>	charge separation photon suppression	$0.2 < p_T < 2 \text{ GeV}/c$ with 20-30% $1/p_T$

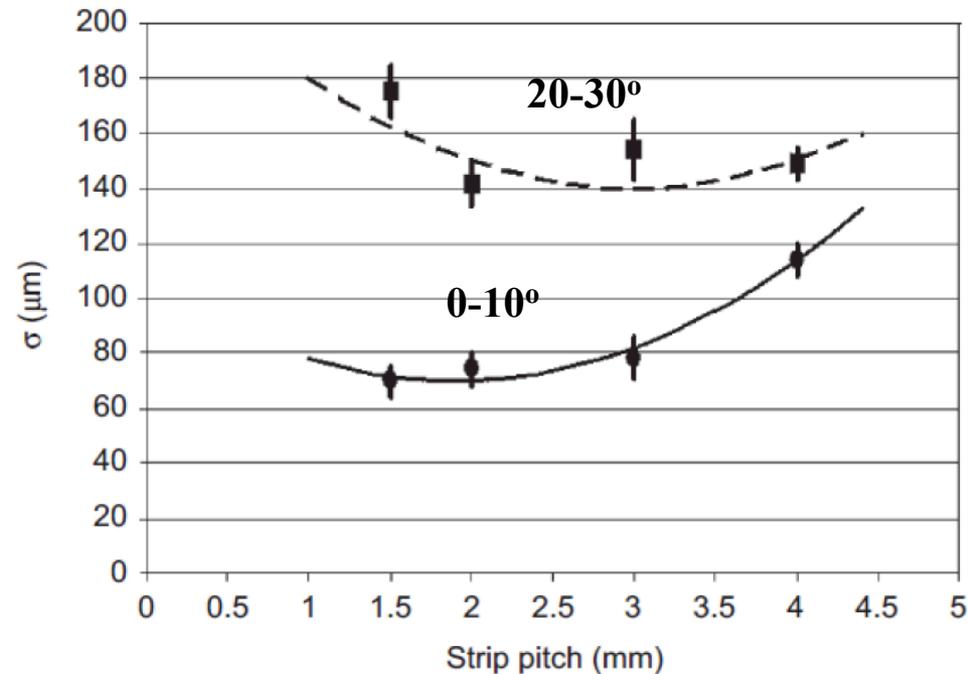
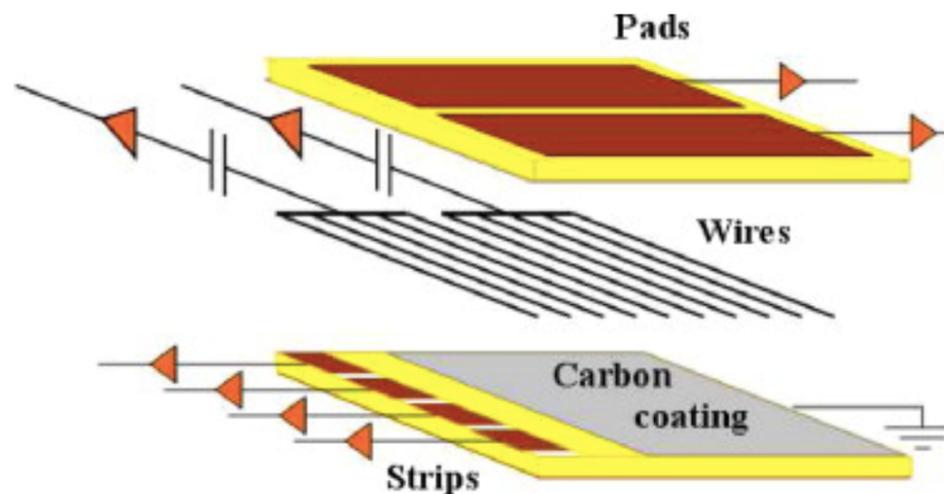
# The tracking



# The sTGC

Four double-sided, pentagon-shape sTGC with x, y, and diagonal-direction readouts will form a disk. We will have ~22000 readout channels in total.

The sTGC module is much smaller than ATLAS sTGC.  
All the PCB boards can be fabricated in China.



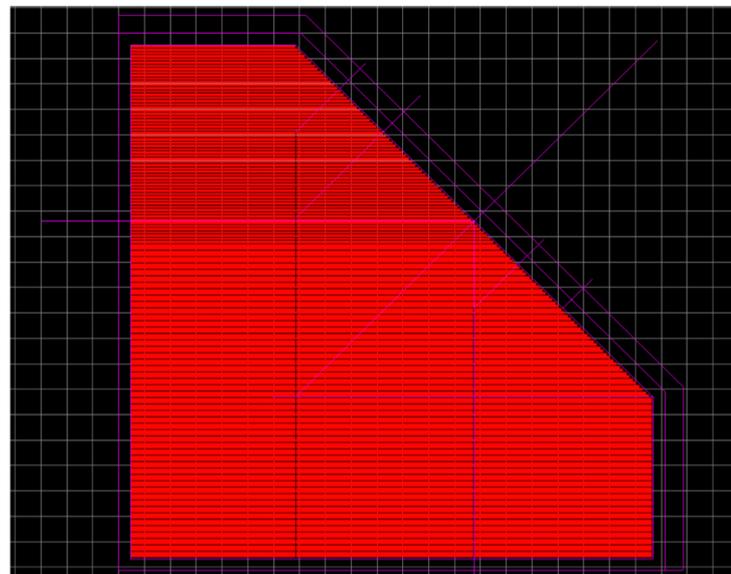
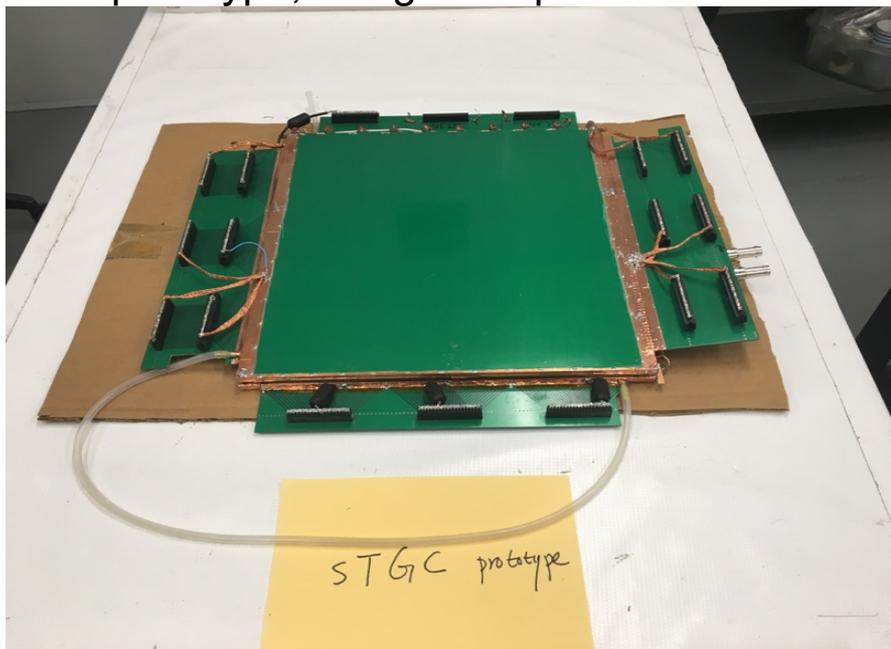
# sTGC module production

Shandong University (SDU) will produce all the **pentagon-shape** modules.

For the 30\*30 cm<sup>2</sup> prototype, we successfully integrated it to STAR; the efficiency at clean room test showed >98% with optimal gas.

For 60\*60 cm<sup>2</sup> prototype, efficiency > 95%, detailed study of position resolution ongoing at SDU.

For final prototype, design completed.

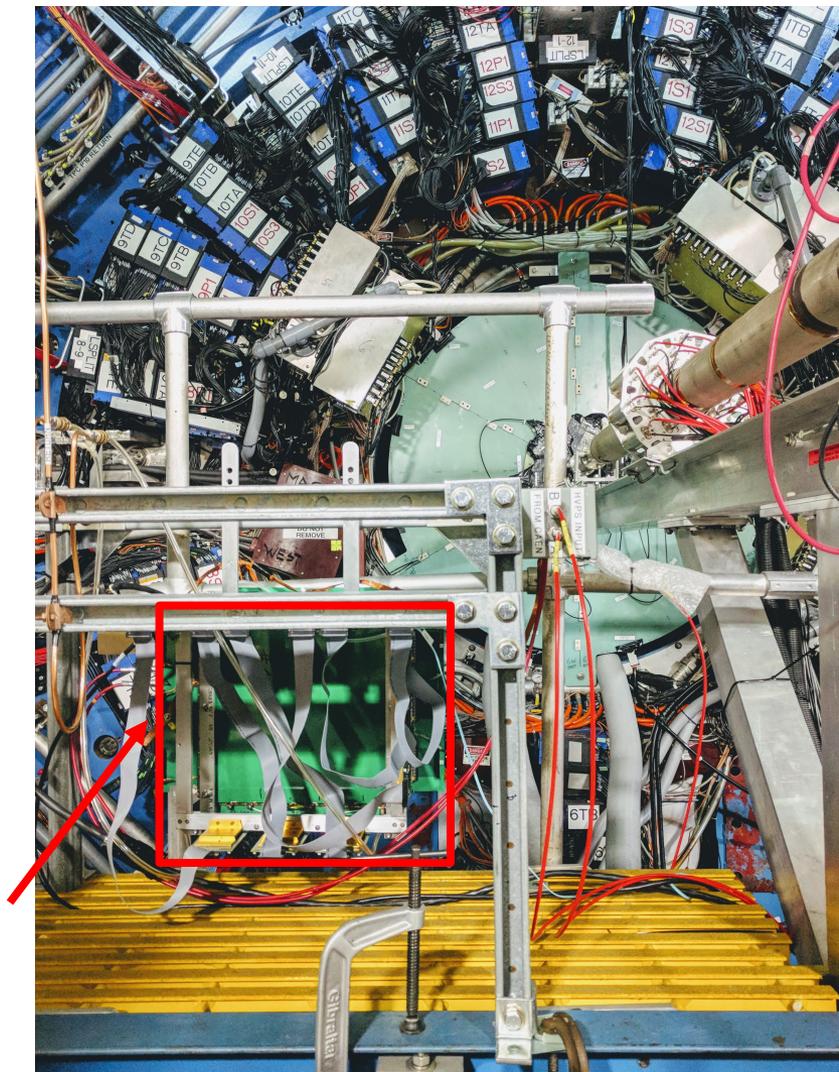


# sTGC prototype at STAR in 2019

Prototype installed on  
June 5, 2019 at STAR

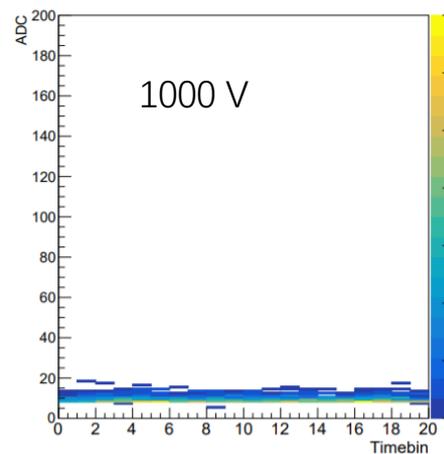
Gas: C10

Performed a voltage  
scan at 7.7 GeV and  
9.2 GeV Au+Au run,  
and took data in 200  
GeV Au+Au

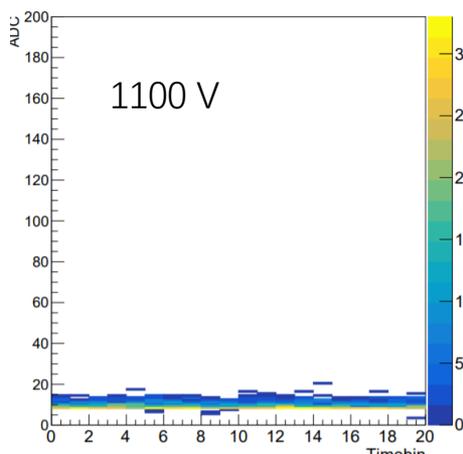


# Time bin vs ADC with different high voltages

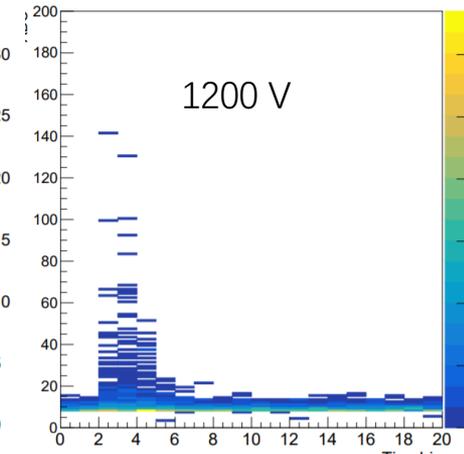
Timebin vs ADC (Top)



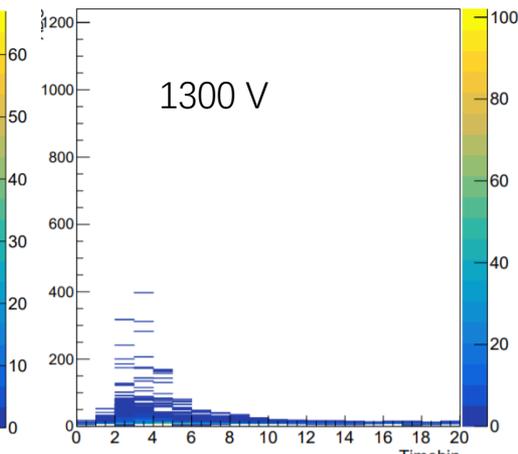
Timebin vs ADC (Top)



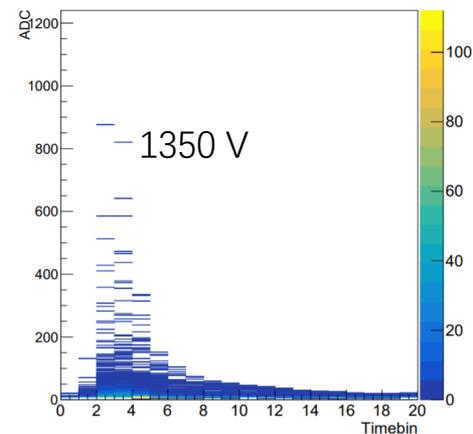
Timebin vs ADC (Top)



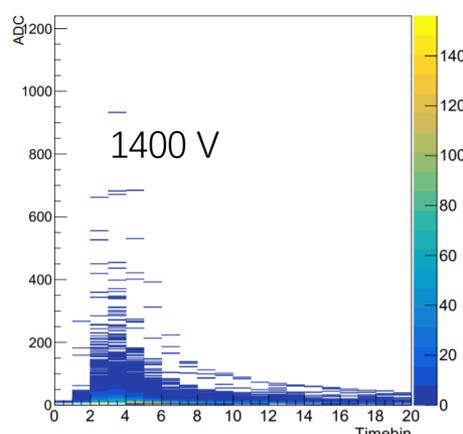
Timebin vs ADC (Top)



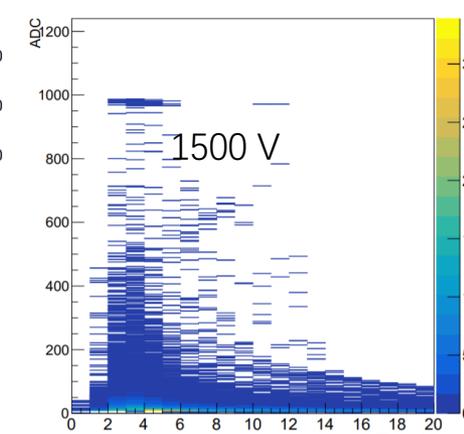
Timebin vs ADC (Top)



Timebin vs ADC (Top)



Timebin vs ADC (Top)



Maximums of y axis in  
1300V , 1400V, 1350V,  
1500V are 1200

Maximums of y axis in  
1000V , 1100V, 1200V,  
are 200

# Schedule presented on 11-19-2018

## Milestones:

Aug 2019, sTGC R&D completed (build another two 60 cm ✕ 60 cm modules)

Sep 2019, sTGC mass production readiness review

Oct 2019 to Oct 2020, mass production of 32+8 (spare) sTGCs

**May 2021, Last batch of sTGCs installed at STAR**

**Schedule float: 6 months**

SDU made a detail assessment for the production time:

#	Step	Duration(hour)
1	Material inspection/cleaning	14
2	PPPCB masking tape pasting	2
3	Graphite mixing/spraying/polishing	8
4	Half-chamber production, HV burn-in	48
5	wire winding, soldering, washing	24
6	Two half combination	24
7	Air tap installation and sealing	48
8	Gas leak inspection and repairing	4
9	Flow in CO2 HV burn-in	12
10	Flow in CO2+N.P X-ray test	24
11	CO2 washing residual N.P.	12

**About 9 days per chamber, including preparation and testing.**

In addition, the ALTAS sTGC production project will end in Aug-Sep, 2019.

If using their technicians, SDU can finish the project in 4-6 months after mass production is started

# Module production schedule

Current STAR sTGC Production Plan at Shandong University, Dec.12<sup>th</sup>, 2019

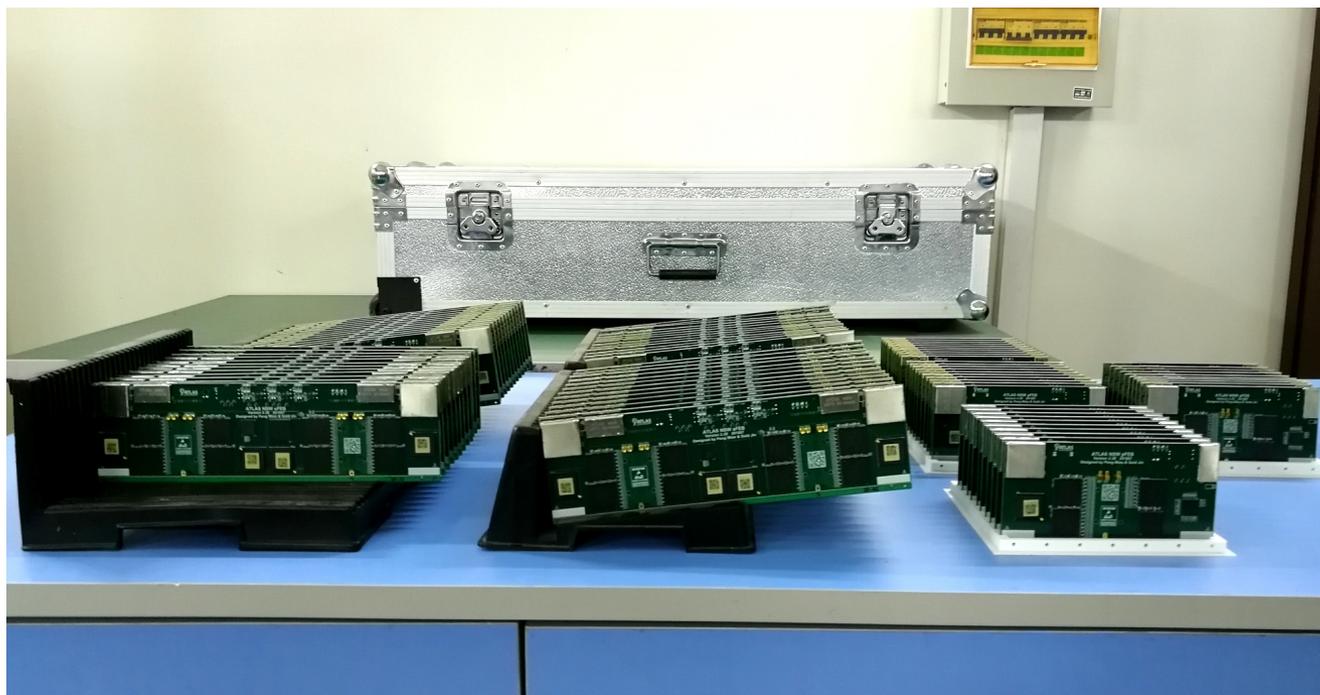
	2019	2020												2021					
	DEC	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC	JAN	FEB	MAR	APR	MAY	JUN
Pentagon Prototype Design	█																		
Vendor Production		█																	
Prototype Production			█																
Final Design				█															
Vendor Production								█											
Mass Production								4 stations shipped by Oct. 2020			5 stations shipped by Jan. 2021			7 stations shipped by Apr. 2021			4 stations shipped by Jun. 2021		

- Need 9 days per chamber, 15 days (3 weeks) per station.
- Parallel work has already been considered.

  
 16 stations shipped

# Electronics: based on VMM chips

- 4 chips per board, 96 FEE boards in total.
- 16 ROD boards
- USTC (Prof. Jin Ge and Dr. Feng Li) are designing the board.



The chips (464 needed) will be purchased through BNL. **Waiting for CERN to provide the info on the exact funds we need transfer for chips (25 ladders) and packaging.**  
**Paperwork on subcontract purchase order of electronics boards through BNL is ongoing**

# Electronics design schedule

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- Schematics of FEB prototype be done in late Feb. Board layout completed in March.
- Schematics of ROD prototype be done in March. Board layout completed in early April.
- FEB and ROD manufacturing and assembly be done in April, then integration test at SDU for 2-3 months(start from May).
- ROD firmware development to work compatible with STAR DAQ from July. Two USTC people will go to US to work with BNL guys.
- Prof. Jin and Dr. Feng Li intend to visit BNL in June or July: FEB site test, ROD interface protocol with STAR DAQ, other site problems for experiments.
- Final design completed before October.
- After mass production, all boards can be shipped to BNL before December.



# Final remarks

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1. Electronics: continue to push for an answer from CERN and from BNL
2. Module production: need a readiness review before mass production in summer
3. Gas: need to install all the components at STAR and test them in run 2020
4. Integration: more frequent communication need happen between SDU+USTC (Chi/Feng) and BNL (Rahul)
5. Software simulation: need to develop clustering algorithm with high efficiency (prototype run in 2020)
6. Visa denial: we need provide a virtual STAR drawing/video and do more email exchanges related to STAR