Development of the SiREAD based readout solution for the Particle Identification Detectors of the EIC

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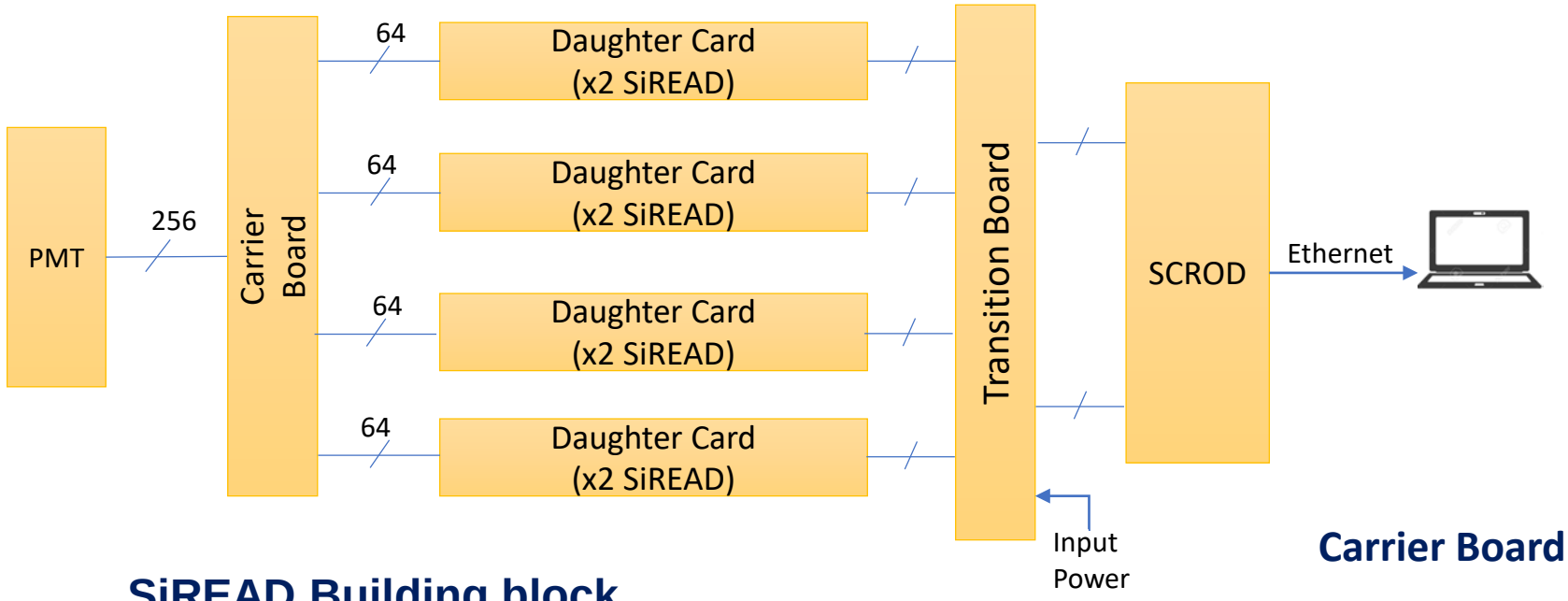
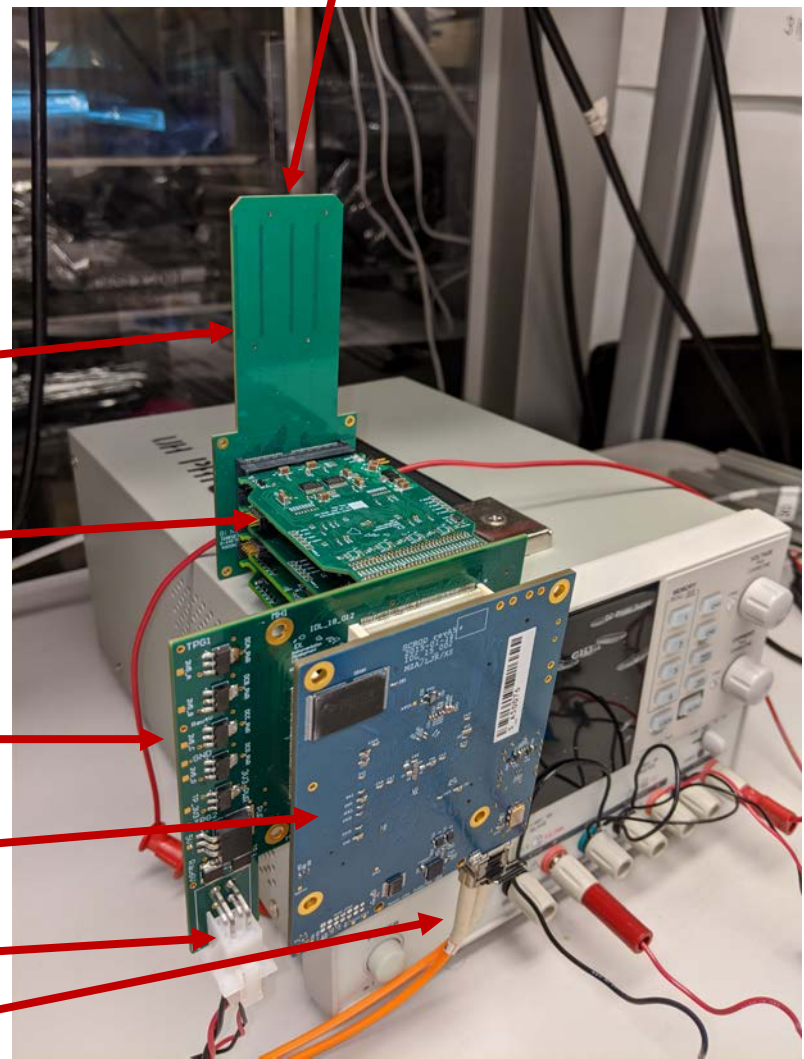
eRD14 PID Consortium Meeting
May 25, 2020

University of Hawai'i Mānoa

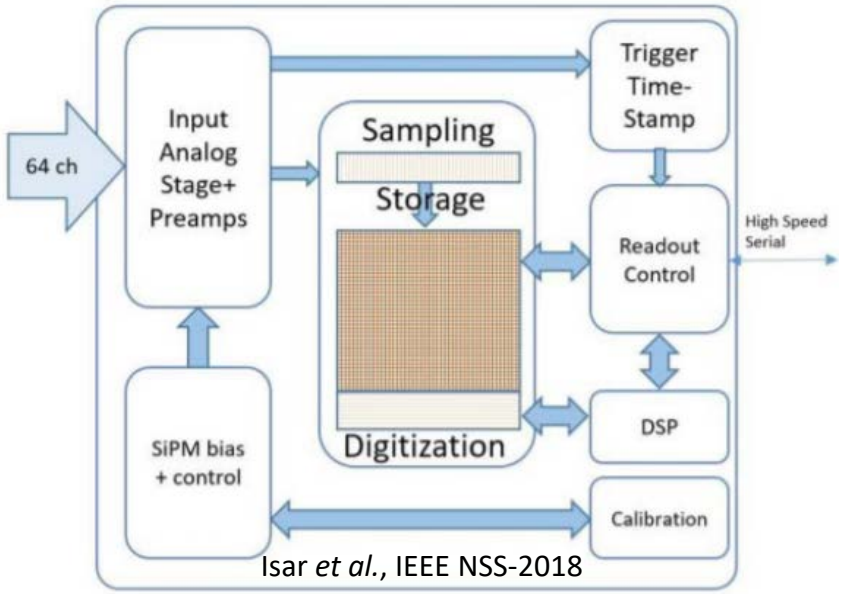
Readout Electronics for mRICH Detectors



PMT would be mounted on the other side of the Carrier Board



SiREAD Building block

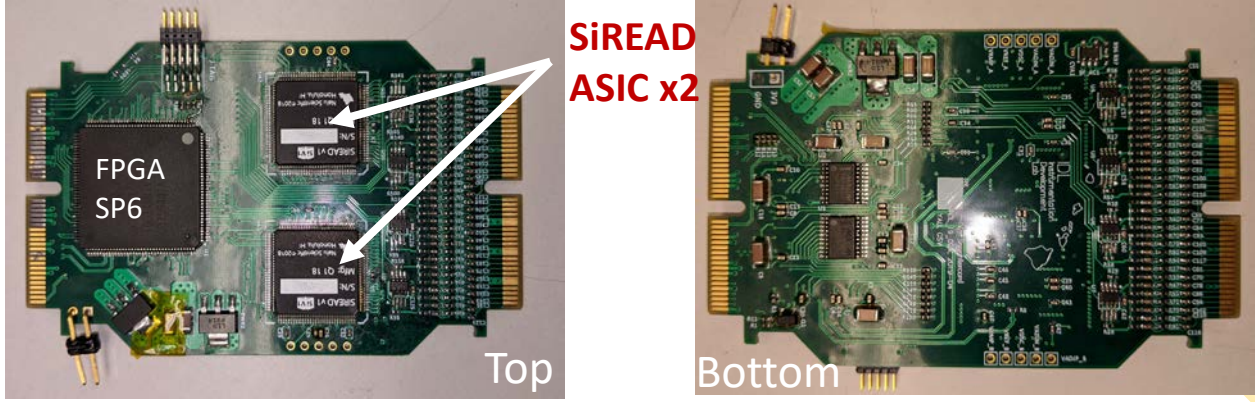


Isar *et al.*, IEEE NSS-2018

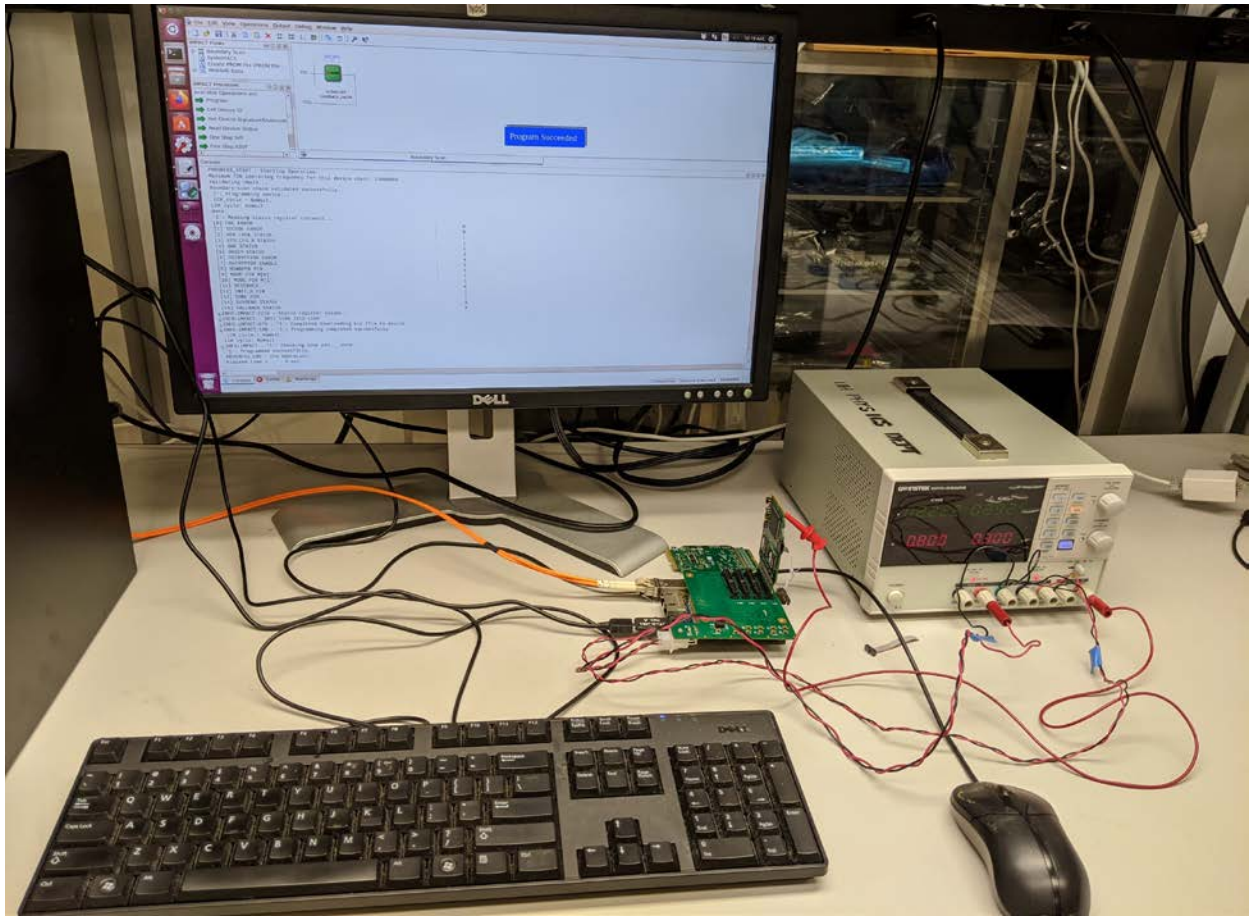
SiREAD Parameter	Specifications
Channels	32
Sampling rate	1 GSa/s
Storage samples/ch	4096
Est. Analog BW	0.7-1.1 GHz
RMS voltage noise	1.3 mV
Signal voltage range	2.1 V
ADC on chip	12 bits
Readout	Serial LVDS
Power consumption	20-40 mW/ch

Development Status

- 25 Nos. of SiREAD Daughter Cards (IDL_19_004) have been fabricated
- The first version of the SiREAD DC firmware has been developed and ready for initial testing
- The communication between PC and SCROD FPGA has been tested with old firmware
- Upgradation of the SCROD FW is underway to implement the communication between SCROD and DCs
- Team from Nalu Scientific is actively involved and accelerated the development of firmware

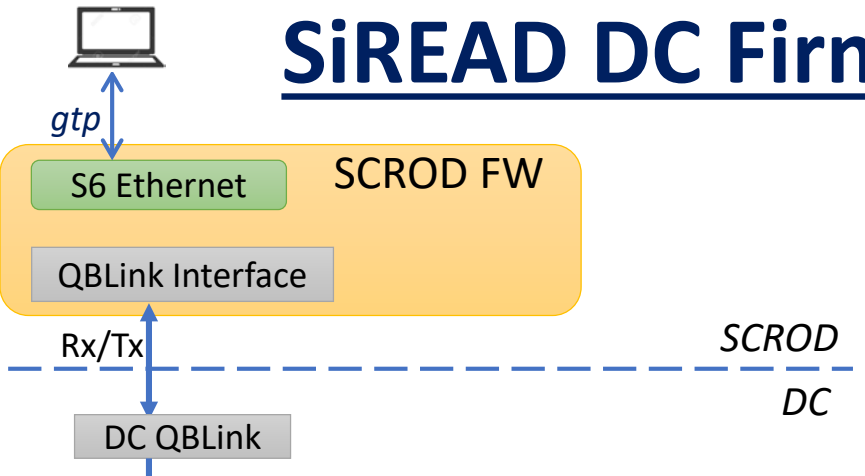


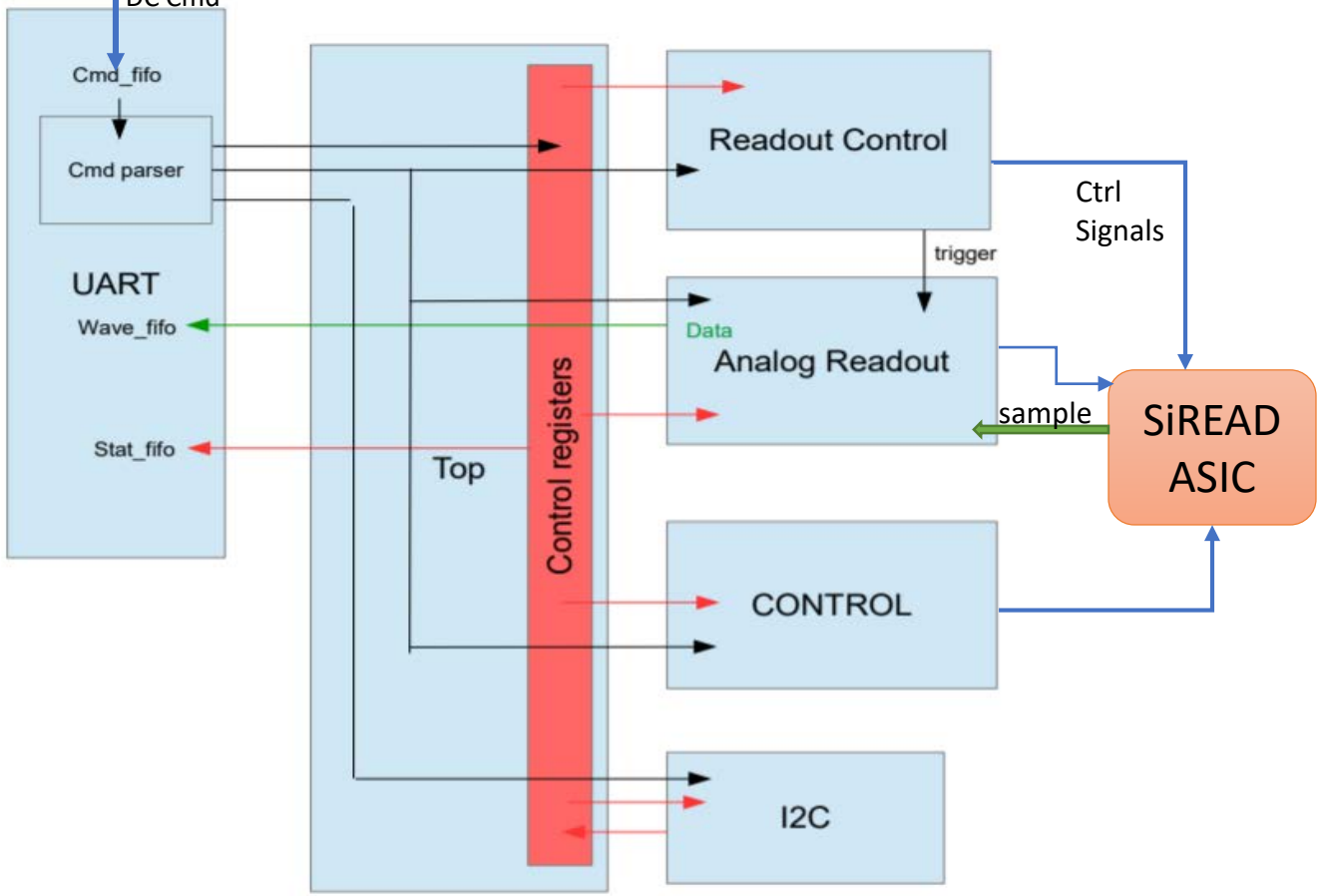
SiREAD Daughter Card



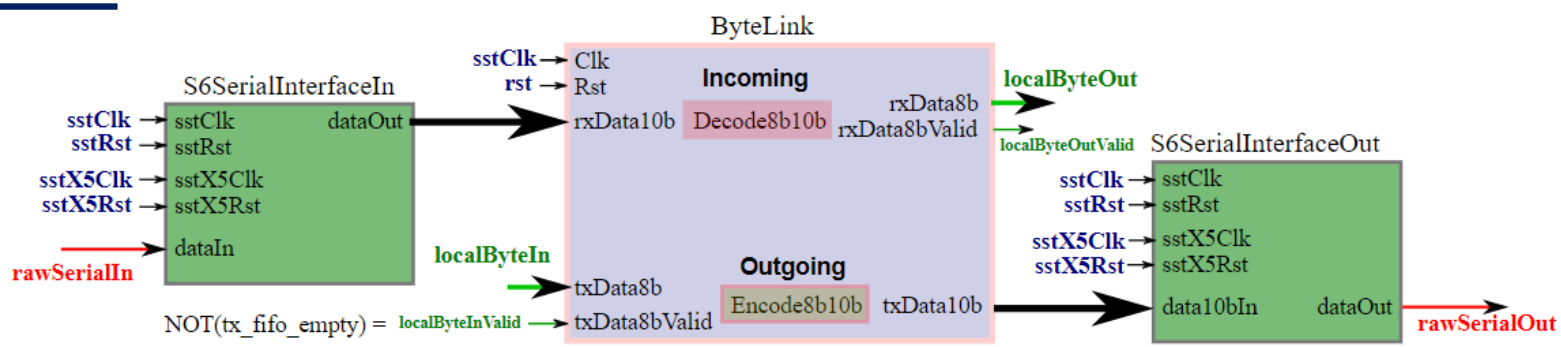
DC powered up and programmed successfully with the first version of the FW

SiREAD DC Firmware





Quad Byte line (QBlink)



- Communication link between the SCROD and DCs is maintained using **QBLink**
- **Readout Control:** starts and stops acquisitions and handles triggers
- **Analog Readout:** handles the control of the SiREAD ASIC including write/read location and the actual readout
- **CONTROL:** writes the analog register

Plan Ahead

Activities Planned	Time-line
Upgradation of SCROD FW	May 2020
Testing, Verification & debugging of: • SCROD communication with PC (optical link, Reg Readback) • SCROD communication with DC (QBLink module) • DC Register Readback	Summer 2020
Hardware Test with 4 DCs & PMT	Early Autumn 2020
Characterization of timing, noise and trigger rate performance	Late Autumn 2020