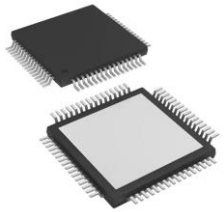
Readout Electronics Status

Migration to FELIX underway…

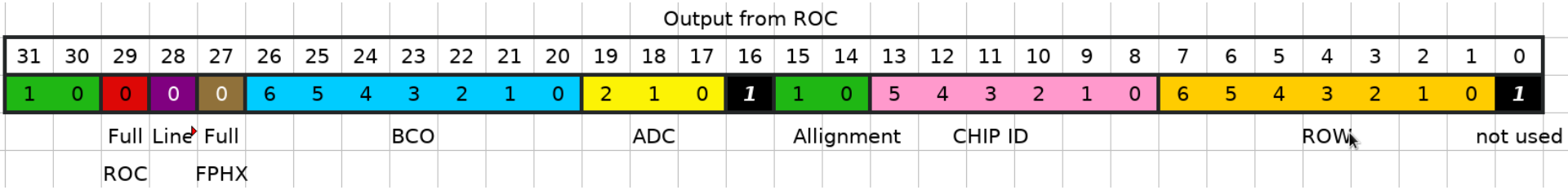
- Using Xilinx KCU105 evaluation board
  - Kintex UltraScale FPGA.
  - FELIX's "little brother".
  - Uses same transceiver architecture as FELIX
    - GTH supports up to 16.375 Gbit/s line rate.
    - 18 GTH transceivers, PCIe3 x8 lane.



- ROC uses a **TLK2711-SP** transceiver.
  - 2.5 Gbit/s @ 125 MHz.
    - 16-bit * 125 MHz results in 2 Gbit before 8b/10b encoding.
  - Idle word different than other TLK transceivers.
- Configured the GTH for 2.5 Gbit/s with a 125 MHz local reference clock.
  - Lock onto K.28.7 idle word, positive comma

Readout Electronics Status

– Need to better understand data from the ROC



– Data split across two TLKs
  - Dealing with synchronization across TLKs
  - Can you have a 16-bit word miss-aligned between two TLKs?
    – We Think so...
– Need to confirm proper idle word.
– Slow control and clock distribution needs to be explored.

Readout Electronics Status

- **Development Roadmap:**
- Understand ROC protocol.
  - VHDL testbench from LANL would help
  - Review documentation.
  - Dual link synchronization would be the most pressing issue.
- GTH Transceiver configuration and testing.
- Need a MPO/MPT to LC breakout cable
  - Fiber map, which fibers to which TLK.
- Fake data pattern generator in lieu of a real ROC .
- Slow control protocol and interface.
- ROC data de-packetization, parsing, merging, then PCIe DMA.
- Start developing PCIe software stack for INTT.