Readout Electronics Status

Migration to FELIX underway…

- Using Xilinx KCU105 evaluation board
- Migration of simulation fro ISE 7.1 to Vivado...
- Simulating sub event building and send packet block.
- Currently, no PCIe block yet...
- **Packet Structure Definition**
  - **FEM ID followed by:**
    - **A[2:0] → ADC Data, C[5:0] → Chip ID, R[6:0] → Row**

15	E	0	X	W	Y	Z	R6	R6		R6	Z	R6		R6	S	1
14	E	1	X	W	Y	Z	R5	R5		R5	Z	R5		R5	S	1
13	E	0	X	W	Y	Z	R4	R4		R4	Z	R4		R4	S	1
12	E	1	X	W	Y	Z	R3	R3		R3	Z	R3		R3	S	1
11	E	0	X	W	Y	0	R2	R2		R2	0	R2		R2	S	1
10	E	1	X	W	Y	0	R1	R1		R1	0	R1		R1	S	1
9	E	0	X	W	Y	0	R0	R0		R0	0	R0		R0	S	1
8	E	1	X	W	Y	0	C5	C5		C5	0	C5		C5	S	1
7	E	0	X	W	Y	0	C4	C4		C4	0	C4		C4	S	1
6	E	1	X	W	Y	0	C3	C3		C3	0	C3		C3	S	1
5	E	0	X	W	Y	0	C2	C2		C2	0	C2		C2	S	1
4	E	1	X	W	Y	0	C1	C1		C1	0	C1		C1	S	1
3	E	0	X	W	Y	0	C0	C0		C0	0	C0		C0	S	1
2	E	1	X	W	Y	0	A2	A2		A2	0	A2		A2	S	1
1	E	0	X	W	Y	0	A1	A1		A1	0	A1		A1	S	1
0	E	1	X	W	Y	0	A0	A0		A0	0	A0		A0	S	0
bit	Event	Flag Word	Det. ID	Mod Add	BCO	FEM_ID	DATA_0	DATA_1	...	DATA_m	FEM_ID	DATA_0	...	DATA_m	CRS	EOP
		Header								Data section					Trailer	

A0-A2 - ADC value for hit
C0 - C5 = chip ID for hit
R0 - R6 = channel number for hit

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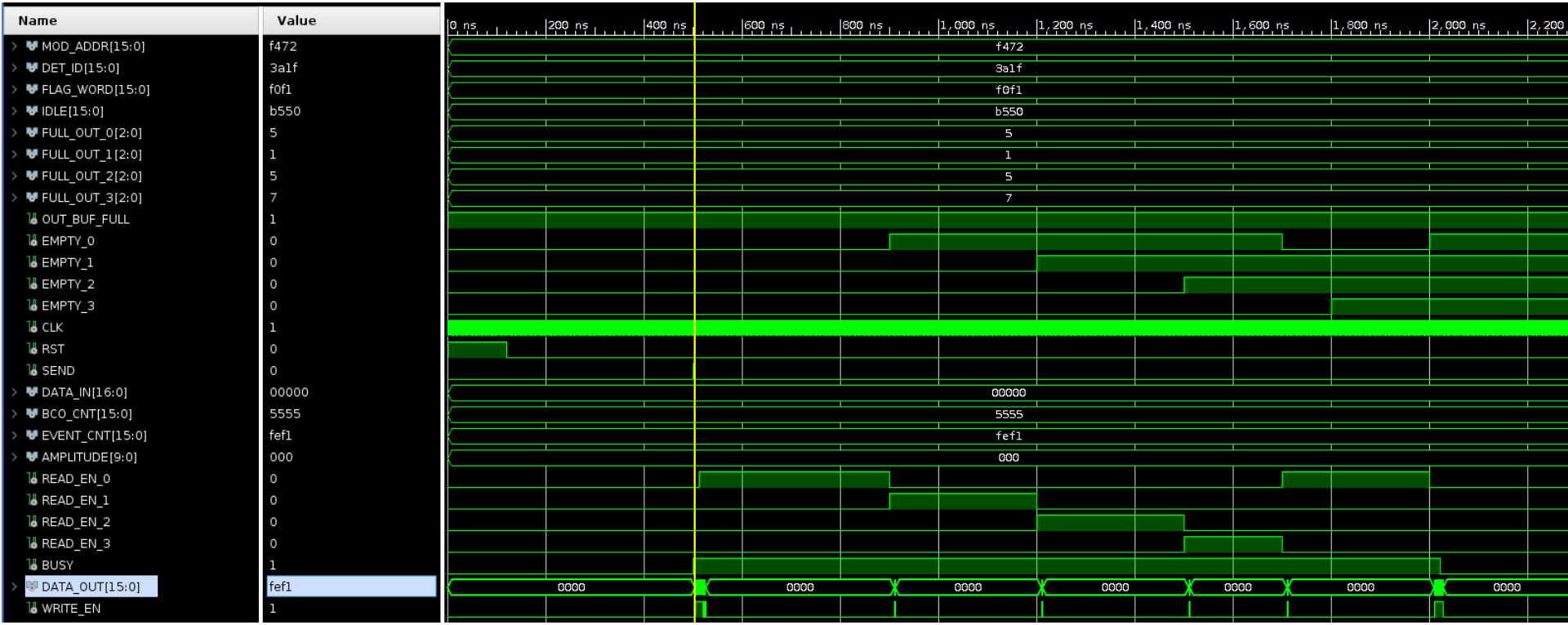
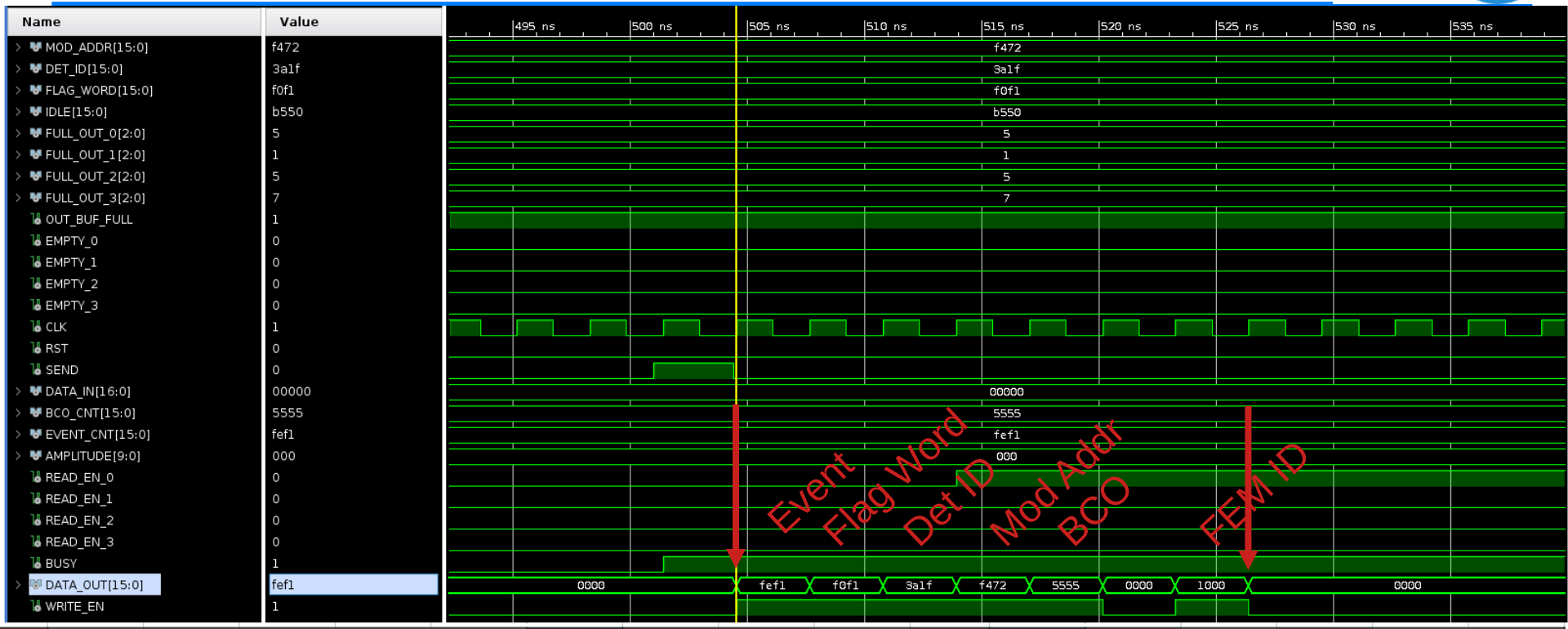
Simulation of Send Packet Block:

- Conforms to the packet structure definition, high level overview:



Readout Electronics Status



bit	Event	Flag Word	Det. ID	Mod Add	BCO	FEM_ID	DATA_0	DATA_1	...	DATA_m	FEM_ID	DATA_0	...	DATA_m	CRS	EOP
15	E	0	X	W	Y	Z	R6	R6		R6	Z	R6		R6	S	1
14	E	1	X	W	Y	Z	R5	R5		R5	Z	R5		R5	S	1
13	E	0	X	W	Y	Z	R4	R4		R4	Z	R4		R4	S	1
12	E	1	X	W	Y	Z	R3	R3		R3	Z	R3		R3	S	1
11	E	0	X	W	Y	0	R2	R2		R2	0	R2		R2	S	1
10	E	1	X	W	Y	0	R1	R1		R1	0	R1		R1	S	1
9	E	0	X	W	Y	0	R0	R0		R0	0	R0		R0	S	1
8	E	1	X	W	Y	0	C5	C5		C5	0	C5		C5	S	1
7	E	0	X	W	Y	0	C4	C4		C4	0	C4		C4	S	1
6	E	1	X	W	Y	0	C3	C3		C3	0	C3		C3	S	1
5	E	0	X	W	Y	0	C2	C2		C2	0	C2		C2	S	1
4	E	1	X	W	Y	0	C1	C1		C1	0	C1		C1	S	1
3	E	0	X	W	Y	0	C0	C0		C0	0	C0		C0	S	1
2	E	1	X	W	Y	0	A2	A2		A2	0	A2		A2	S	1
1	E	0	X	W	Y	0	A1	A1		A1	0	A1		A1	S	1
0	E	1	X	W	Y	0	A0	A0		A0	0	A0		A0	S	0

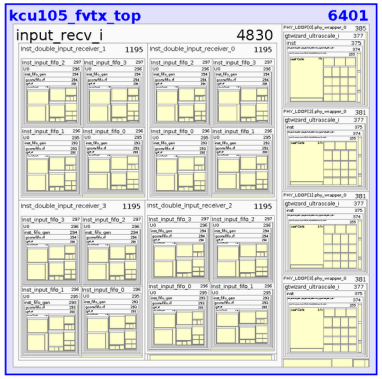
Header — Data section — Trailer

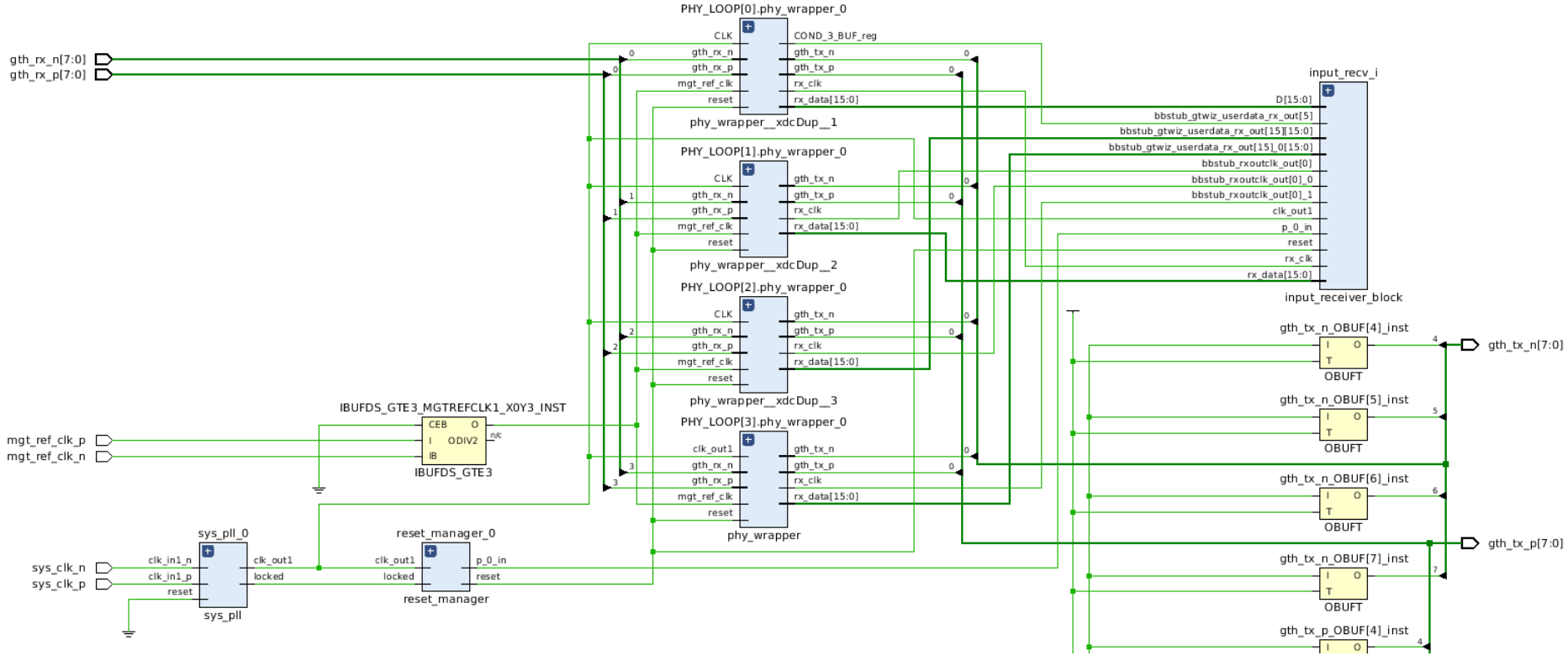
A0-A2 - ADC value for hit
C0 - C5 = chip ID for hit
R0 - R6 = channel number for hit

Readout Electronics Status

ISE to Vivado Migration: Input Receiver Block

- To our surprise, only needed to update FIFO
- Configured PHY to lock to K28.5
  - No sync code between PHYs (yet…)
  - 4 PHYs locked to MGT LOCs





Readout Electronics Status

Development Roadmap:

- ROC to FELIX Data Link:
  - FELIX transceiver configuration (done)
  - ROC link decoder (done)
  - ROC depacketizer (done)
  - ROC link synchronization (in progress)
- FELIX to ROC Slow Control:
  - Link encoder, packetizer, controller (in progress)
- ROC Data Packager to PCIe ← **We are here!**
  - Sub event builder (in progress)
  - Data packager (in progress)
  - Data flow controller
- PCIe to Linux host
  - PCIe interface block with slow control and DMA
  - INTT PCIe Linux control software
  - INTT data file format