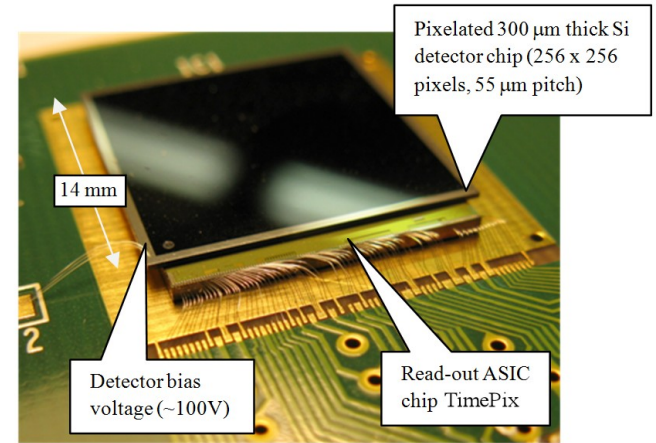
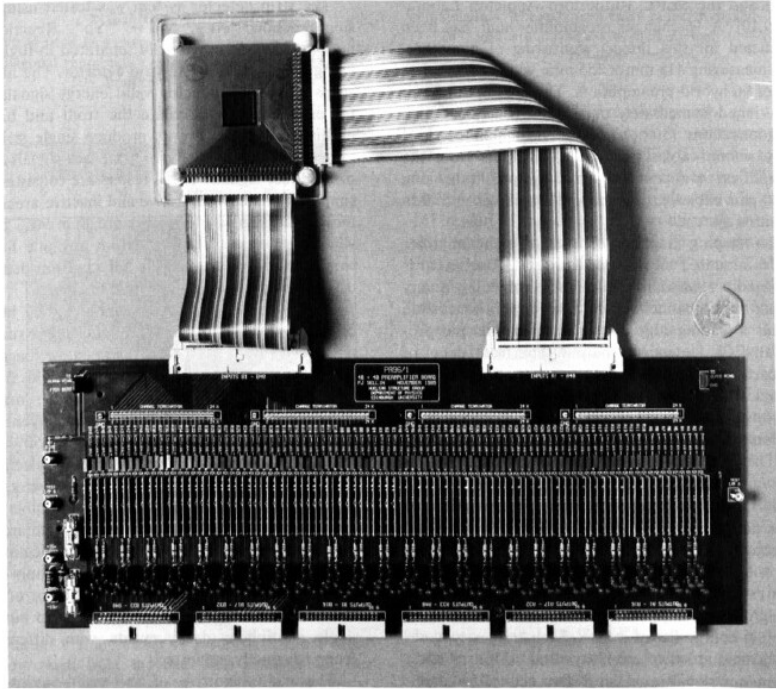


# Could Timepix be useful at EIC

- We (Glasgow group) are involved in EIC
  - But not yet in any specific detector project
- Low  $Q^2$  tagger at CLAS12, Jlab
  - Development, construction, slow controls
  - Data analysis in progress
- Current projects with timepix3
  - Polarimeter for linearly polarised photons
  - RFPMT for picosecond timing
- UK Infrastructures bid for EIC
  - Glasgow component - to investigate timepix detectors for potential use at EIC
- Could timepix4 have a role at EIC?

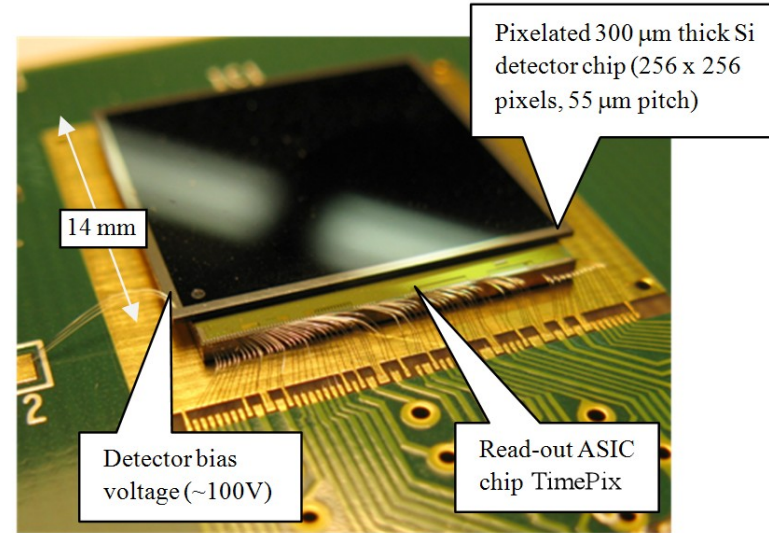


# Timepix3



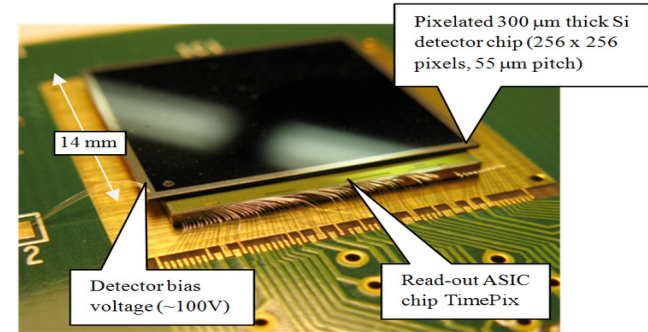
Double sided silicon strip detector (1992 – my PhD)  
15x15mm, 48 x 48 strips = 96 channels  
~1 $\mu$ s shaping time.  
State-of-the-art in 1992

Spot the difference

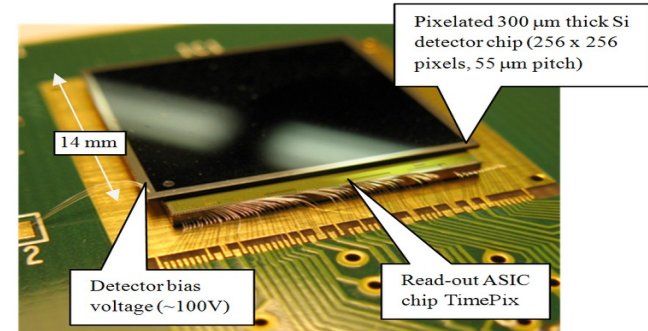


timepix3 (2018)  
14x14mm, 256 x 256 pixels = 65536 channels  
F~10ns shaping time.  
State-of-the-art today.

General Requirements	
Pixel size	55 $\mu\text{m}$ x 55 $\mu\text{m}$
Pixel matrix array	256 x 256
Target floorplan	3 sides buttable and minimum periphery
Highly Configurable	HEP platform for many projects
Time stamp and TOT recorded simultaneously	YES
Analog Power Pulsing	YES
No event counting mode	Only for testing
Technology	IBM 130nm DM 4-1
Power consumption	<1.5W/cm <sup>2</sup> (~45 $\mu\text{W}$ /pixel) @1.5 V
TSVs possibility	YES
Chip Readout Modes	
Data-driven readout (token pass)	YES
Zero-suppressed and Sparse data readout	YES
Dead time free	YES (if count rate < 40Mhits/s/cm <sup>2</sup> )
Time Stamp (ToA)	
Global Time stamp (bunchID)	40 MHz (25ns)
Global Time stamp range	14bits (409.6 $\mu\text{s}$ )
Accurate Time stamp per pixel	4bits $\rightarrow$ 1.56ns resolution (640 MHz)
Local Oscillator frequency	640 MHz
On-Superpixel local oscillator tuning	Locked using periphery PLL
Charge measurement (TOT)	
TOT Clock reference	40 MHz (25ns)
TOT range	10 bits
Periphery	
Analog Blocks	Band-Gap, DACs and Test Pulse
E-fuses (chip ID, hard-wire configuration)	YES
Programmable PLL	40 $\rightarrow$ 40, 80, 160, 320, 640 MHz
Periphery/output clock	40, 80, 160, 320 MHz
RO architecture	[1 ... 8] SLVS DDR 8b/10b Encoding

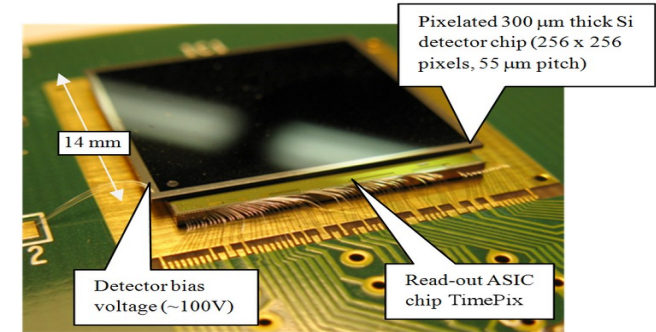


General Requirements	
Pixel size	55 $\mu\text{m}$ x 55 $\mu\text{m}$
Pixel matrix array	256 x 256
Target floorplan	3 sides buttable and minimum periphery
Highly Configurable	HEP platform for many projects
Time stamp and TOT recorded simultaneously	YES
Analog Power Pulsing	YES
No event counting mode	Only for testing
Technology	IBM 130nm DM 4-1
Power consumption	<1.5W/cm <sup>2</sup> (~45 $\mu\text{W}$ /pixel) @1.5 V
TSVs possibility	YES
Chip Readout Modes	
Data-driven readout (token pass)	YES
Zero-suppressed and Sparse data readout	YES
Dead time free	YES (if count rate < 40Mhits/s/cm <sup>2</sup> )
Time Stamp (ToA)	
Global Time stamp (bunchID)	40 MHz (25ns)
Global Time stamp range	14 bits (409.6 $\mu\text{s}$ )
Accurate Time stamp per pixel	4bits $\rightarrow$ 1.56ns resolution (640 MHz)
Local Oscillator frequency	640 MHz
On-Superpixel local oscillator tuning	Locked using periphery PLL
Charge measurement (TOT)	
TOT Clock reference	40 MHz (25ns)
TOT range	10 bits
Periphery	
Analog Blocks	Band-Gap, DACs and Test Pulse
E-fuses (chip ID, hard-wire configuration)	YES
Programmable PLL	40 $\rightarrow$ 40, 80, 160, 320, 640 MHz
Periphery/output clock	40, 80, 160, 320 MHz
RO architecture	[1 ... 8] SLVS DDR 8b/10b Encoding



- Ideal features for spectrometer focal plane type applications..  
High rate capability  
Excellent position resolution.

General Requirements	
Pixel size	55 $\mu\text{m}$ x 55 $\mu\text{m}$
Pixel matrix array	256 x 256
Target floorplan	3 sides buttable and minimum periphery
Highly Configurable	HEP platform for many projects
Time stamp and TOT recorded simultaneously	YES
Analog Power Pulsing	YES
No event counting mode	Only for testing
Technology	IBM 130nm DM 4-1
Power consumption	<1.5W/cm <sup>2</sup> (~45 $\mu\text{W}$ /pixel) @1.5 V
TSVs possibility	YES
Chip Readout Modes	
Data-driven readout (token pass)	YES
Zero suppressed and Sparse data readout	YES
Dead time free	YES (if count rate < 40Mhits/s/cm <sup>2</sup> )
Time Stamp (ToA)	
Global Time stamp (bunchID)	40 MHz (25ns)
Global Time stamp range	1 Mbits (409.6 $\mu\text{s}$ )
Accurate Time stamp per pixel	4bits $\rightarrow$ 1.56ns resolution (640 MHz)
Local Oscillator frequency	640 MHz
On-Superpixel local oscillator tuning	Locked using periphery PLL
Charge measurement (ToT)	
TOT Clock reference	40 MHz (25ns)
TOT range	10 bits
Periphery	
Analog Blocks	Band-Gap, DACs and Test Pulse
E-fuses (chip ID, hard-wire configuration)	YES
Programmable PLL	40 $\rightarrow$ 40, 80, 160, 320, 640 MHz
Periphery/output clock	40, 80, 160, 320 MHz
RO architecture	[1 ... 8] SLVS DDR 8b/10b Encoding



- Ideal features for spectrometer focal plane type applications. High rate capability, Excellent position resolution.
- High rate (application dependent) Needs to be handled onboard.

Frame based (as opposed to event)  
So - not really dead time free.

Heat. Needs to be cooled.  
Small and Expensive. No tracking barrels

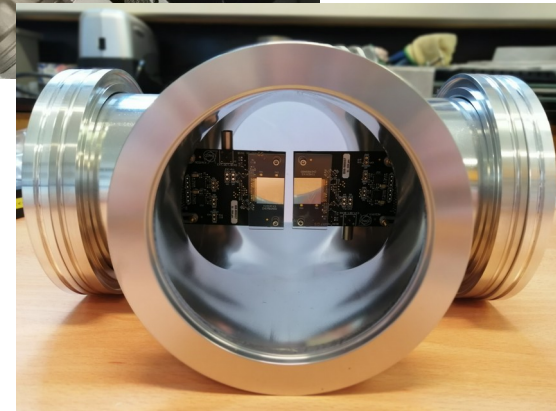
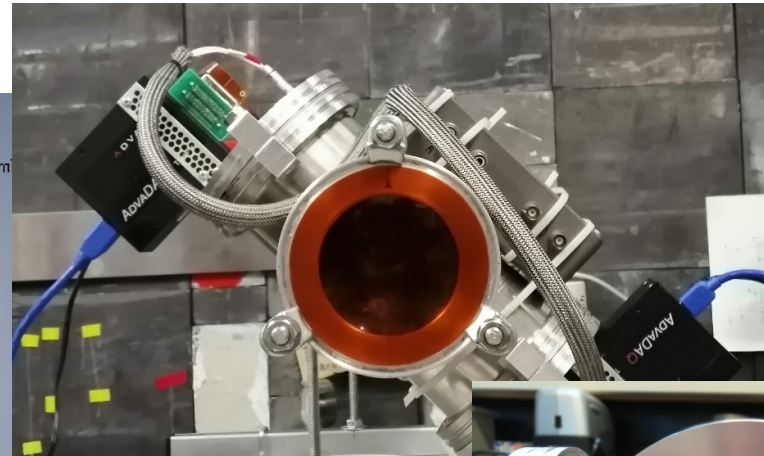
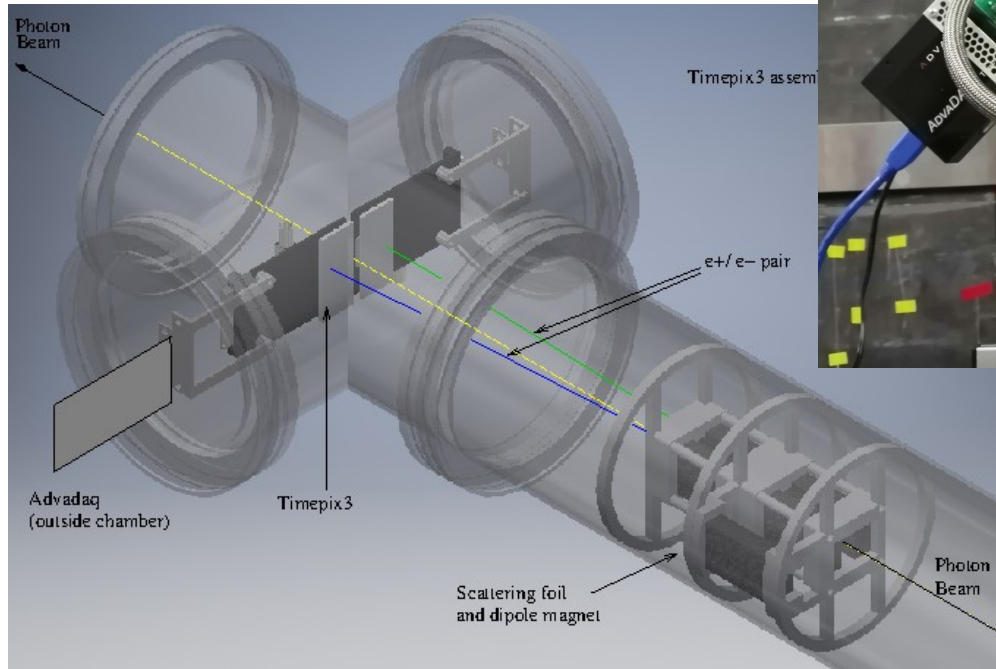
# Timepix3 example – pair polarimeter

Simon Gardner

A pair polarimeter (in progress now)

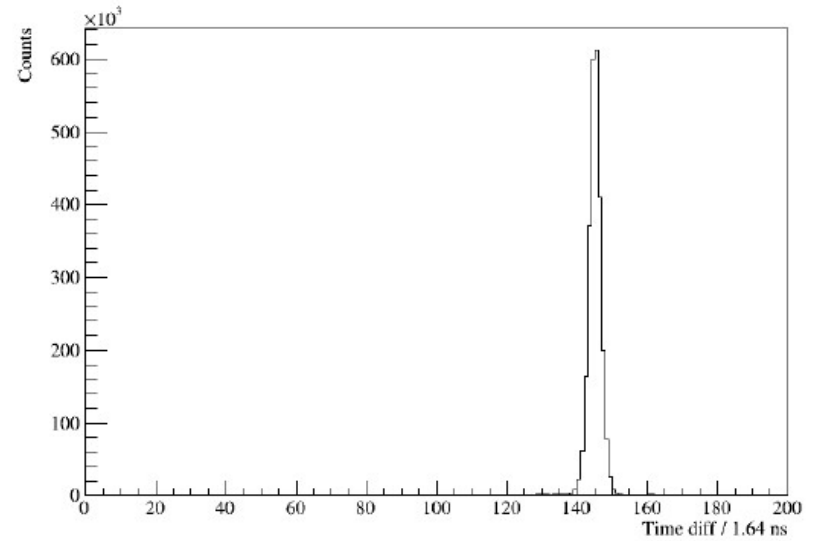
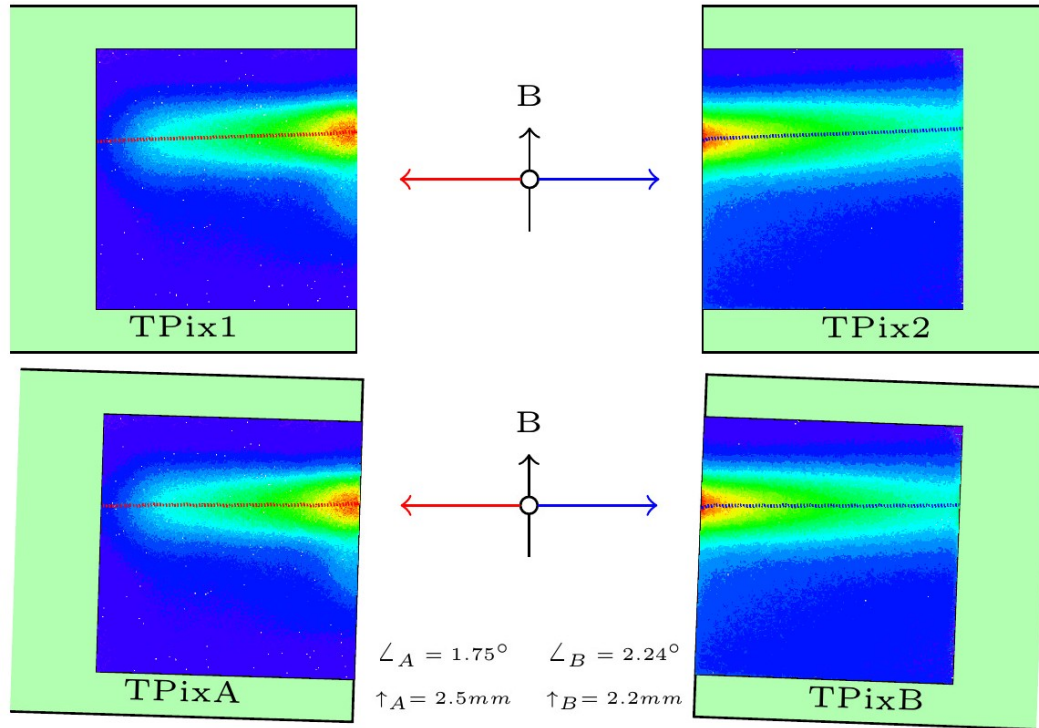
In vacuum. Close to beam. Low event rate (kHz/cm<sup>2</sup>).

Prototype is shown, with only 1 timepix3 in either side (off the shelf, ADVADAQ).



# Timepix3 example – Pair polarimeter

Simon Gardner

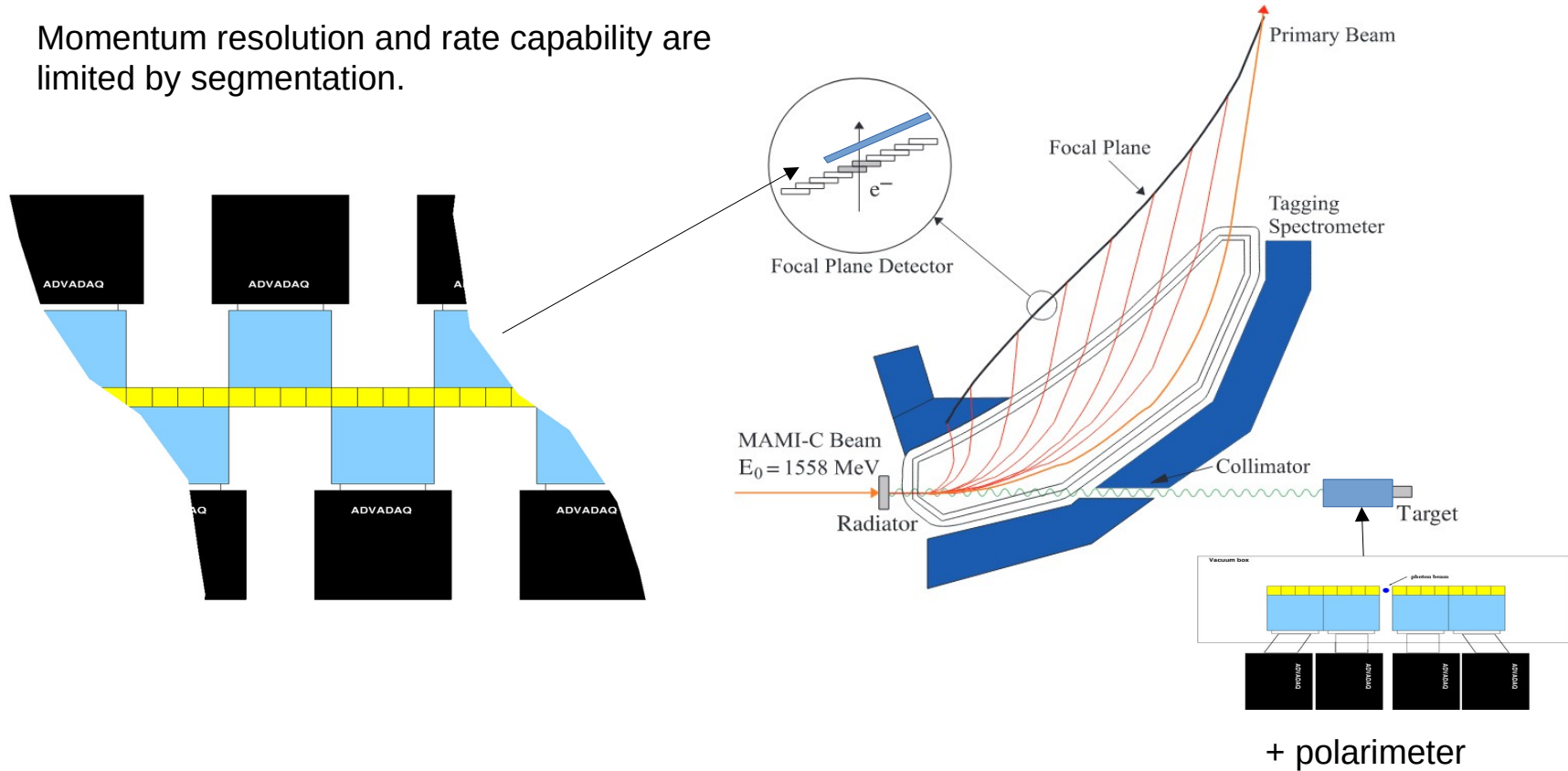


Coincidence between timepix AB

# Timepix example – focal plane microscope

A Focal plane microscope for a spectrometer.  
Not in vacuum. High event rate (MHz/cm<sup>2</sup>).

Momentum resolution and rate capability are limited by segmentation.





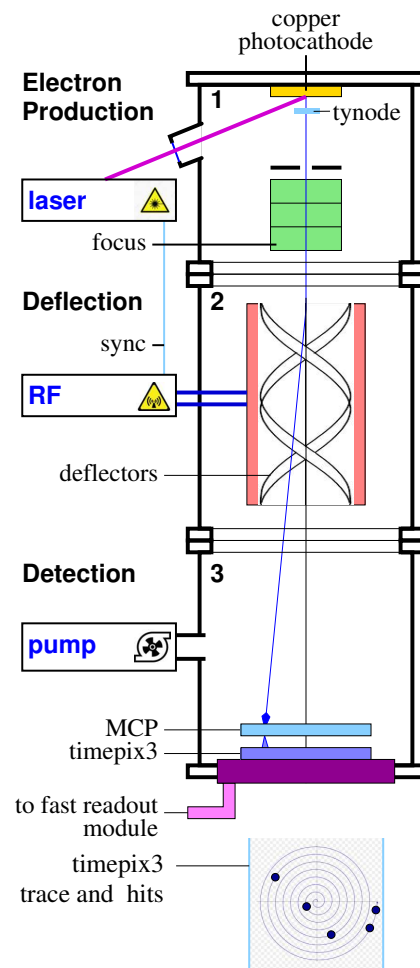
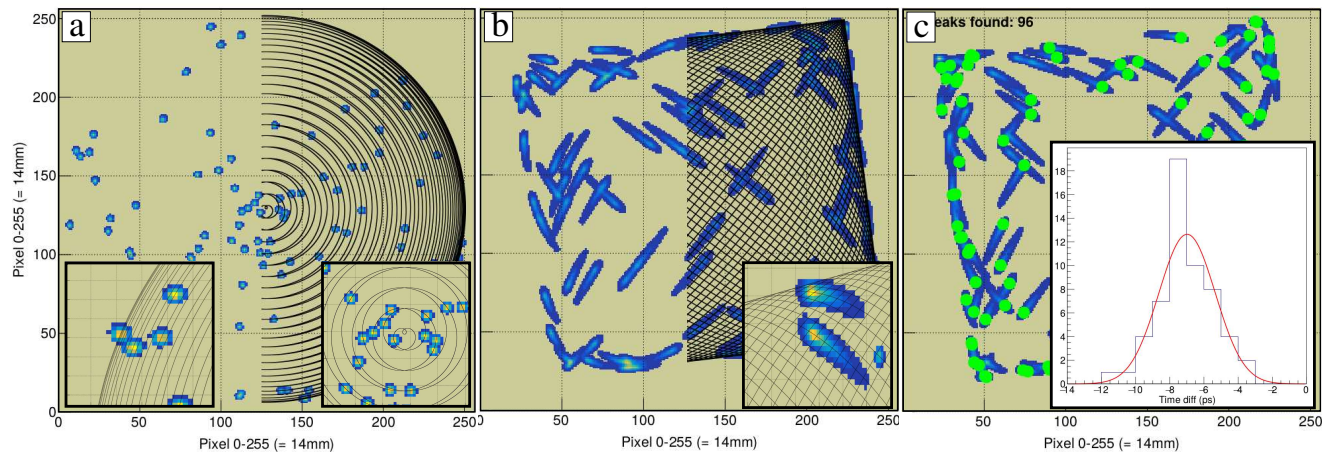
# Timepix example – RFPMT

RFPMT – for ps timing of single photons.

Times converted into positions with RF deflector.

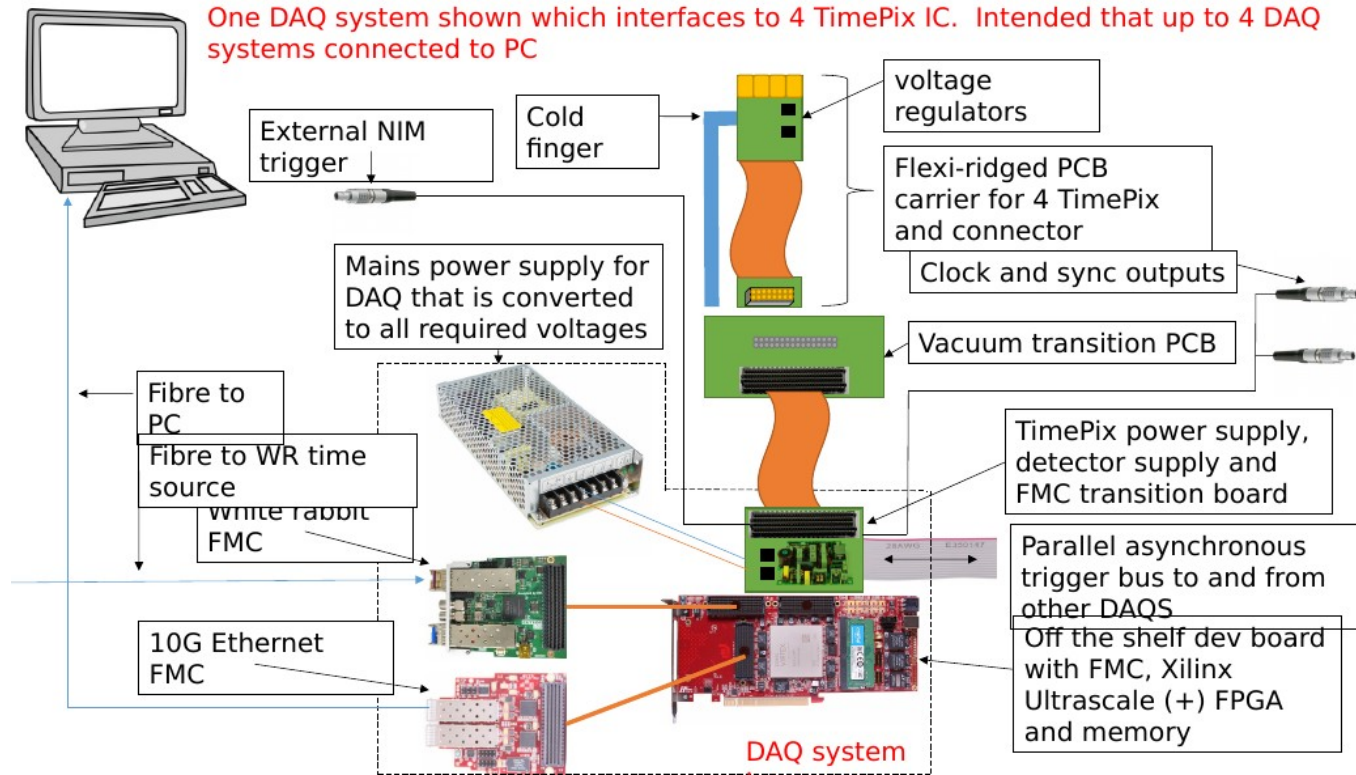
Timepix3 high vacuum endcap development – Glasgow + Daresbury.

Simulation and tracking analysis well developed.



# FPGA based module for 4 x timepix3

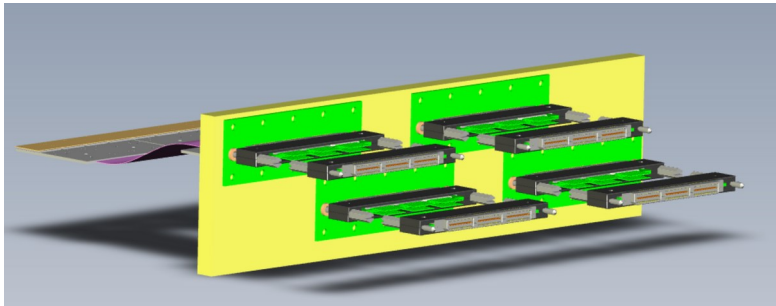
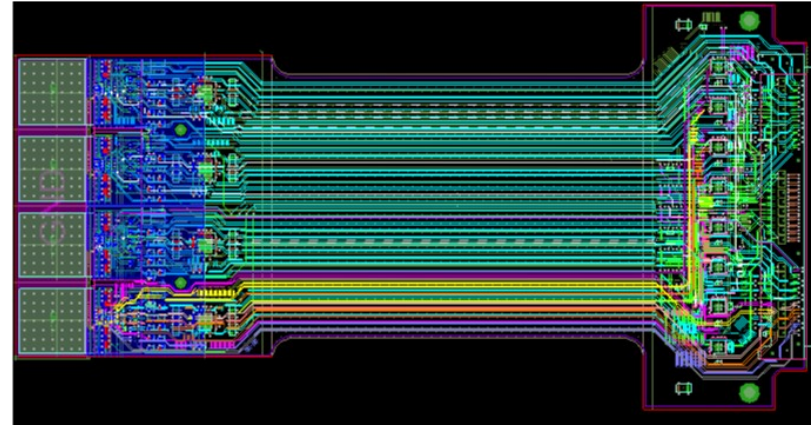
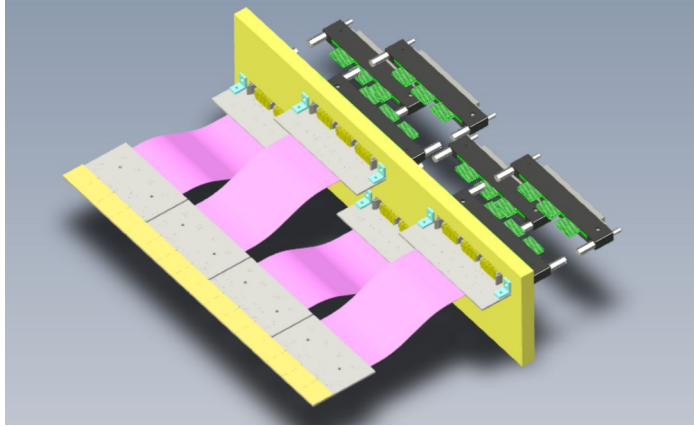
James Lawson, UKRI, Daresbury. Nov 2018



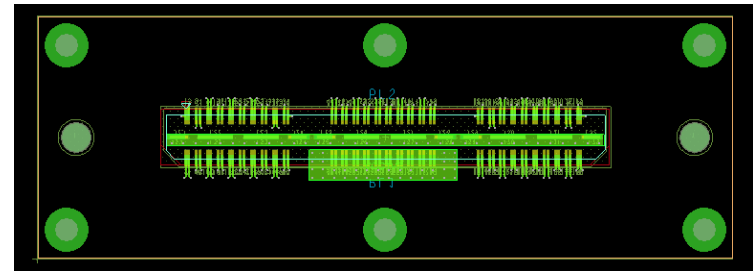
Currently in development between Glasgow and UKRI, Daresbury Group.

# FPGA based module for 4 x timepix3

Mos Kogimtzis, UKRI, Daresbury. Dec 2019



mechanical assembly of 4x4 timepix3\_asic\_pcb



asic and flange pcbs

# Timepix3 vs Timepix4

Timepix4: A 4-side tillable large single threshold particle detector chip with improved energy and time resolution and with high-rate imaging

		Timepix3 (2013)	Timepix4 (2019)	
Technology		130nm - 8 metal	65nm - 10 metal	
Pixel Size		55 x 55 $\mu\text{m}$	55 x 55 $\mu\text{m}$	
Pixel arrangement		3-side buttable 256 x 256	4-side buttable 512 x 448 <b>3.5x</b>	
Sensitive area		1.98 $\text{cm}^2$	6.94 $\text{cm}^2$	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA	
		Event Packet	48-bit	64-bit <b>33%</b>
		Max rate	$0.43 \times 10^6$ hits/ $\text{mm}^2/\text{s}$	<b><math>3.58 \times 10^6</math> hits/<math>\text{mm}^2/\text{s}</math></b>
		Max Pix rate	1.3 KHz/pixel	<b>10.8 KHz/pixel 8x</b>
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit) <b>10x</b>
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr) <b>5x</b>
		Max count rate	$\sim 0.82 \times 10^9$ hits/ $\text{mm}^2/\text{s}$	$\sim 5 \times 10^9$ hits/ $\text{mm}^2/\text{s}$ <b>8x</b>
	TOT energy resolution		< 2KeV	< <b>1Kev</b>
	Time resolution		1.56ns	<b><math>\sim 200\text{ps}</math></b>
Readout bandwidth		$\leq 5.12\text{Gb}$ (8x SLVS@640 Mbps)	<b><math>\leq 163.84\text{ Gbps}</math> (16x @10.24 Gbps)</b>	

xa

1

# Infrastructures EIC proposal

## Glasgow have proposed investigating

Rate capability

Data processing and reduction / triggering

Timing and Energy resolution

Radiation hardness

Performance in a B field (eg 3T).

Implementation in vacuum

Cooling

Development of small timepix3 based prototype to take to beam tests

## MAPS vs. timepix Depends on the application

### Maps advantages compared to timepix

can be large area

cheaper than hybrid pixel detector

small pixel

less scatter for MIPS

### Maps disadvantages compared to timepix

slow`

no timing info

integration of charge (for some apps could be + or -)

can't stop X-rays as epi layer is ~20 um.

# Could timepix 4 benefit EIC ?

Glasgow group mainly involved with experiments at JLAB

Main Physics interests lie with exclusive processes

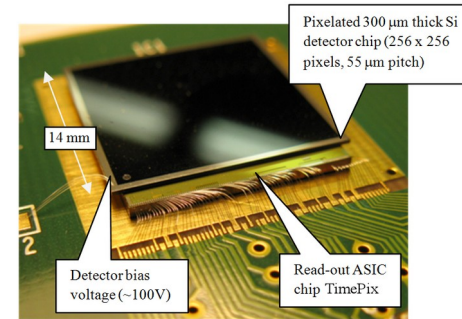
- DVCS and DVMP for nucleon structure and imaging
- Low  $Q^2$  meson production for
  - Baryon spectroscopy at low  $W$
  - Meson spectroscopy at high  $W$

This mainly requires small  $t$ - production => proton along beam at EIC

Far Forward Ion and Low  $Q^2$  tagging critical for these experiments

# Summary

- Timepix3 – some very useful features
  - Already used in Glasgow projects
- Timepix4 – coming soon
  - 4-side buttable, bigger, better
- UK Infrastructures bid for EIC
  - Glasgow component - to investigate timepix detectors for potential use at EIC
- Could timepix4 have a role at EIC?



## Glasgow Participants

Daria Sokhan	Leader of Glasgow EIC activities.
Derek Glazier	Simulation and analysis tools
Ken Livingston	Detector development, applications of Timepix3 and readout development.
Simon Gardner	Detector development, simulation, analysis - Timepix3 polarimeter
Dima Manueski	Timepix / Medipix expert

# Extra



# EIC smear fast simulations

Example  $ep \rightarrow ep \pi^+\pi^-$

Take virtual photon flux for e-scattering

Take t-slope = 4 GeV for meson production

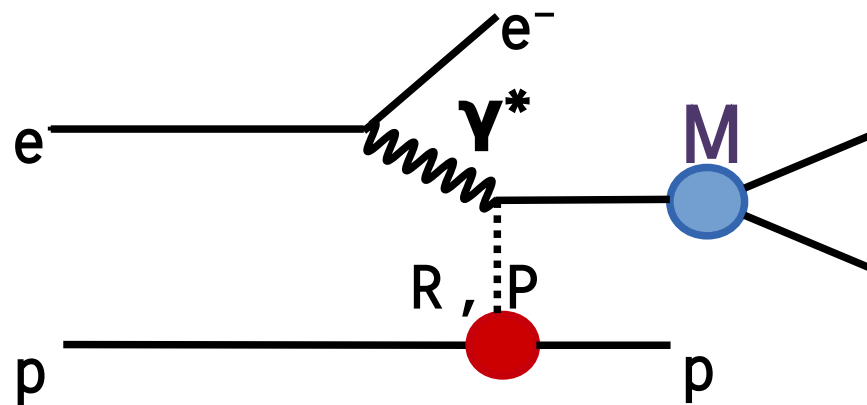
Use eic\_smear Handbook detector

Add Far Forward ion region

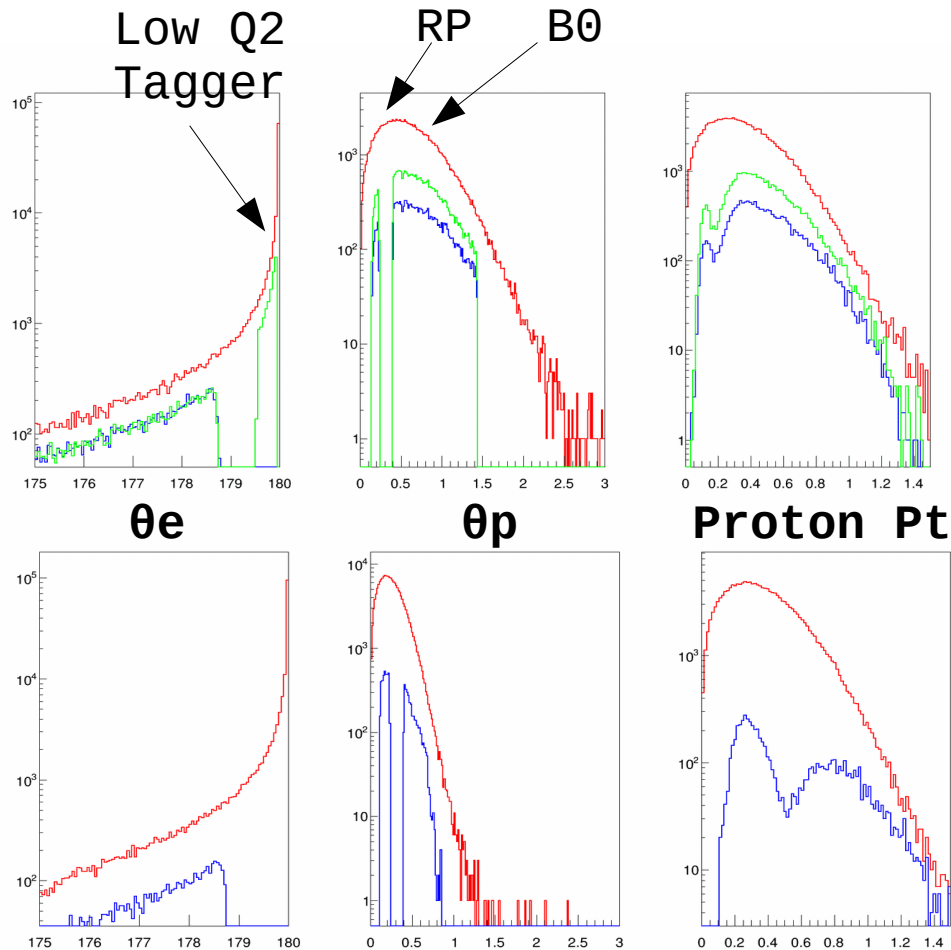
Roman Pot  $0.002 \rightarrow 0.004$  rad +  
B0  $0.007 \rightarrow 0.025$  rad

Add Low Q2 tagger

$0.001 \rightarrow 0.008$  rad



# EIC smear fast simulations



$$E_e = 3 \text{ GeV}$$
$$E_p = 41 \text{ GeV}$$

$$E_e = 5 \text{ GeV}$$
$$E_p = 100 \text{ GeV}$$

**Generated Events**  
**Reconstructed 4 particles**  
**With LowQ2 tagger**

FF Ion is essential for  
detection of protons

e- detection to  $178.5^\circ$   
With calorimeter in  
handbook

How realistic ?

Low Q2 tagger can  
significantly  
Increase yield