

# Production and Ladder Test Preparation in NCU

# Executive Summary

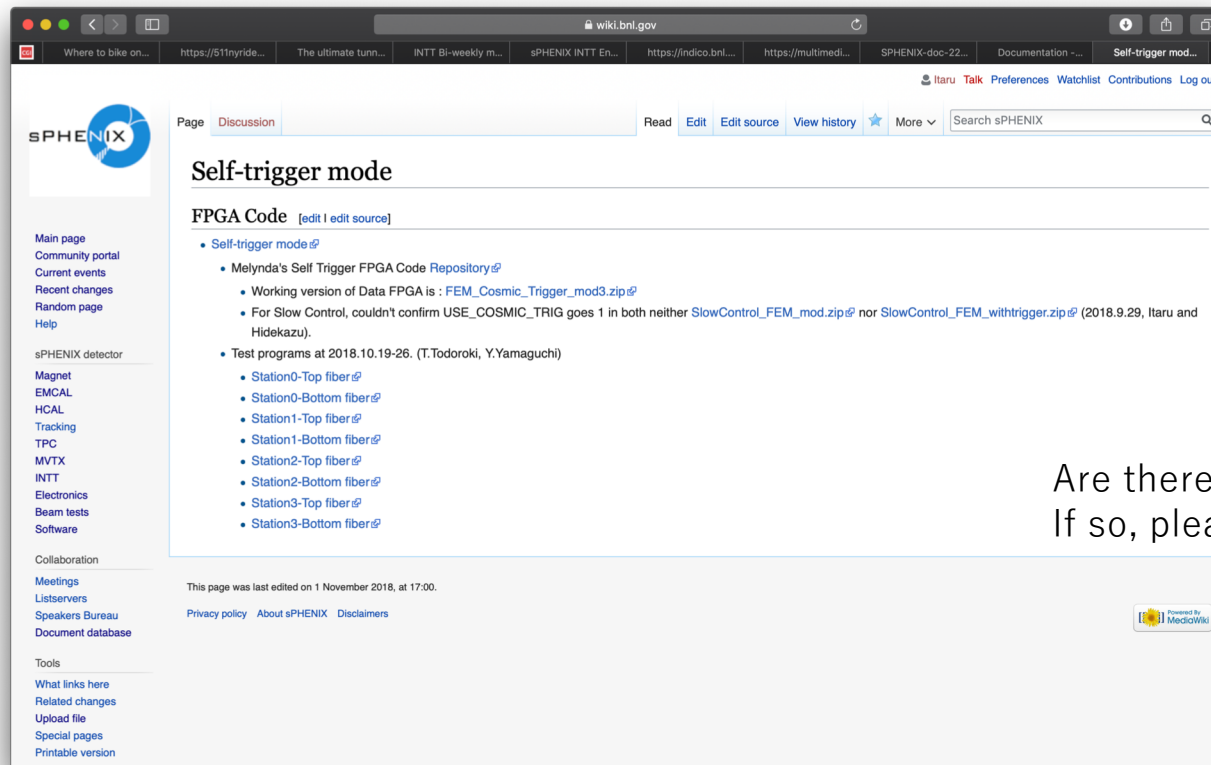
- Silicon Sensors
  - 100 Sets (batch-2) production silicons are to be delivered today as scheduled.
  - Sensors will be shipped to NCU once they are ready.
- FPHX
  - ~1500 good FPHX chips are delivered to NCU on April 29<sup>th</sup>.
- HDI
  - Shipped 39 HDI's to BNL and are delivered today.
  - Move on to 2<sup>nd</sup> batch once new design around bias connectors are confirmed in BNL
- Stave
  1. Shipped 4 staves + 3 tubes to BNL and are delivered today.
  2. Paper works for the procurements towards production is on going.
- Trigger Scintillators and PMTs
  - Reuse existing scintillators and PMTs in NCU
  - Thanks to NCU group for PO to G-tech. Light guides are delivered to NCU.

# 1<sup>st</sup> Ladder Performance Check Menu @ NCU

STEP	Test	Condition	Purpose	Extra tools
1	Calibration	Bias off Bias on	Wirebonding btwn FPHX and HDI. FPHX health check.	Bias Power Supply and cable
2	Bias Scan	Bias on HV vs. Current	Wire bonding btwn FPHX and Silicon. Ground contact/short.	
3	Noise	Bias on, self-trigger	Noise distribution and rate	Self-trigger FPGA
4	Source	Bias on, external trigger by a scintillator	Find dead channel in silicon sensor	External Trigger FPGA, Support structure, source, a trigger scintillator
5	Cosmic ray	Bias on, external trigger by sandwich scintillators. Multi-layered ladders.	Uniformity of the entire area and MIP observation. Long term stability,	External Trigger FPGA, Support structure, trigger scintillators
6	Else?			

Update from April 7<sup>th</sup> slide

# Self-Trigger FPGA for the test stand



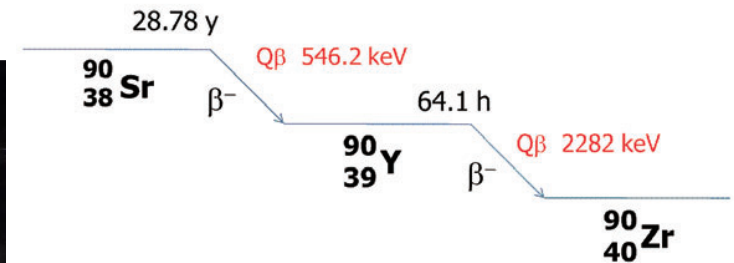
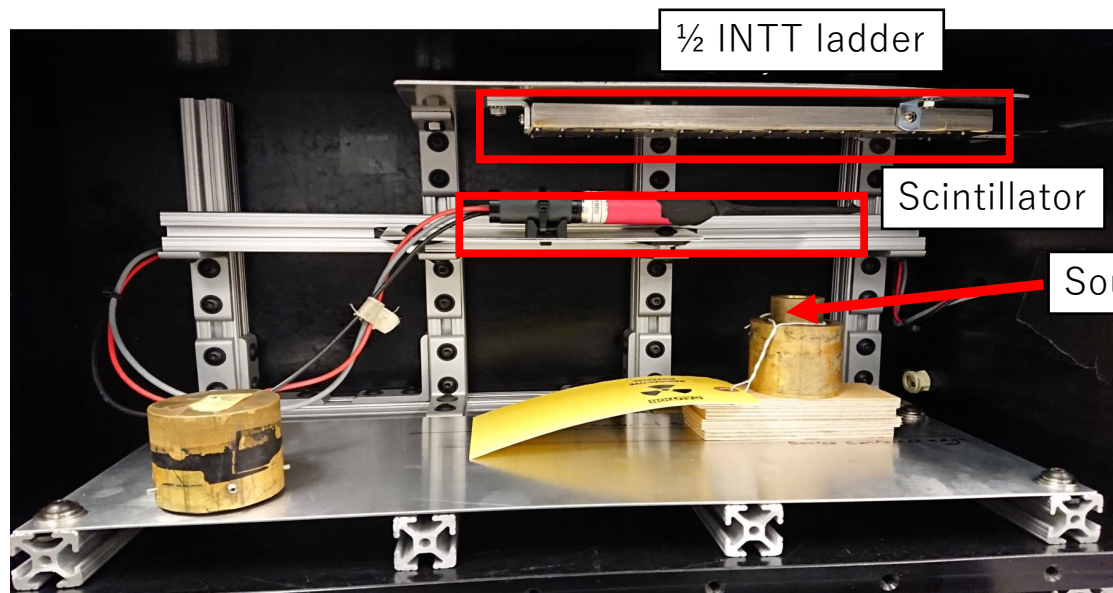
Are there custom version in NWU?  
If so, please post in our wiki.

[https://wiki.bnl.gov/sPHENIX/index.php/Self-trigger\\_mode](https://wiki.bnl.gov/sPHENIX/index.php/Self-trigger_mode)



# Source Test Setup in 2017

H. Masuda Master Thesis  
Section 4.2.3.

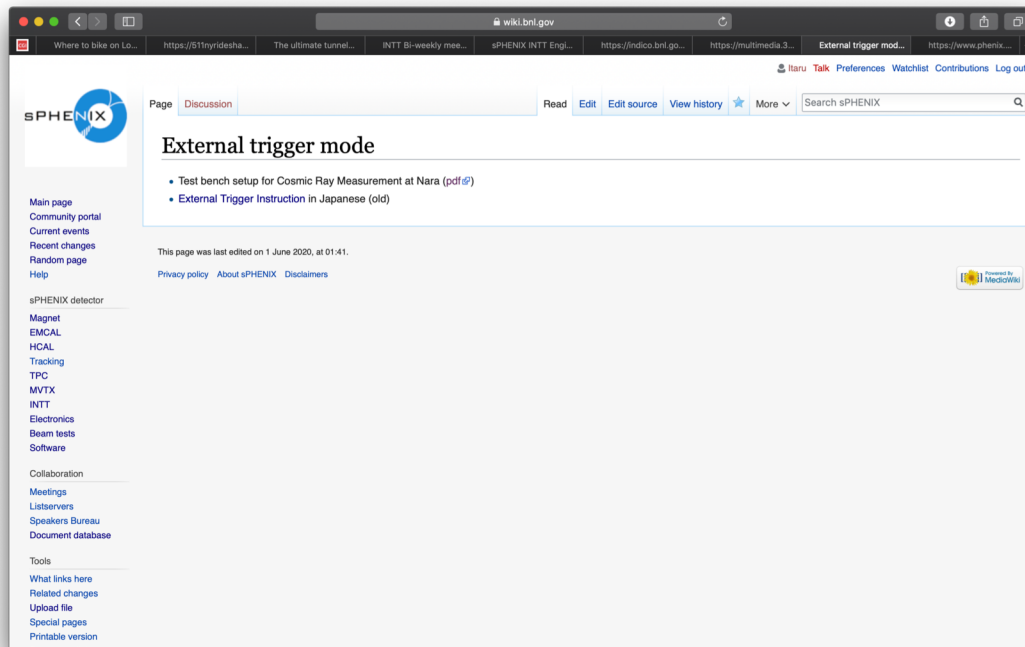


ADC Setup

ADC	設定値	対応電圧	Note
ADC0	25	310mV	
ADC1	35	350mV	
ADC2	48	400mV	2strip shared peak(MIP)
ADC3	98	600mV	
ADC4	148	800mV	
ADC5	172	900mV	1strip peak(MIP)
ADC6	223	1100mV	
ADC7	248	1200mV	

Note: since the thickness of the scintillator @ NCU is 12.5mm, the layout suppose to be source-ladder-scintillator.

# Cosmic Ray Data Taking Instruction

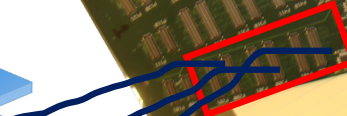


See detailed instruction by Mika

[https://www.phenix.bnl.gov/WWW/p/draft/hachiya/INTT/20200502\\_shibata\\_TBsetupForCosmicMeasurement.pdf](https://www.phenix.bnl.gov/WWW/p/draft/hachiya/INTT/20200502_shibata_TBsetupForCosmicMeasurement.pdf)

- Coincidence between sandwich trigger scintillators (12.5mm thick)

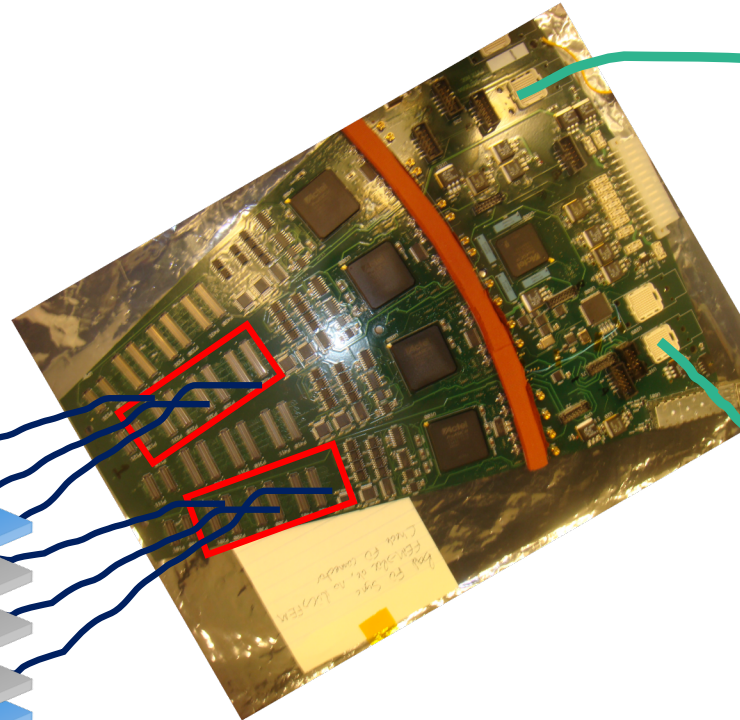
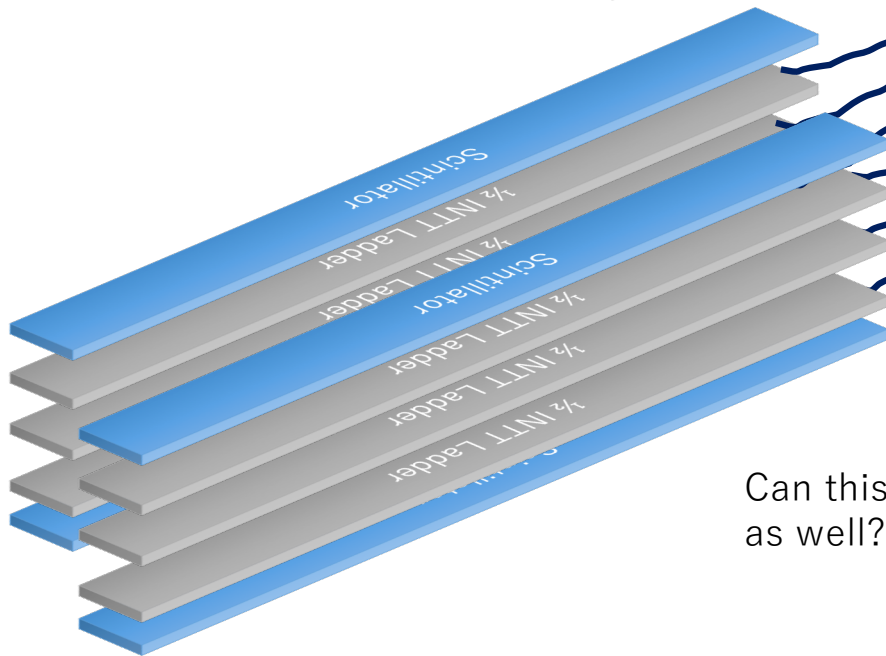
- Simultaneous measurement with multiple ladders to save time



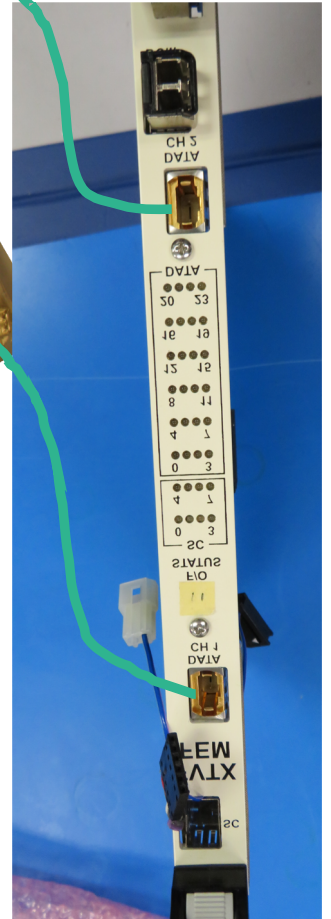
Multi 1/2 ladder simultaneous readout supposes to be tested at NWU.

# Cosmic Ray Test

- Double column readout?
- If this works, 6 ladders can be tested simultaneously.



Can this double column readout be test at NWU as well?



# Debugging Plan of 2<sup>nd</sup> FEM-IB in Taiwan

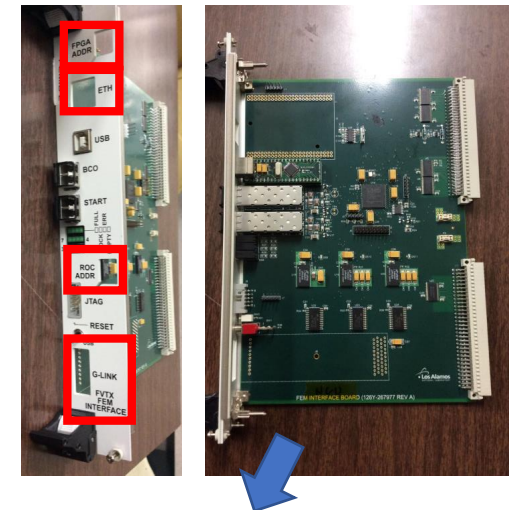
- Takashi agreed to take care of the debugging in NWU.
- Please ship 2<sup>nd</sup> FEM-IB to NWU from NCU.
- Suggested debugging procedure.
  - Whether you can program the FPGA?
  - Is the CLK/START it distributes looks OK?
  - Does it and its FEM respond to slow control command?
  - And you can run some test signal to debug pings which is usually very helpful.
- Will look into more sophisticated debugging method using a chipscope.

## **bad FEM IB 1**

### **Things not attached**

(In the test at NWU, we didn't use any NWU's things for below places.)

- FPGA ADDR
- ETH
- ROC ADDR
- G-LINK



FEM INTERFACE BOARD (126Y-267977 REV A)



# Additional Task Request to NWU in June

1. Multiple  $\frac{1}{2}$  ladder simultaneous readout test.
2. Multiple column readout of ROC.
3. FEM-IB debugging.

## Task List

- |  |   |  |
|--|---|--|
| 1. Further understanding of ladder performance                     | } | Data analysis (software)                           |
| • 3% inefficiency (Timing ?)                                       |   |  |
| • Data timing study (can be tested with Cosmic ray and Test pulse) |   |  |
| • Inefficiency by massive data from crazy chips                    | } | Work at test bench (hardware)                      |
| • Timing jitter among ladders                                      |   |  |
| • Long time stability of DAQ (noise + cosmic ray) for at least 24h |   |  |
| 2. Upgrade the test bench  | } | Work at test bench (hardware)                      |
| • Data from Trigger counter recorded by CAMAC                      |   |  |
| • Necessary to study the data timing wrt clock.                    |   |  |
| 3. Bus extender tests  | } | Data analysis<br>Work in parallel with BE R&D team |
| • Data analysis is going for Eye diagram                           |   |  |
| • Thermal shock test (Apr. 9 – May 20, 40 days)                    |   |  |
| • New prototype production (End of May)                            |   |  |
| 4. QA for new ladder   |   | good to start after May 7 <sup>th</sup>            |
| • MIP test by Cosmic ray and RI source ( $\beta$ -ray)             |   |  |
| 5. Upgrade LV control system for full detector                     | } | Work at test bench (hardware)                      |
| 6. INTT multiplicity trigger                                       |   |  |
| • Feasibility study with GEANT + HIJING                            |   | Data analysis                                      |

2020/4/8

I would like to focus on them, especially 1)-4) in this 2-3 months,

NWU plan