Recent SOI Detector Test Results

3D Integrated Pixel Sensor with SOI Technology for the ILC

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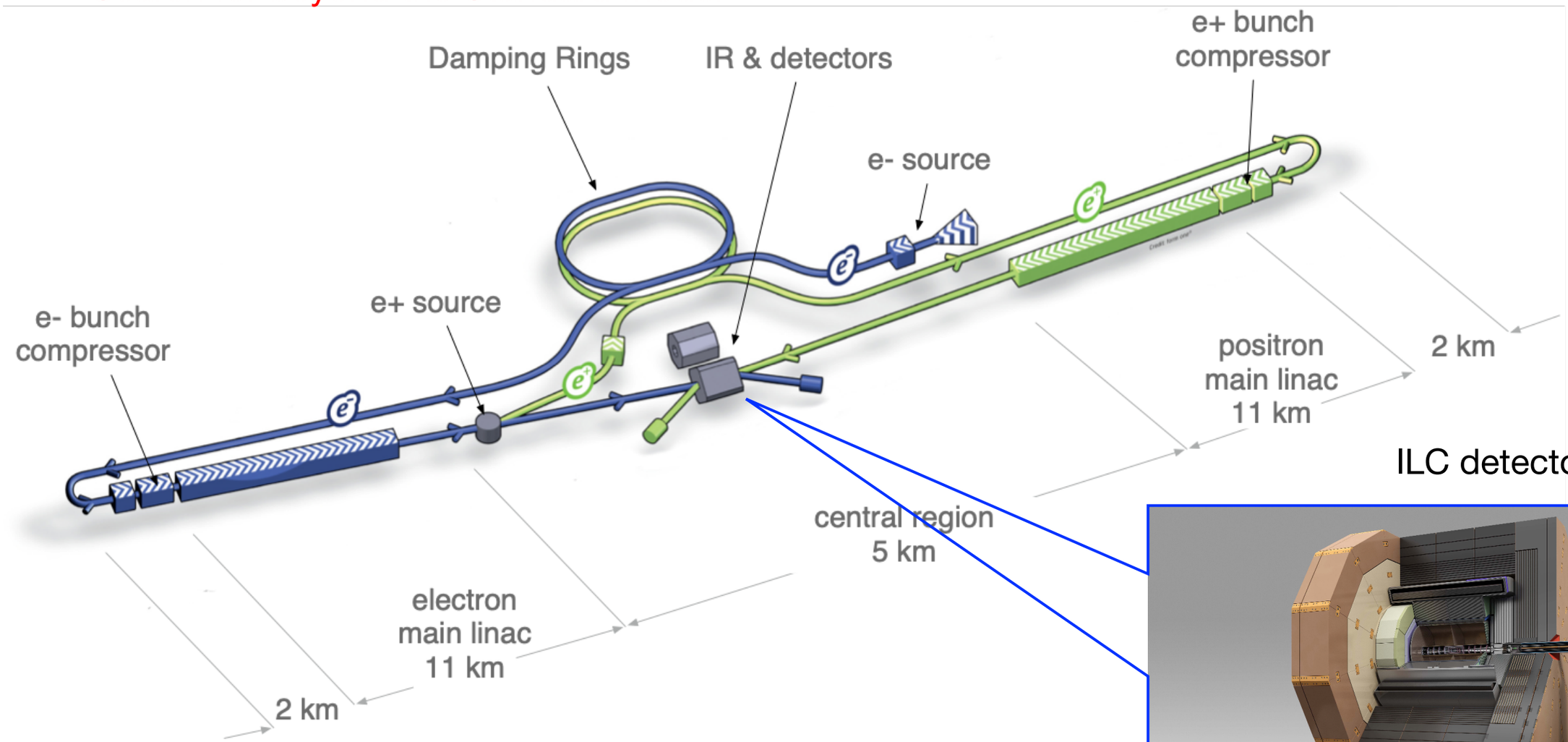
SOIPIX for the EIC at BNL

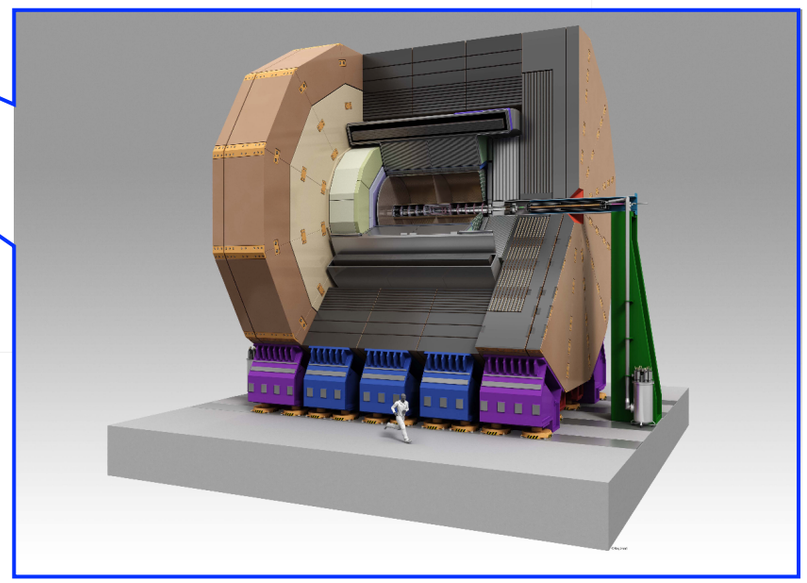
ILC Experiment

ILC Experiment

- e^+e^- linear collider
- Center of mass energy: 250 - 500 GeV (extendable to 1 TeV)
- Precise measurement of the Higgs boson
- Search for beyond the Standard Model



ILC detector concept (ILD)



ILC TDR vol.4: Detectors
ILD Concept Group, T. Abe et al., arXiv:1006.3396 [hep-ex].

ILC Vertex detector

Requirements:

1) Single point resolution: better than 3 μm

   Pixel size: ~20 × 20 μm^2

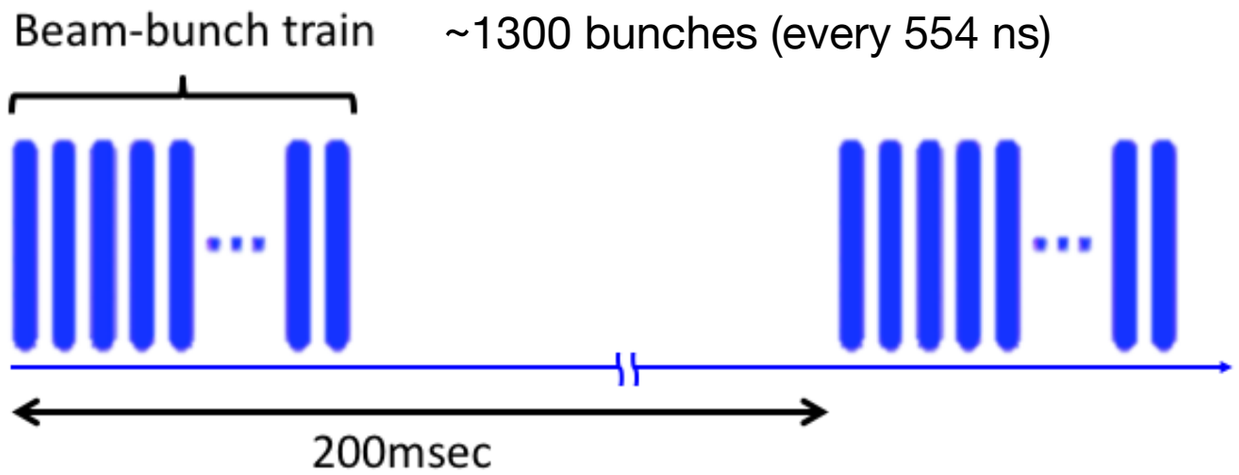
2) Time resolution: single-crossing (554 ns interval) time resolution

3) Detector occupancy: < 2 %

4) Low material budget: X ≤ 0.1 – 0.2 % X_0 / Layer
   corresponds to ~ 100 - 200 μm Si, (supports, cables and cooling add further material)
   low-power ASICs (~ 50 mW/cm^2) + gas-flow cooling

5) Radiation hardness:
   TID : < 1 kGy / year
   NIEL: < 10^{11} 1MeV n_{eq} / cm^2 / year

We are designing and evaluating prototype pixel sensor with SOI technology to fulfill the requirements.



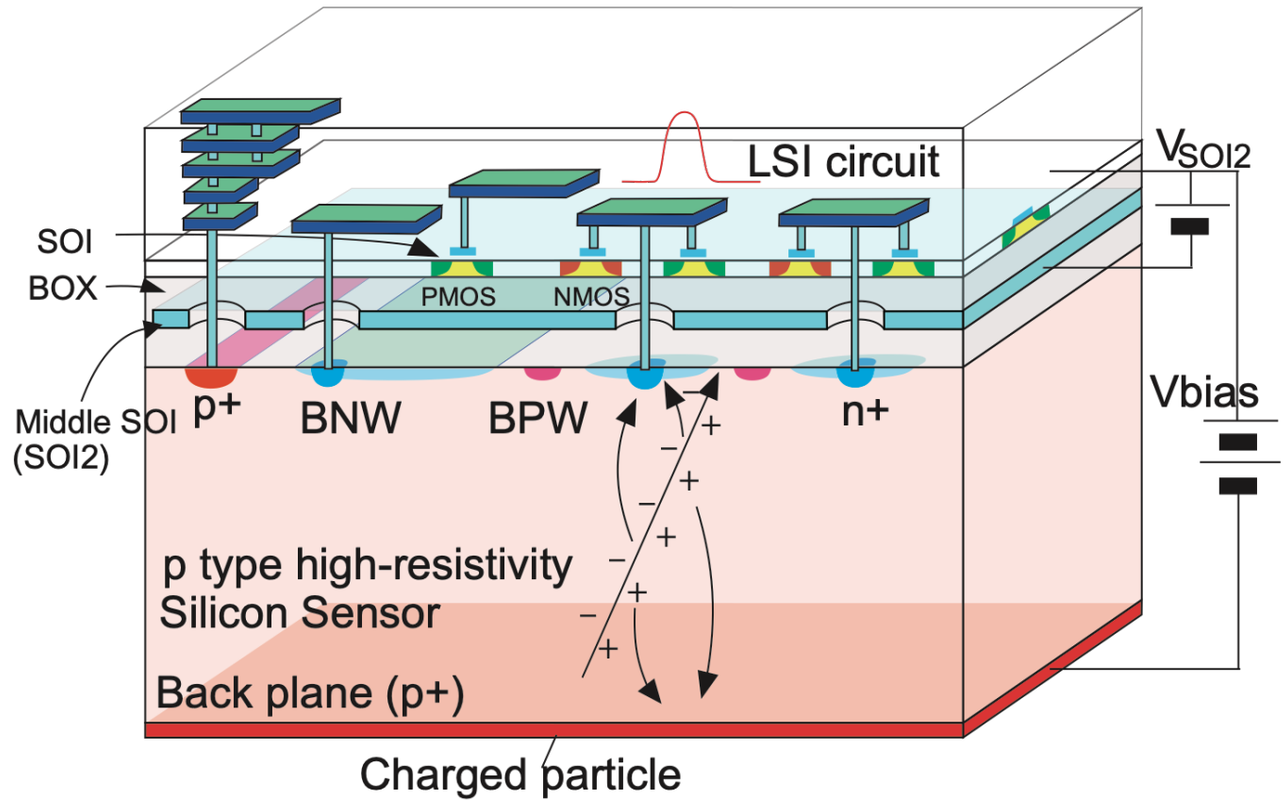
SOI Pixel Detector

SOI: Silicon-on-Insulator technology

Utilize 0.2 μm FD-SOI CMOS process by Lapis Semiconductor Co. Ltd. (Japan)

SOI Pixel Detector: Monolithic type detector

- LSI is processed on Buried Oxide layer (BOX)
- Smaller pixel size, complex circuit in pixel
- Low material budget
- High speed, low power
- Less single event effects (SEE) probability
- Low cost



Double SOI Pixel Detector

Middle Si layer suppresses

- Back gate effect
- Sensor-Circuit cross talk
  - Middle Si layer shields coupling between sensor and circuit.
  - It is useful for analog and digital mixed circuit in pixel.
- Radiation damage (TID)
  - It is able to compensate electric field generated by trapped holes in the BOX.
  - It can be used in high radiation environment (~1MGy).
  - (K. Hara, Vertex2017, Sep. 11-15, 2017, Las Caldas)

Sensor thickness: 50 - 500 μm
Sensor Resistivity: > 1 kΩ·cm
SOI2 thickness: 150 μm (*n*-type)
SOI2 Resistivity: < 10 Ω·cm

Functions for ILC Vertex Detector

Necessary functions for the ILC vertex detector:

- Single point resolution

  Pixel size: less than 20 μm

  Calculate weighted center of charges (Charges are spread over multi pixels).

  → Record analog signal of hit pixels.

- Timing resolution

  Bunch crossing occurs every 554 ns in 1-msec-long bunch train with an interval 200 ms.

  Identify the collision bunch of hits to reconstruct an event.

  → Record timestamp of hit pixels.

- Detector occupancy

  Hit information has to be held during 1 beam-bunch train.

  Increase pixel occupancy.

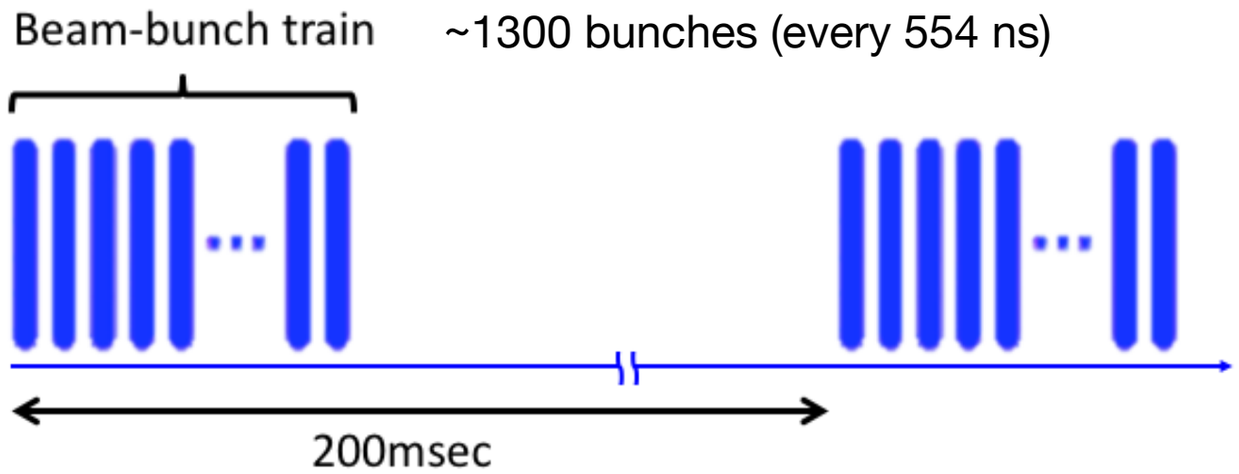
  → Need multiple memories

- High speed data transfer

  Data have to be sent to backend before next bunch train injection.

  → Reduce the data to transfer.

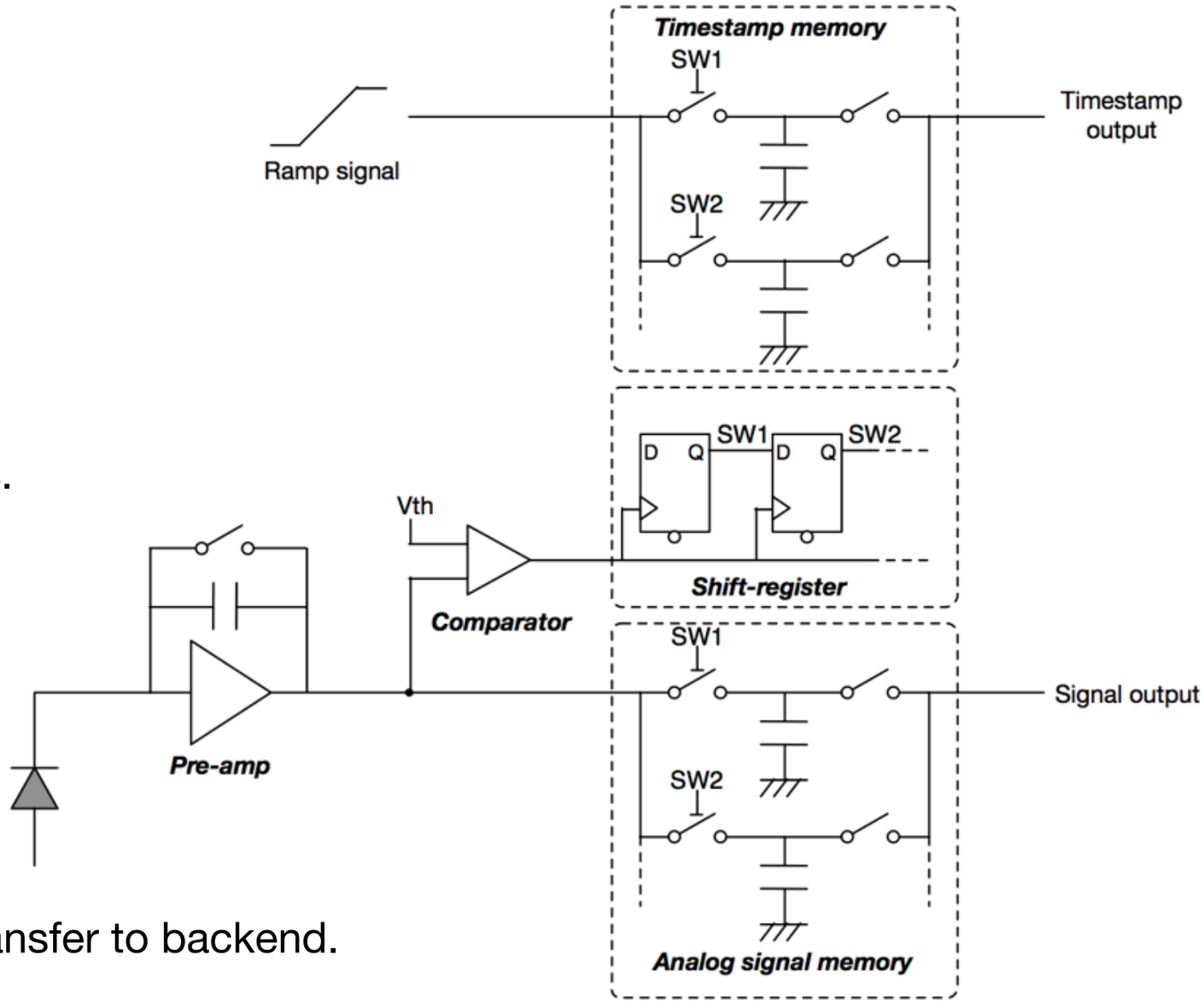
We designed a prototype pixel detector SOFIST.



Architecture of SOFIST

In a Pixel

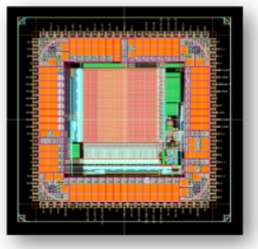
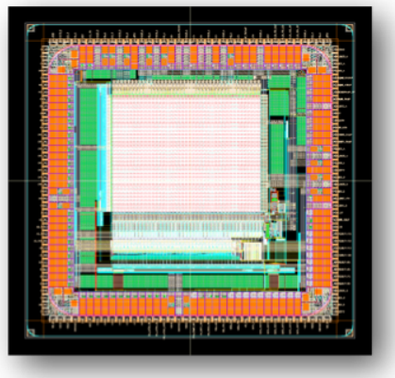
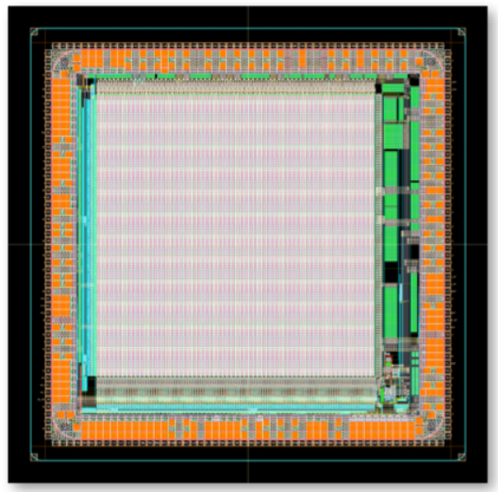
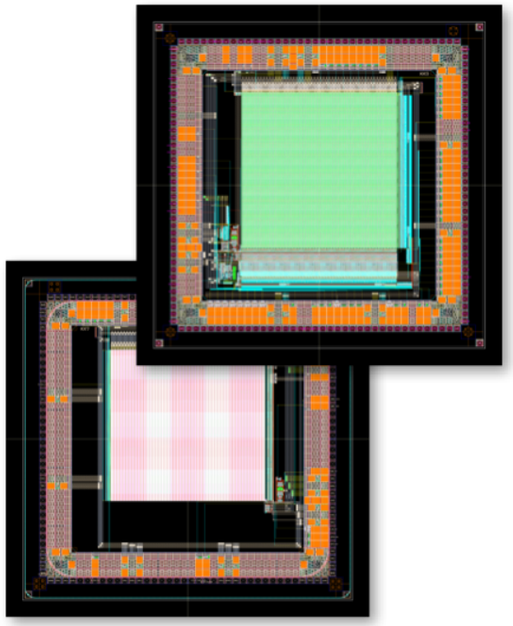
- Pre-amplifier
- Comparator
  Keep the analog signal and time stamp
  if a signal exceeds a threshold V_{th}.
- Shift register
  Hit memory
  Latch for multiple memories.
- Analog signal memory
  Store signal charges for three (or more) hits.
- Time stamp circuit
  Store time stamps for three (or more) hits.



On Chip

- Column ADC
  Digitize analog signal and time stamp.
- Zero-Suppression logic
  Extract hit pixels and reduce the data to transfer to backend.

SOFIST

	SOFIST1	SOFIST2	SOFIST3	SOFIST4 (3D)
	Beam test at FNAL in Jan. 2017 Analog signal	Beam test at FNAL in Feb. 2018 Analog signal or Timestamp	Beam test at FNAL in Feb. 2019 Analog signal and Timestamp	Beam test at FNAL in Feb. 2020 Analog signal
				
Chip Size (mm^2)	2.9 × 2.9	4.45 × 4.45	6 × 6	4.45 × 4.45
Pixel Size (μm^2)	20 × 20	25 × 25	30 × 30	20 × 20
Pixel Array	50 × 50 (Analog Signal)	64 × 64 (Time Stamp) 16 × 64 (Analog Signal)	128 × 128 (Analog signal and Time stamp)	104 × 104 (Analog signal and Time stamp)
Functions (Pixel)	Pre. Amplifier (CSA) Analog signal memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 2) Analog signal memory (2 hits) or Time stamp memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)
Functions (On Chip)	Column ADC (8 bit)	Column ADC (8 bit) Zero-suppression logic	Column ADC (8 bit)	Column ADC (8 bit)
Wafer	FZ *n* -type (Single SOI)	Cz *p* -type (Double SOI)	FZ *p* -type (Double SOI)	FZ *p* -type (Double SOI)
Wafer Resistivity (kΩ·cm)	2 ≤	1 ≤	3 - 10	3 - 10
Status	Delivered (Dec. 2015) Position resolution ~1.4 μm	Delivered (Jan. 2017) Time resolution ~1.55 μs	Delivered (May. 2018) Under evaluation	Delivered (Jan. 2019 ~)

SOFIST1

Hit position reconstruction

Calculate weighted center of charges (6 × 6 pixels).

Track reconstruction

Find track candidates by four layers of FPIX.
The track that has the minimum chi2 is chosen
for calculating the residual.

Residual

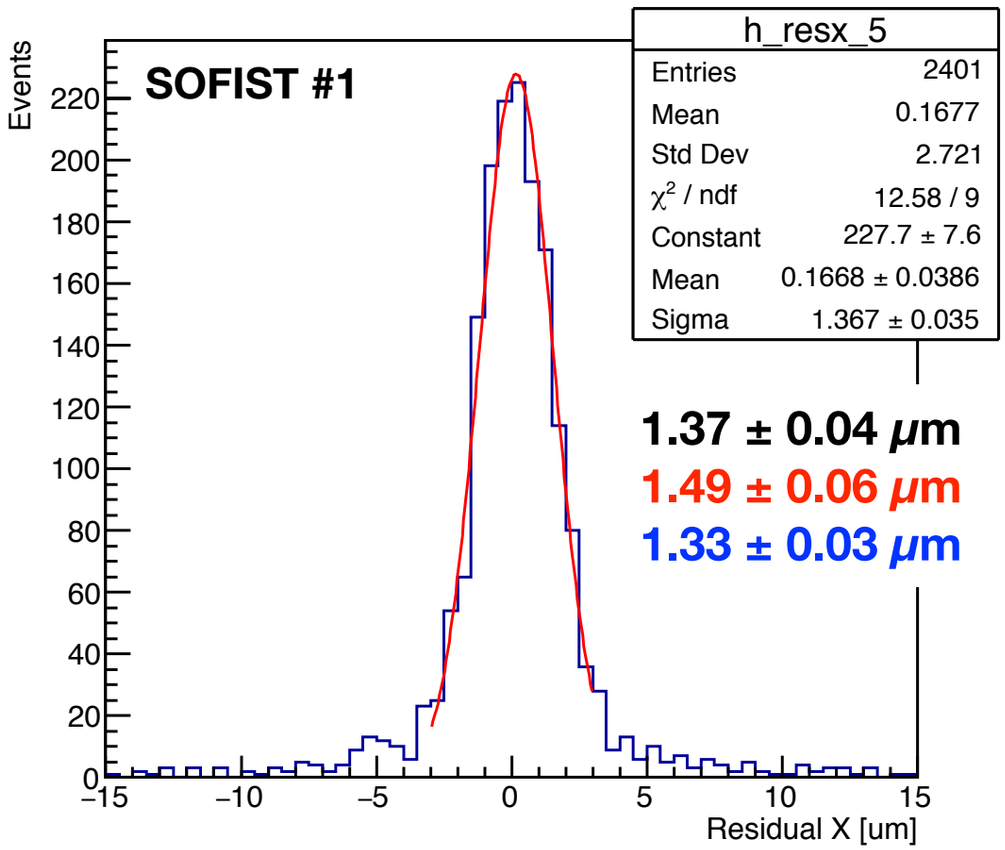
Difference between reconstructed track and actual hit
on the SOFIST.

Readout and Sensor depletion layer

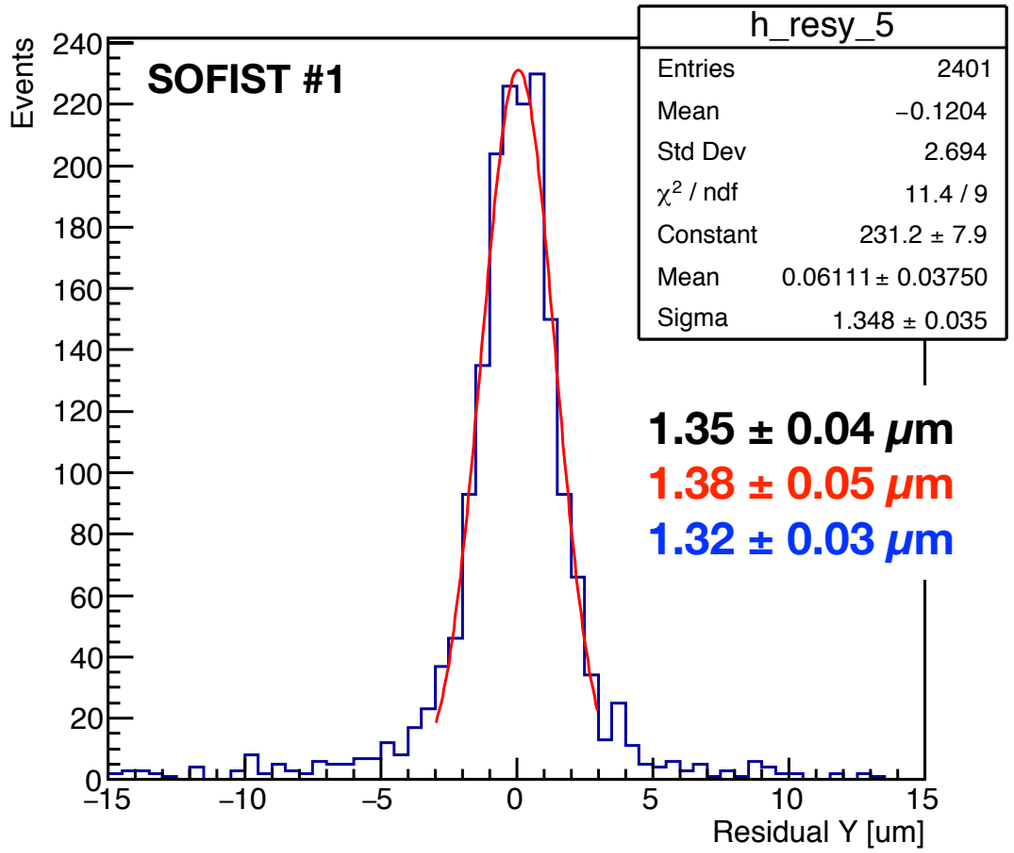
12-bit external ADC, 500 μm (Full depletion)
8-bit on-chip ADC, 500 μm (Full depletion)
12-bit external ADC, 200 μm (Partial depletion)

Sensor Thickness: 500 μm

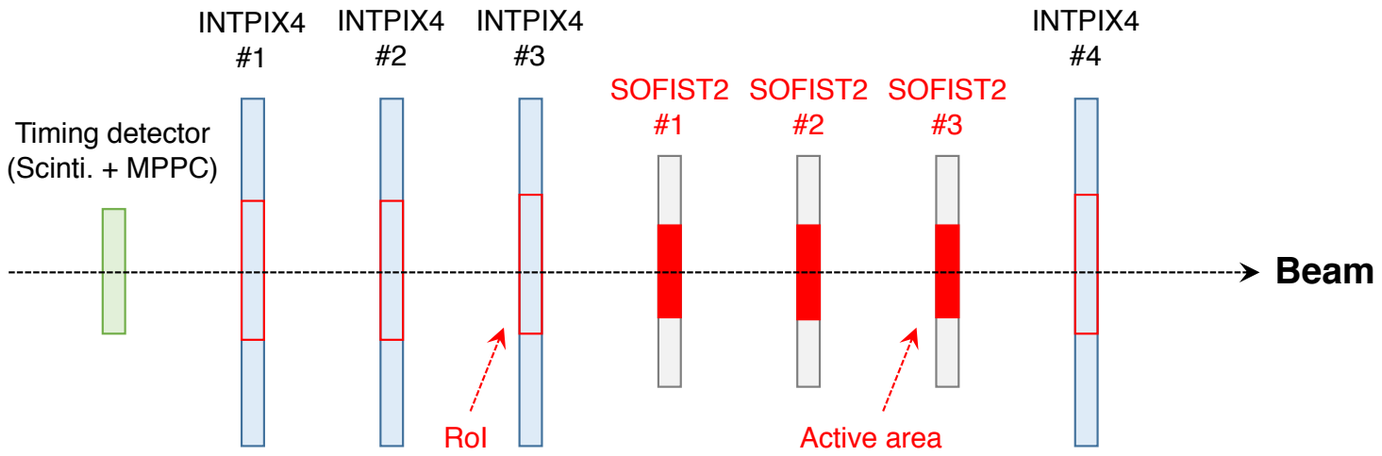
Residual X



Residual Y



SOFIST2

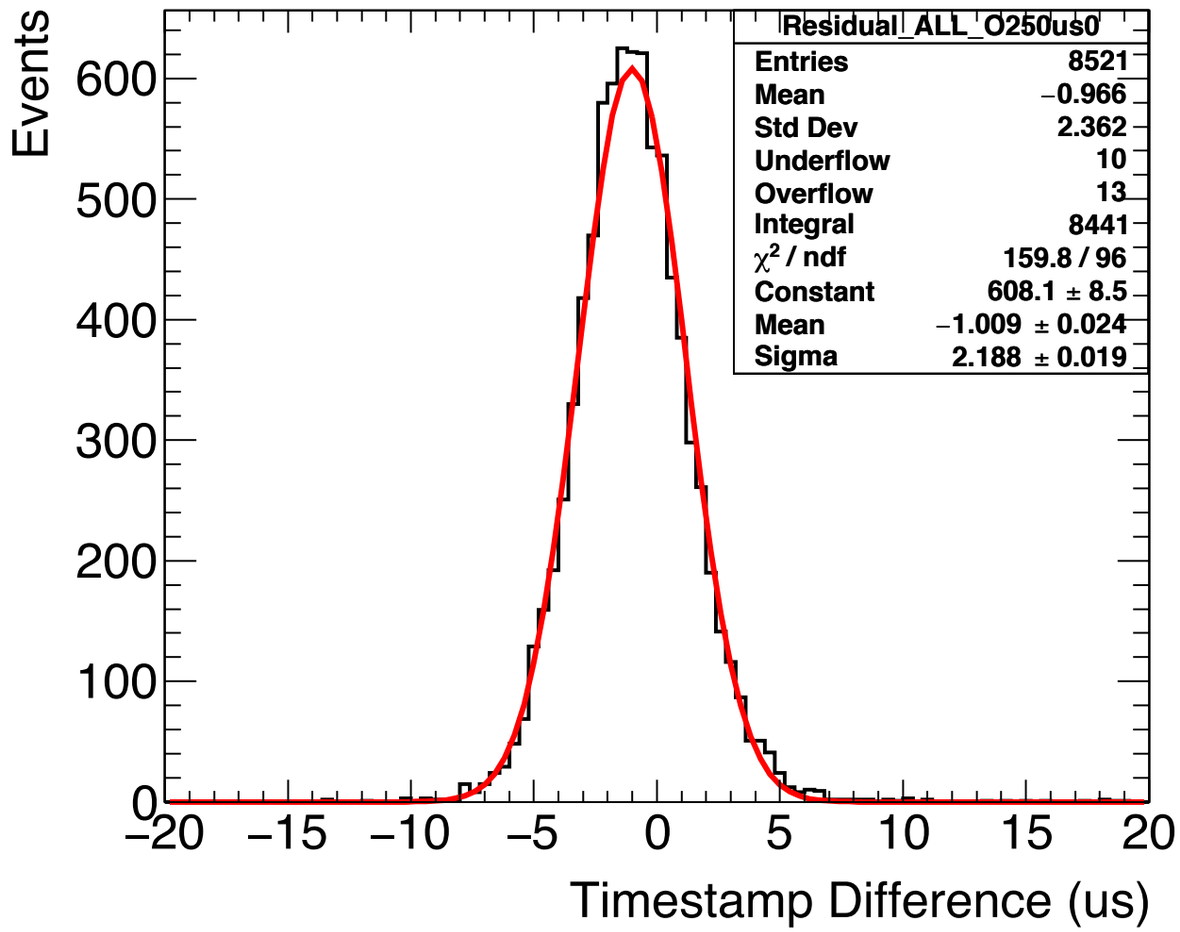


Alignment

Tracking by telescope (INTPIX4) is not performed.
Roughly aligned among SOFIST by hit position correlation.

Timestamp residual

Timestamp difference between #1 and #2.
(Hit position of #2 is within 2 pixels of #1.)



Sensor Thickness: 65 µm

Intrinsic resolution: 2.19/√2 ~ 1.55 *µs*

SOFIST3

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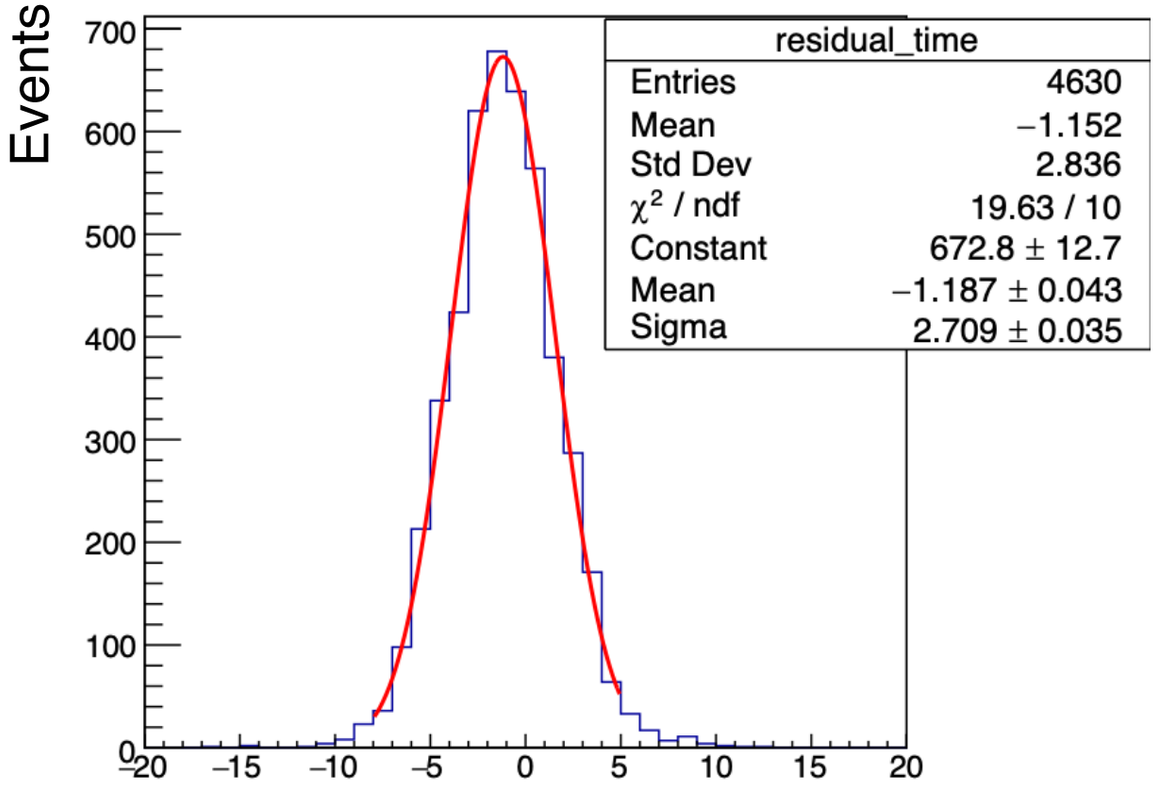
Timestamp residual

Timestamp difference between #1 and #4.

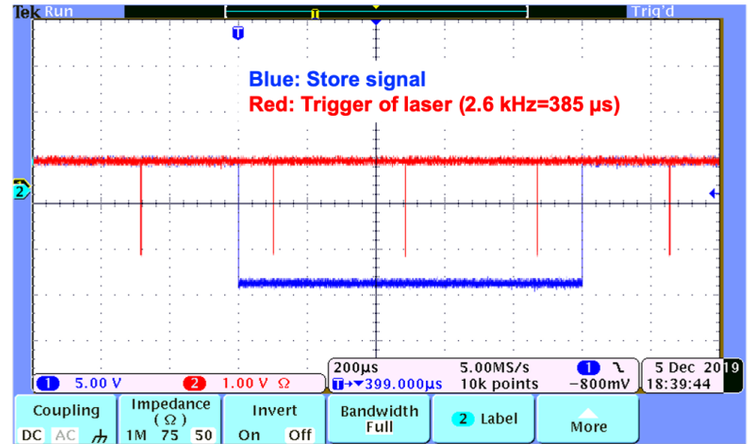


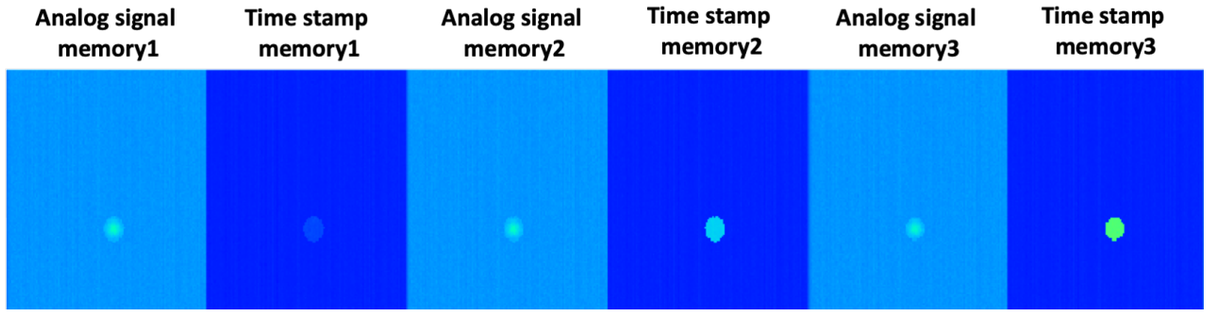
Intrinsic resolution: 2.71/√2 ~ 1.92 *μs*

Sensor Thickness: 300 μm

Multi-memory readout test

SOFIST3 has three hit, analog signal and timestamp memories. Multi-memory readout scheme was tested by injecting a IR laser three times in a 1 ms period.





Analog signal

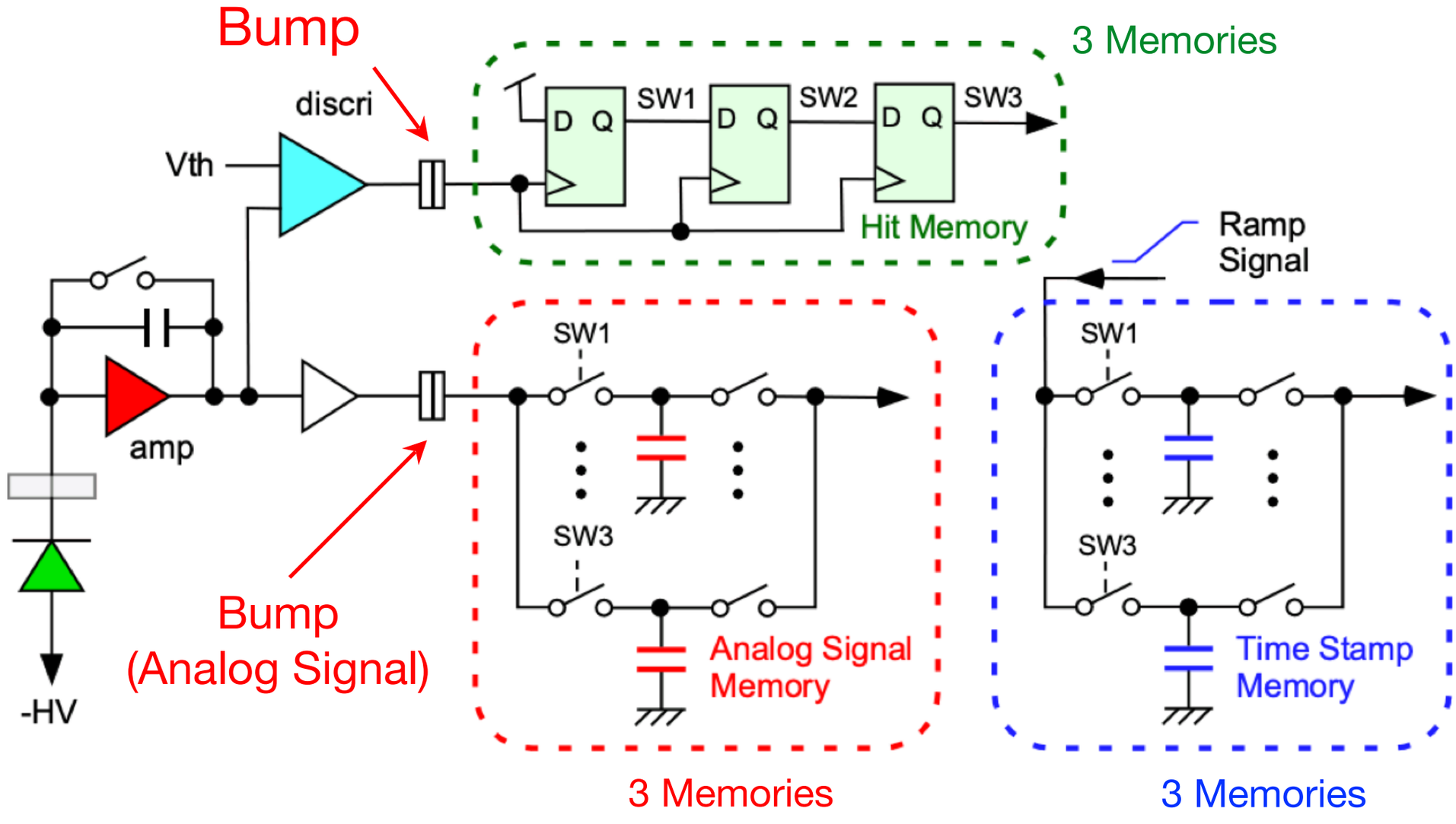
Represent stable laser pulses (~180 ADC).

Timestamp

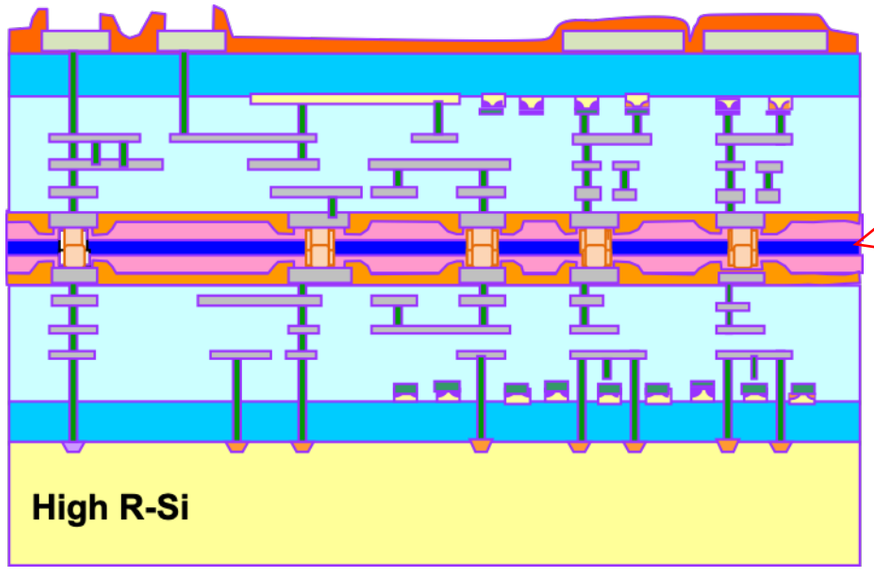
Show different timing of the laser injection (110, 490, 880 ADC).

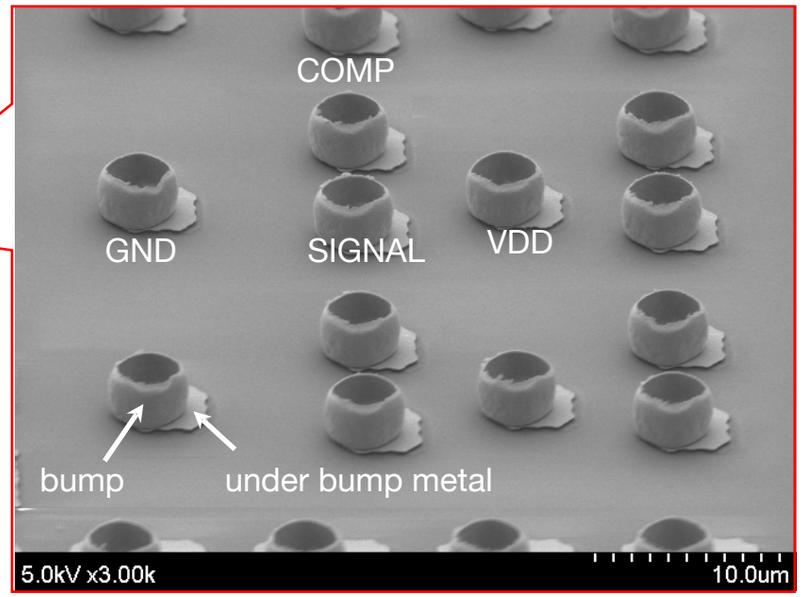
SOFIST4 Pixel

SOFIST4 pixel has all necessary functions in a pixel.
Pre. amplifier and comparator are implemented in lower pixel.
Memories (hit, analog signal and timestamp for three hits) are implemented upper pixel.
Lower and upper pixels are connected by Au cylinder micro bump (Tohoku-MicroTec Co., Ltd.)



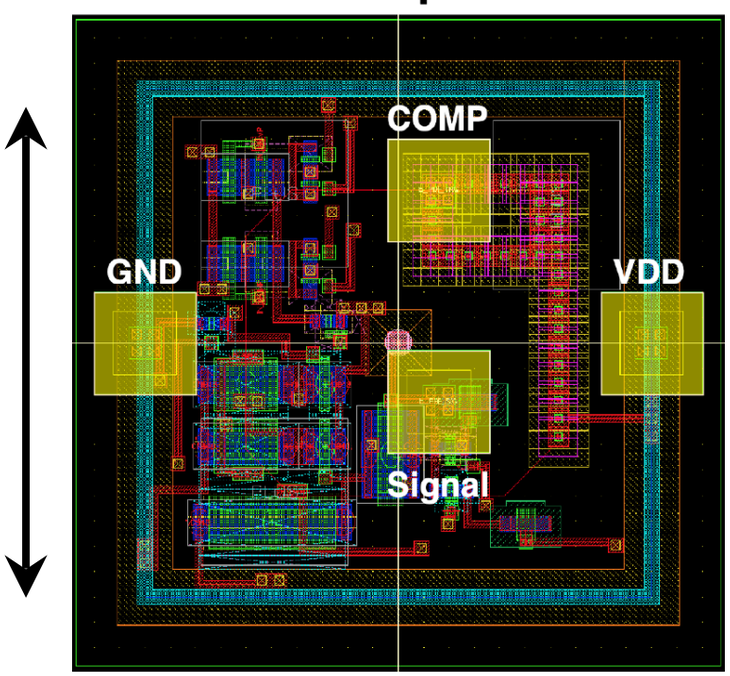
Bumps for Pixel





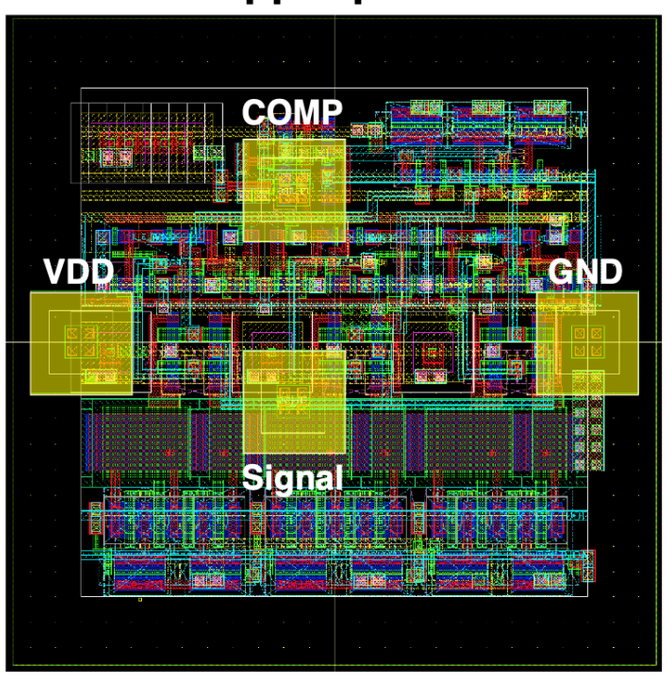
Au cylinder bump
Diameter: 3μmϕ

Lower pixel

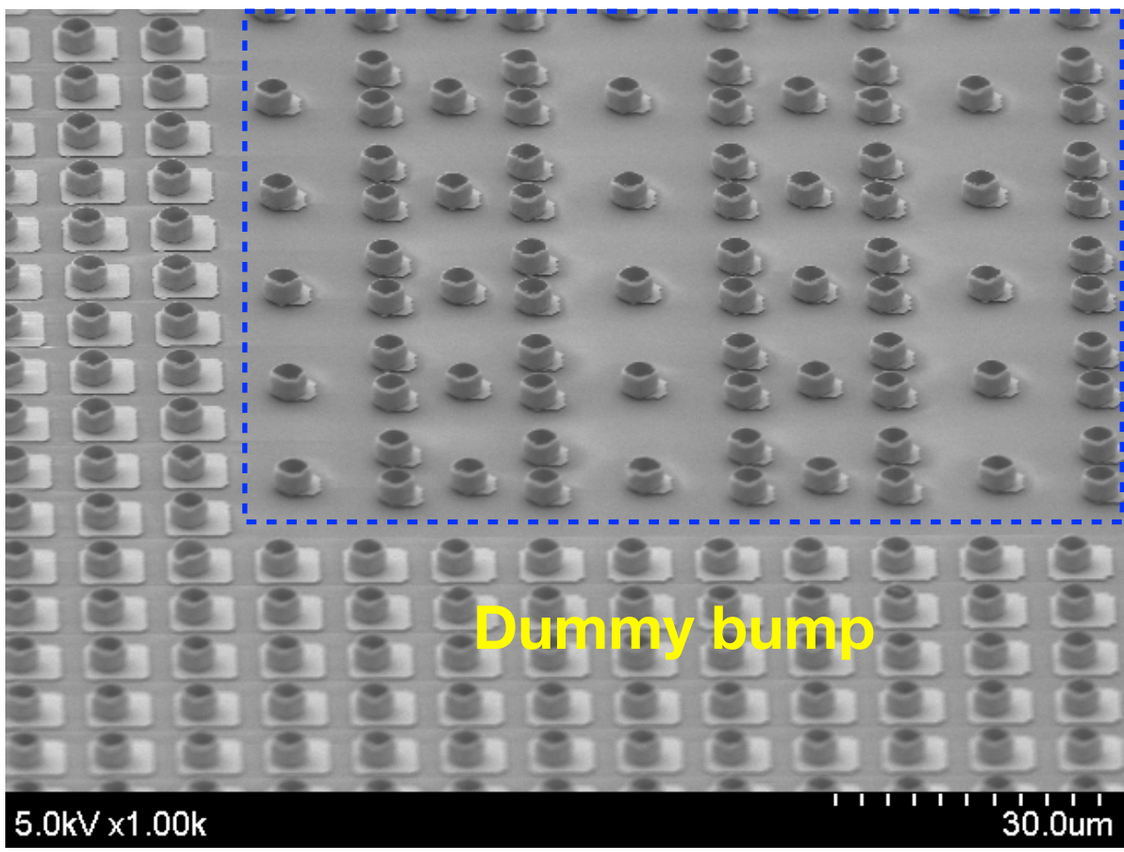


$20 \times 20\ \mu m^2$

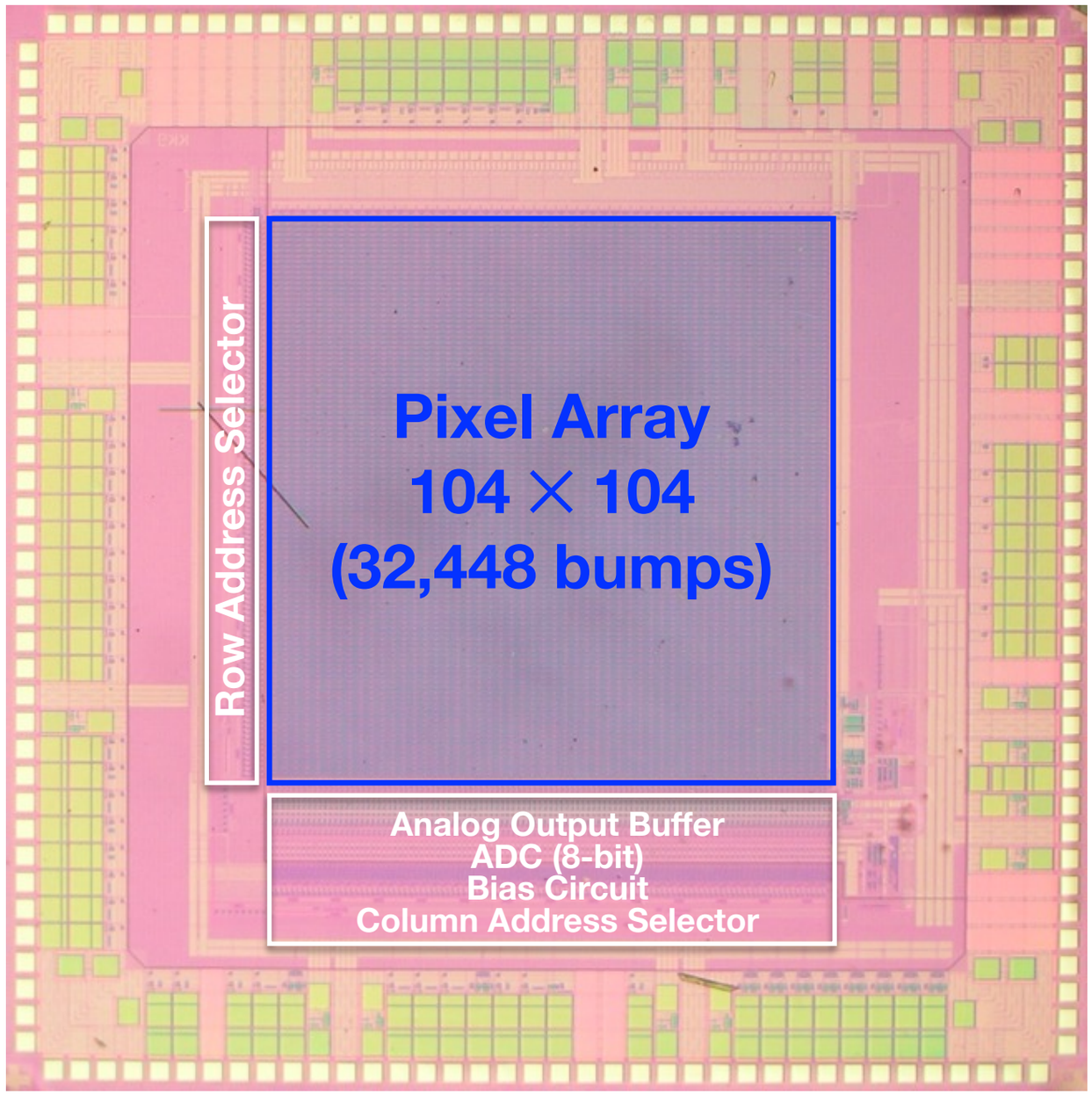
Upper pixel



Pixel array



SOFIST4 Chip



Design:

Chip size: 4.45 × 4.45 mm²

Pixel size: 20 × 20 μm²

Active area: 2.08 × 2.08 mm²

Sensor type: Double SOI, FZ *p*-type

Sensor thickness: 300 μm

Sensor resistivity: 3 – 10 kΩ · cm

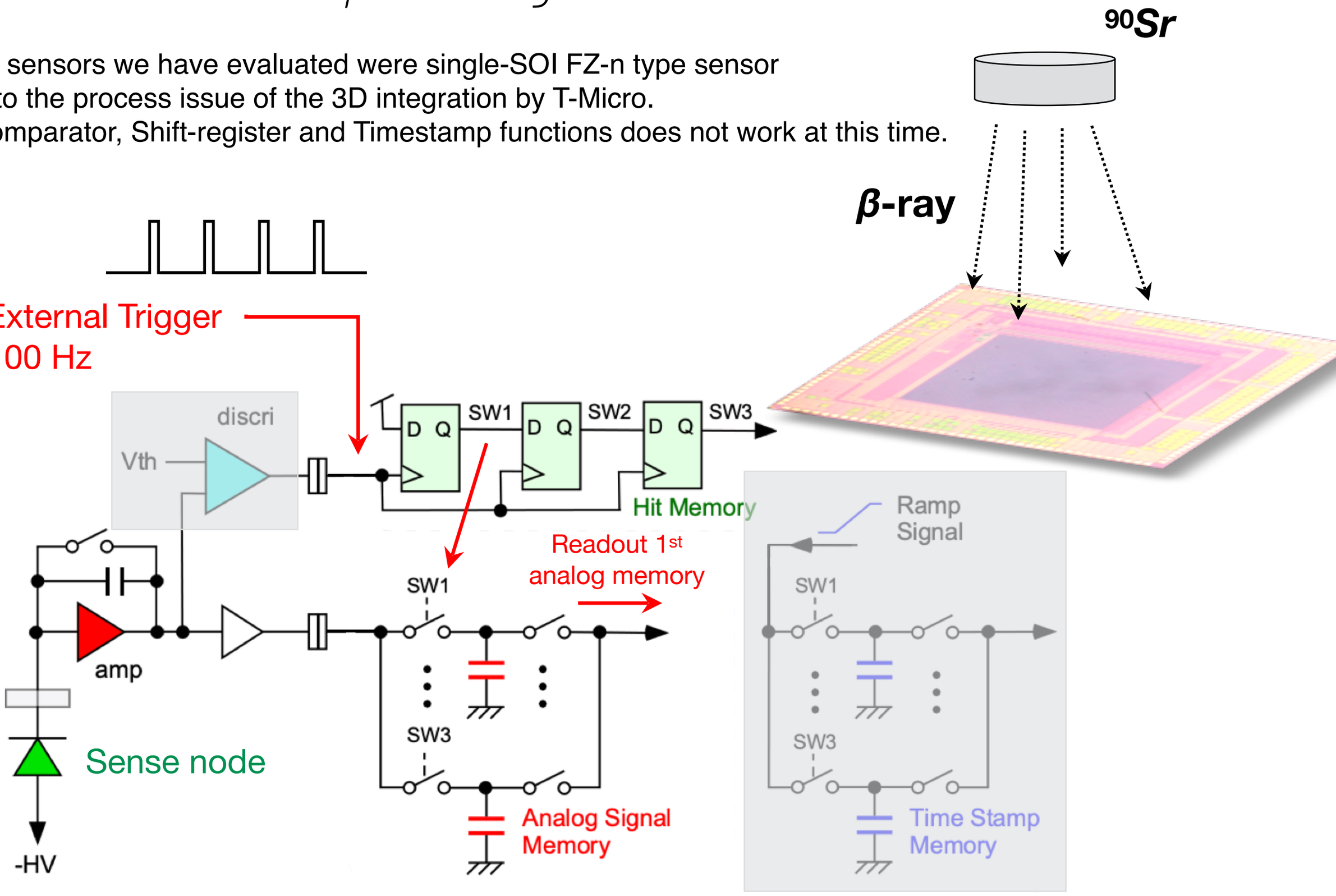
Memory: Analog 3 hits
Timestamp 3 hits
Hit 3 hits

On-Chip: 8-bit Column ADC

Total bumps: 32,448 for pixel array
3,520 for I/O cell

β-ray tracks

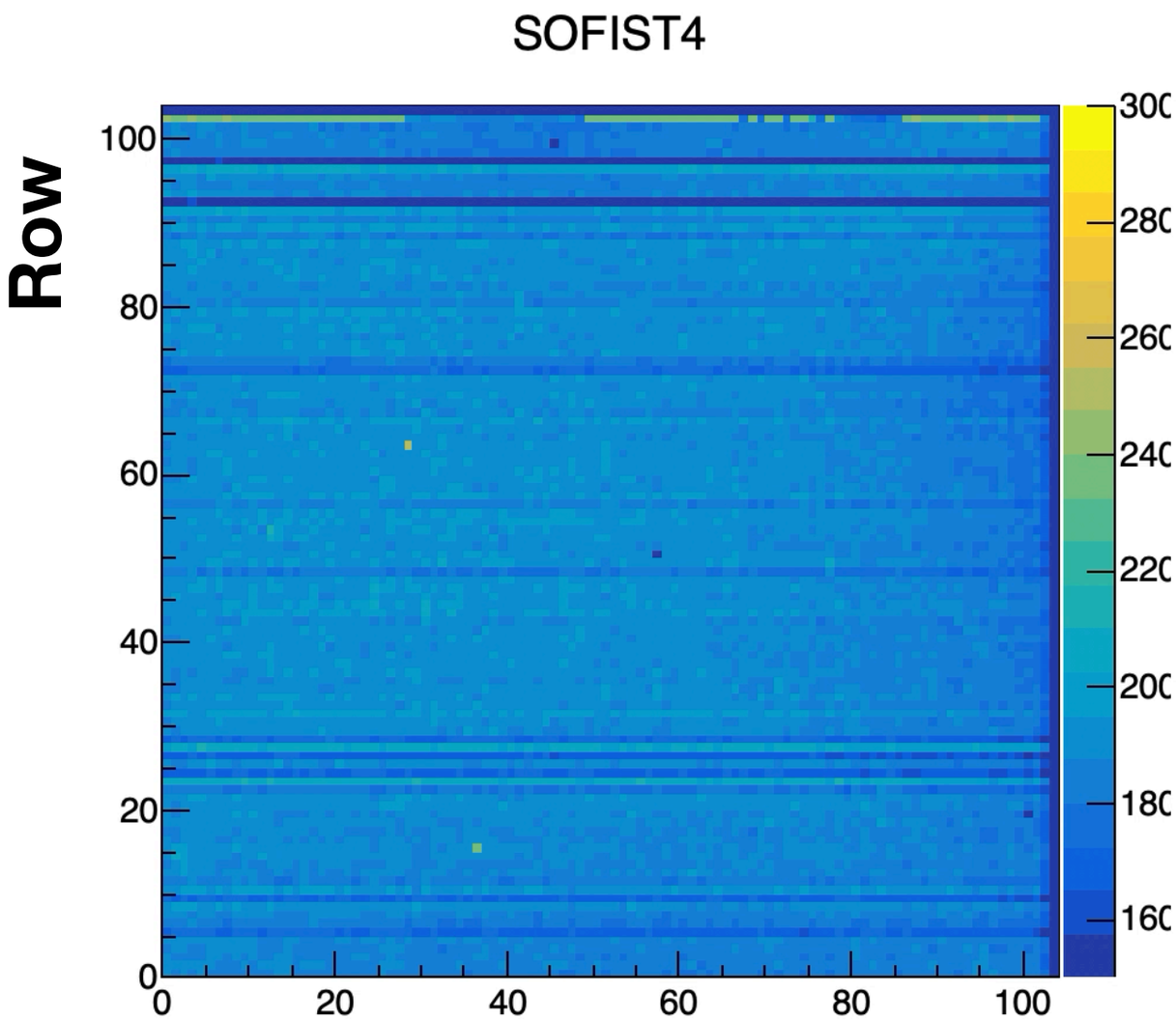
*The sensors we have evaluated were single-SOI FZ-n type sensor
due to the process issue of the 3D integration by T-Micro.
→Comparator, Shift-register and Timestamp functions does not work at this time.

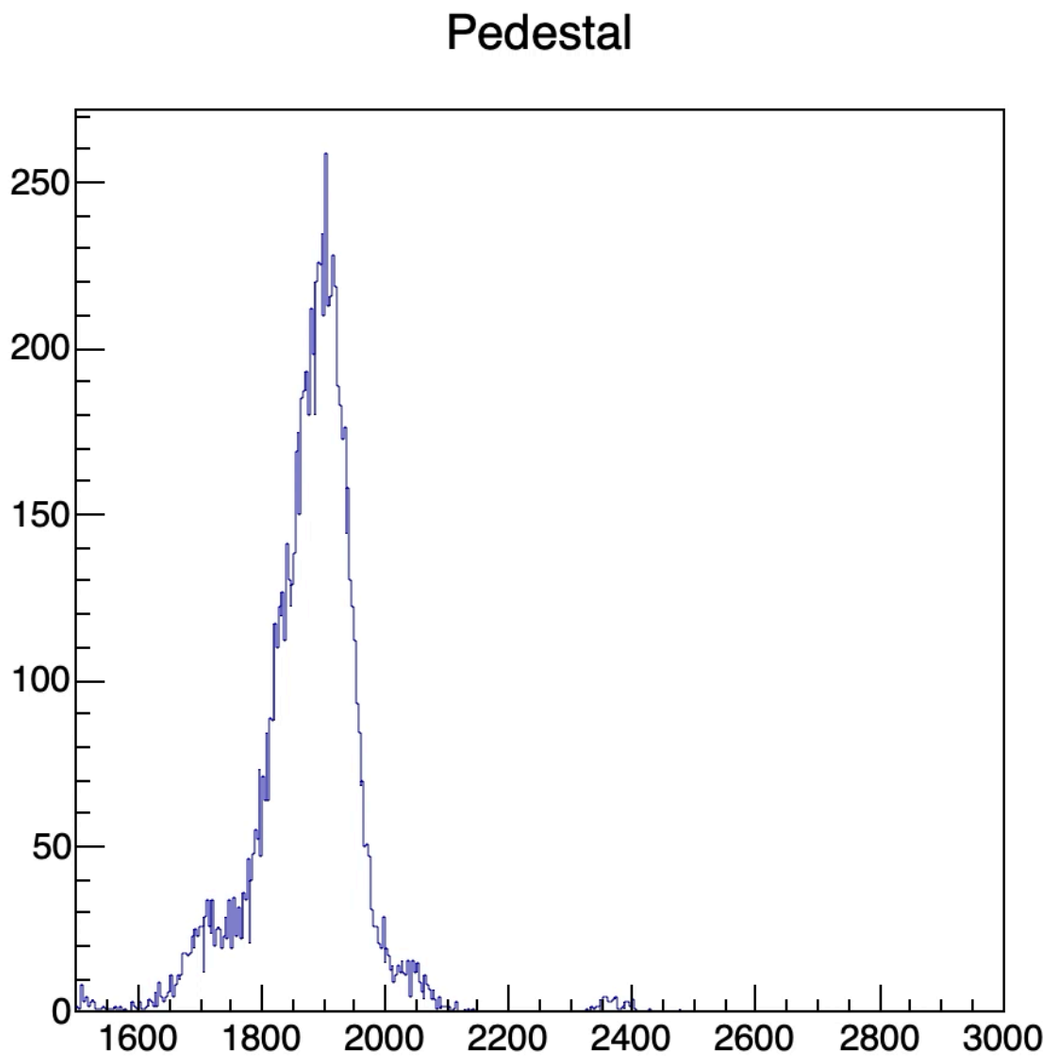


β-ray tracks

* Movie

T. Tsuboyama, KEK



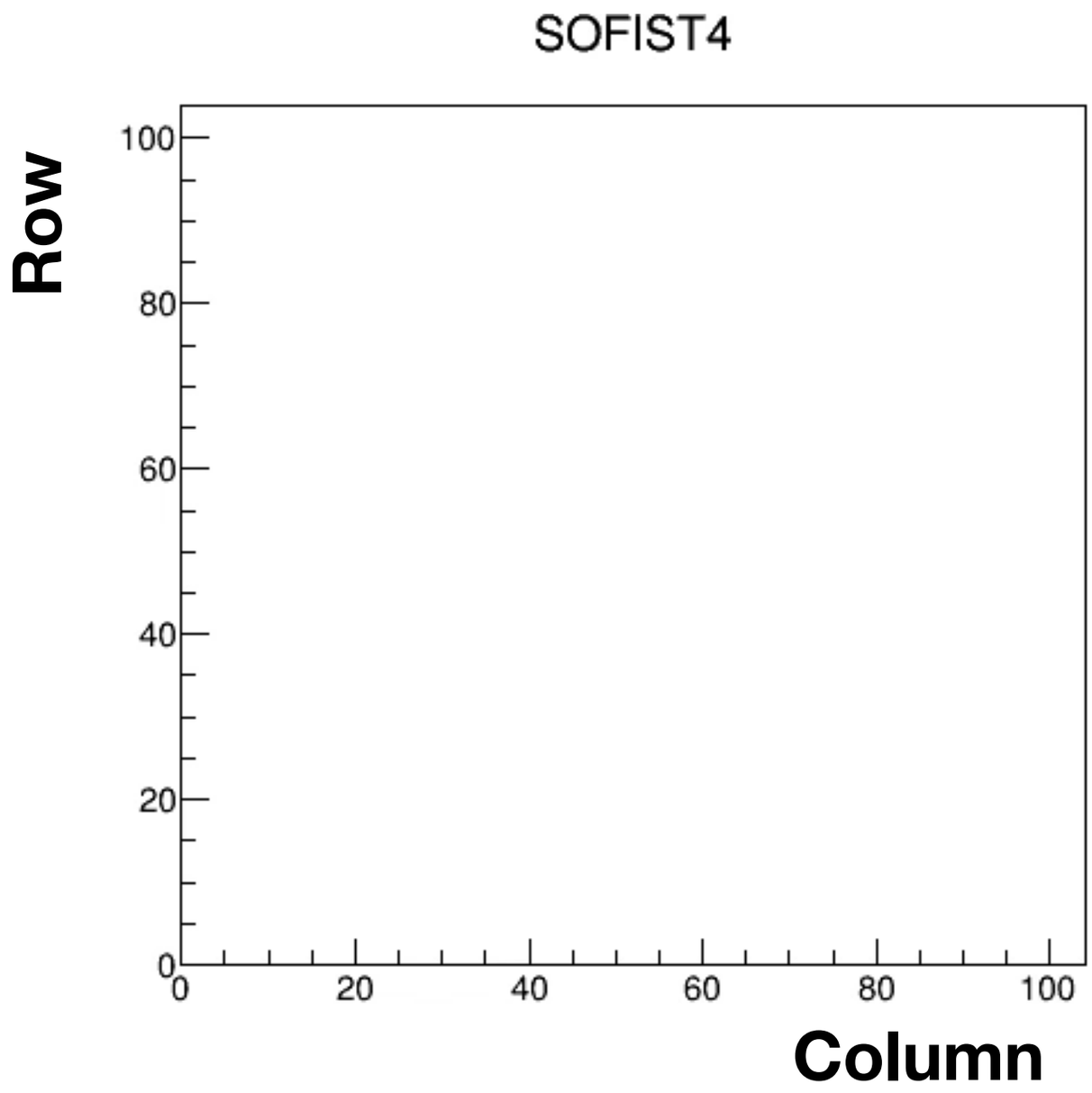


Bump Connection Yield

* Movie

Hit Map

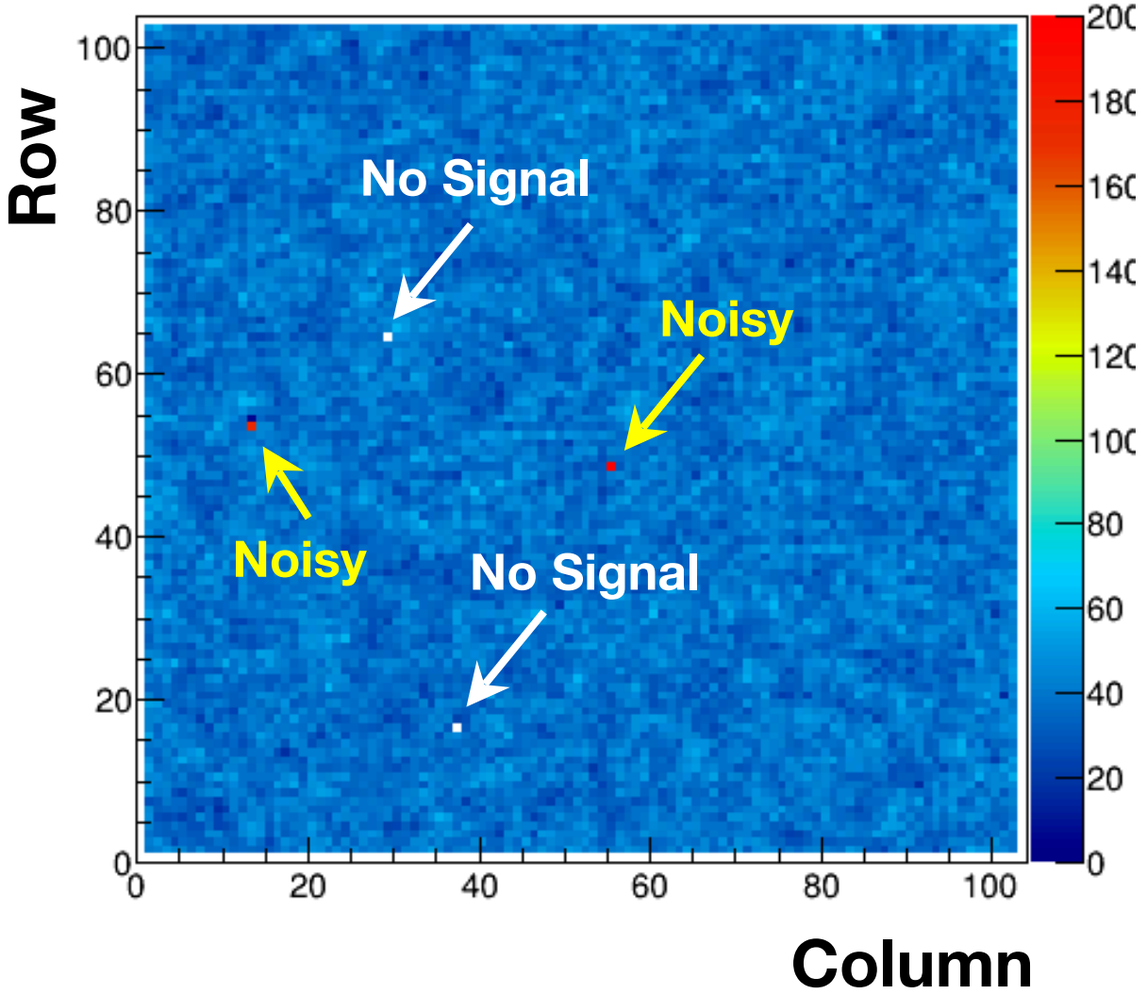
T. Tsuboyama, KEK

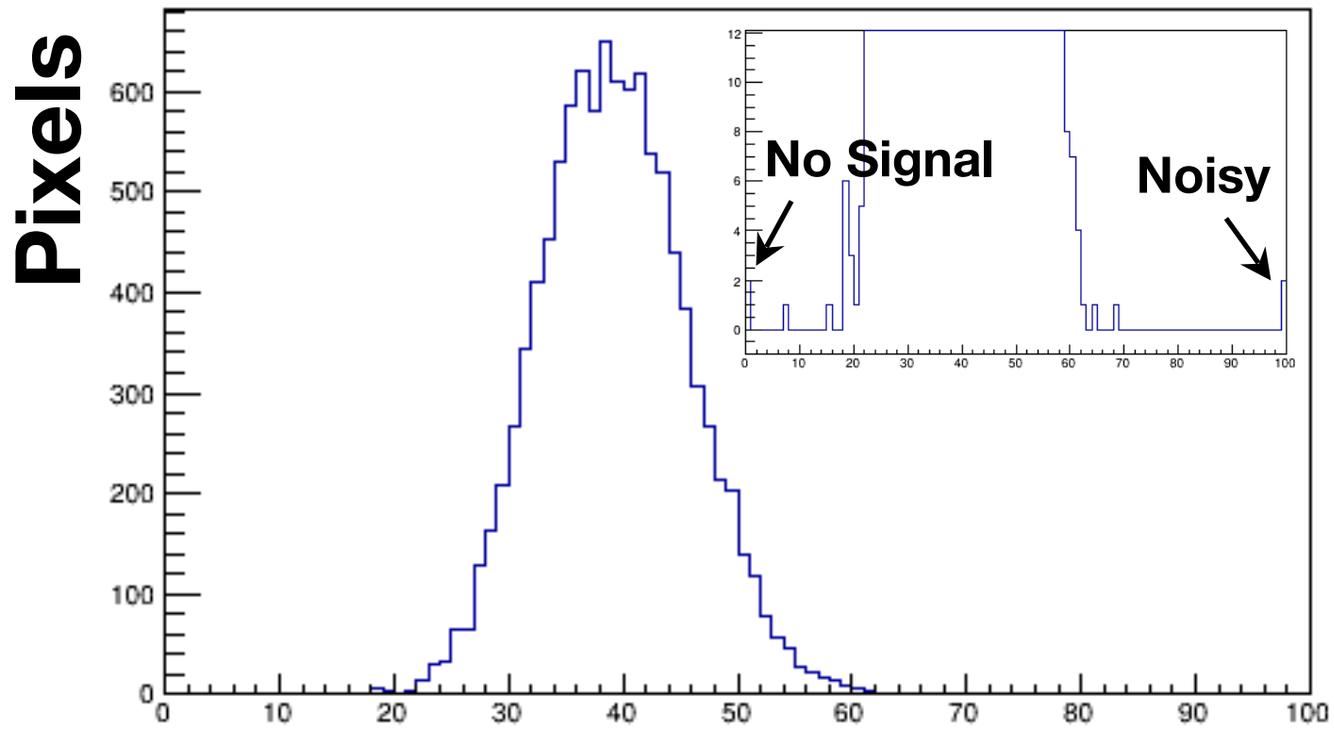


Bump Connection Yield

T. Tsuboyama, KEK

Hit Map (50 kEvents)





Connection Yield:
(102 × 102 – 2) / 102 × 102 ~ 99.98 %

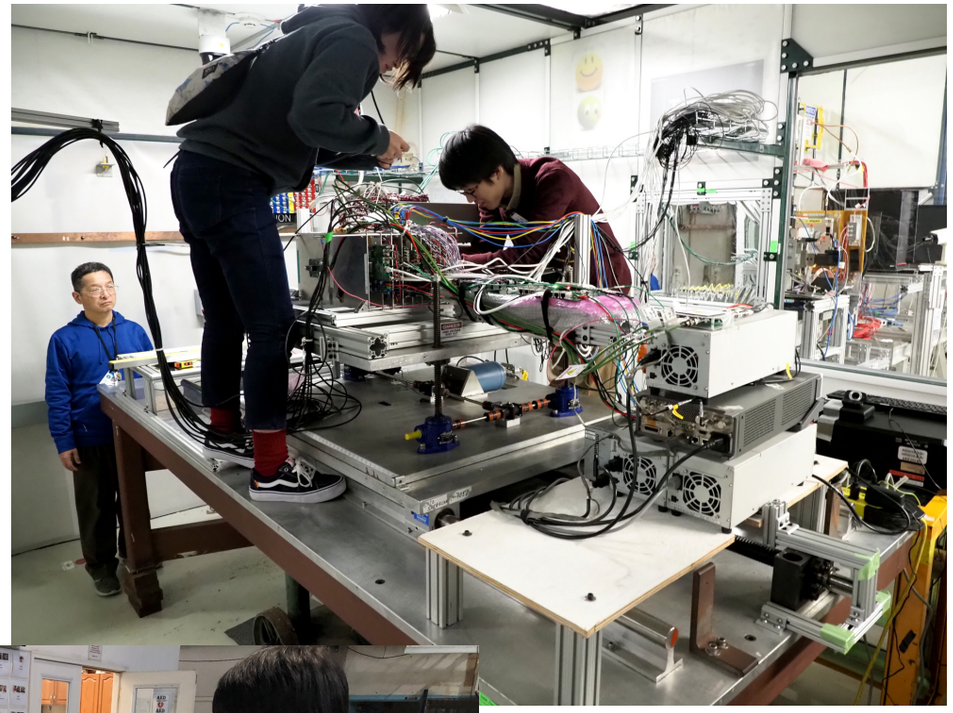
Reject the outermost pixels for the calculation.

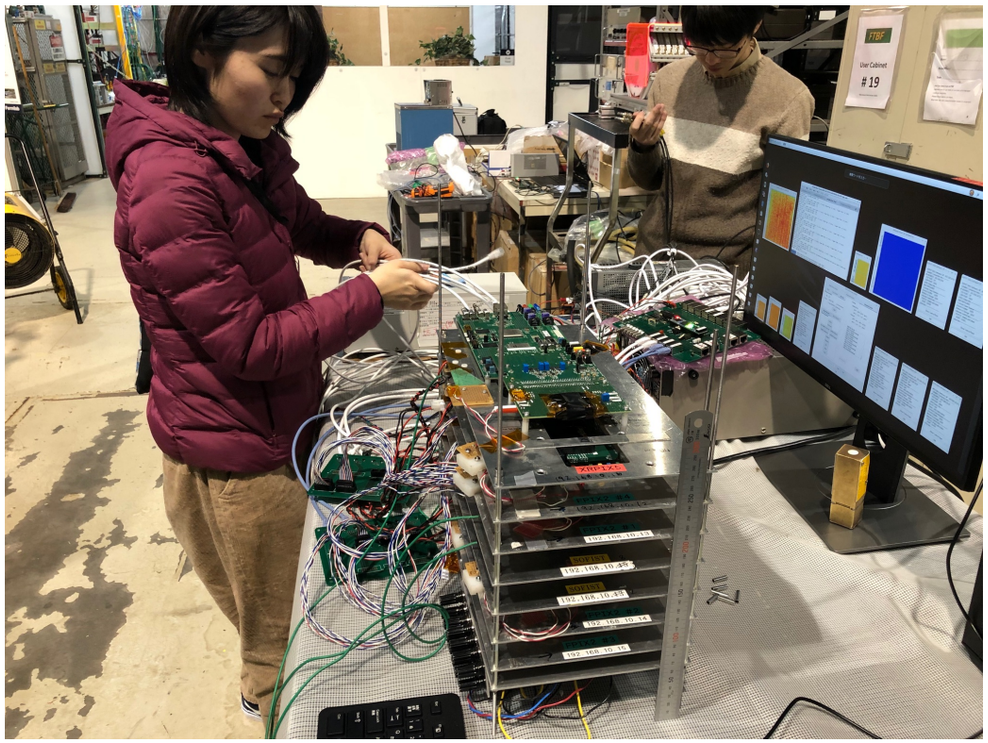
Beam Test 2020 @ FTBF

Fermilab Beam Test Facility
Beam time: Feb. 26th - Mar. 8th, 2020
120 GeV proton beam

Members
- TMCIT, KEK, Univ. Tsukuba and Miyazaki Univ. (Japan)

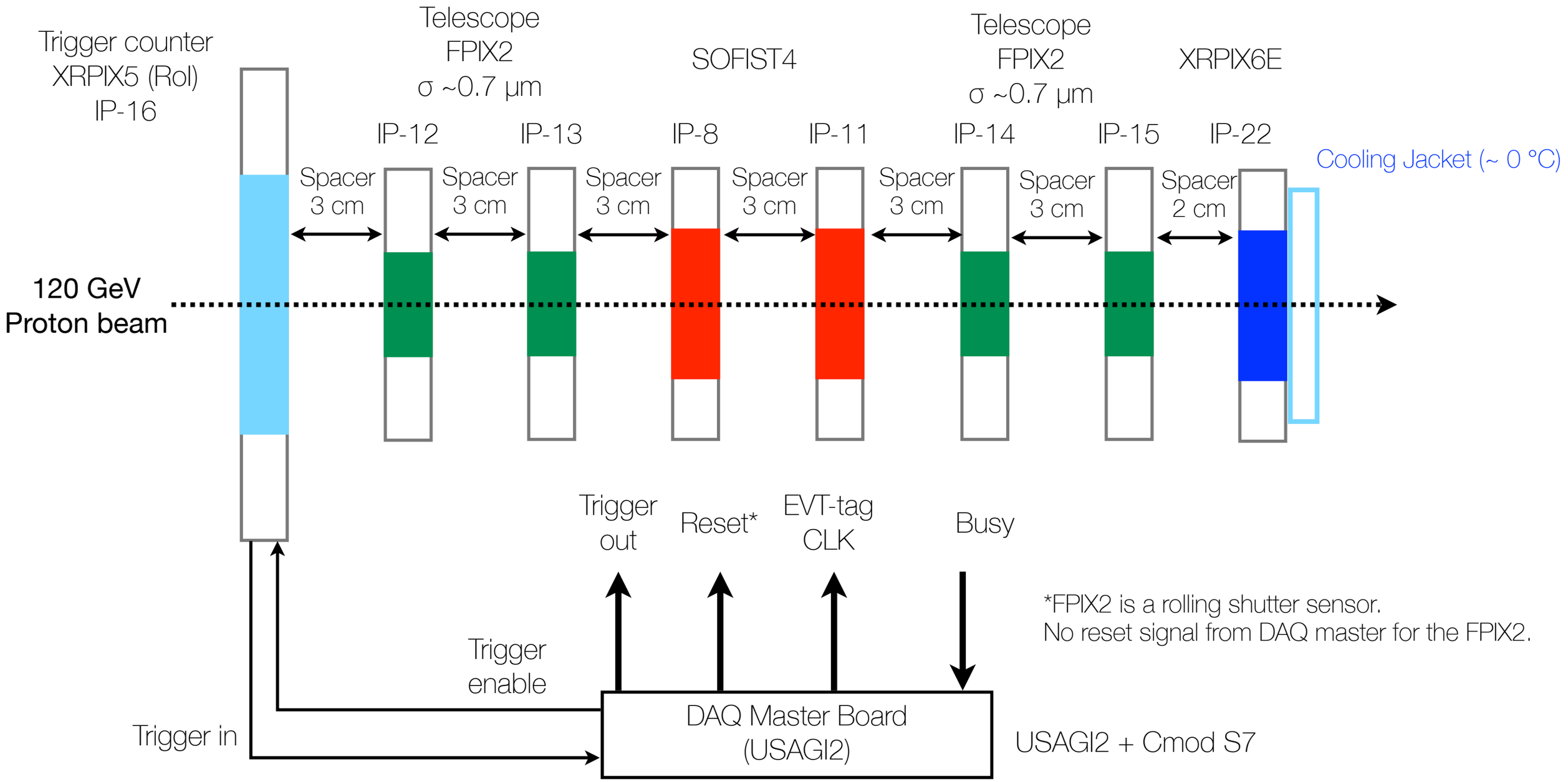
Sensors (All SOIPIX)
- SOFIST4 and XRPIX6E (DUT)
- FPIX2 (Telescope)
- XRPIX5 (Trigger)



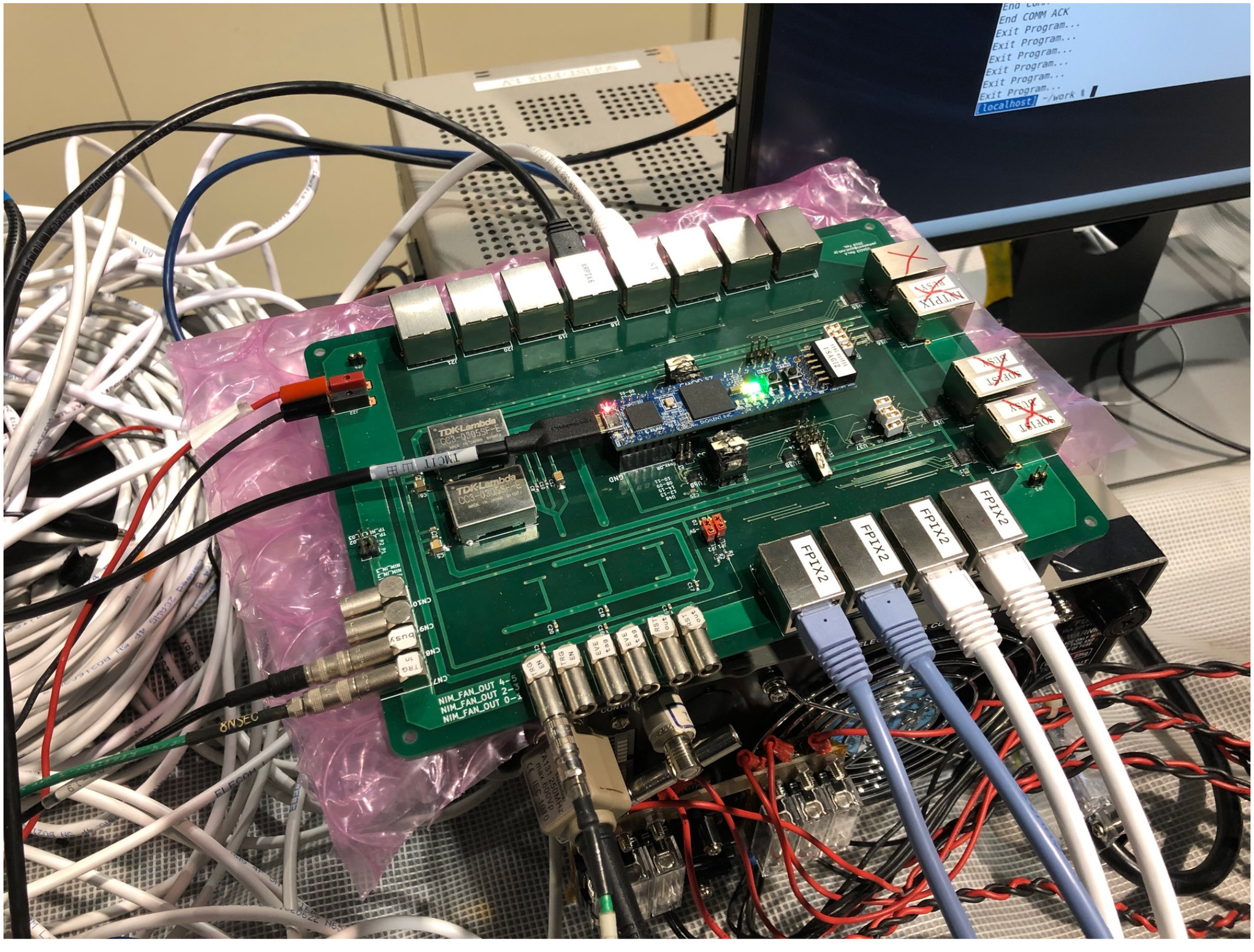


Setup

Telescope + Trigger counter + DUT

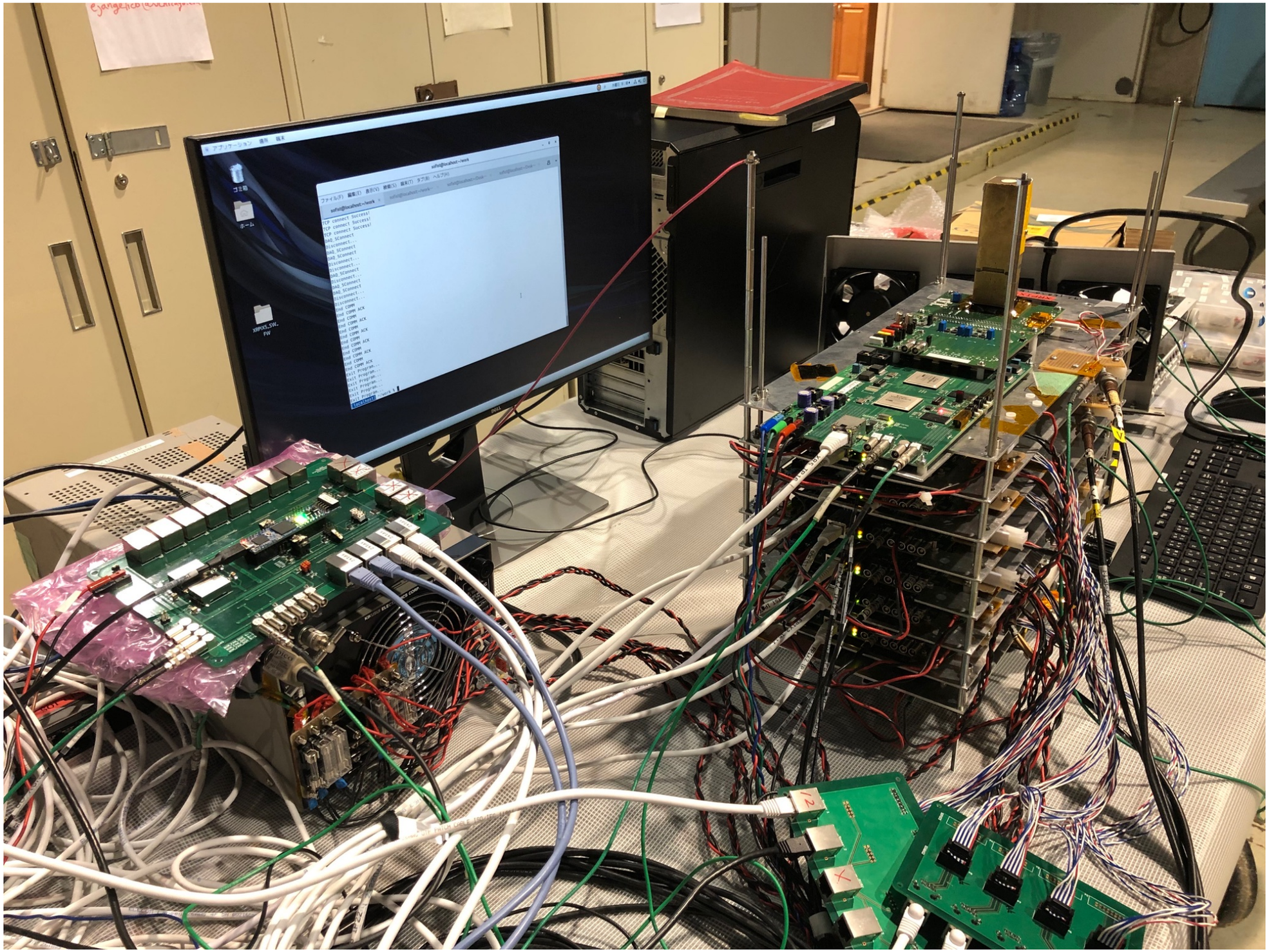


DAQ Master (USAGI2)



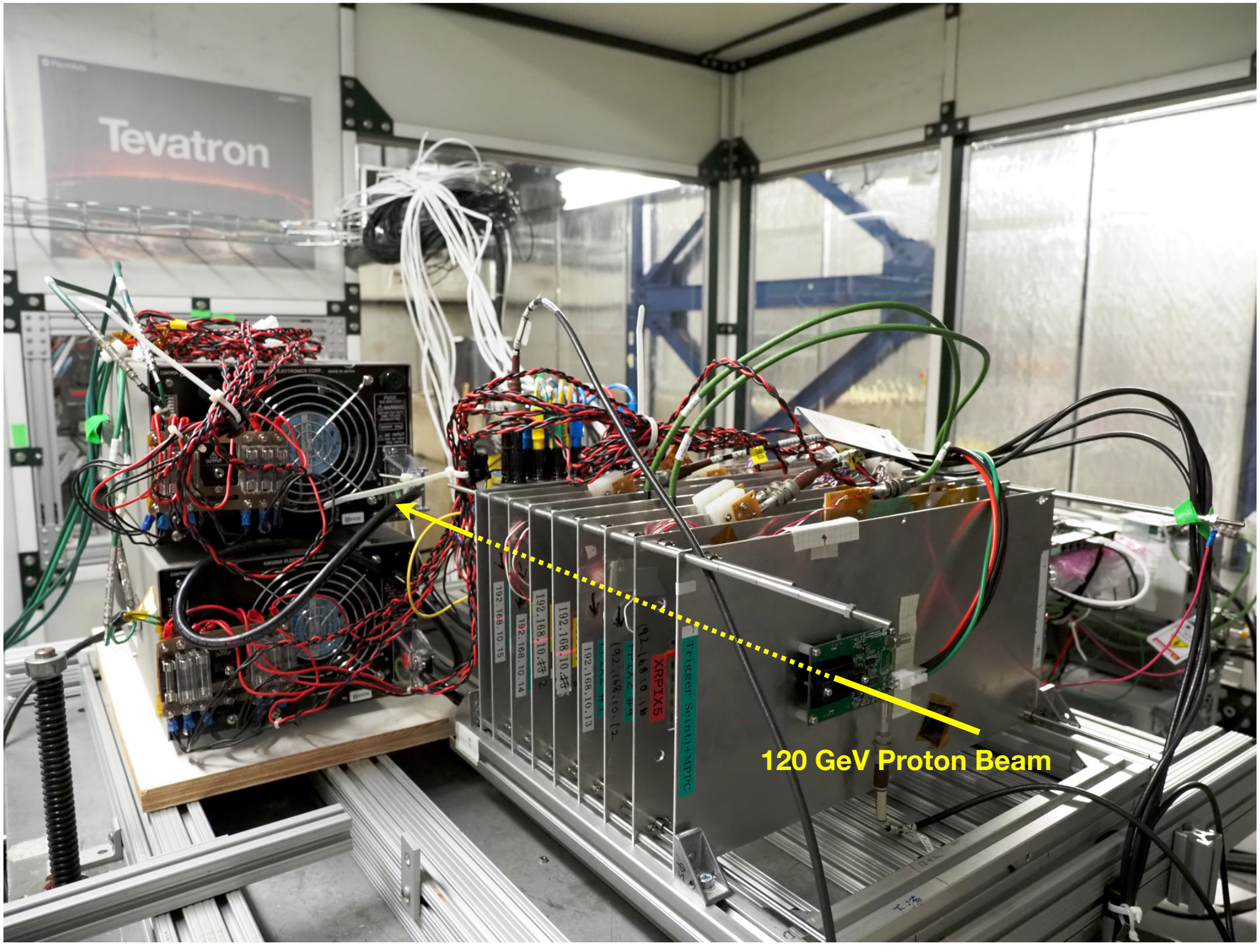
Setup

Checking the DAQ system by beta source



Setup

Setup at the beam line



Hit Correlation

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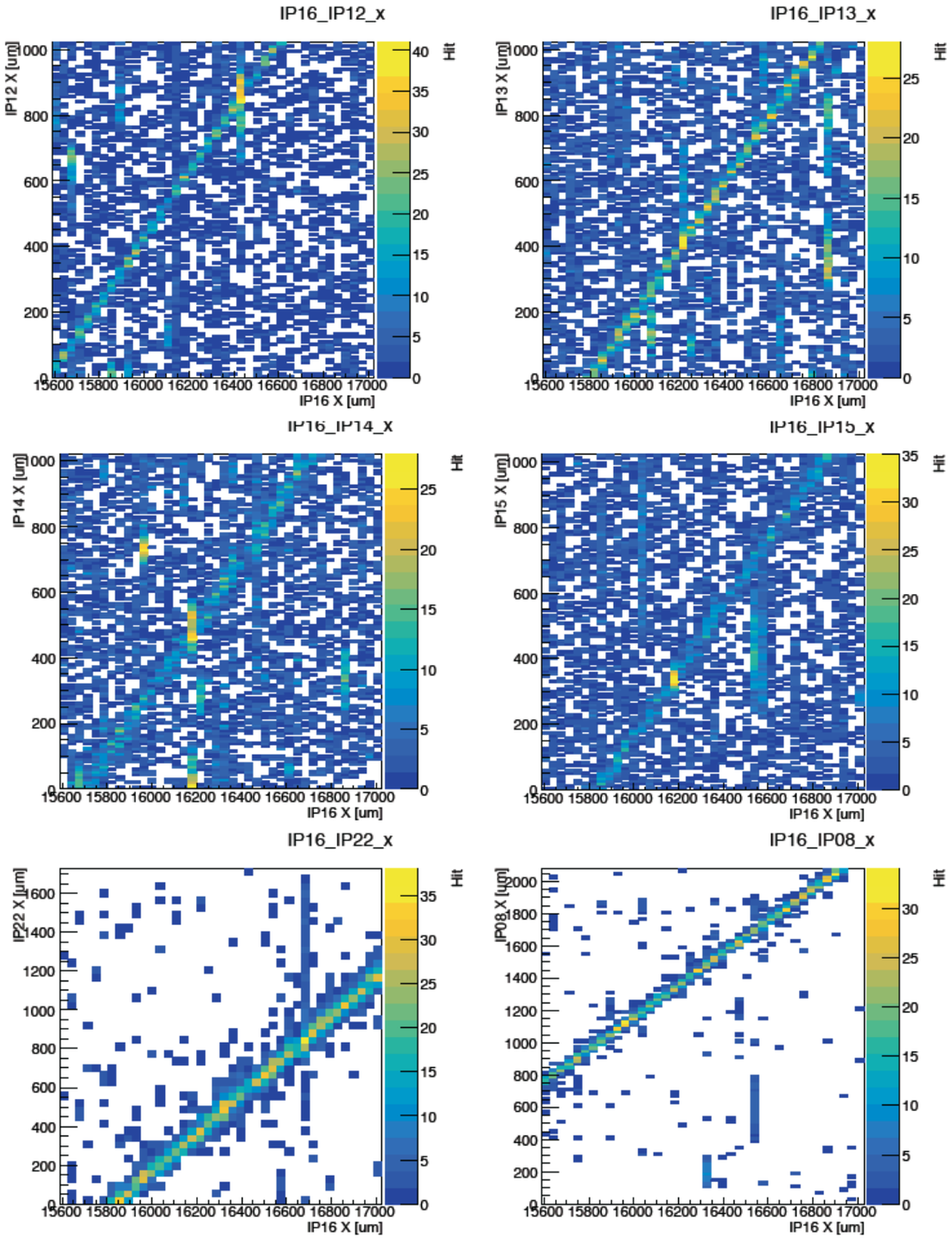
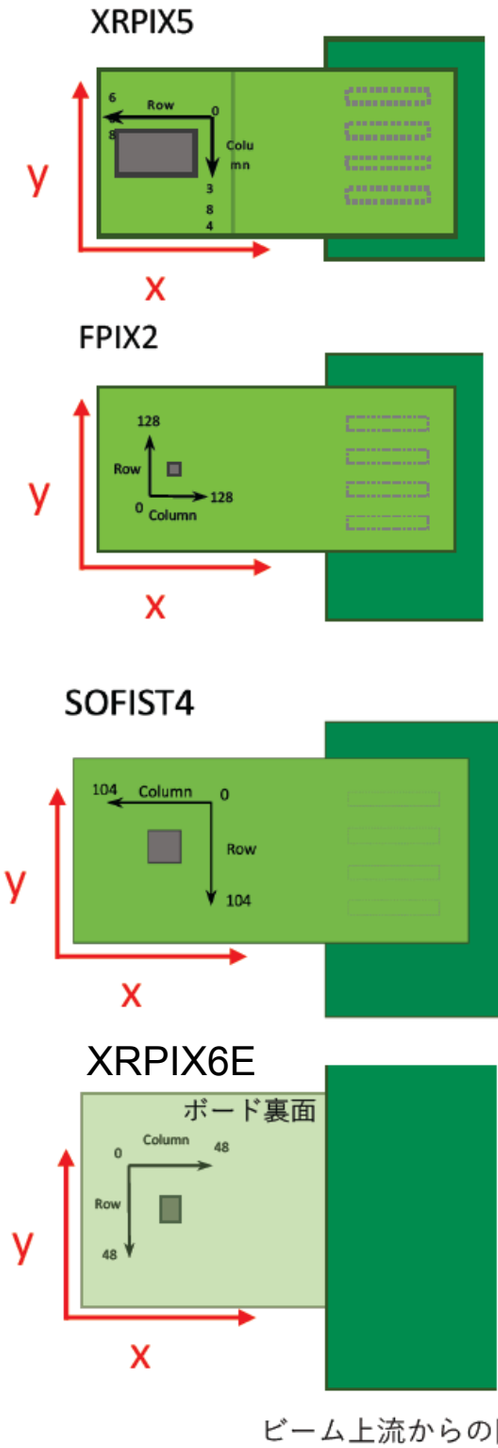
RunID_0243

XRPIX5との
x座標の相関





IP16

IP12-15

IP8, 11

IP22

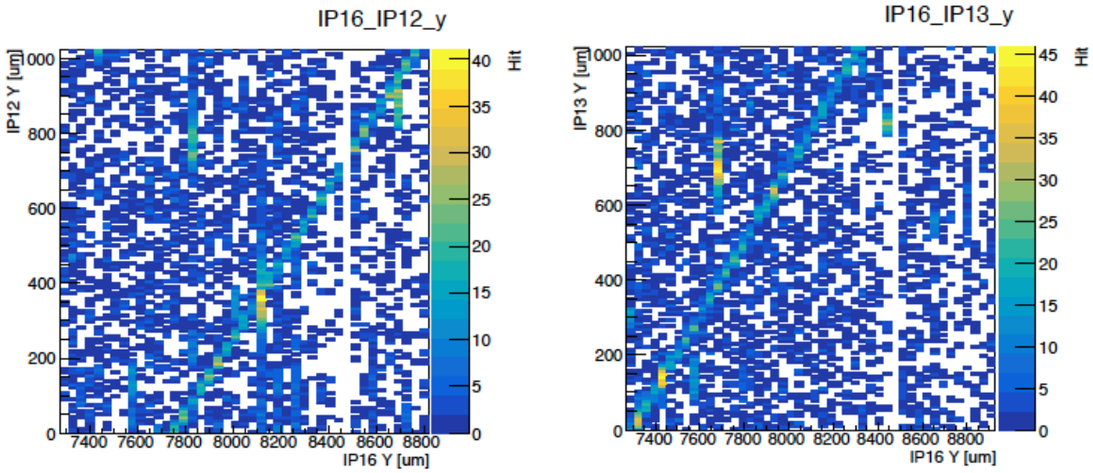
ビーム上流からの図

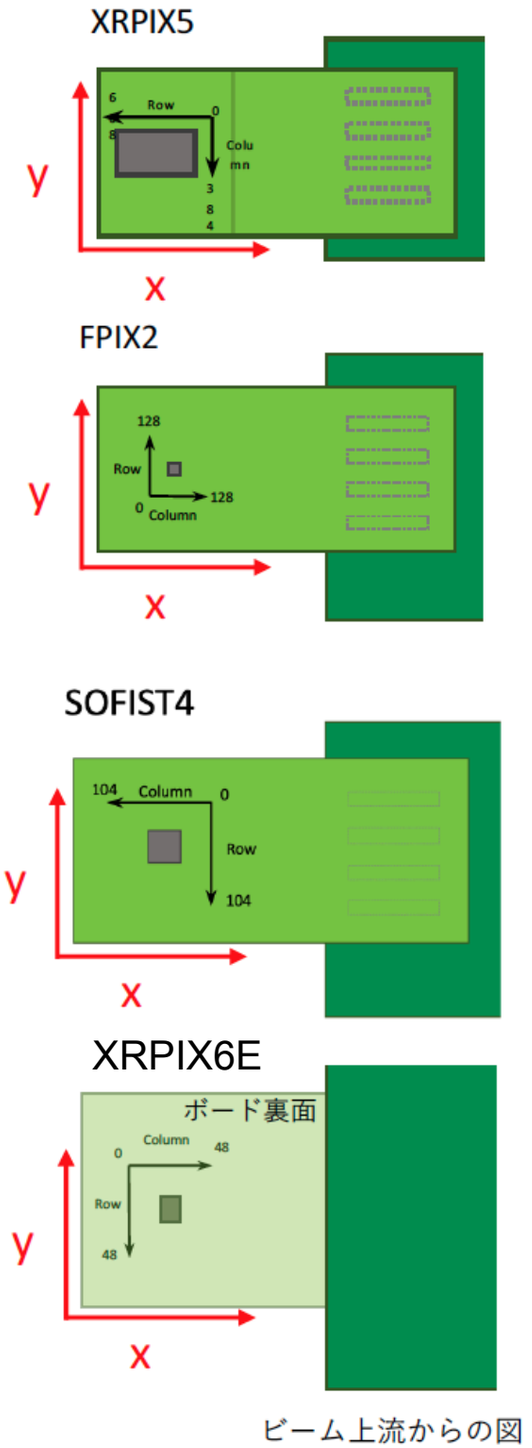
Hit Correlation

H. Murayama, Univ. Tsukuba

RunID_0243

XRPIX5との
y座標の相関





IP16

IP12-15

IP8, 11

IP22

Summary

Monolithic type pixel detector has been developed with SOI technology
for the ILC vertex detector.

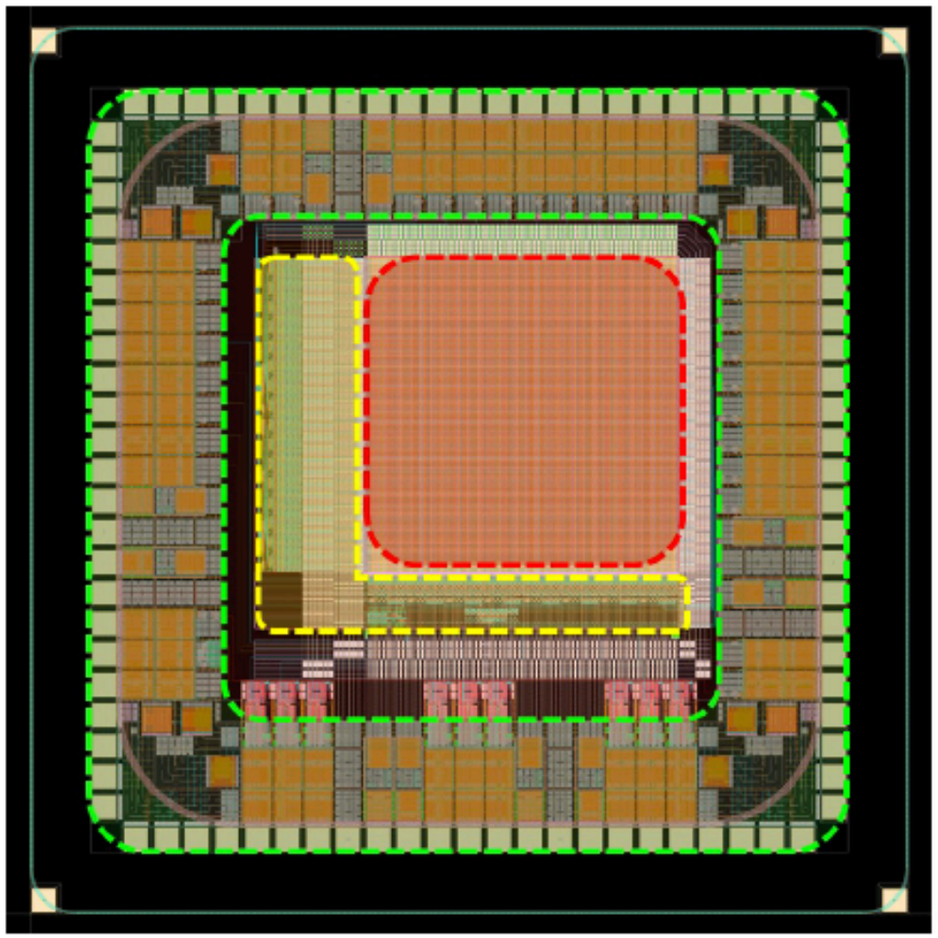
We have already demonstrated 1.4 μm of spatial resolution and 1.55 μs of
time resolution by the prototype, SOFIST1 and 2.

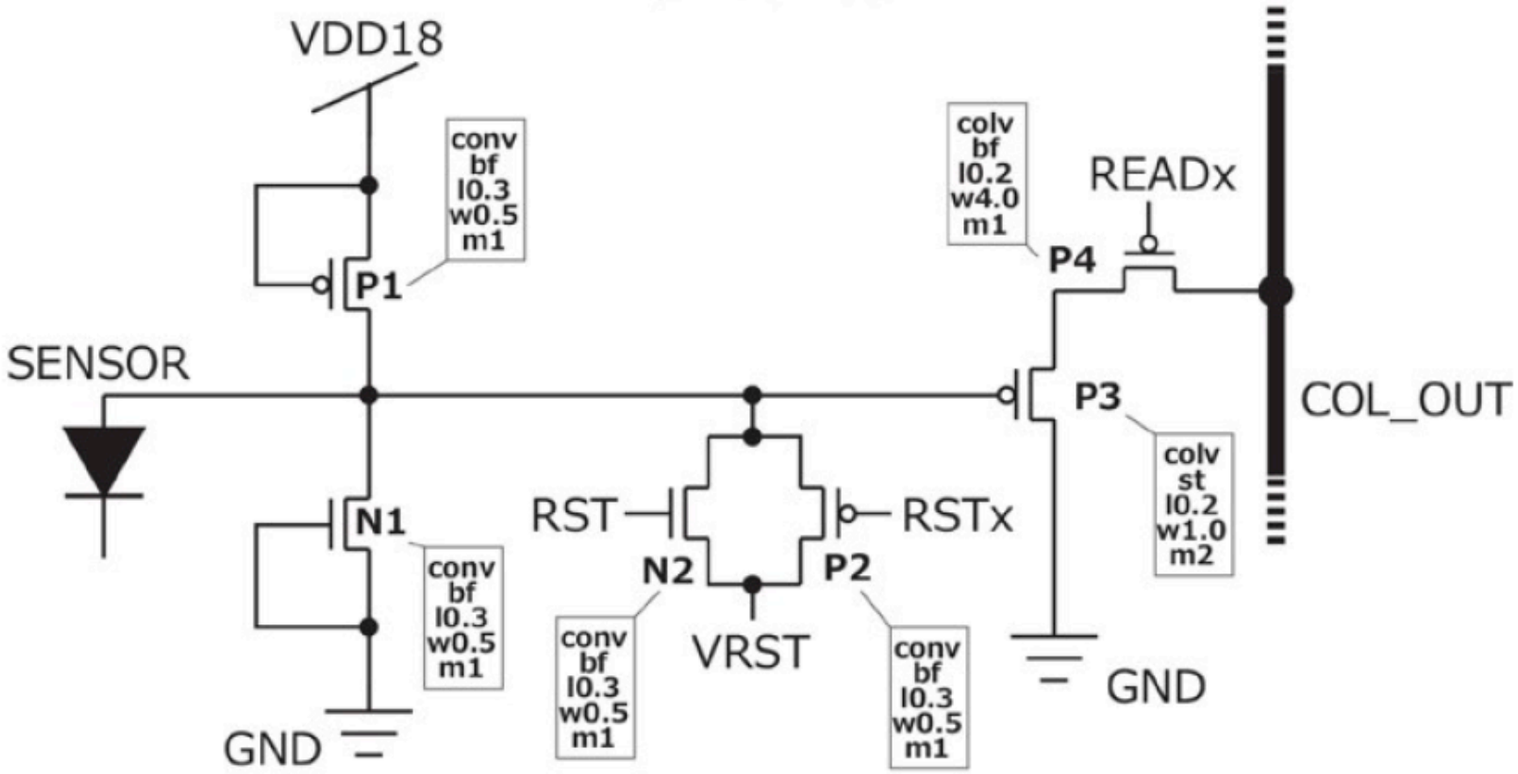
SOFIST4 is 3D integrated SOI pixel detector
→ Three kinds of multiple memories, Hit, Position, and Timestamp are implemented
in 20 × 20 μm^2.
Demonstrated the images of the β-ray tracks of ^{90}Sr with
a bump connection yield of 99.9%.
Data analysis of the beam test in 2020 is still working in progress.

We are planning to reprocess SOFIST4 to evaluate the full function.
Additionally, we'd like to try to integrate thinned SOFIST4 sensor (~65 μm thickness).

Backup

FPIX2





chip size	2.9 mm × 2.9 mm
pixel size	8 μm × 8 μm
# of pixels	128 × 128
active region	1024 μm × 1024 μm
parallel readout	8 (128 × 16 pixels / readout)
readout scheme	rolling shutter

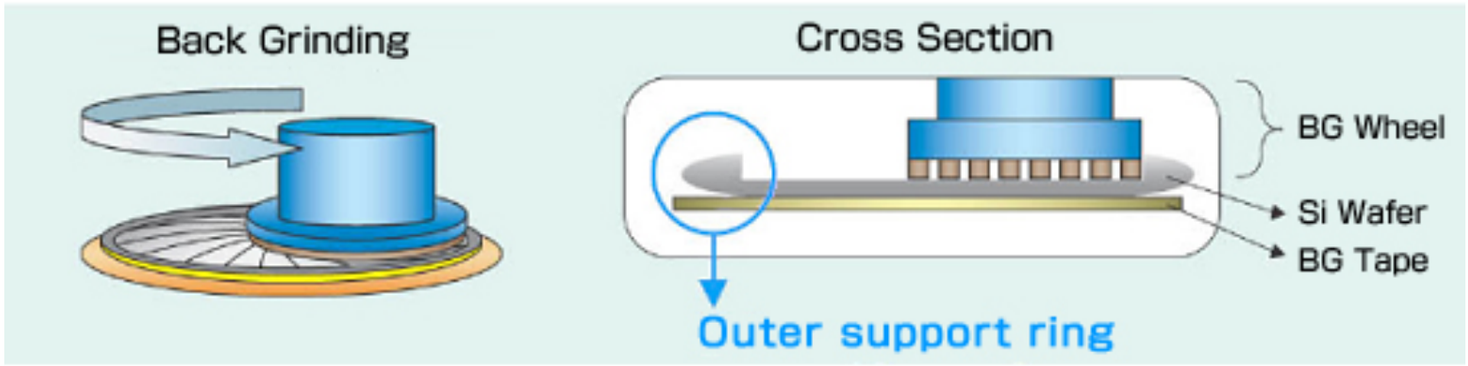
Sensor: Single SOI, FZ-p, ~25 kΩ・cm, 500 μm thick

Position resolution ~0.7 μm
tested at FTBF in 2017

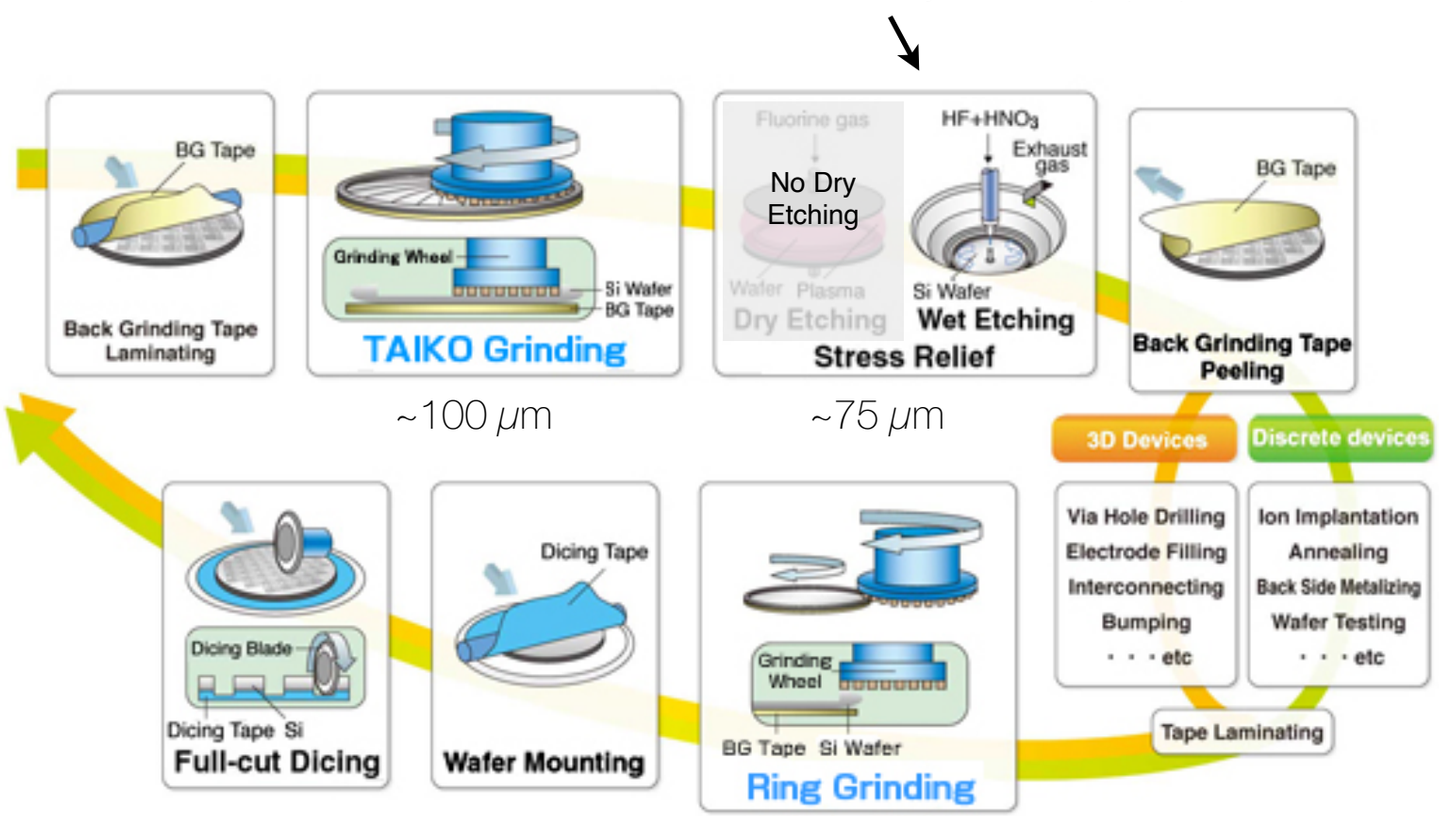
Wafer Thinning

DISCO
Kiru·Kezuru·Migaku Technologies

TAIKO Process by DISCO Corporation (Japan)



Stress relief with wet etching by
Mimasu Semiconductor Industry Co., Ltd. (Japan)



TAIKO Process
with outer support ring

- Lower wafer warpage
- Improve of wafer strength
- Easy wafer handling
- Easy backside processing (ion implantation, annealing, Metalizing etc) after thinning

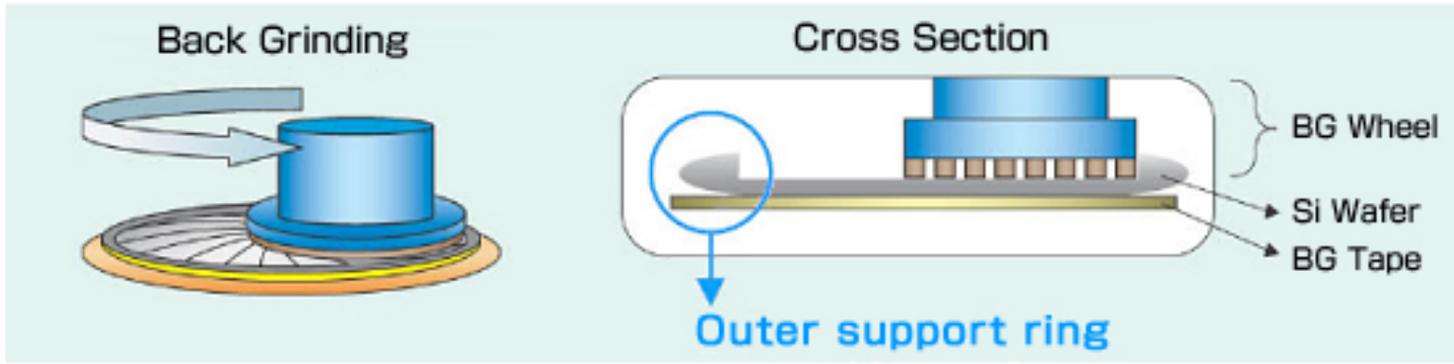
Back side process after thinning

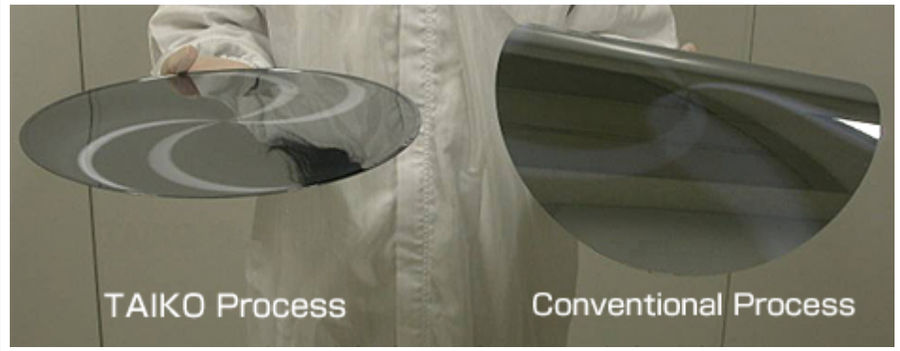
- Boron implantation (ULVAC, Japan)
- Laser Annealing (SHI, Japan)

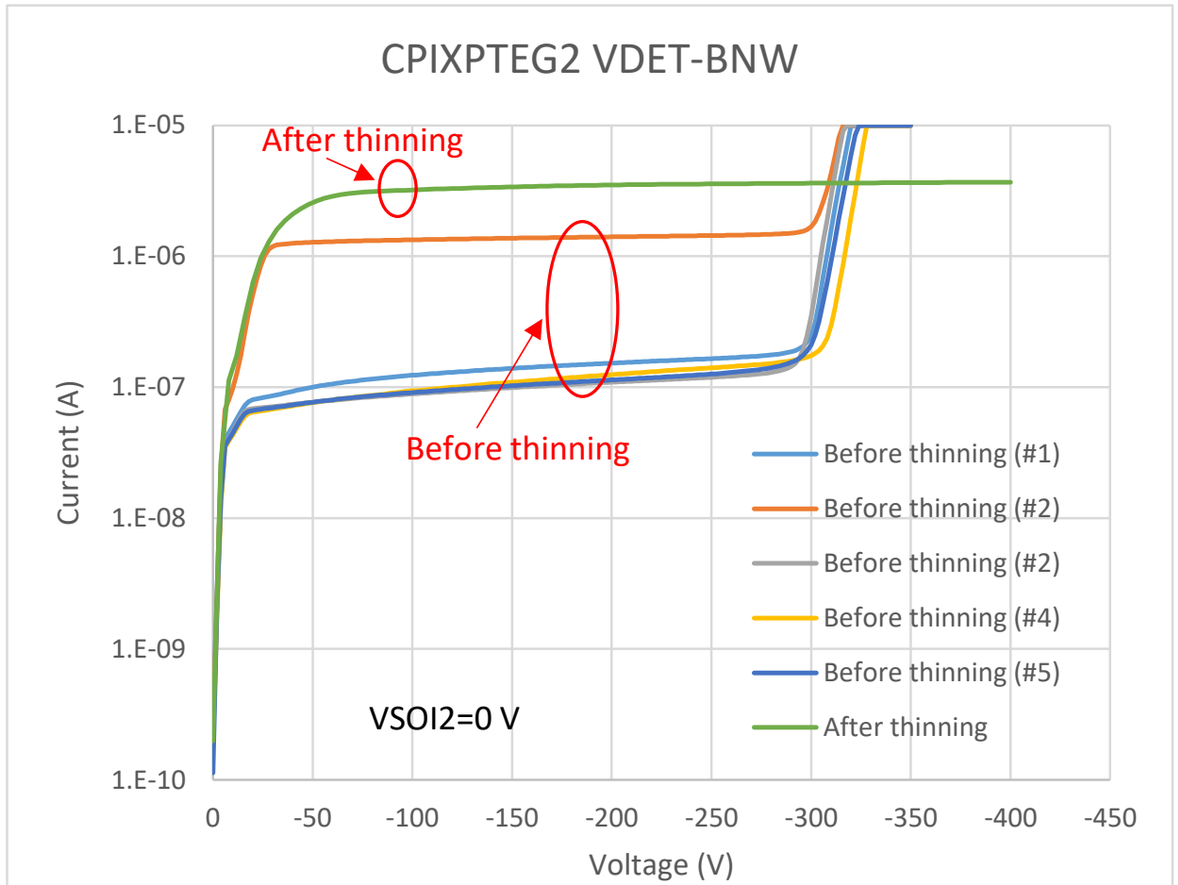
Wafer Thinning

DISCO
Kiru·Kezuru·Migaku Technologies

TAIKO Process by DISCO Corporation (Japan)







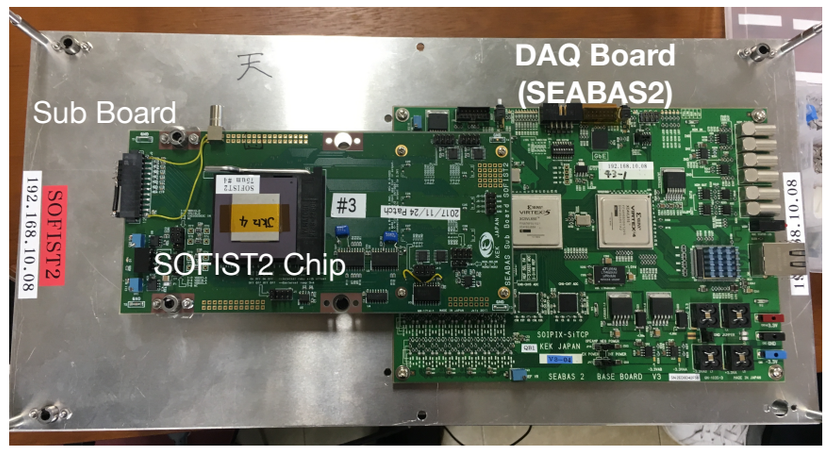
Sensor I-V after thinning (other SOIPIX)

Leak current increased by ~1.5 orders of magnitude.
No break down by 400 V after thinning.

Still investigating these behavior.

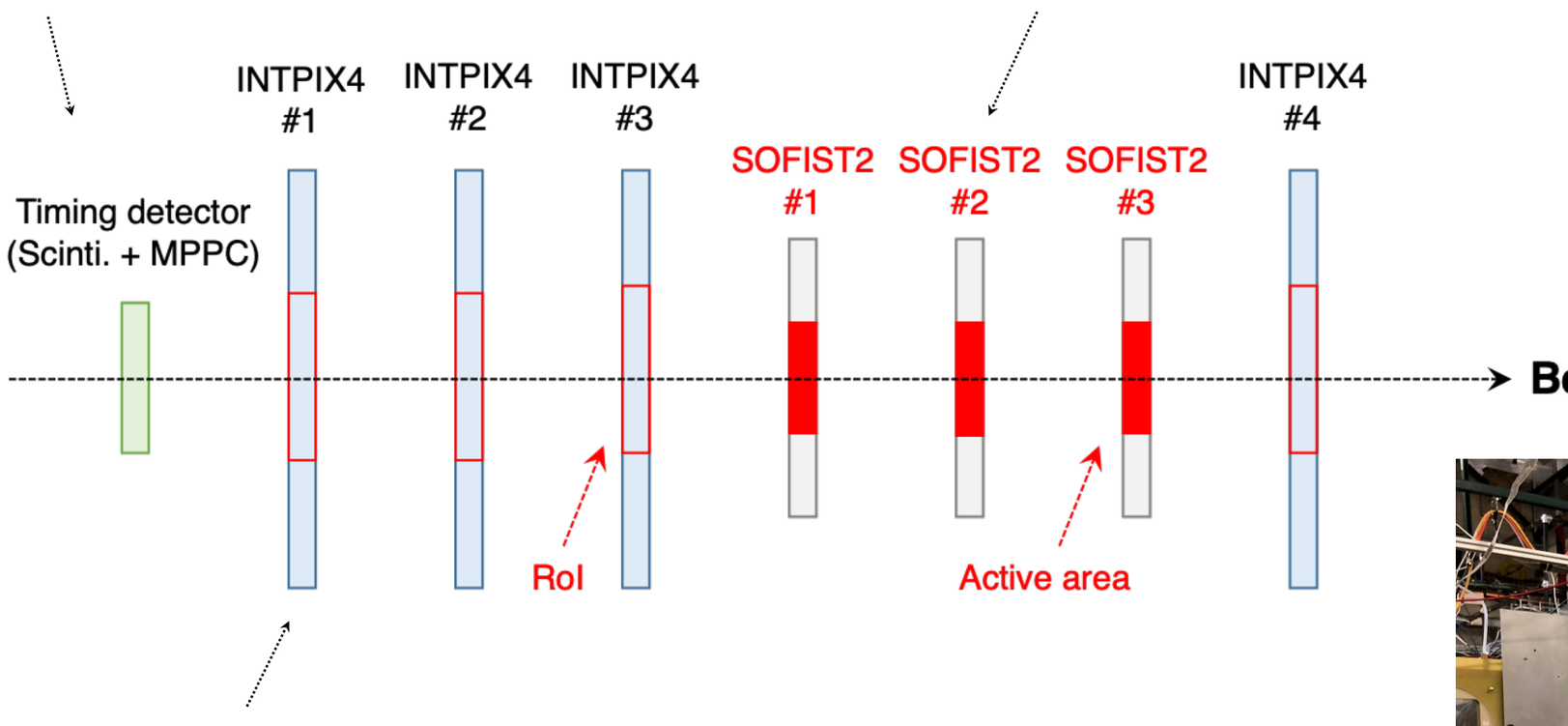
Beam Test

Beam: 120 GeV proton (Fermilab Beam Test Facility, Jan. 2018)
DAQ rate: ~120 events/s

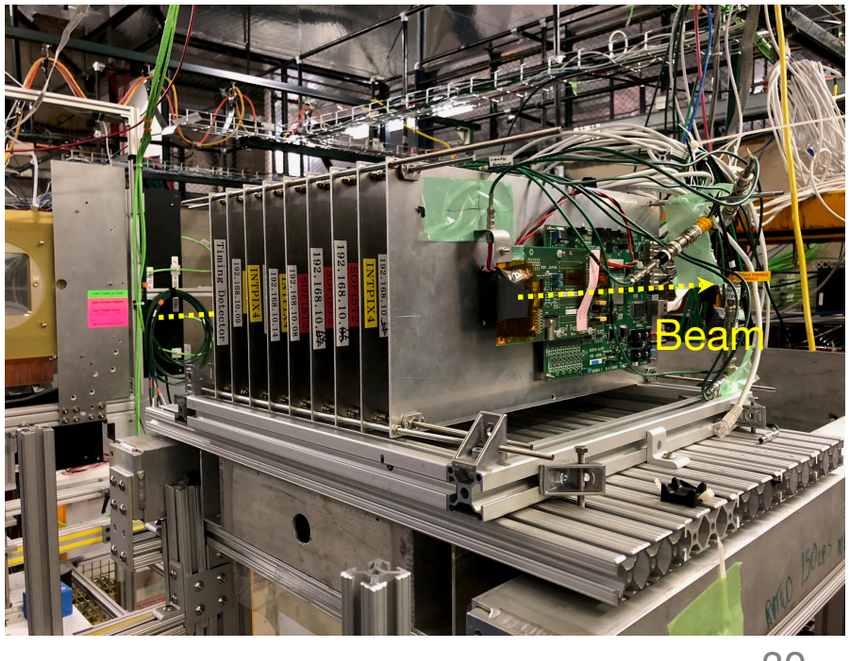


Event Trigger and Timing detector
Record hit timing for checking consistency to SOFIST.
Scinti. size: 3 × 3 mm²
MPPC size: 3 × 3 mm²
Readout: Comp. + AND + NIM converter
(Signal is sent to Master DAQ, SEABAS2)

SOFIST ver.2
Pixel size: 25 × 25 μm²
Pixel array: 80 × 64 (2.0 × 1.6 mm²)
Readout: External 12-bit ADC (SEABAS2)
Sensor thickness: 75 μm



INTPIX4 (SOIPIX)
Telescope for SOFIST
Pixel size: 17 × 17 μm²
Pixel array: 832 × 512 (14.1 × 8.7 mm²)
Function: Region of Interest readout
Readout: External 12-bit ADC (SEABAS2)



Beam Test Result

位置分解能

テレスコープで再構成したトラックと SOFIST 上のヒット位置の差

タイムスタンプの分解能

二枚の SOFIST2 間でのタイムスタンプの差

（互いのヒット位置が 2 ピクセル以内のもの）

Readout and Sensor depletion layer

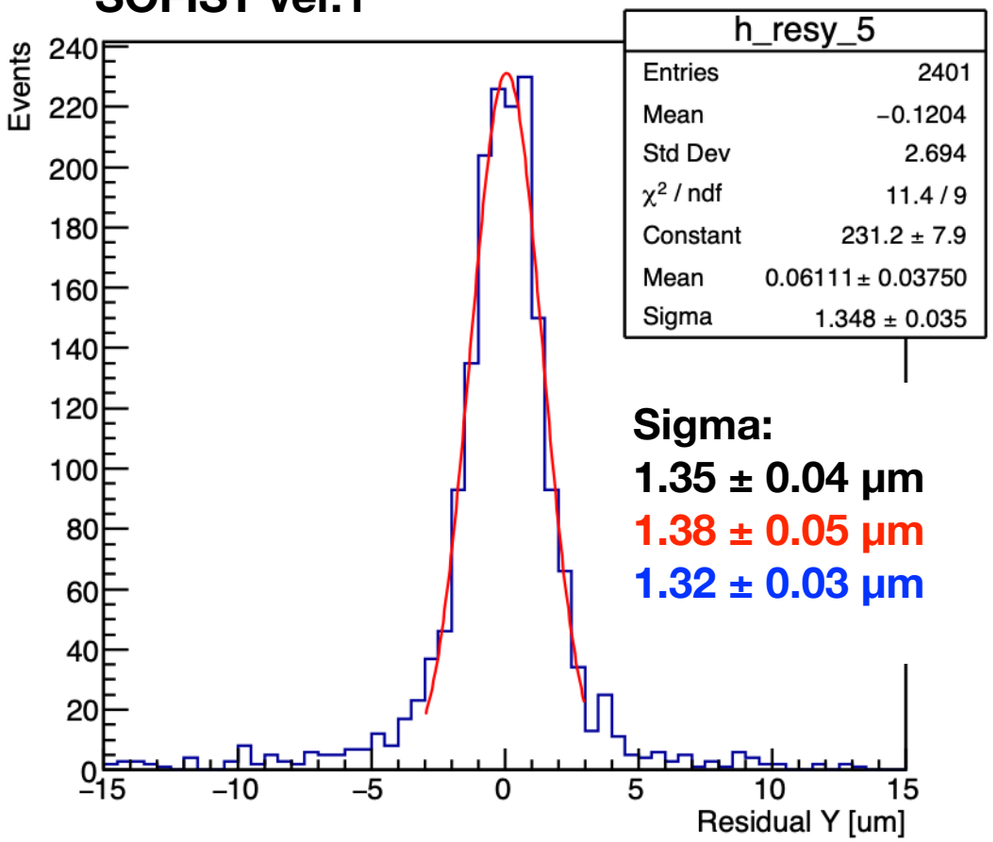
12-bit external ADC, 500 μm (Full depletion)

8-bit on-chip ADC, 500 μm (Full depletion)

12-bit external ADC, 200 μm (Partial depletion)

位置分解能

SOFIST ver.1



Sigma:

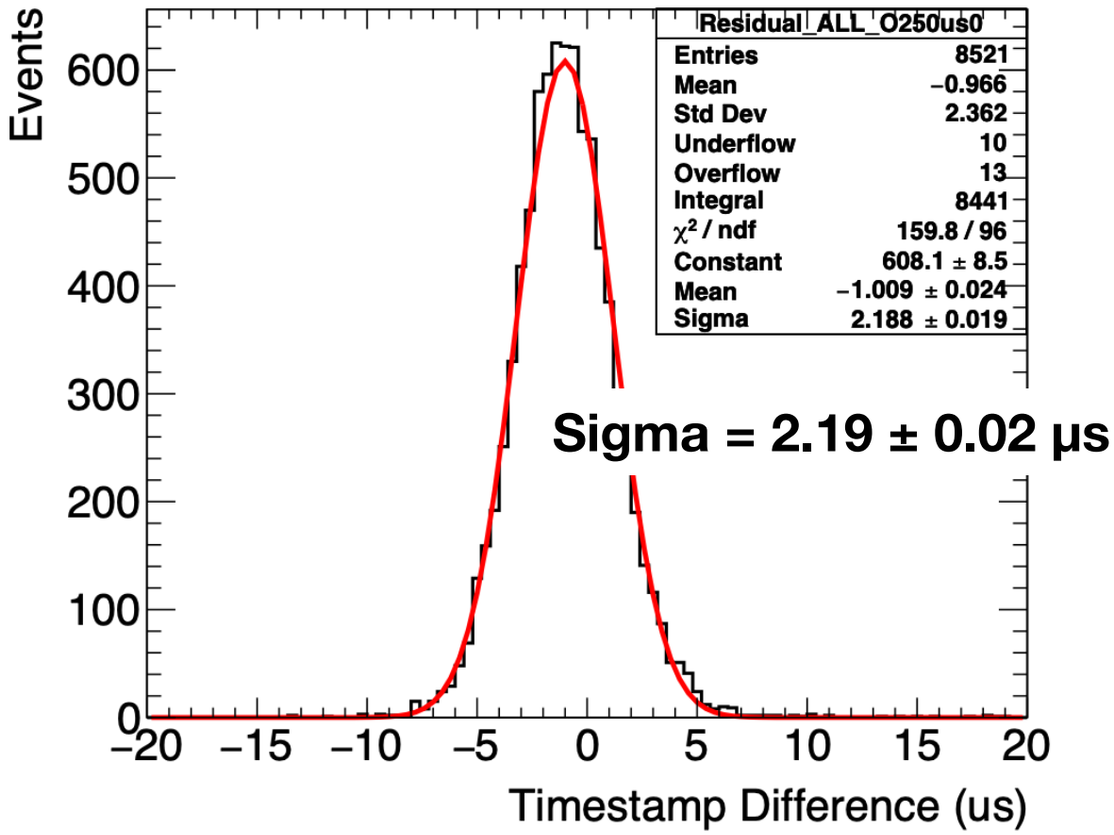
1.35 ± 0.04 μm

1.38 ± 0.05 μm

1.32 ± 0.03 μm

タイムスタンプの分解能

SOFIST ver.2 #1 and #2



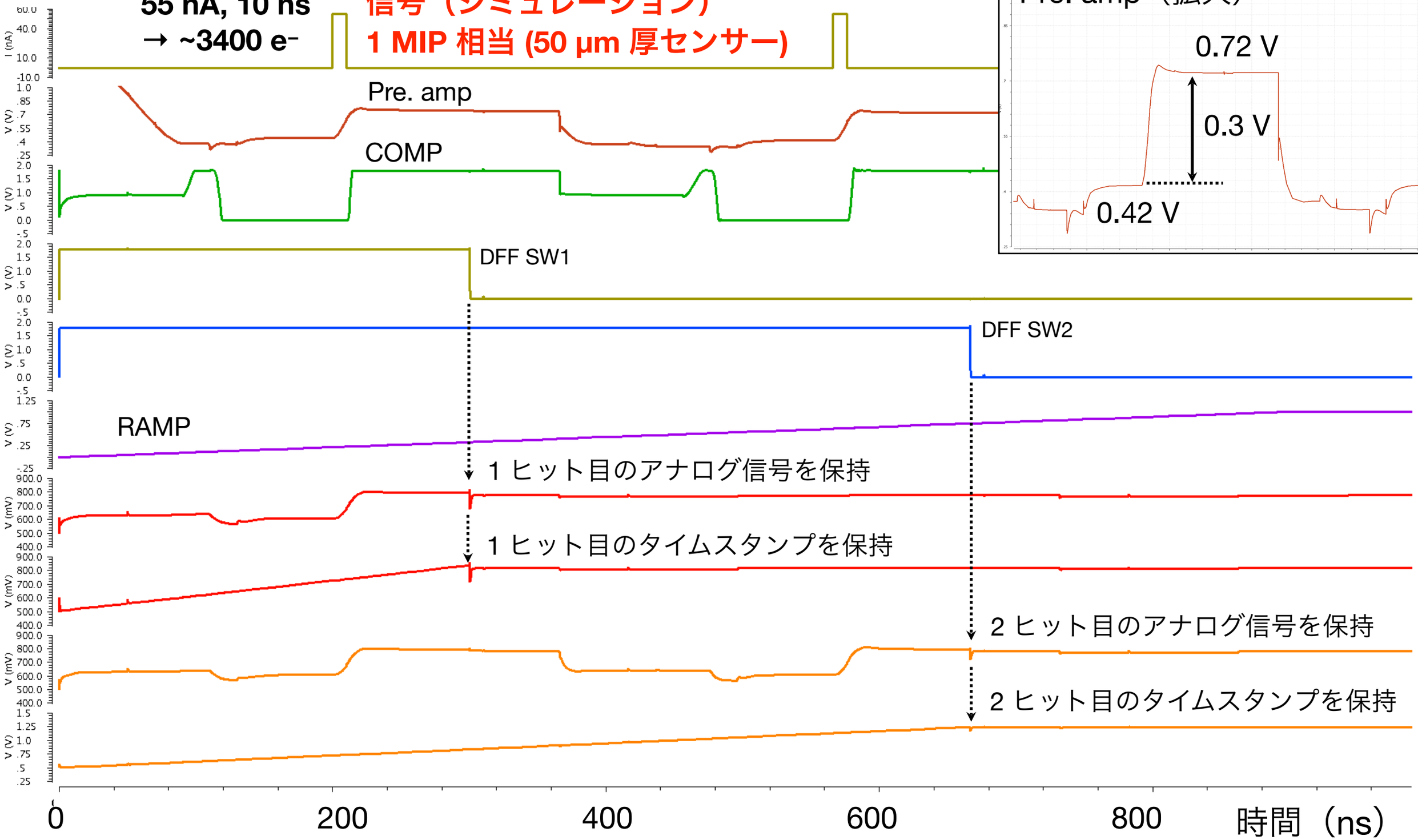
Sigma = 2.19 ± 0.02 μs

Intrinsic resolution: ~ 1.2 μm

(Position resolution of the telescope ~0.7 μm)

Intrinsic resolution: 2.19/√2 ~ 1.55 μs

Time Stamp and Analog Pixel



SOFIST ver.3

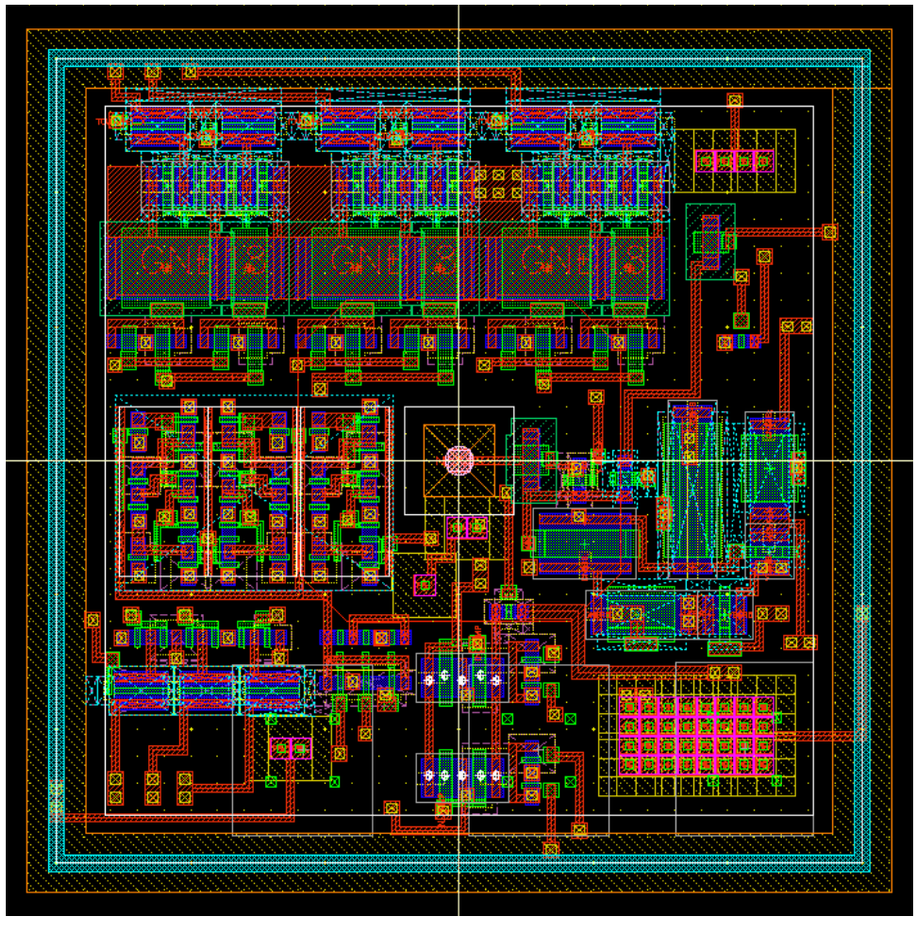
Pixel

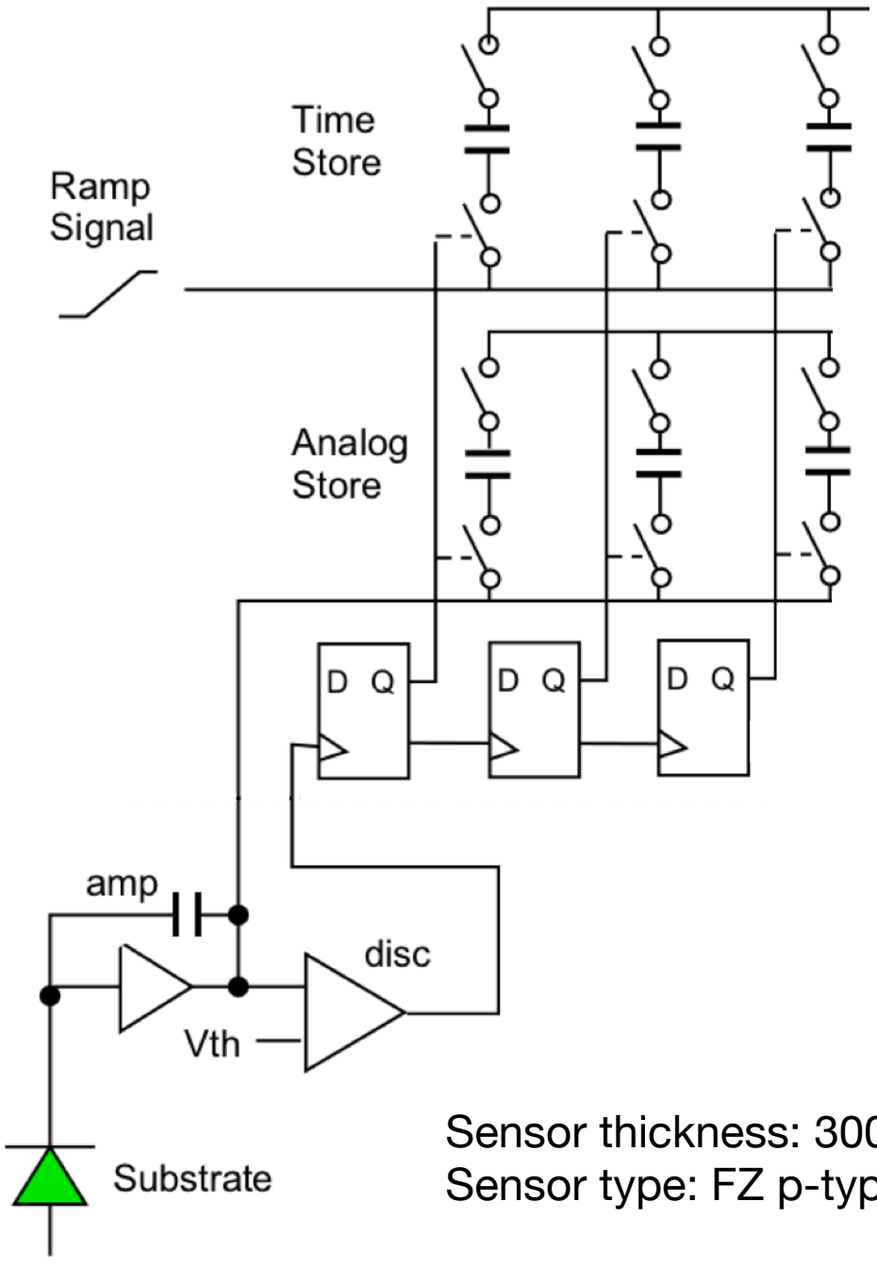
- Pre. amplifier (Charge sensitive amplifier)
- Comparator (Chopper inverter)
- Shift register
- Analog signal memories (three memories)
- Time stamp memories (three memories)

On chip

8 bit column ADC

Pixel size: 30 × 30 μm^2





Sensor thickness: 300 or 65 μm
Sensor type: FZ p-type, DSOI

ピクセル内に必要な全ての機能を実装した.
ただしピクセルサイズは 30 μm 角なので信号処理回路の評価が主な目的.

DAQ

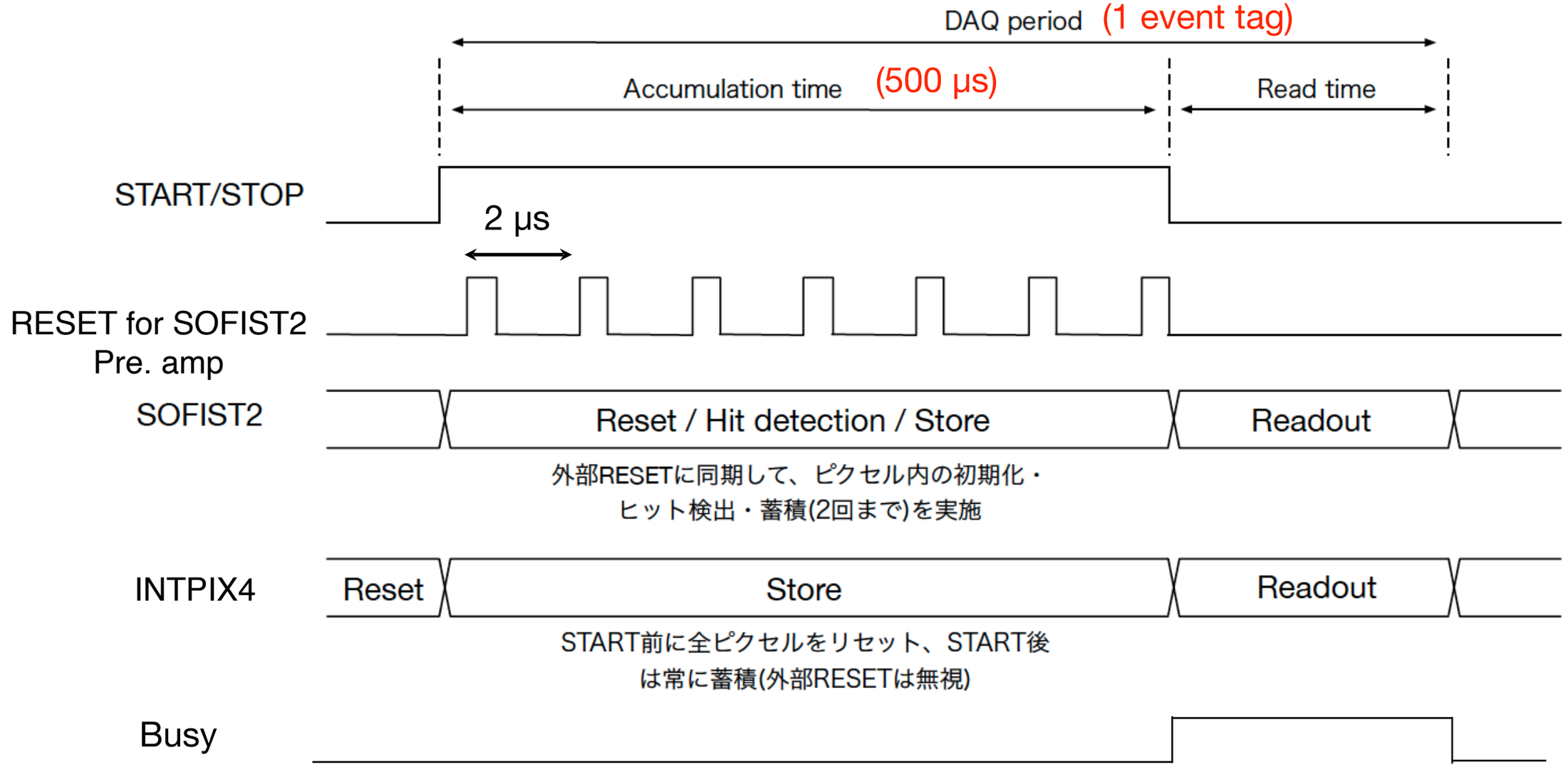
1 event tag あたりの各検出器の動作

Event tag trigger からシグナルを受け取ったら DAQ period（1 event tag）を開始する.

SOFIST2 は周期的にプリアンプのリセットを行い 500 μs のあいだのヒットのタイムスタンプをピクセル内に記録する.

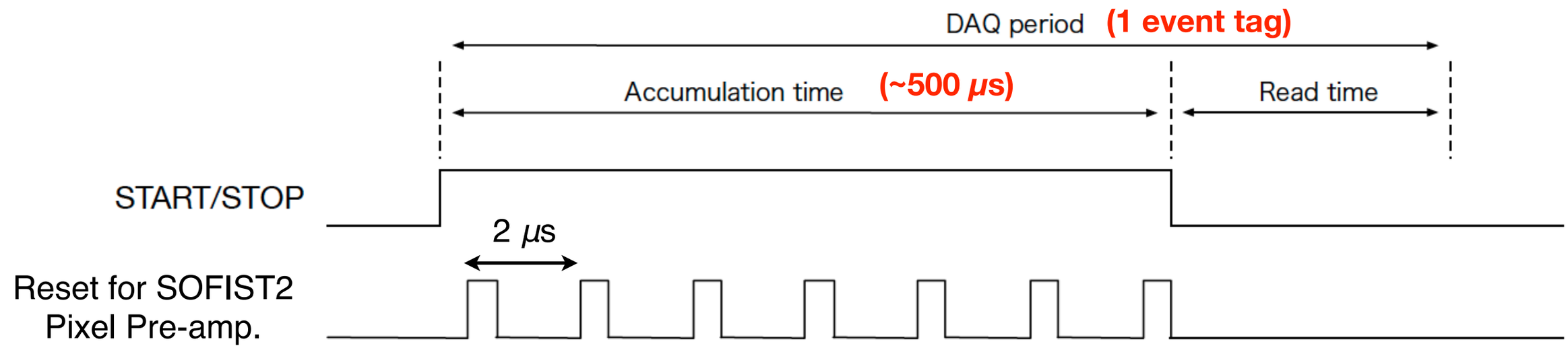
INTPIX4 は 500 μs のあいだ積分し続ける. 時間情報は event tag のみ.

リードアウト中は SOFIST2/INPIX4 から DAQ master へ busy を送る（event tag trigger を受け付けない）.



STORE Mode

Operation of each detector in 1 event tag (DAQ period)



SOFIST2		Reset / Hit detection / Store	Readout
INTPIX4	Reset	Store	Readout
Timing detector		Time record	Readout

Record hit timestamp in a event tag.

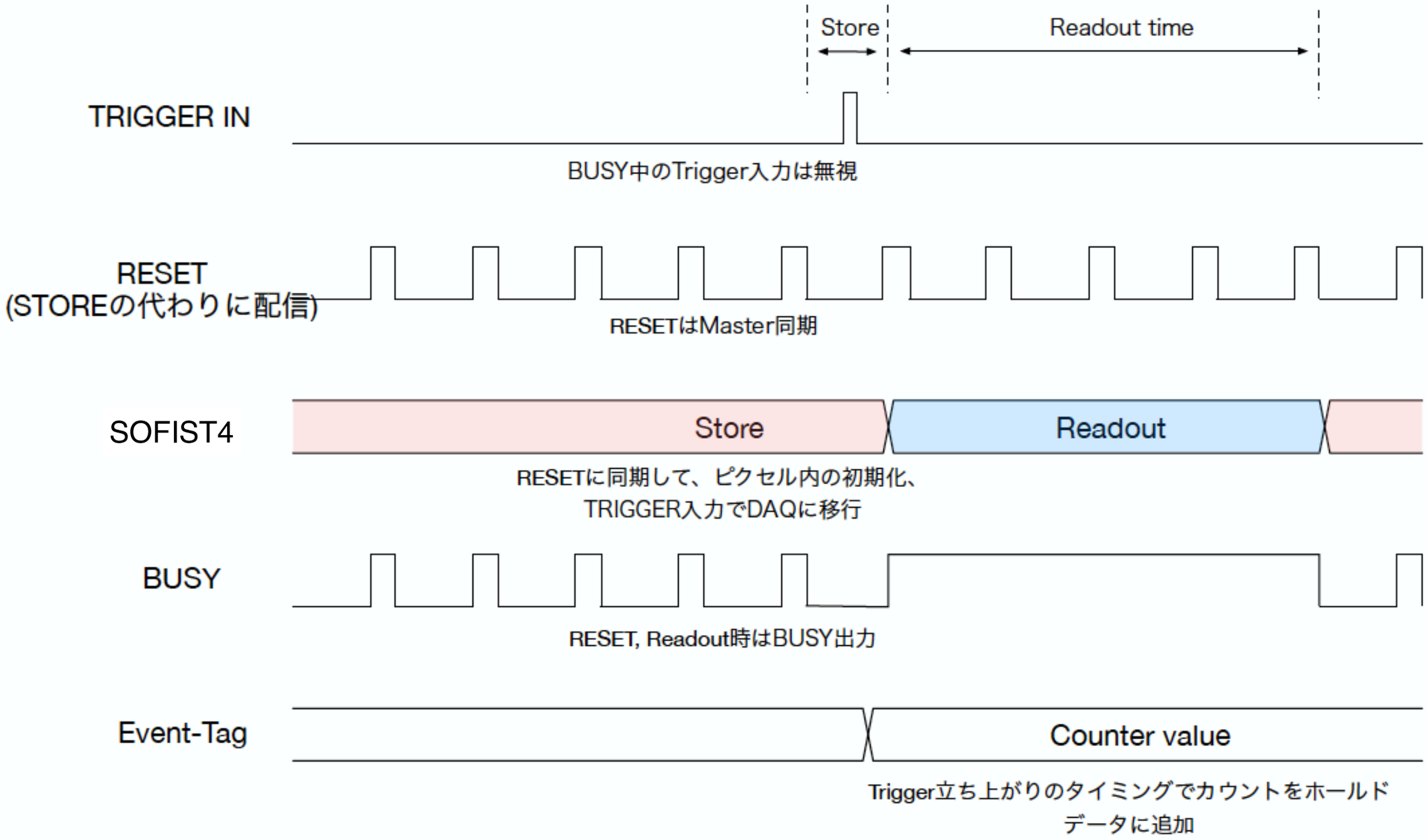
Reset pre-amp. every 2 μs / Hit detection / Store (analog signal/timestamp).

Time information is only event tag.

Reset pixel amp. before START
Integrate signal for 500 μs.

Record elapsed time after START
for every hit detection for 500 μs.

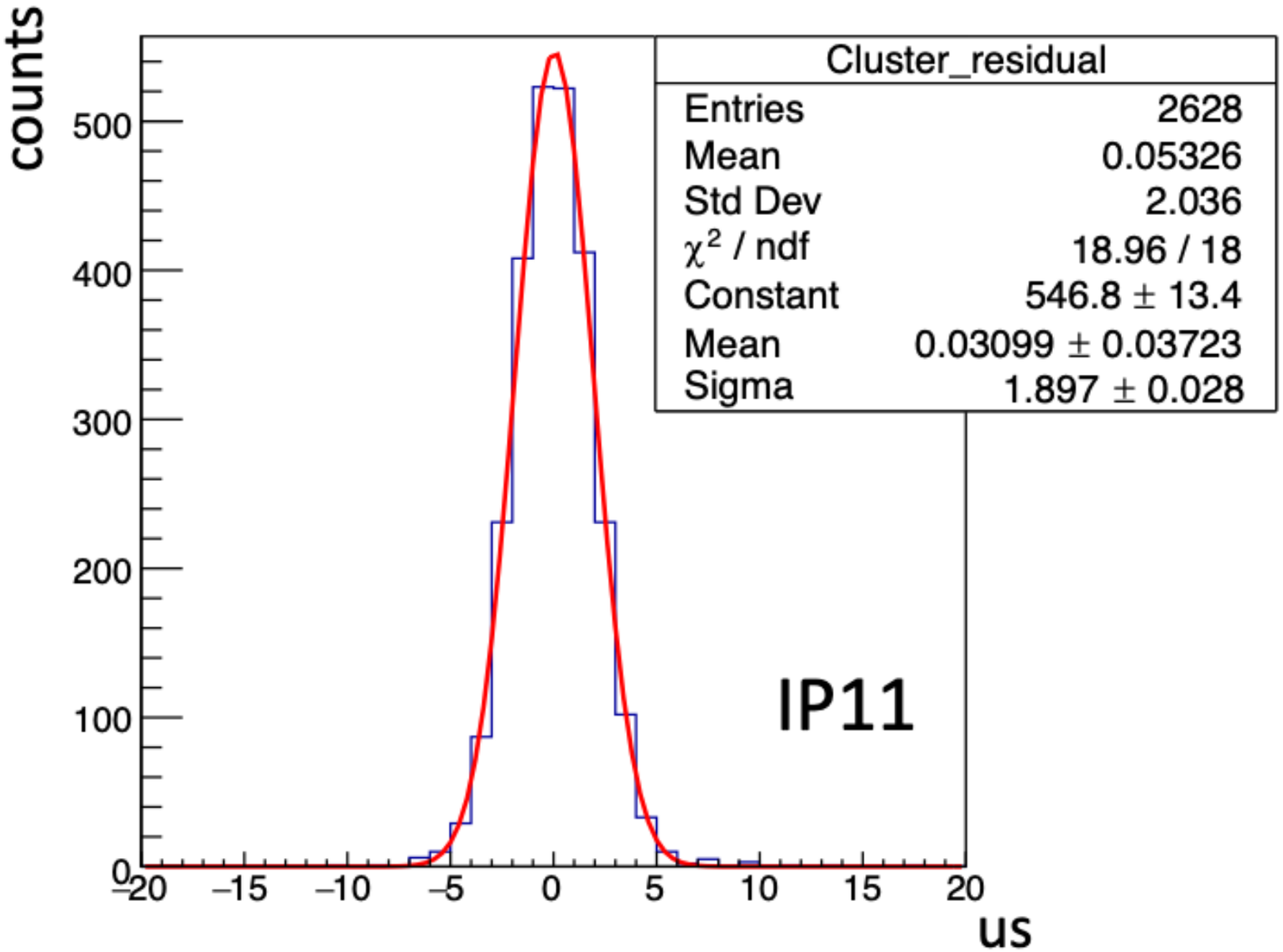
Trigger Mode



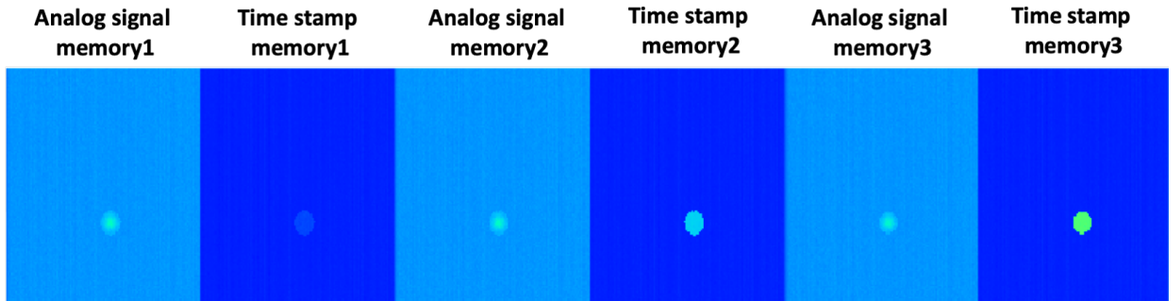
SOFIST3

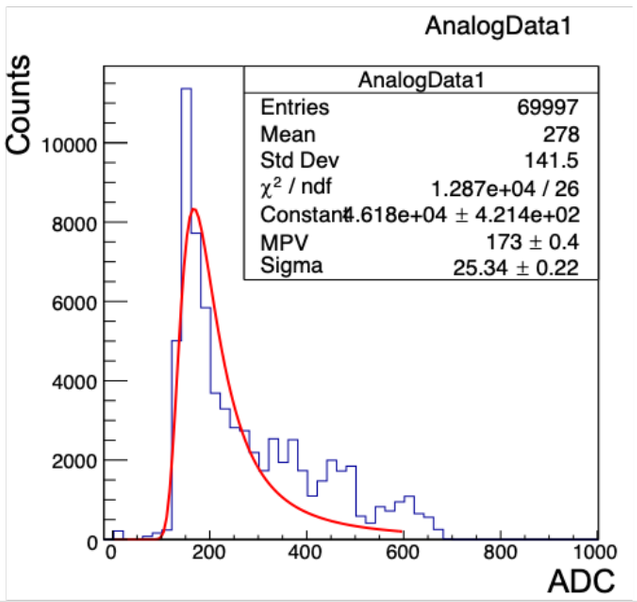
Time difference of cluster size 2 event

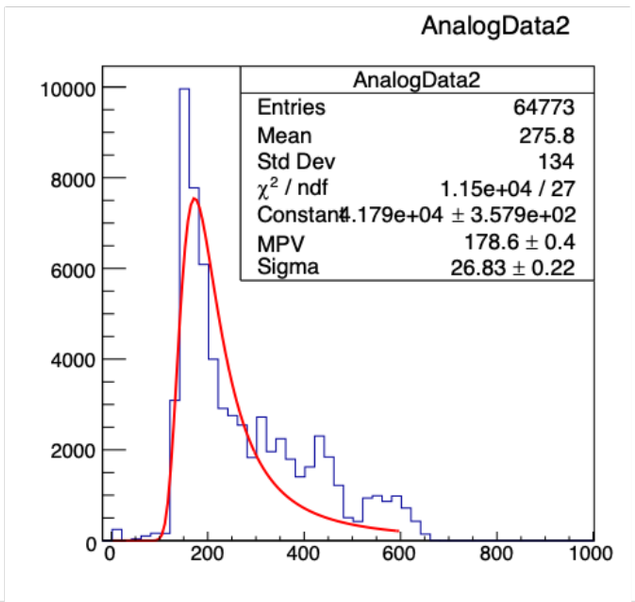
In principle, timestamp of two pixels (cluster size 2) are the same.

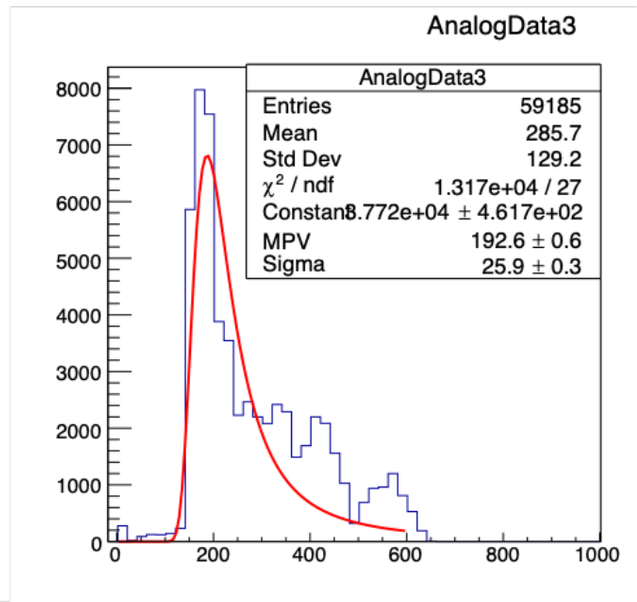


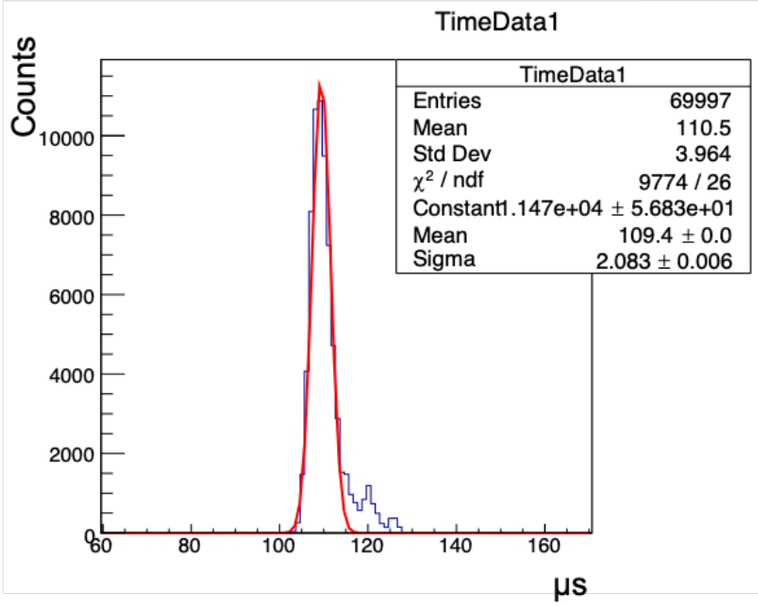
SOFIST3

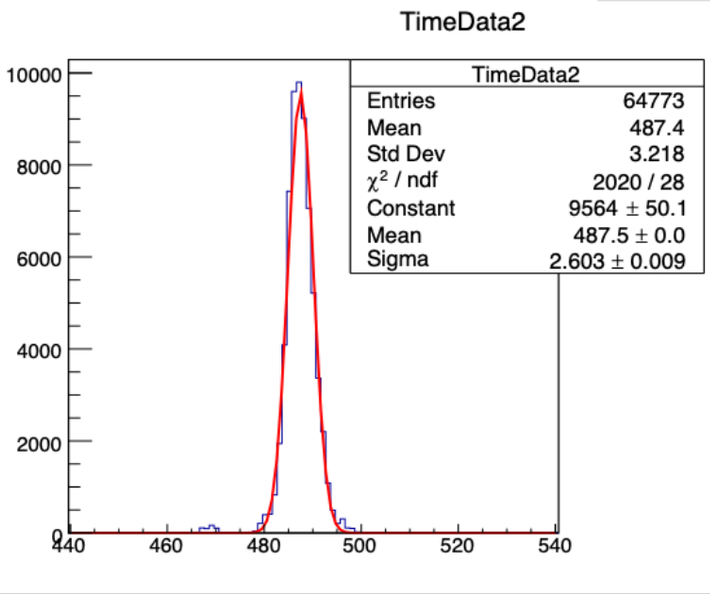

Analog signal memory1
Time stamp memory1
Analog signal memory2
Time stamp memory2
Analog signal memory3
Time stamp memory3

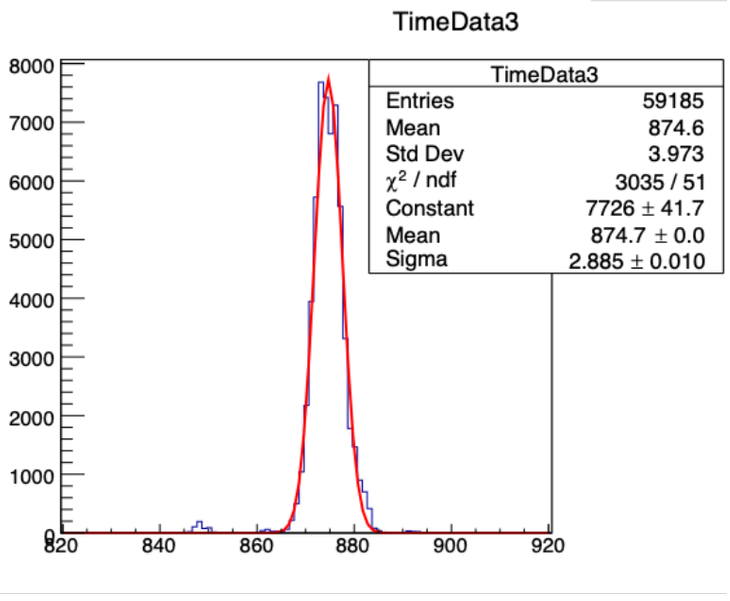

AnalogData1
Counts
AnalogData1
Entries 69997
Mean 278
Std Dev 141.5
χ² / ndf 1.287e+04 / 26
Constant 4.618e+04 ± 4.214e+02
MPV 173 ± 0.4
Sigma 25.34 ± 0.22
ADC


AnalogData2
AnalogData2
Entries 64773
Mean 275.8
Std Dev 134
χ² / ndf 1.15e+04 / 27
Constant 4.179e+04 ± 3.579e+02
MPV 178.6 ± 0.4
Sigma 26.83 ± 0.22

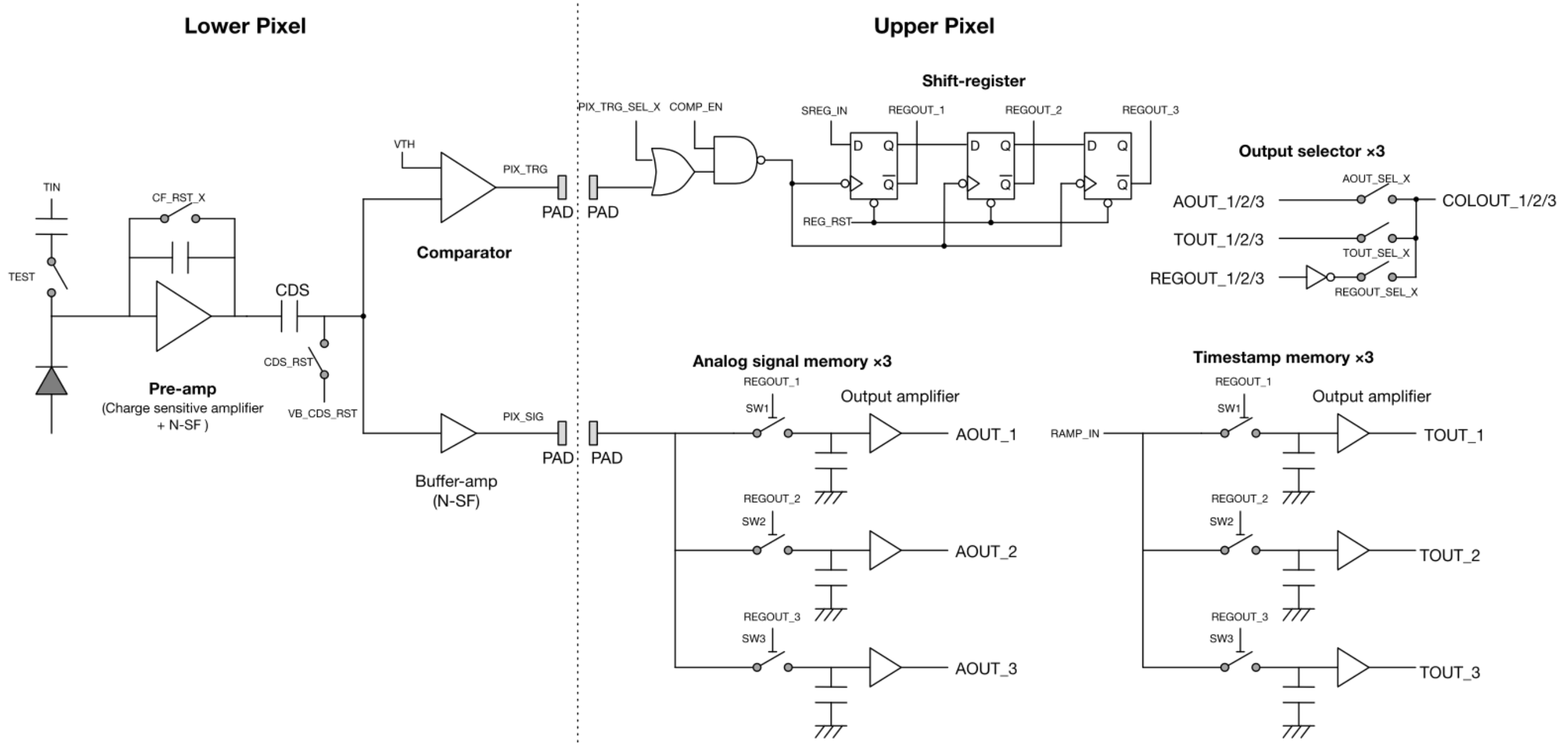

AnalogData3
AnalogData3
Entries 59185
Mean 285.7
Std Dev 129.2
χ² / ndf 1.317e+04 / 27
Constant 8.772e+04 ± 4.617e+02
MPV 192.6 ± 0.6
Sigma 25.9 ± 0.3


TimeData1
Counts
TimeData1
Entries 69997
Mean 110.5
Std Dev 3.964
χ² / ndf 9774 / 26
Constant 1.147e+04 ± 5.683e+01
Mean 109.4 ± 0.0
Sigma 2.083 ± 0.006
μs


TimeData2
TimeData2
Entries 64773
Mean 487.4
Std Dev 3.218
χ² / ndf 2020 / 28
Constant 9564 ± 50.1
Mean 487.5 ± 0.0
Sigma 2.603 ± 0.009

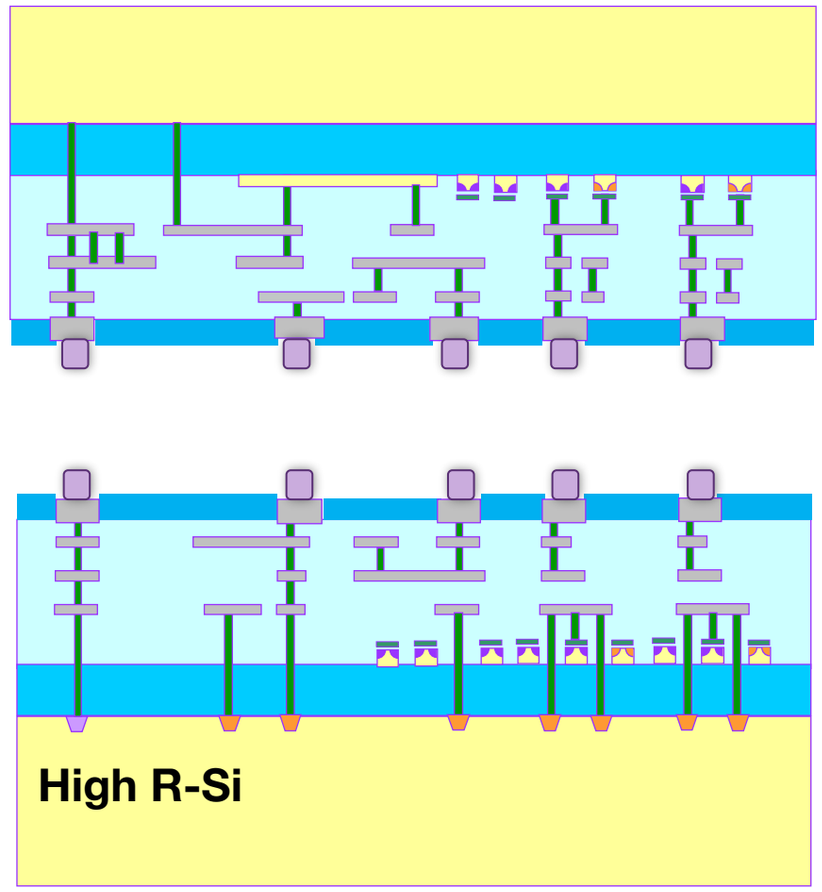

TimeData3
TimeData3
Entries 59185
Mean 874.6
Std Dev 3.973
χ² / ndf 3035 / 51
Constant 7726 ± 41.7
Mean 874.7 ± 0.0
Sigma 2.885 ± 0.010

SOFIST4 Pixel

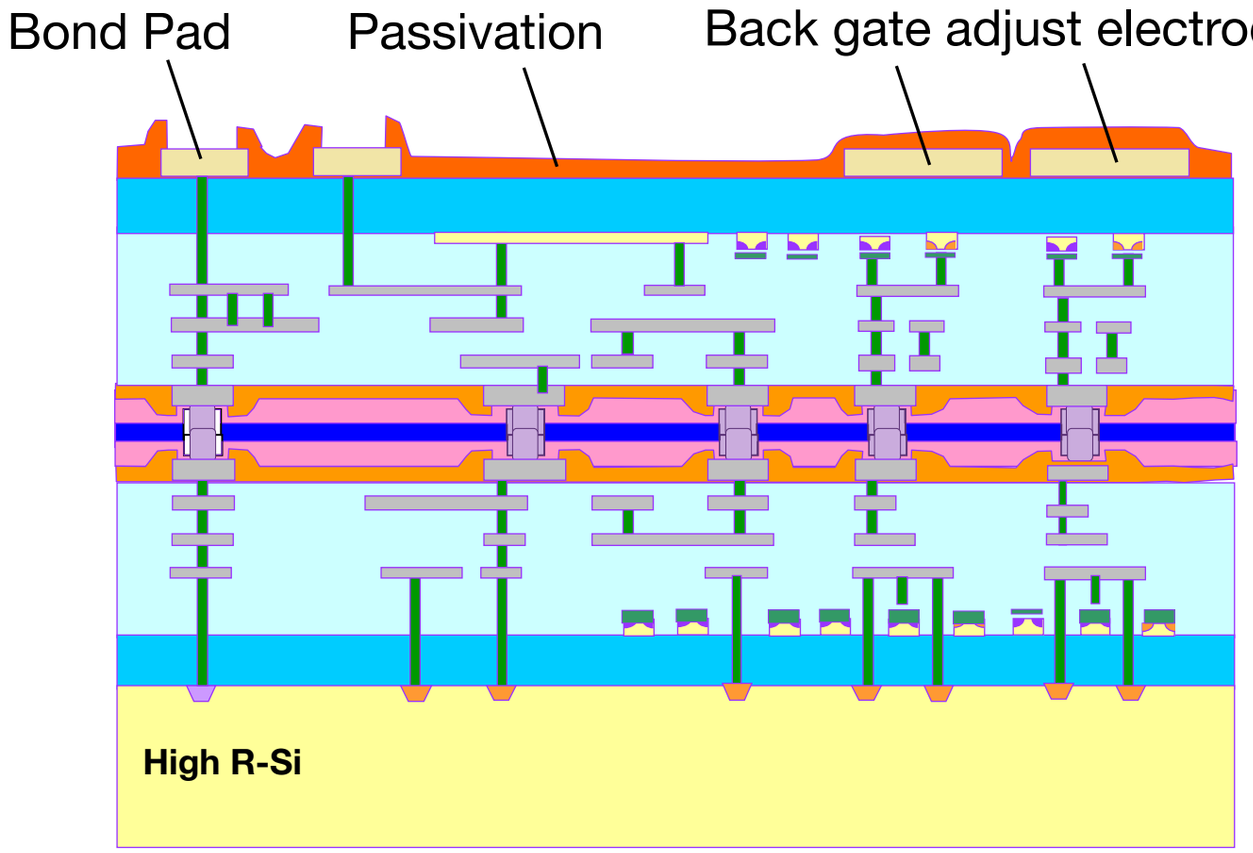


SOI Based 3D Integration

Upper Chip

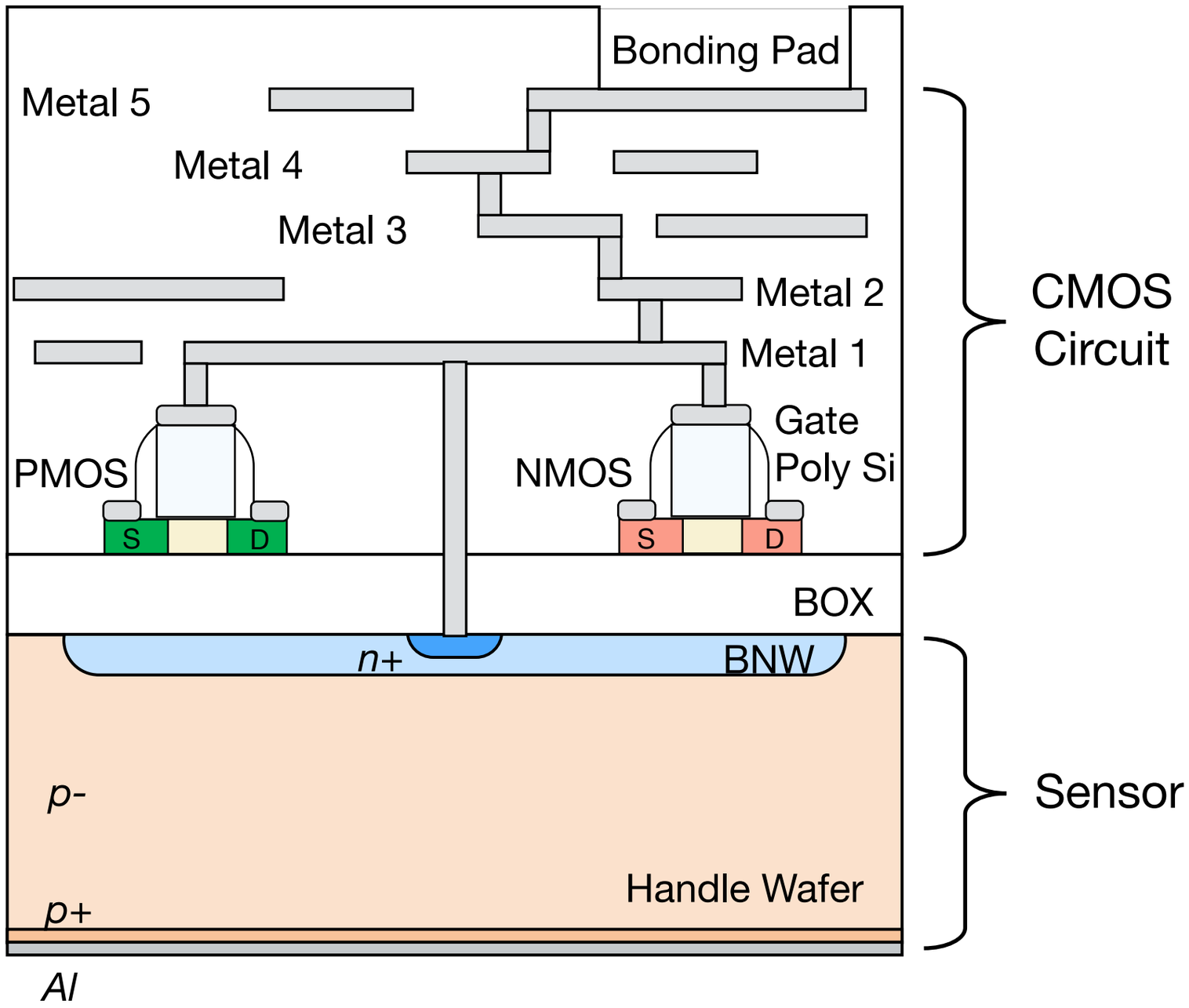


Lower Chip



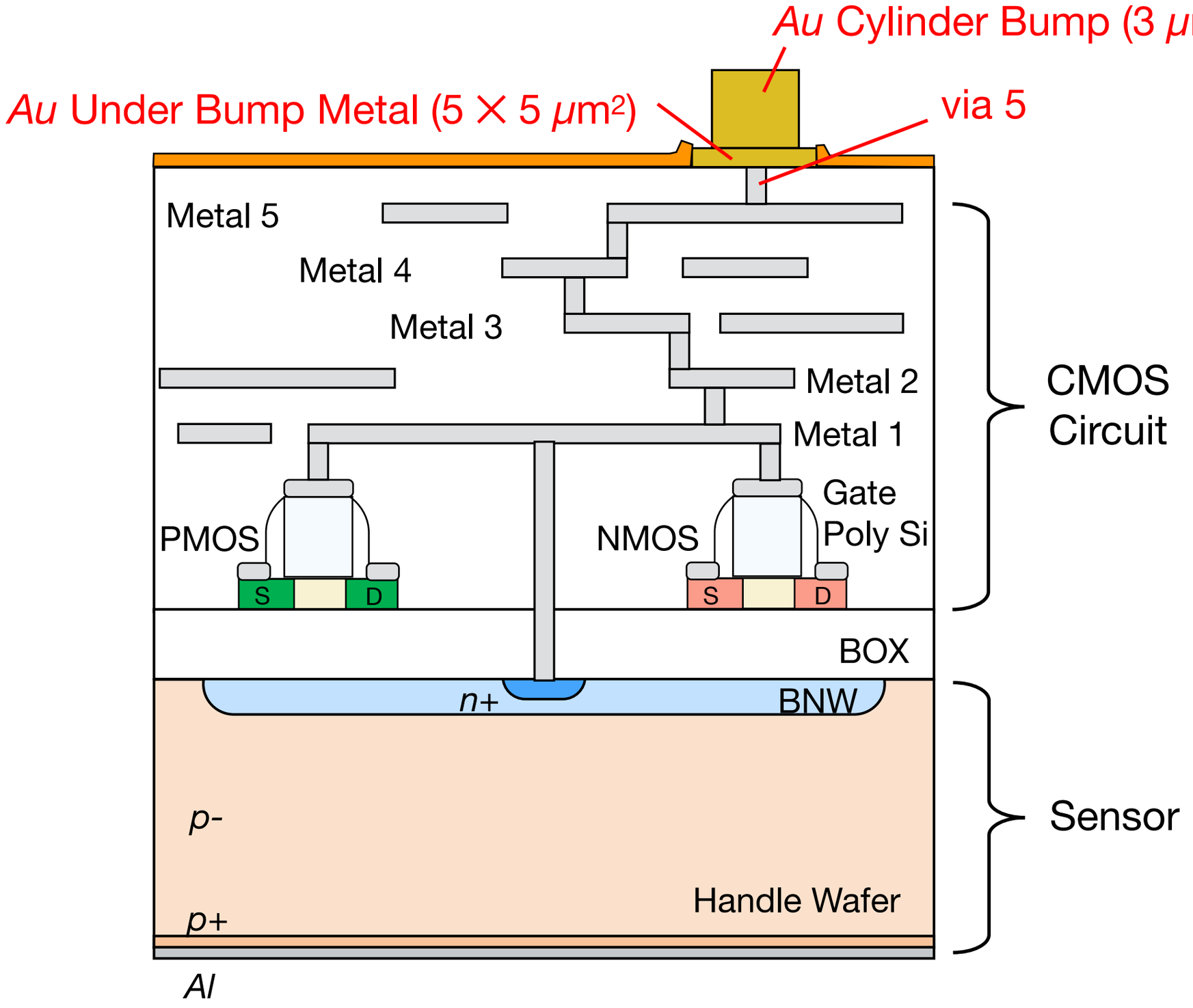
SOI Based 3D Integration

Normal SOIPIX

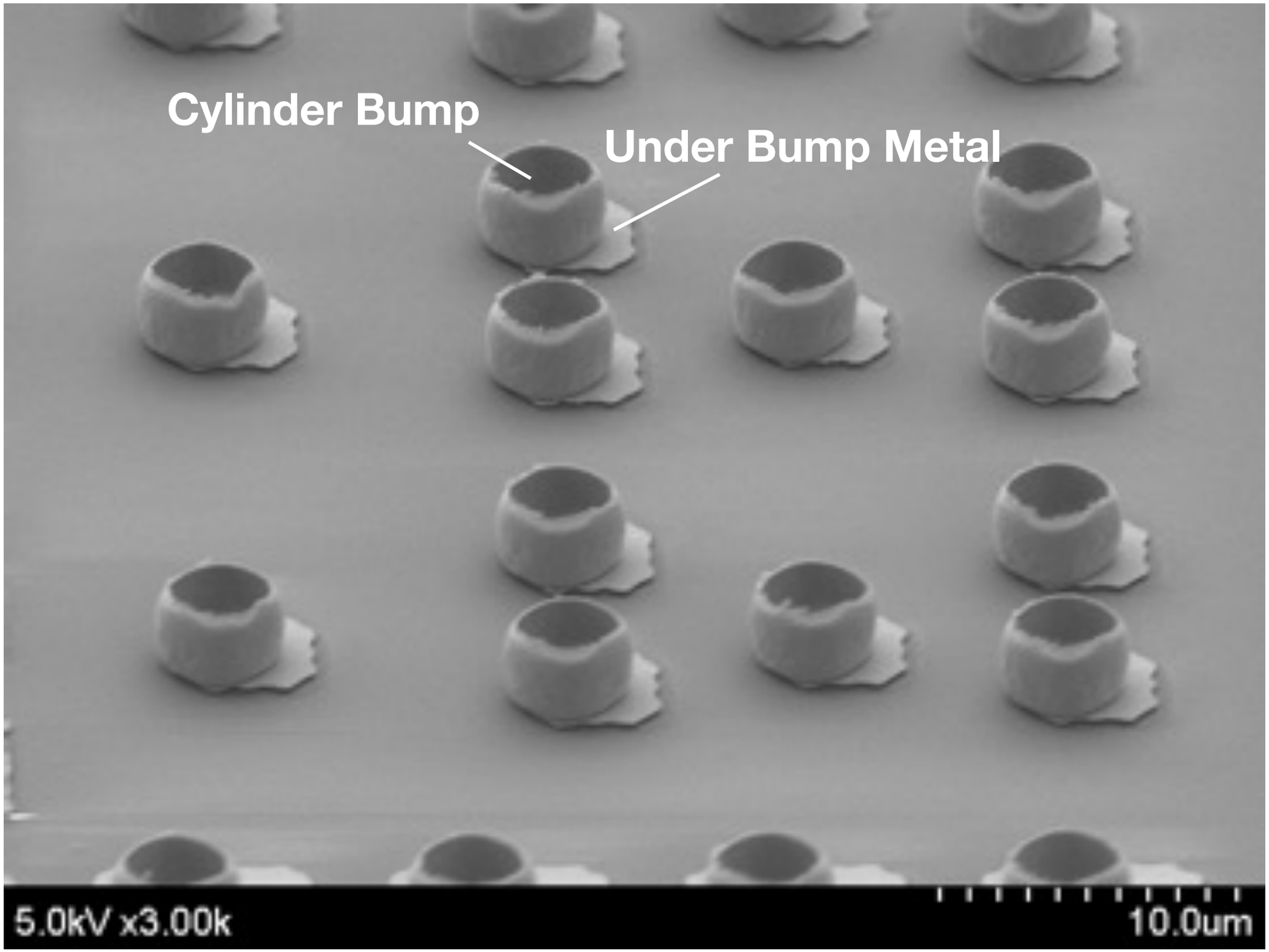


SOI Based 3D Integration

SOIPIX for 3D
Lower Chip

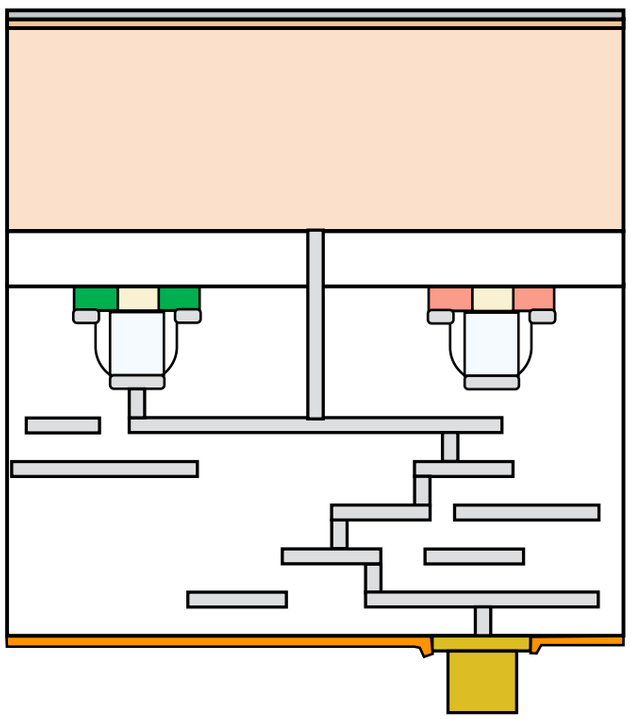


Au Micro Cylinder Bump

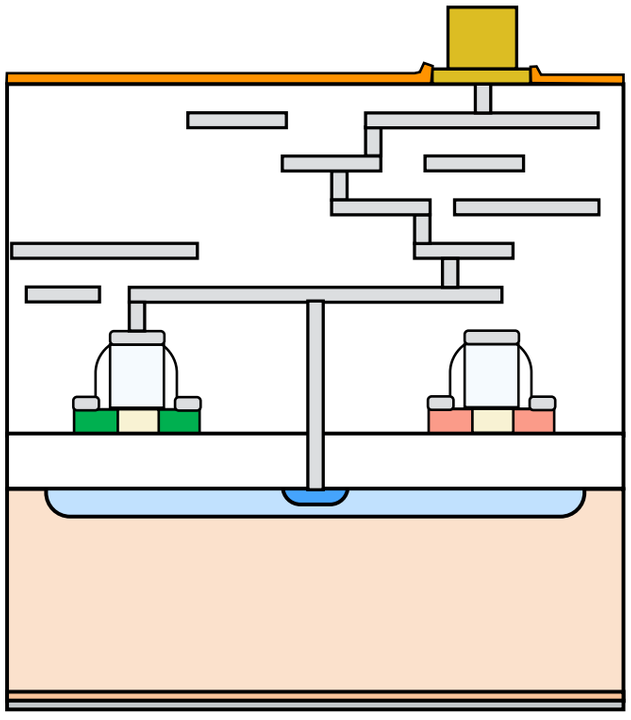


SOI Based 3D Integration

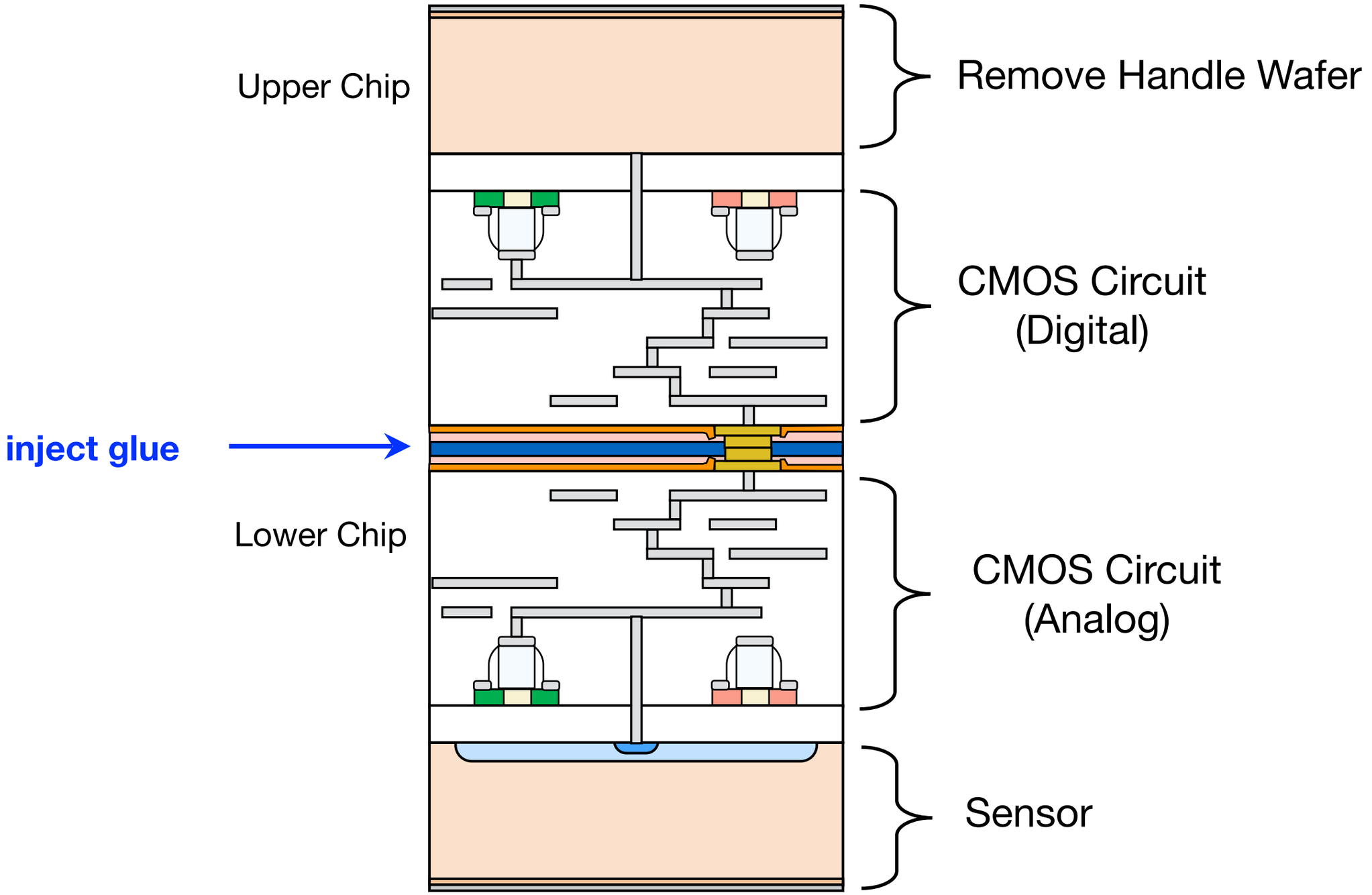
Upper Chip



Lower Chip

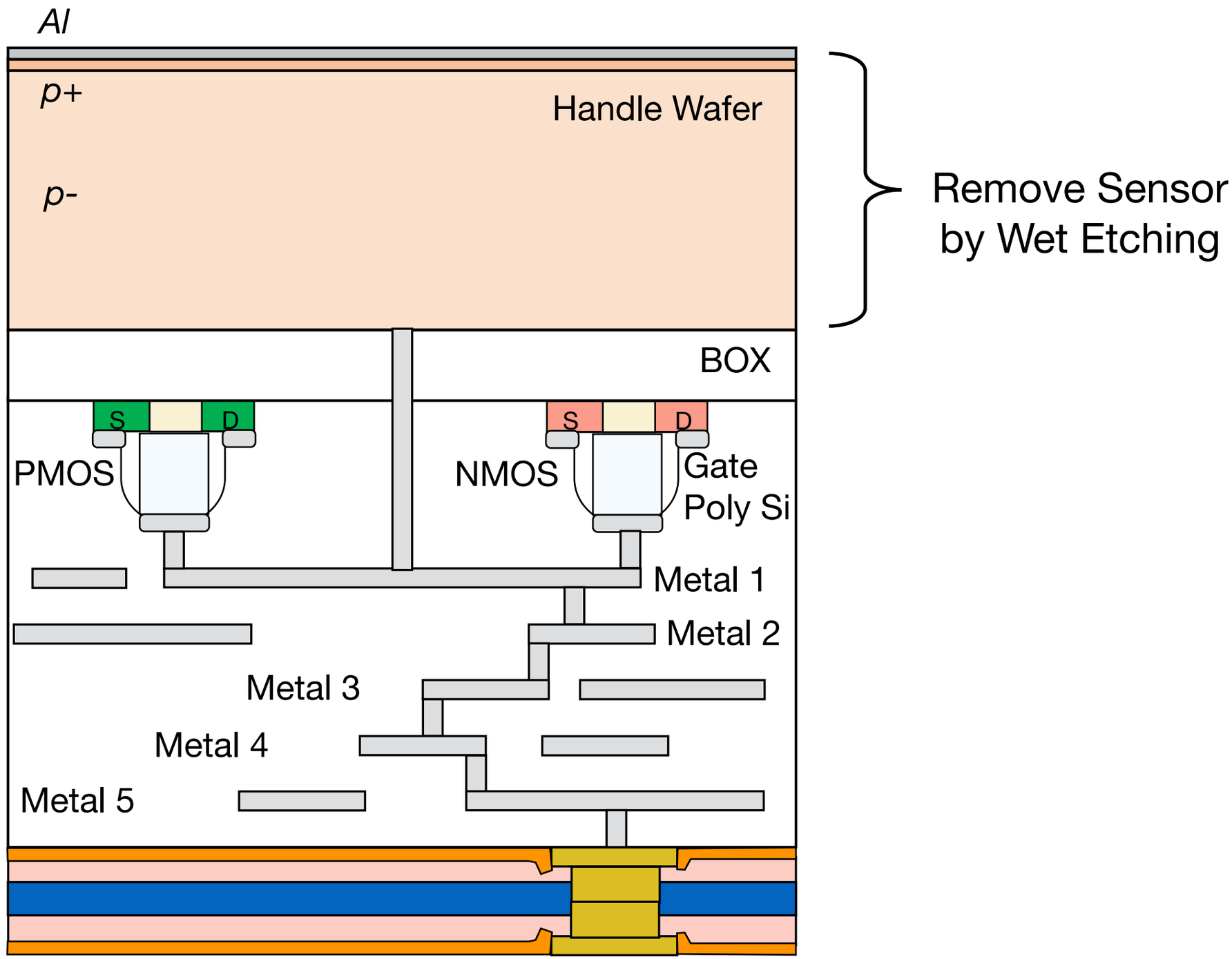


SOI Based 3D Integration



SOI Based 3D Integration

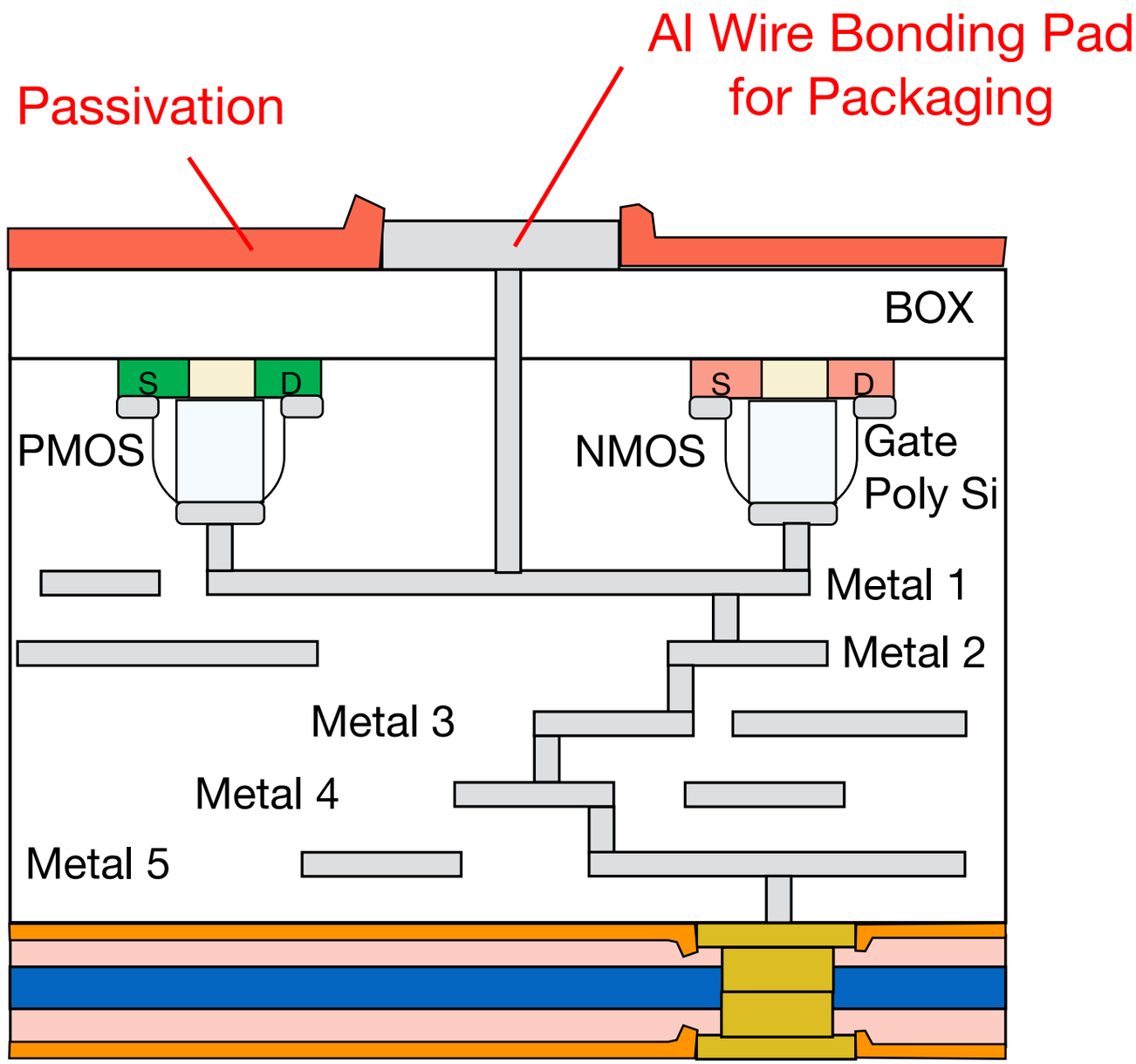
Upper Chip



Lower Chip

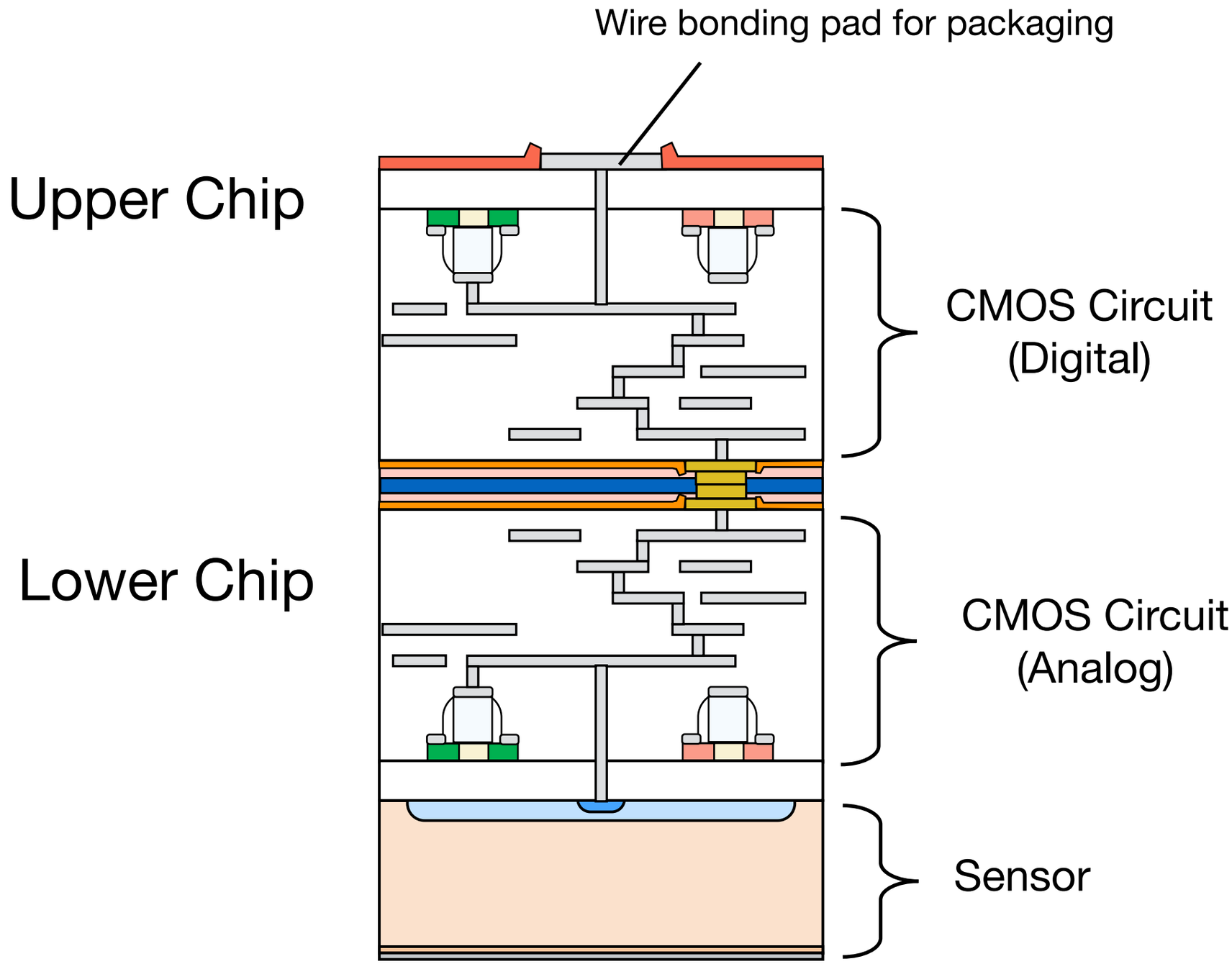
SOI Based 3D Integration

Upper Chip

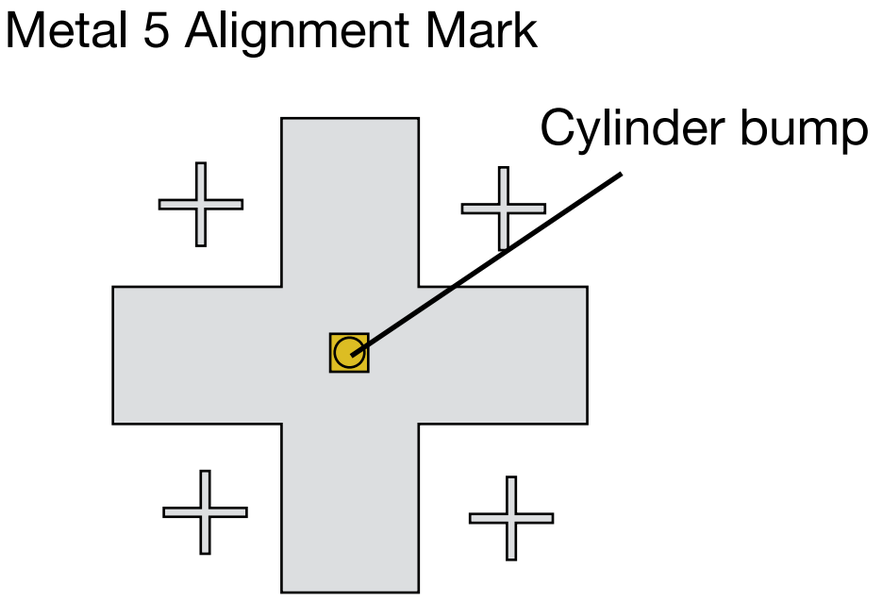


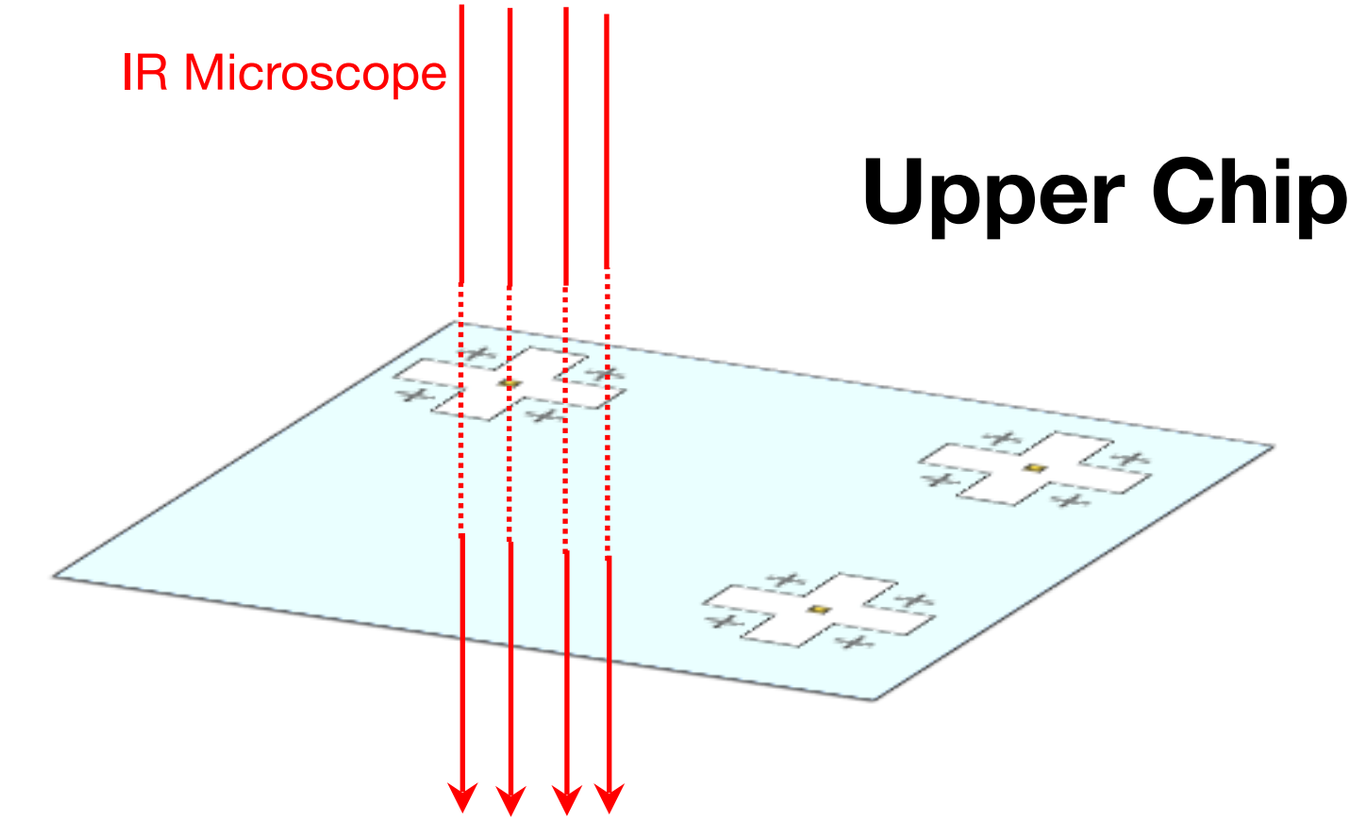
Lower Chip

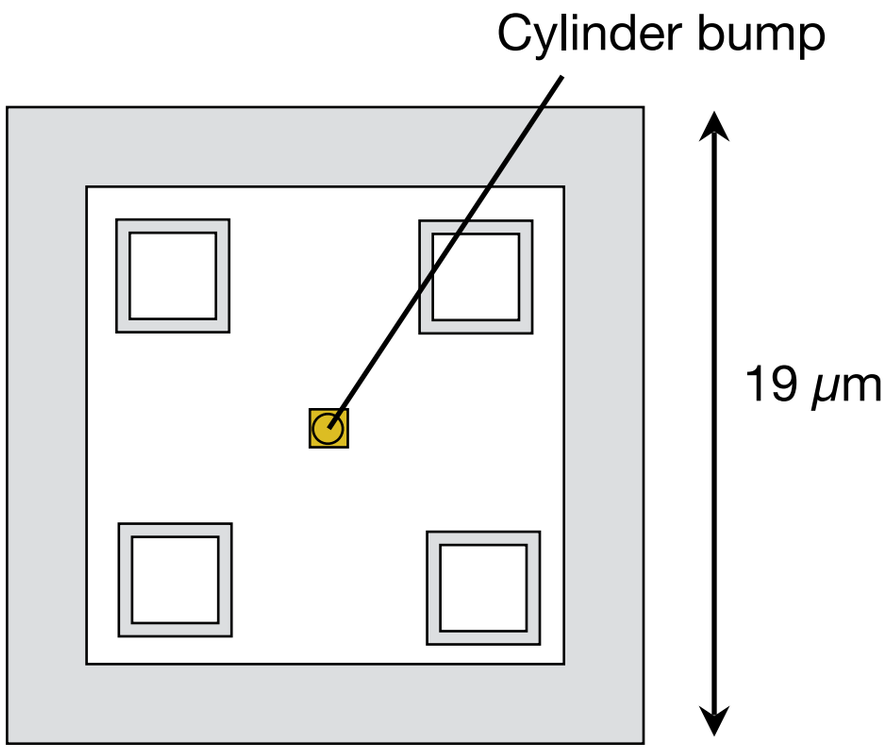
SOI Based 3D Integration

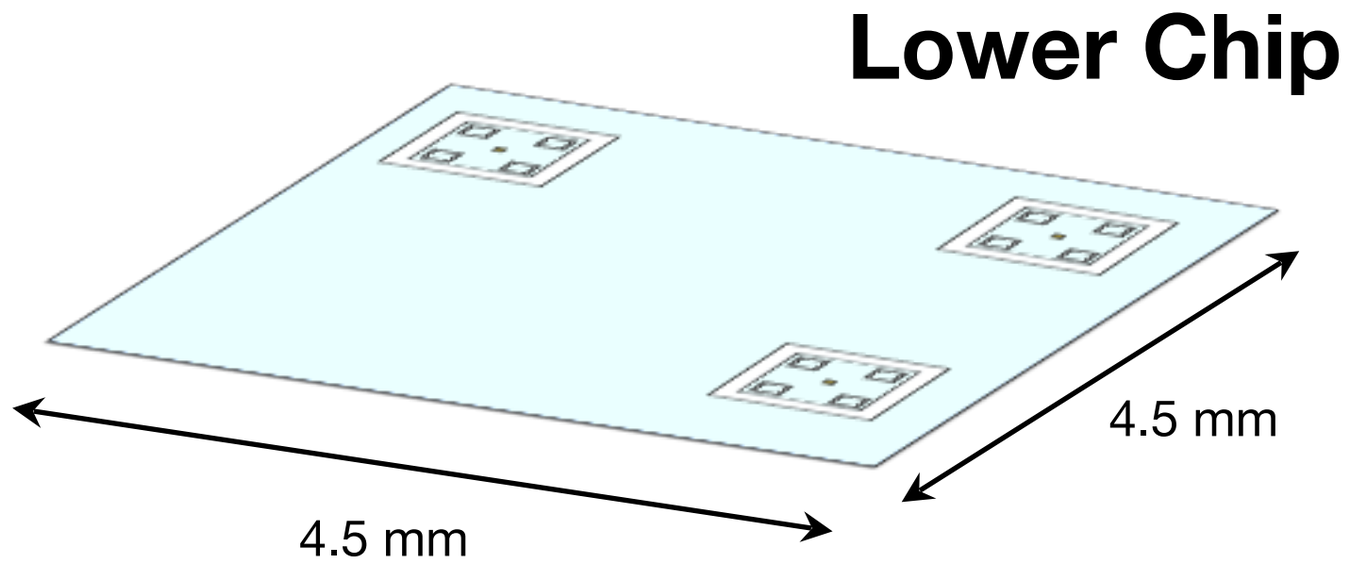


SOI Based 3D Integration



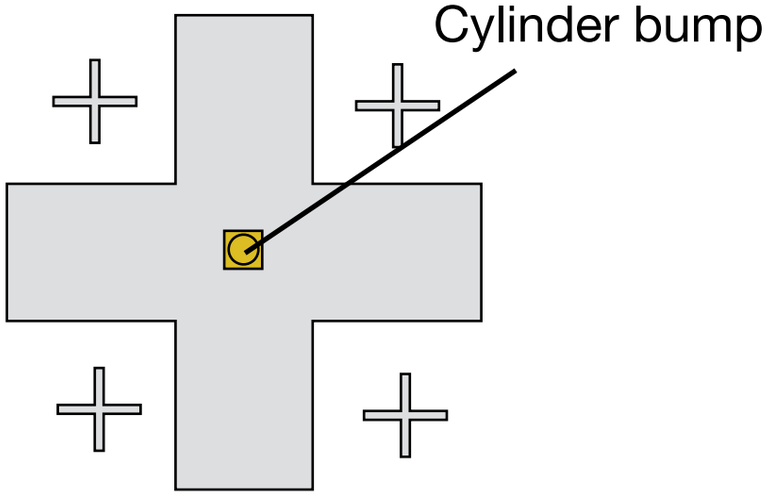


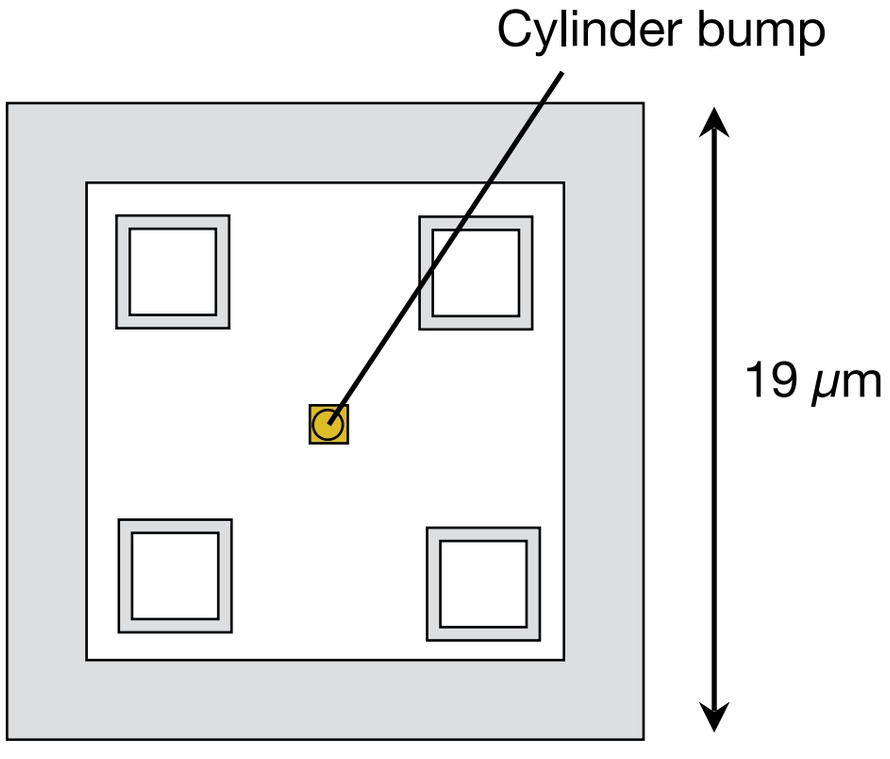




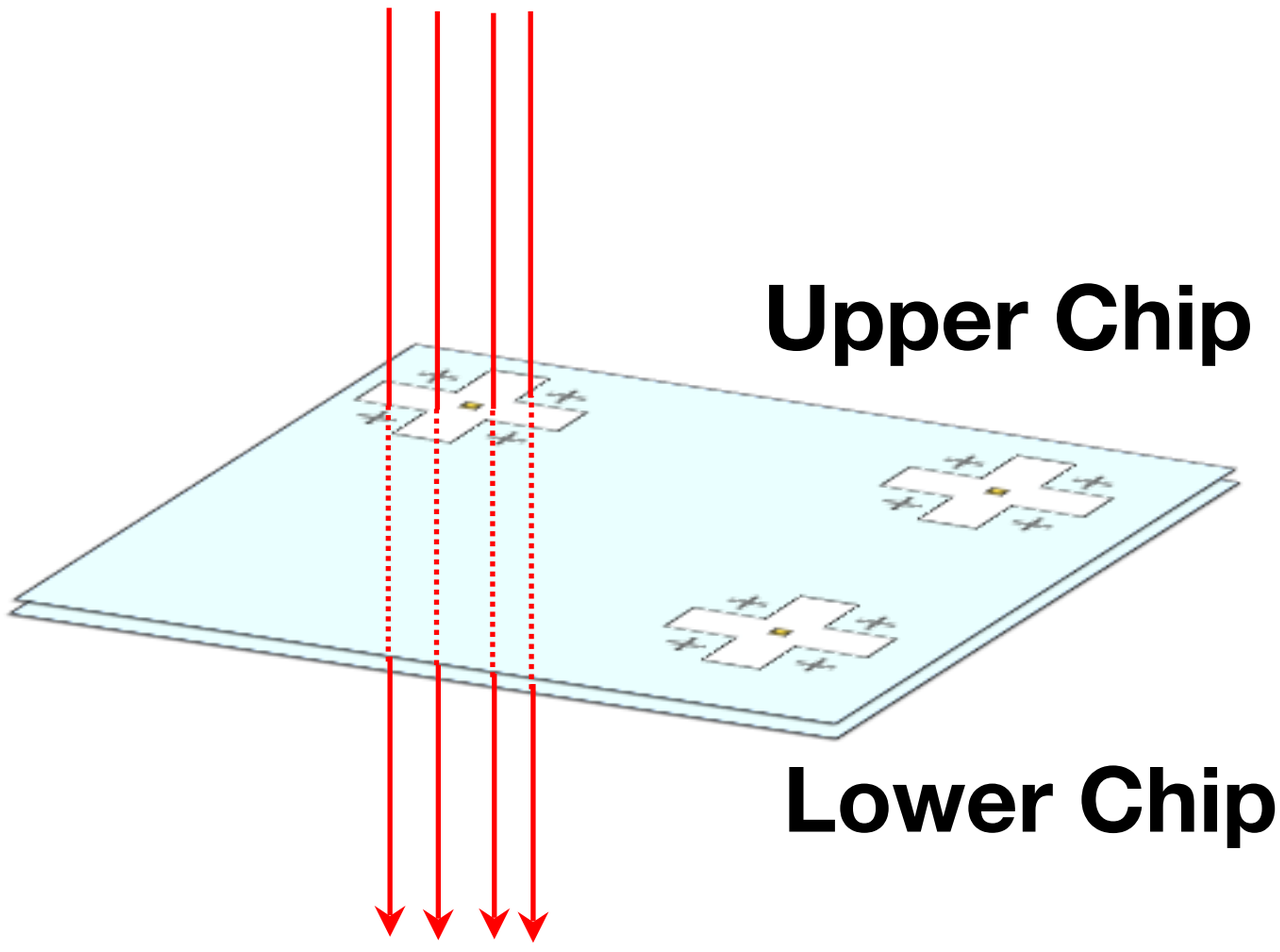
SOI Based 3D Integration

Metal 5 Alignment Mark

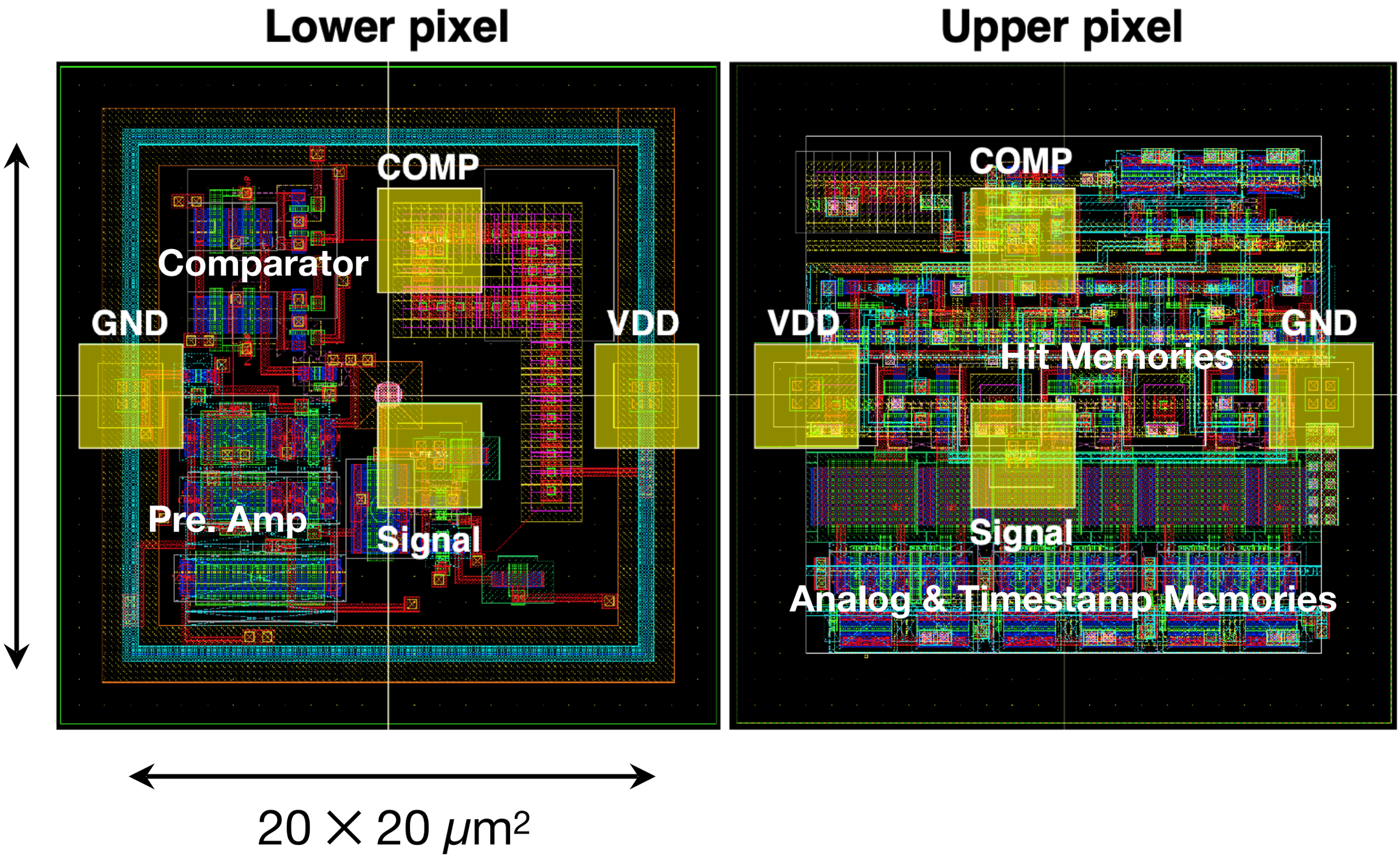




IR Microscope



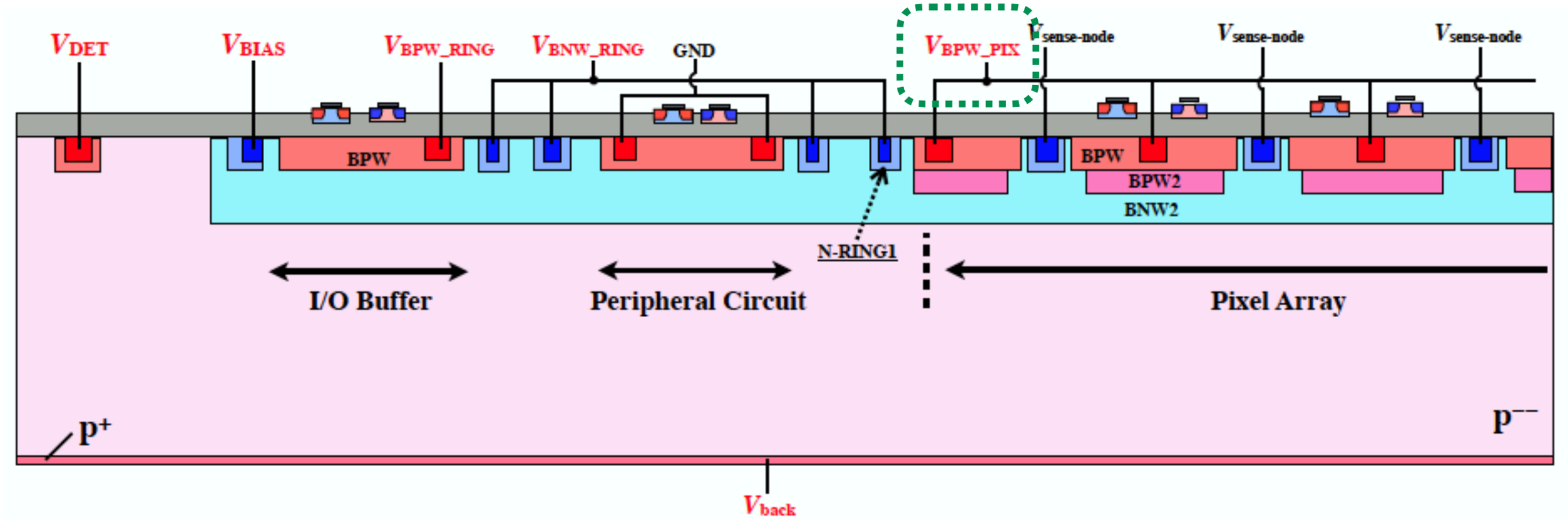
SOFSIT4 Pixel



PDD 構造

センスノード付近のポテンシャルは V_BPW_PIX で制御している.

V_BPW_PIX のチャージシェアへの影響は？



Run 247 - 252
V_BPW_PIX Scan: -1.1, -1.4, -1.6, -1.7, -1.8, -2.0 V

LVDS version 4

USAGI2 Conceptual Design

SOFIST3 x 4

Busy <0:3> → <0:3> LVDS Receiver → OR

NIM は足りなかったら
Pmod を作る.

RJ45
SOFIST3 #1

LVDS Driver → STORE/TRIGGER, RESET, EVT_TAG_CLK, N/A

LVDS Driver → STORE/TRIGGER, RESET, EVT_TAG_CLK, N/A

SOFIST3 #2 RJ45

RJ45

INT7 #1 → LVDS Driver → STORE/TRIGGER, RESET, EVT_TAG_CLK, N/A

INT7 #2 → LVDS Driver → STORE/TRIGGER, RESET, EVT_TAG_CLK, N/A

INT7 #3
INT7 #4 → STORE/TRIGGER, RESET, EVT_TAG_CLK, N/A

Pmod

1	J1	J2	48
2			47
3			46
4			45
5			44
6			43
7			42
8			41
9			40
16	J3	J4	33
17			32
18			31
19			30
20			29
21			28
22			27
23			26
24			25

OR circuit → pin 48

J1 と同様

OR circuit → pin 31

NIM → pin 29

NIM → pin 26

<0:1>

FANOUT (FANOUT = 2)
<0:4>
<0>
<2>

XRPIX5 x 1
SEABAS1 NIMIN/OUT

- STORE/TRIG_EN
- EVT_TAG_CLK
- EVT_TAG_TRG

VCC 5 V GND

USAGI2 上のコネクタは RJ45 か LEMO

USAGI3 and KoUSAIG3

DAQ Master Board

Cmod S7 から DAQ に必要な信号を配布／受信するための I/O ボード
昨年の反省を踏まえて USAGI3 を作ったが，現地で殆どの LVDS ドライバーに不具合が起き（破損？ESD？）
結局 USAGI2 を使った（slave の BUSY の OR は NIM モジュールでとる）.

電源: 3.3 V
レギュレーターで ± 5 V を生成