TIGER ASIC for GEM Readout

EIC DAQ/Electronics Readout ASICs Meeting
June 19, 2020

Istituto Nazionale di Fisica Nucleare

Manuel Da Rocha Rolo

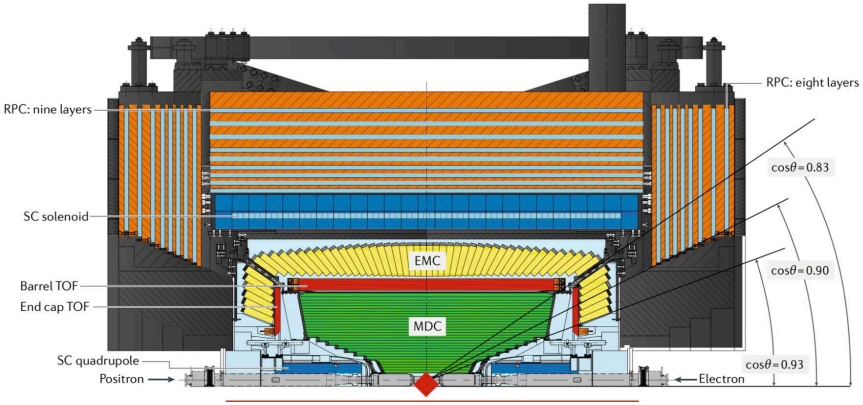
The BESIIICGEM project has been funded by European Commission within the calls H2020-MSCA-RISE-2014 and FEST RISE-MSCA-H2020-2020

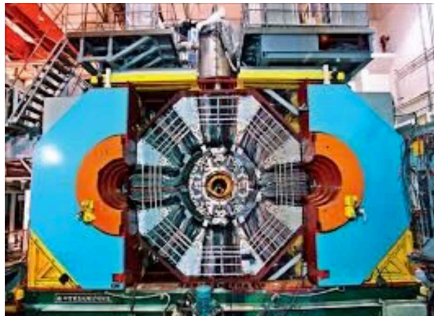
HORIZON 2020 European Commission

The BESIII Experiment at BEPCII

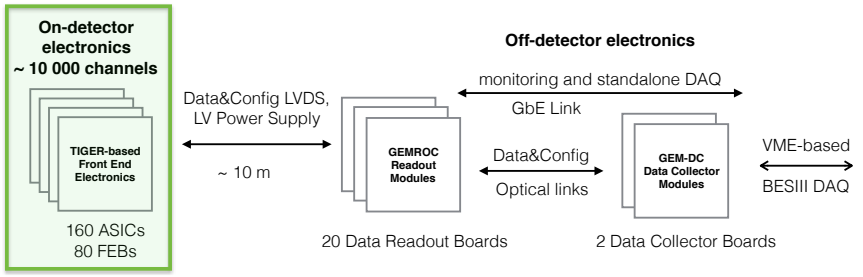
- The BESIII experiment @ BEPCII (Beijing Electron-Positron Collider) - operation since 1989, upgrade to BEPCII in 2008
- BESIII Collaboration counts ~500 authors from 67 Institutions, 14 Countries

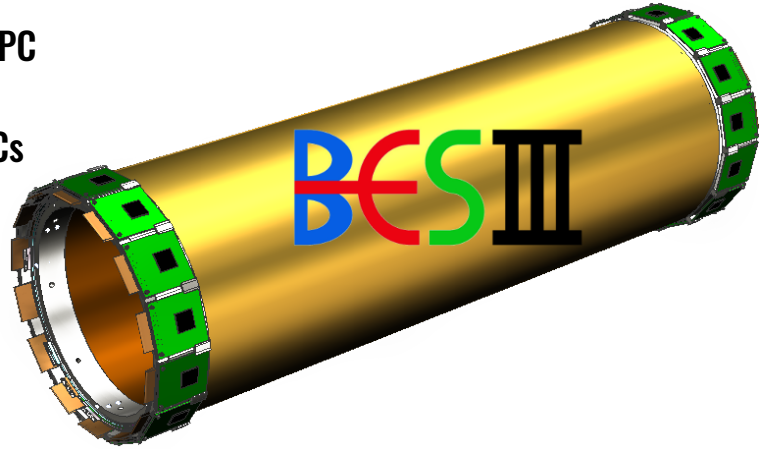
Parameters	BEPCII
Center of mass Energy	$(2.0 \div 4.6)$ GeV
Peak luminosity at 2×1.89 GeV	$\sim 10^{33}$ cm^{-2} s^{-1}
Circumference	237.5 m
Number of rings	2
RF frequency	499.8 MHz
Number of bunches	2×93
Beam current	2×0.91 A
Bunch spacing	2.4/8 m ns^{-1}
Bunch length (σ_z)	1.5 cm
Bunch width (σ_x)	~ 380 μm
Bunch height (σ_y)	~ 5.7 μm





- new lightweight tracker based on an innovative Cylindrical Gas Electron Multiplier (CGEM) detector for the upgrade of the BESIII spectrometer
- analogue readout of the CGEM enables the use of charge centroid and μ-TPC algorithms to improve the spatial resolution
- 10 000 channels are readout by 160 dedicated 64-channel front-end ASICs



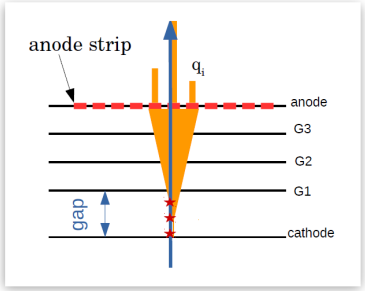


Upgrade of the BESIII Inner Tracker

- Spatial resolution: σ_{xy} = 130 μm , σ_z = 300 μm
- Momentum resolution: σ_{pt}/p_t = 0.5% @ 1 GeV/c
- Efficiency = 98%
- Material budget ≤ 1.5% of X_0 for all layers
- Rate capability: ~10^4 Hz/cm^2
- Coverage: 93% 4π

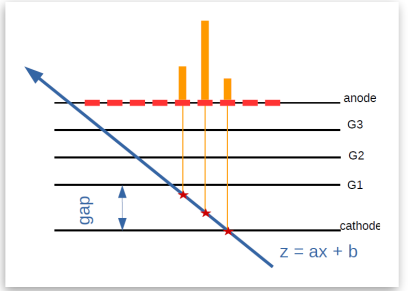
Reconstruction algorithms

Charge Centroid (CC)

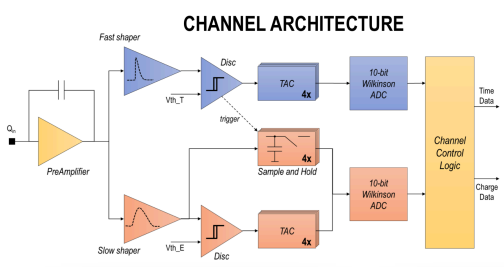


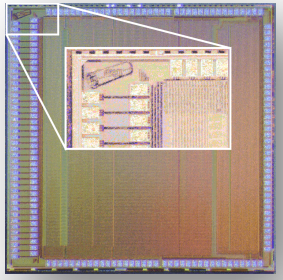
Weighted average of strip positions by collected charge

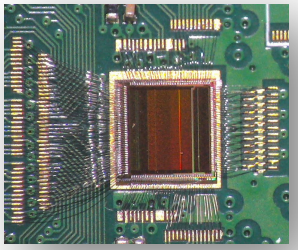
μ-TPC readout

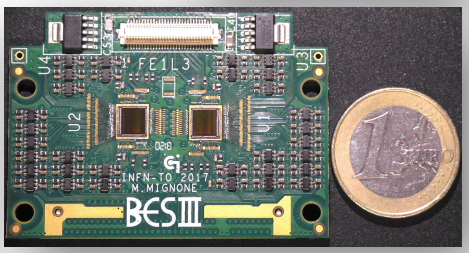


2D track reconstruction exploiting time of arrival and drift velocity









TIGER ASIC for the CGEM-IT Readout

- provides an analogue readout (time and charge information) for CC and μ-TPC algorithms
- 64-channel Application Specific Integrated Circuit

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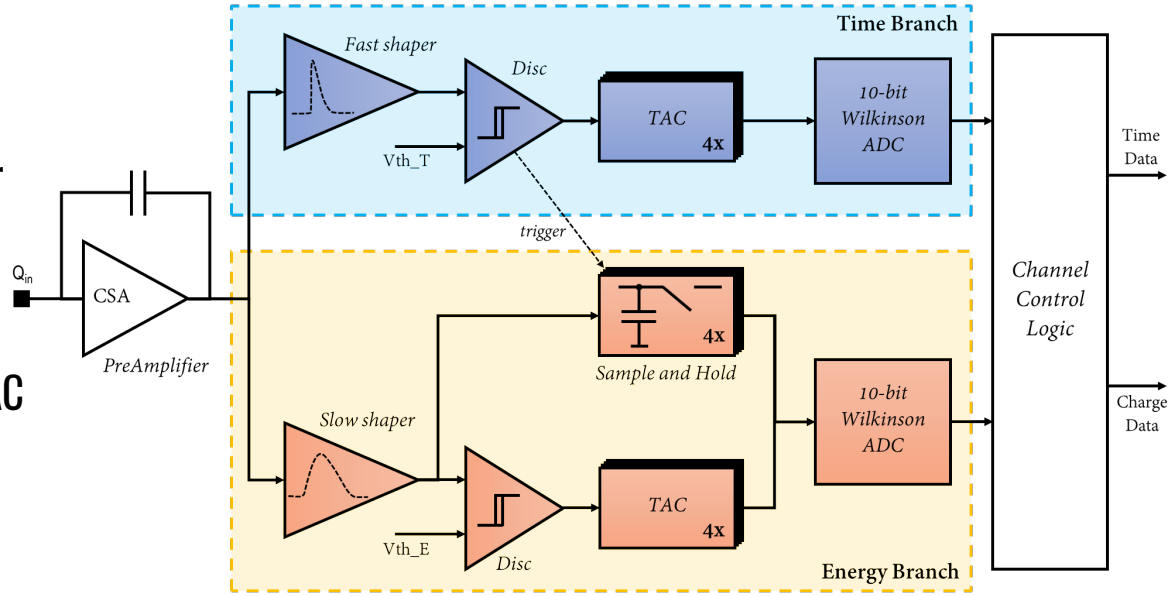
TIGER ASIC for the BESIII CGEM-IT

- TIGER has been designed for the readout of the CGEM-IT (Cylindrical Gas Electron Multiplier Inner Tracker)
  - new inner tracker of BESIII Experiment
  - 10 000 channels readout by 160 64-channel TIGER ASICs
- Time and charge measurements with fully-digital output
  - Charge centroid and μ-TPC algorithms
  - 130 μm spatial resolution with strip pitch of 650 μm
- Sensor capacitance dependent on strips length, up to 100 pF
- Input charge: 2 - 50 fC
- Time resolution for μTPC mode: 5 ns
- Rate per channel: 60 kHz (4x safety factor)
- Power consumption: < 12 mW/ch
- SEU-tolerant

Efficiency	98%
Rate capability	10 kHz/cm^2
$\sigma_{r\Phi}$	130 μm
σ_z	300 μm
σ_{pt}/p_t	0.5% at 1 GeV/c
Coverage	93% 4π
Material budget	< 1.5 X_0
Inner radius	78 mm
Outer radius	178 mm
Magnetic field	1 T

Channel Architecture

- Analogue Front-End:
  - Charge Sensitive Amplifier
  - dual-branch shaper optimized for time and charge measurements
- Trigger-less readout architecture:
  - 2 LE discriminators with 6-bit DAC for threshold equalization
  - dual-threshold readout mode
- Timestamp on rising edge of fast branch
  - Time resolution < 5 ns
  - Low-power TDCs based on analogue interpolation
- Charge measurement:
  - ToT: timestamp on rising/falling edge
  - S/H: slow shaper output sampled and digitized with a 10-bit Wilkinson ADC



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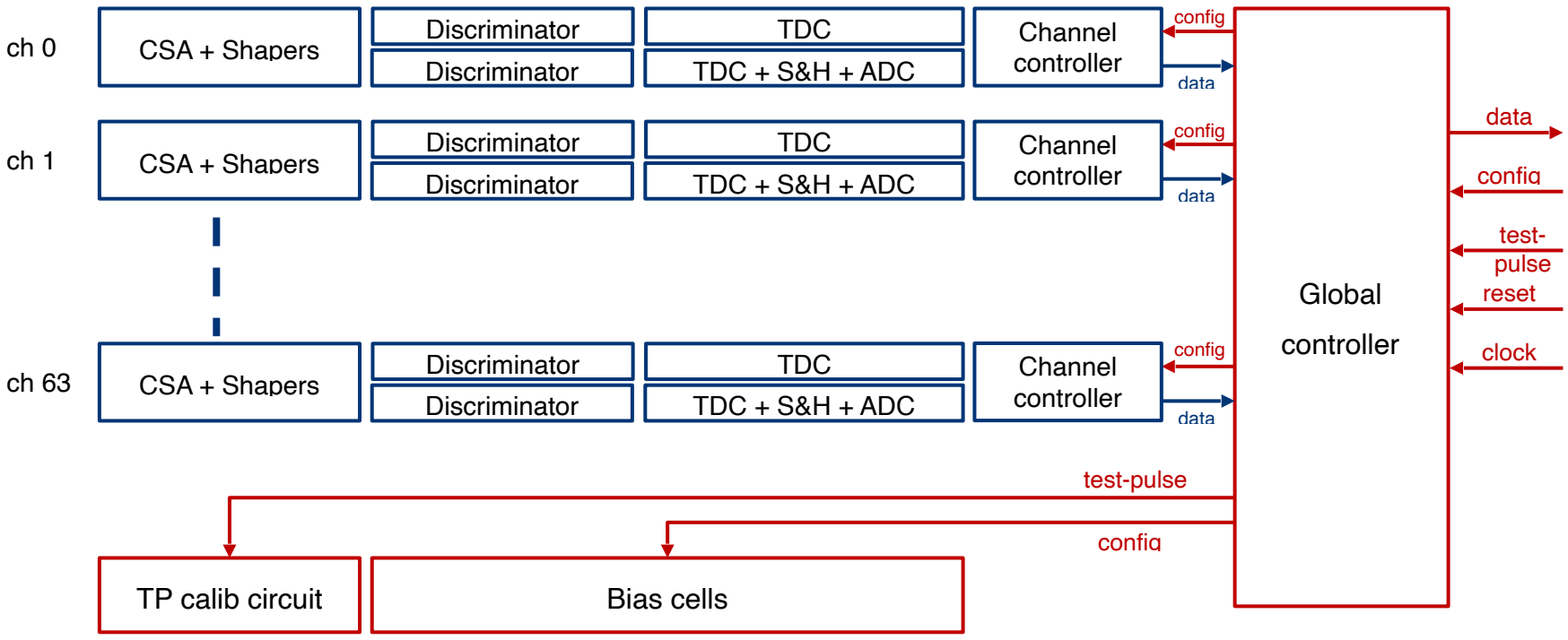
ASIC Architecture

- The ASIC embeds an array of 64 channels (amplifier, discriminator, TDC/ADC), a digital global controller, bias and references generators and a test-pulse calibration circuit.



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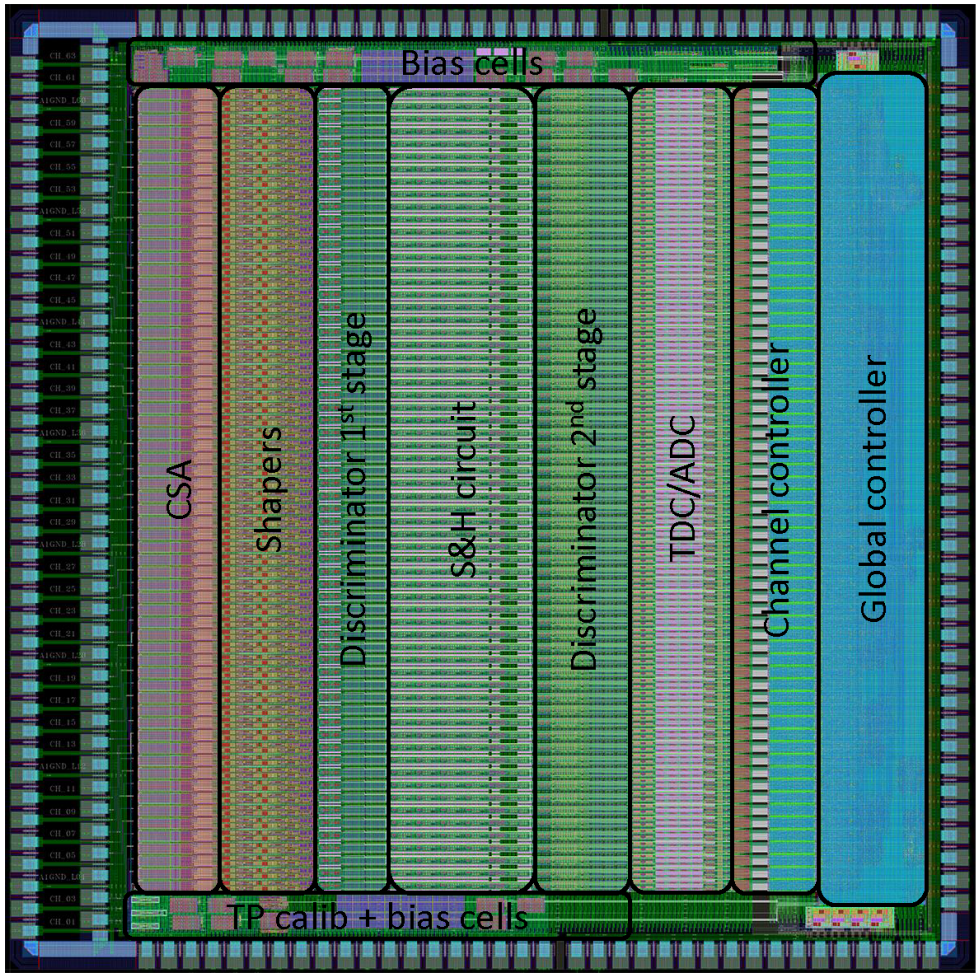
Chip Floorplan

- 5 x 5 mm^2 110nm CMOS technology
- Digital backend adapted from TOFPET2* (SEU protected)
- 64 channels: CSA, shapers, TDC/ADC, local controller
- On-chip bias and power management
- On-chip calibration circuitry
- Trigger-less operation, fully digital output
- 160-200 MHz system clock
- 4 TX SDR/DDR LVDS links, 8B/10B encoding
- 10 MHz SPI-like configuration link
- Power consumption < 12 mW/ch
- Sustained event rate > 100 kHz/ch



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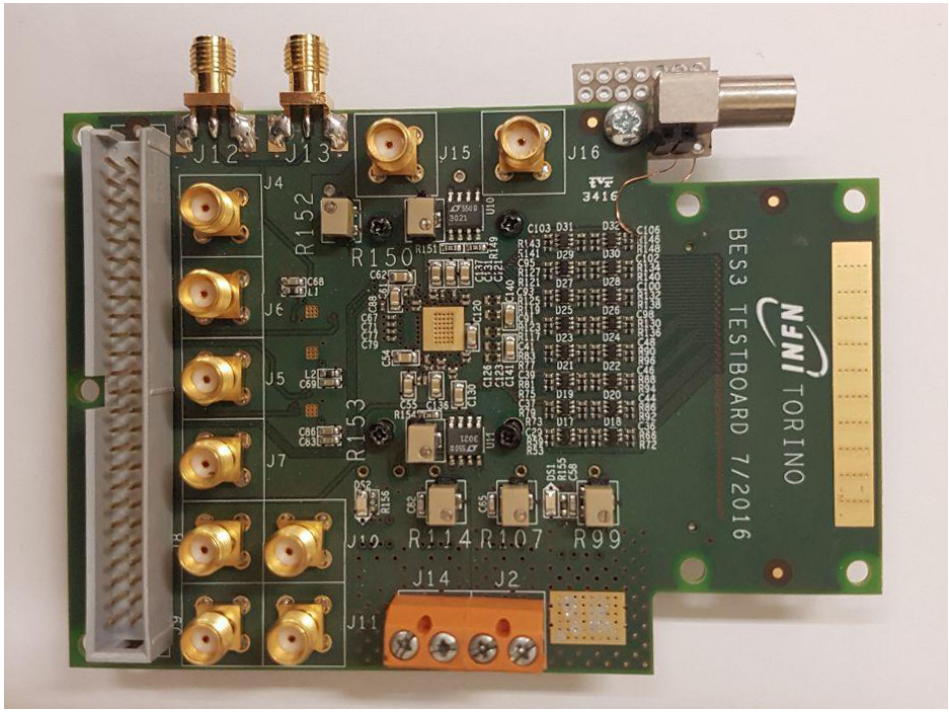
*https://doi.org/10.1088/1748-0221/14/03/P03029

Chip Test Board

Test-board for ASIC electrical characterization

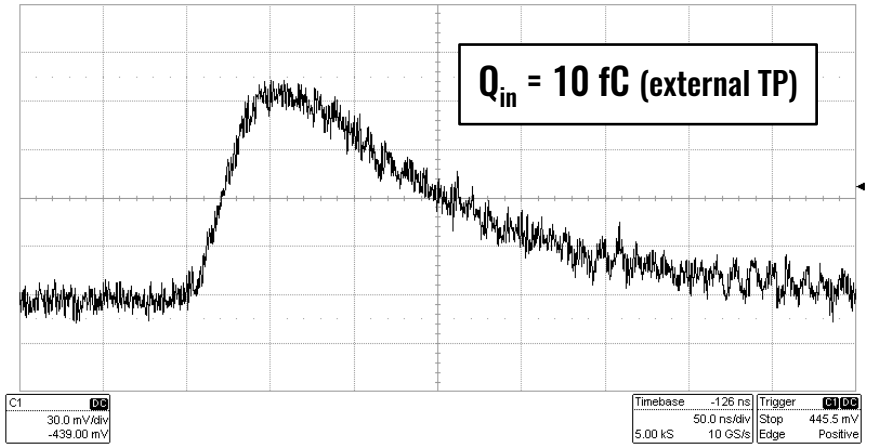
- Trimming capability for analogue and digital power domains and external reference voltages

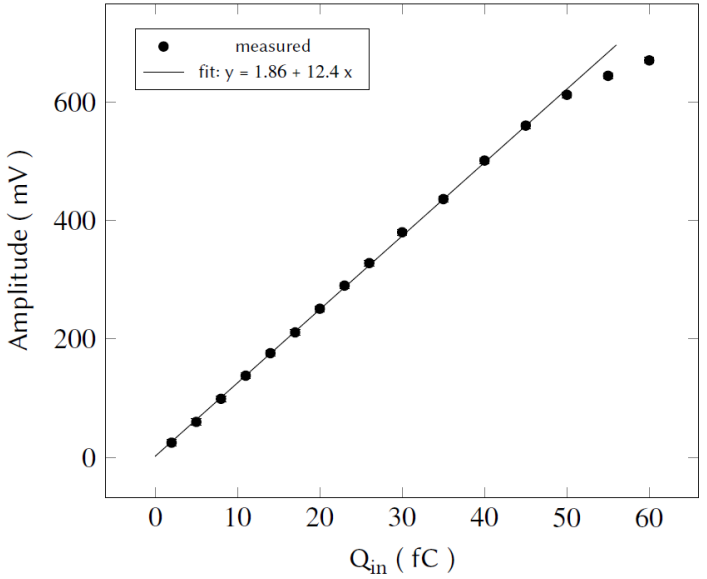
- Debug IO ports:
    2. External test-pulse injection
    3. External capacitor insertion
    4. T-branch shaper output and threshold probe points (ch. 63)
    5. Digital back-end control signals (TDC and S&H)



Electrical Characterization

Front-end response and linearity





ΔV ≈ 120 mV

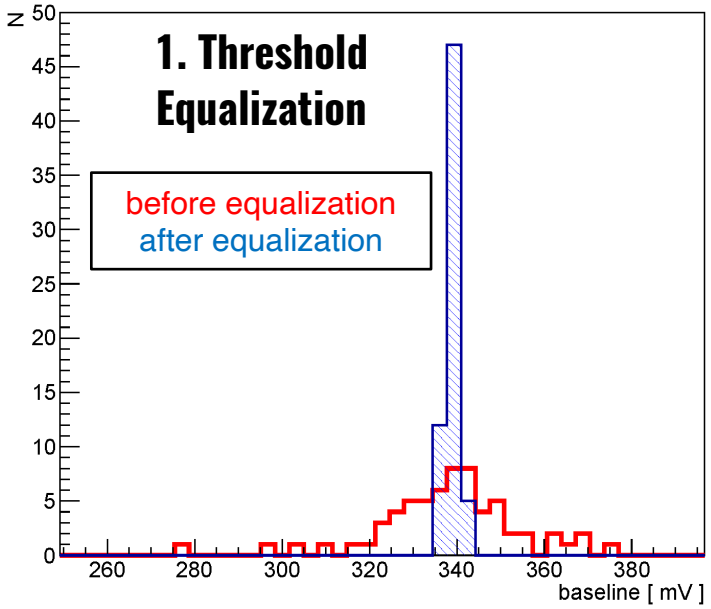
Peaking time ≈ 60 ns

Gain ≈ 12.4 mV/fC

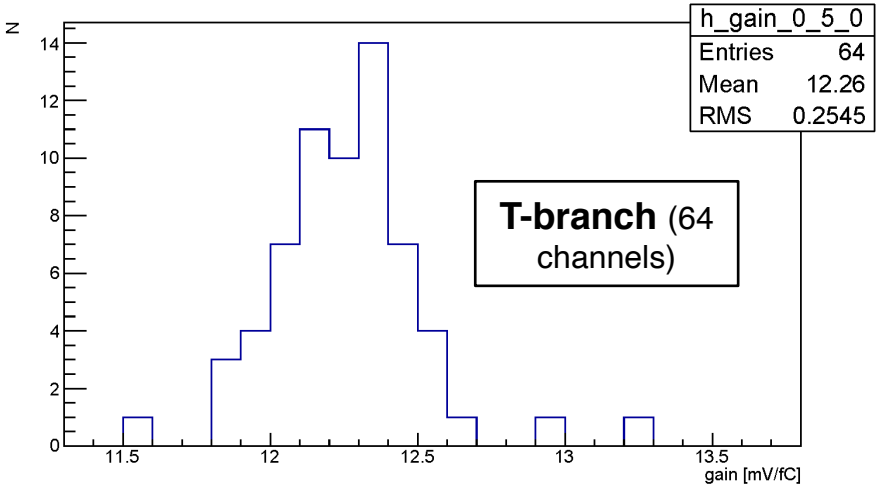
Electrical Characterization

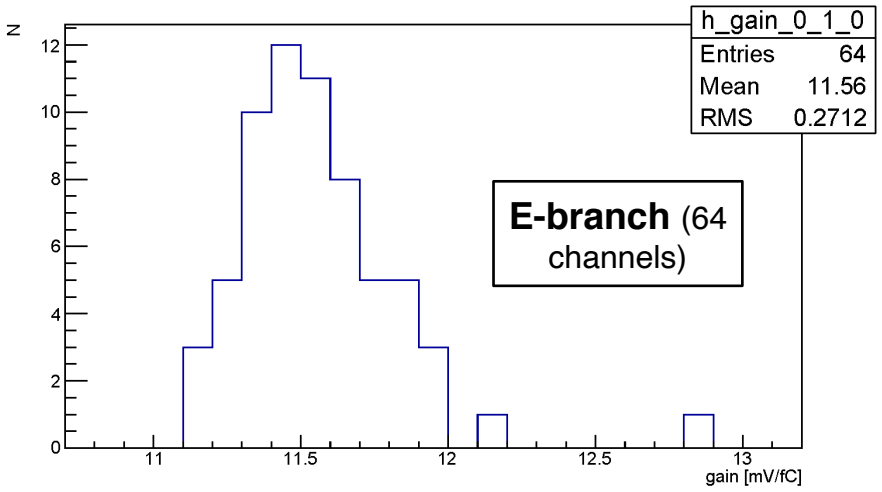
Threshold scan and gain dispersion

1. V_{th} scan to generate LUT and equalize thresholds
   - ➢ below 5 mV RMS dispersion after V_{th} equalization
2. V_{th} scan with internal TP to measure gain of 64 channels on both branches



2. Gain dispersion

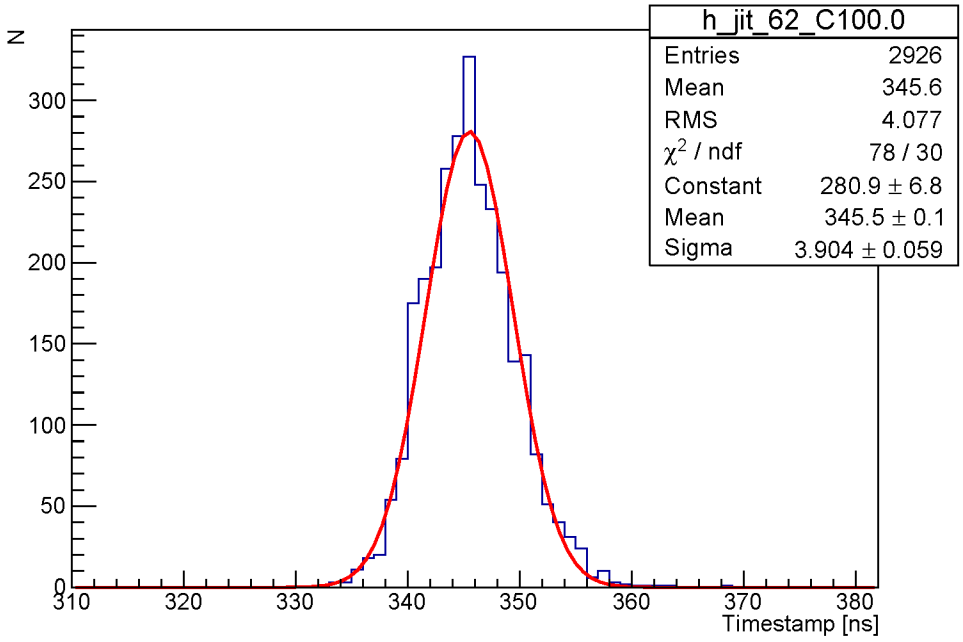




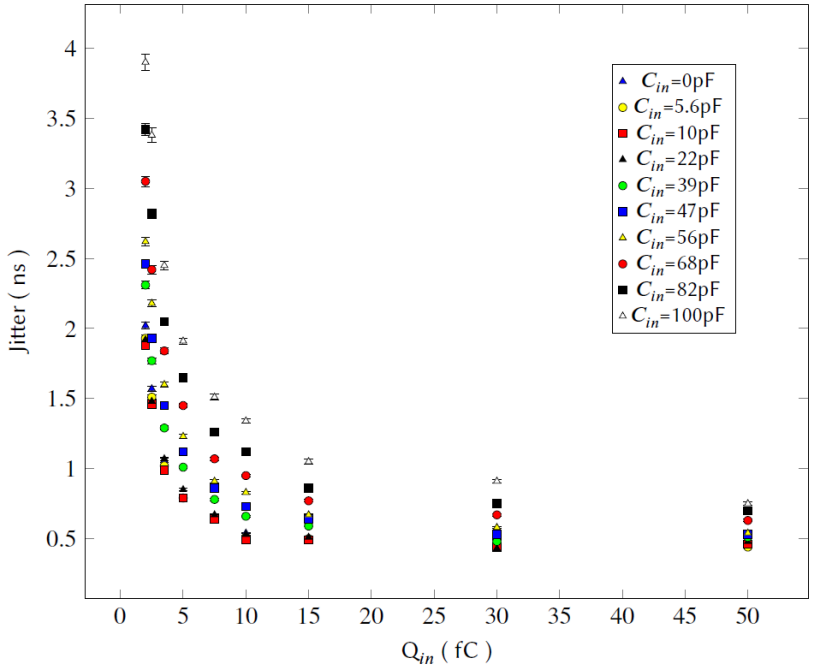
Electrical Characterization

Timing Resolution

- TP injected to VFE, generated by on-chip calibration circuit
- Here, fixed amplitude and time skew in respect to system clock



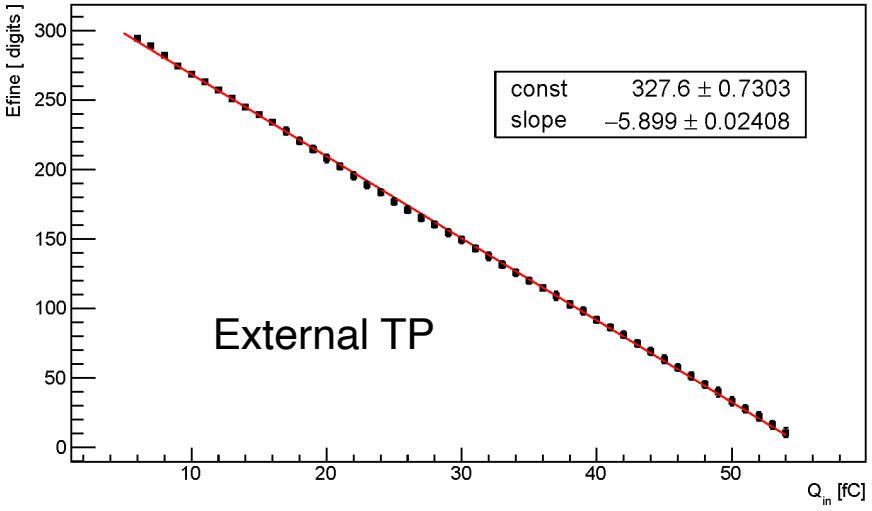
- Jitter vs. Q_{in} vs. C_{in}

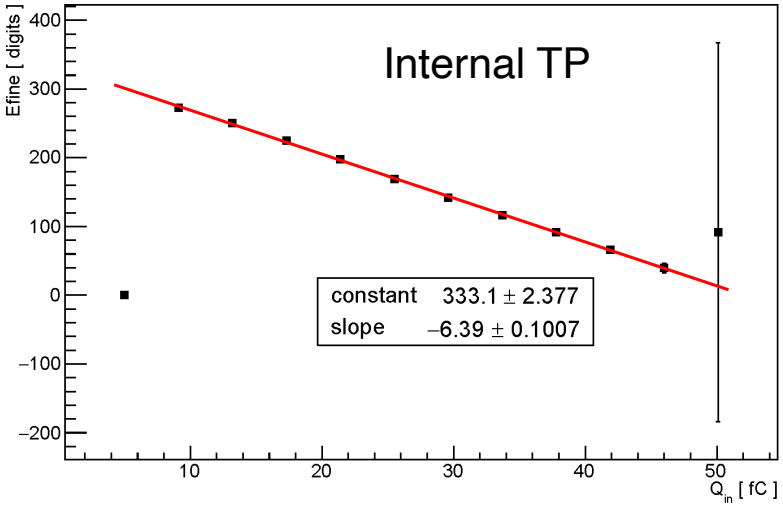


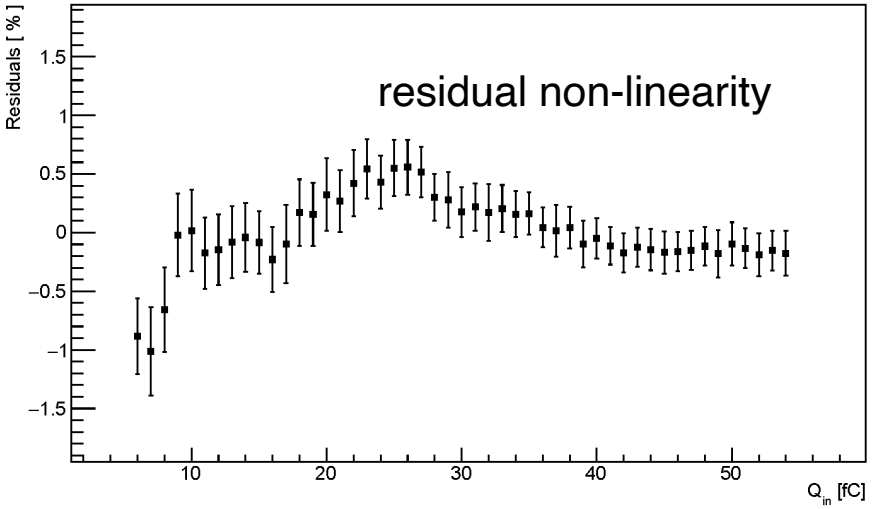
Electrical Characterization

Charge Measurement

- S/H **dynamic range** and **linearity** with external test-pulse generator (ch. 63 input debug port)
- Back-annotation for **internal test pulse calibration** to assess all channels







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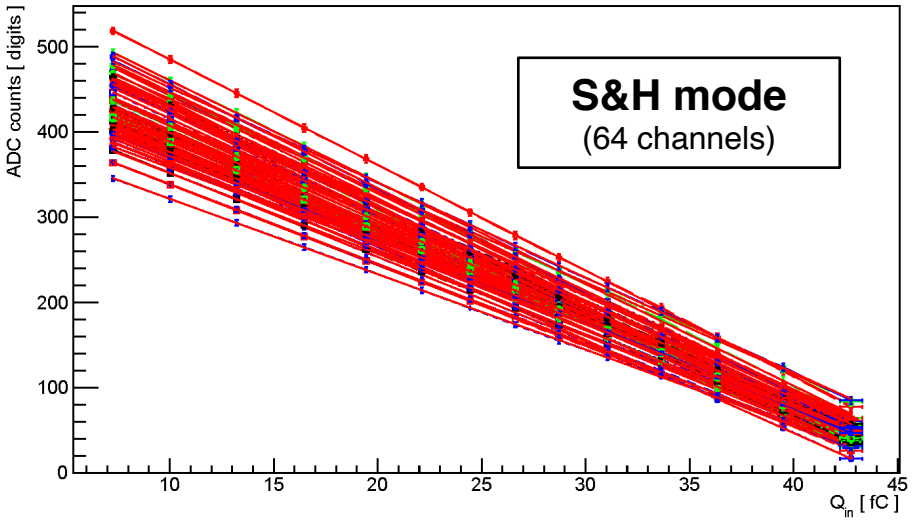
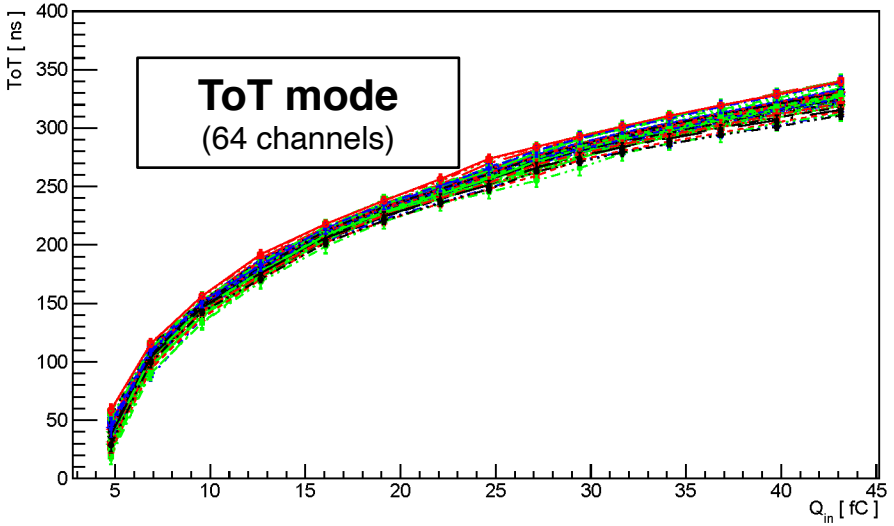
Electrical Characterization

Charge Measurement



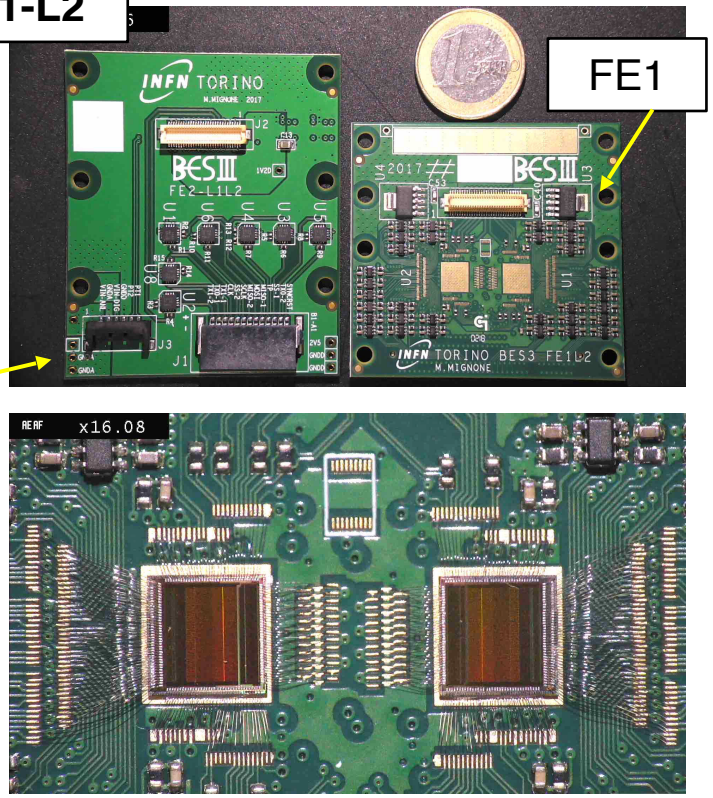


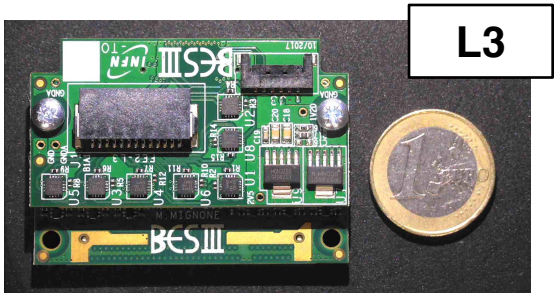
- **Linear response** from S&H circuit - easy to calibrate
- S&H limited by **saturation** of FE and ADC above 50 fC
- ToT response intrinsically not linear with CR-RC shapers
- **ToT provides** moderate energy resolution at low Qin, allows for **extended dynamic range**

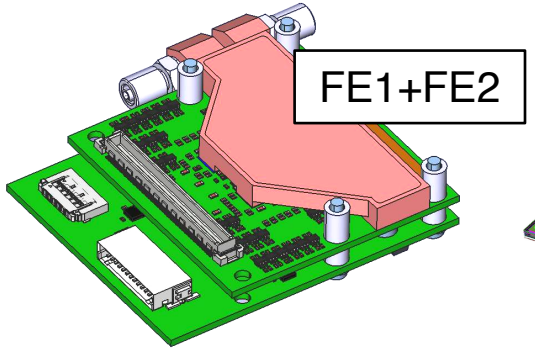
FEB (Front-End Board)

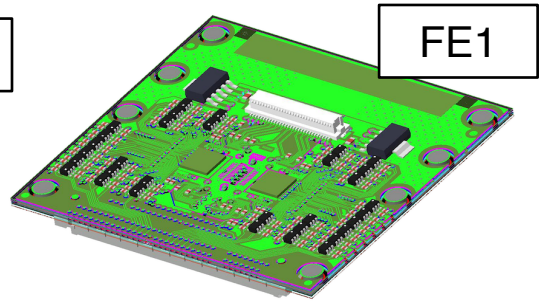
Front-End Board (FEB) for the on-detector CGEM electronics

- Stack of two printed circuit boards:
  - ➢ FE1: analogue-most layer
  - ➢ FE2: digital layer
- 2 TIGER ASICs mounted on FE1 (128 channels per FEB)
- Water-cooling heat exchanger plate for operation at controlled temperature
- Different layout and routing for L3 FEBs due to space constraints inside BESIII

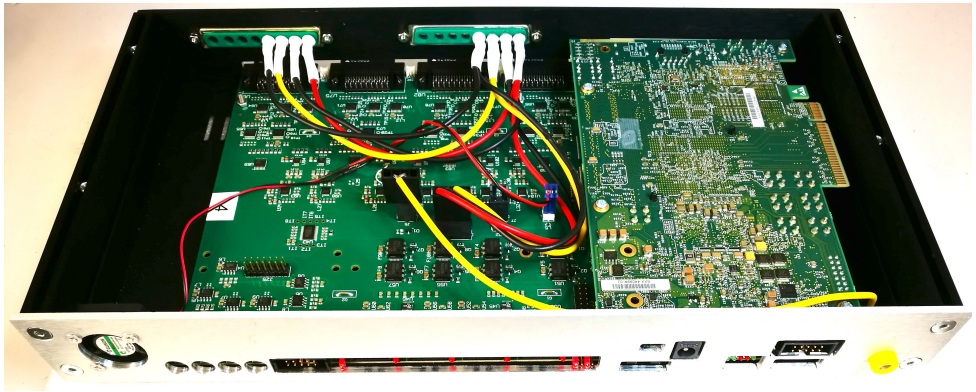


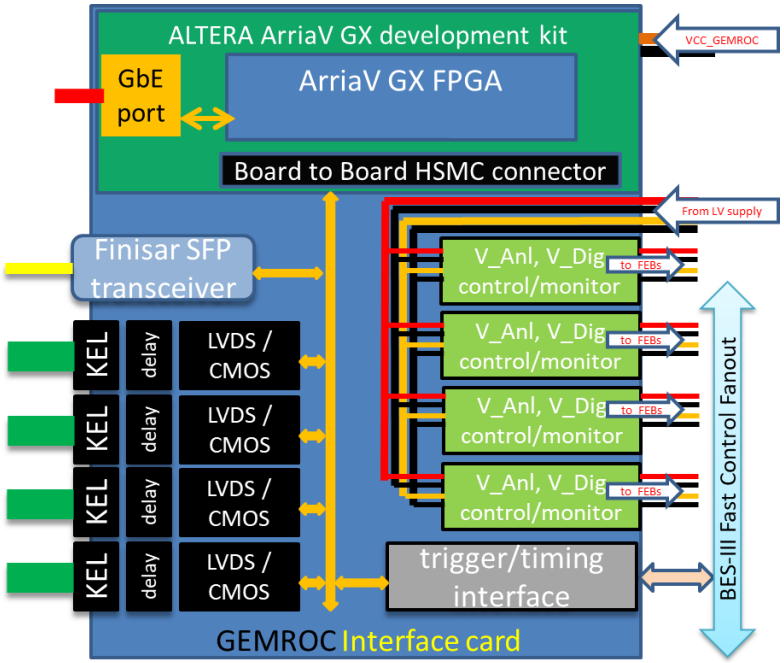






GEMROC (GEM ReadOut Card)

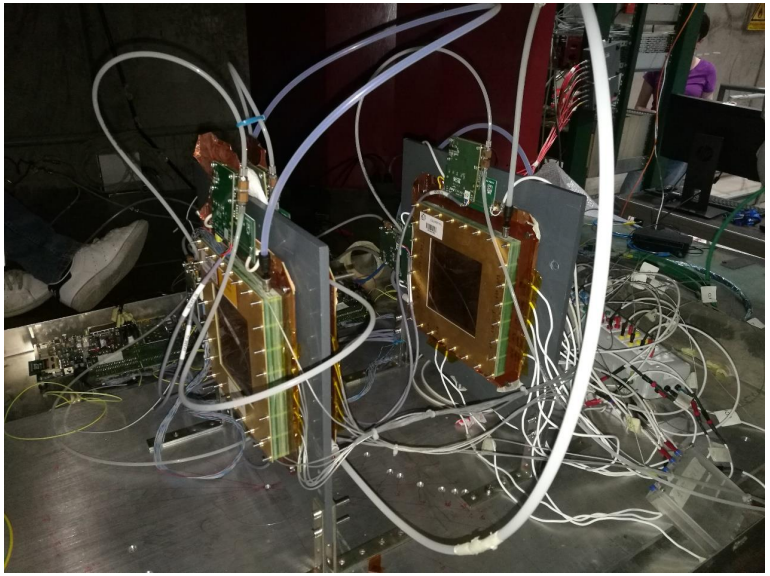




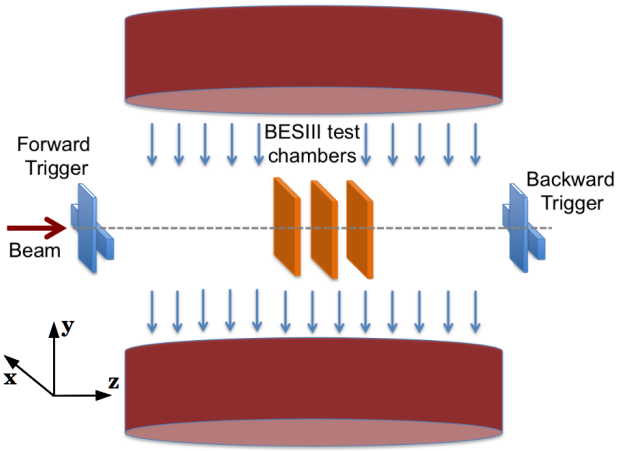
- Developed by INFN Ferrara
- Off-detector electronics for the readout of the CGEM-IT detector (160 TIGER)
- Provides power, configuration and data interface to the TIGER ASICs (up to 8 TIGER for each GEMROC)
- Trigger-Matching operations (trigger-less mode also available)

Beam tests with planar GEMs

- 2 beam tests to validate the ASIC with the sensor:
  - 10 x 10 cm^2 planar GEMs
  - XY orthogonal strips
  - Turin FPGA-based DAQ -> readout of 8 TIGER



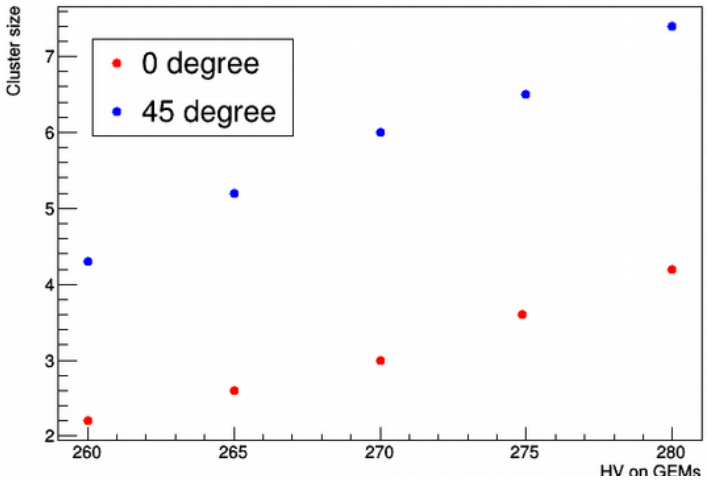
- Nov 2017: Mainz Microtron (TIGER prototype version)
- Apr 2018: CERN H4 beam line (TIGER final version)



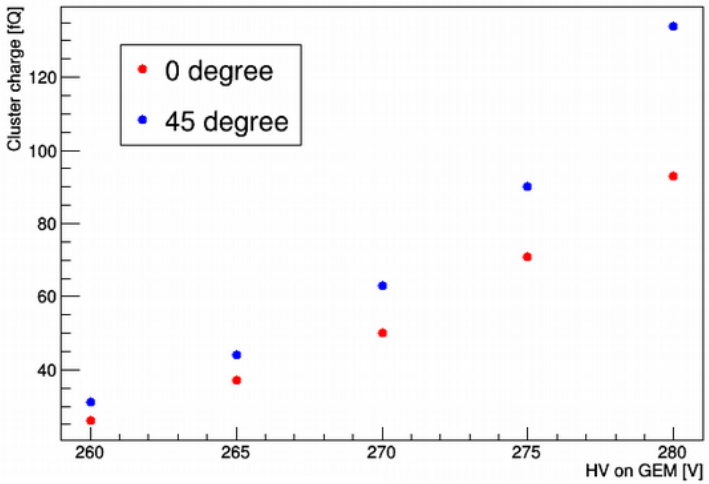
Trigger-less readout: trigger from scintillator bars injected as a digital test-pulse on one TIGER channel to be used as a reference for offline trigger-matching

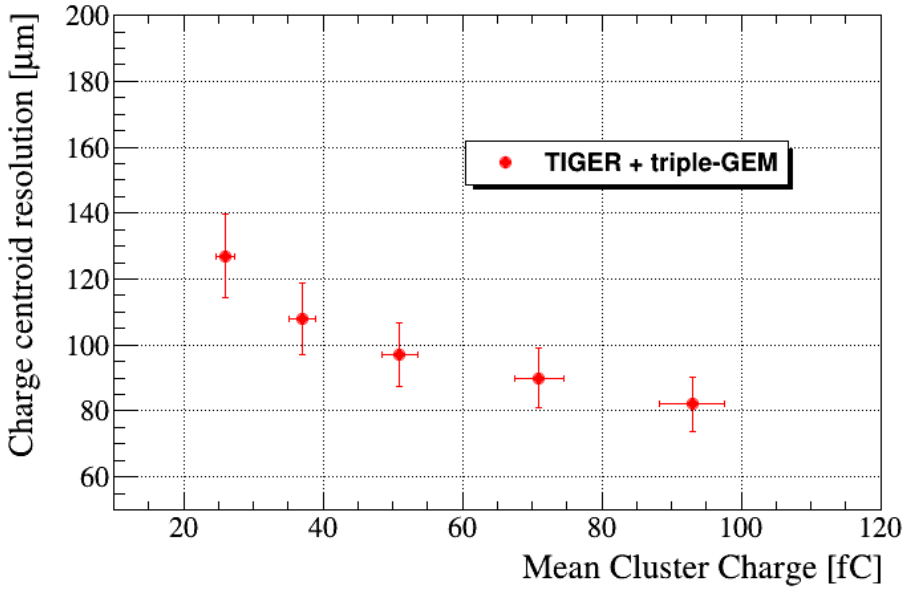
Beam tests with planar GEMs

Event Cluster size



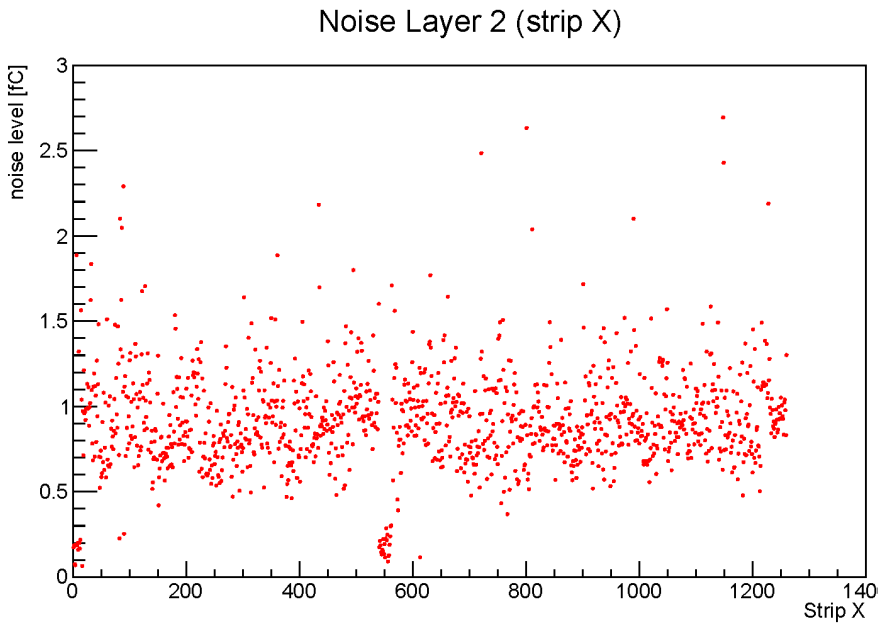
Event Cluster charge

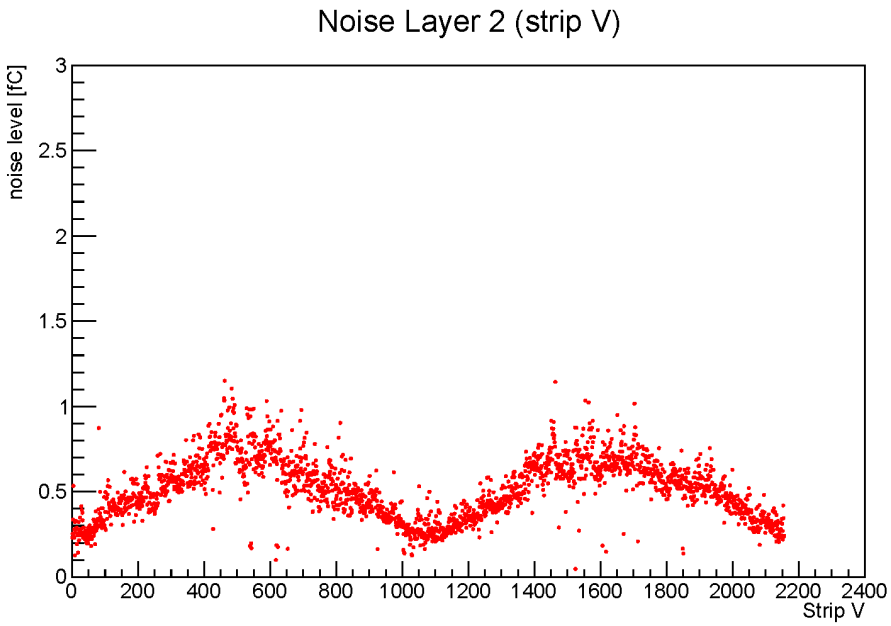




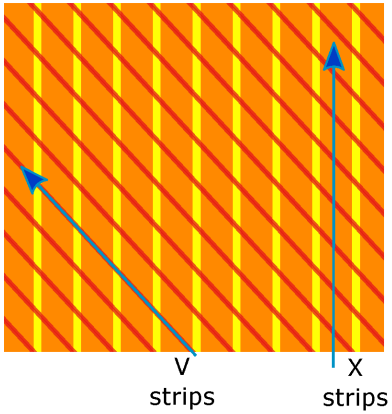
Charge Centroid spatial resolution

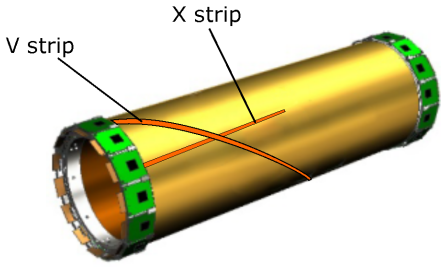
Noise measurements on CGEM





- Almost flat distribution for **X-strips**
- **V-strips** noise follows the strips length





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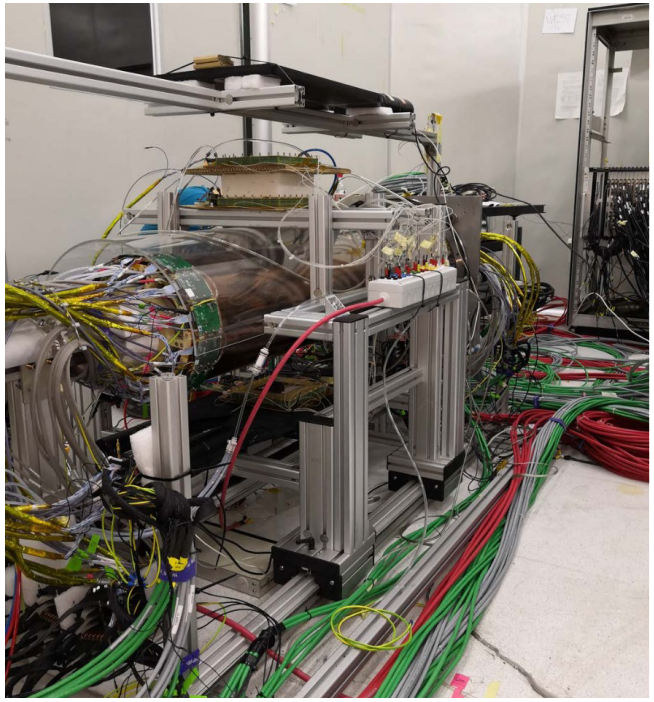
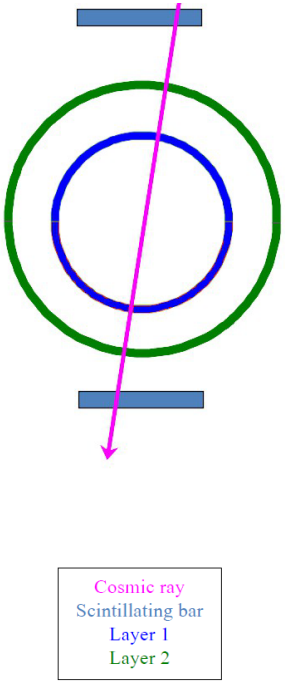
CGEM-IT commissioning and tests

Two out of three layers of the CGEM-IT detector are assembled together and cosmic rays acquisitions are now ongoing at IHEP (Beijing, China)

- *88 TIGER ASICs readout by 11 GEMROC modules (>5000 electronics channels instrumented)*
- *GUFI (Graphical User Front-end Interface) software provides DAQ control tools for:*
  - *Trigger-matched cosmic acquisition*
  - *Trigger-less operation for periodic maintenance*





R. Farinelli, "Preliminary results from the cosmic data taking of the BESIII cylindrical GEM detectors", talk at INSTR-20, Novosibirsk, Russia

Thanks for your attention.

Istituto Nazionale di Fisica Nucleare

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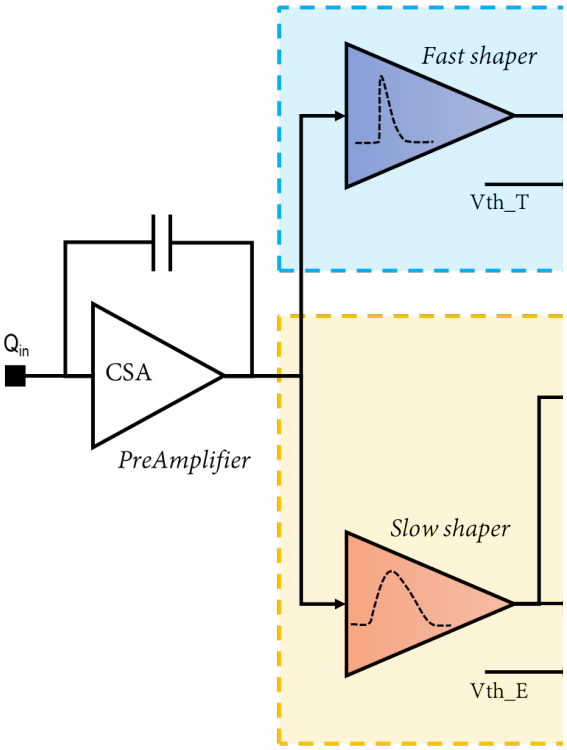
Analog Front-End



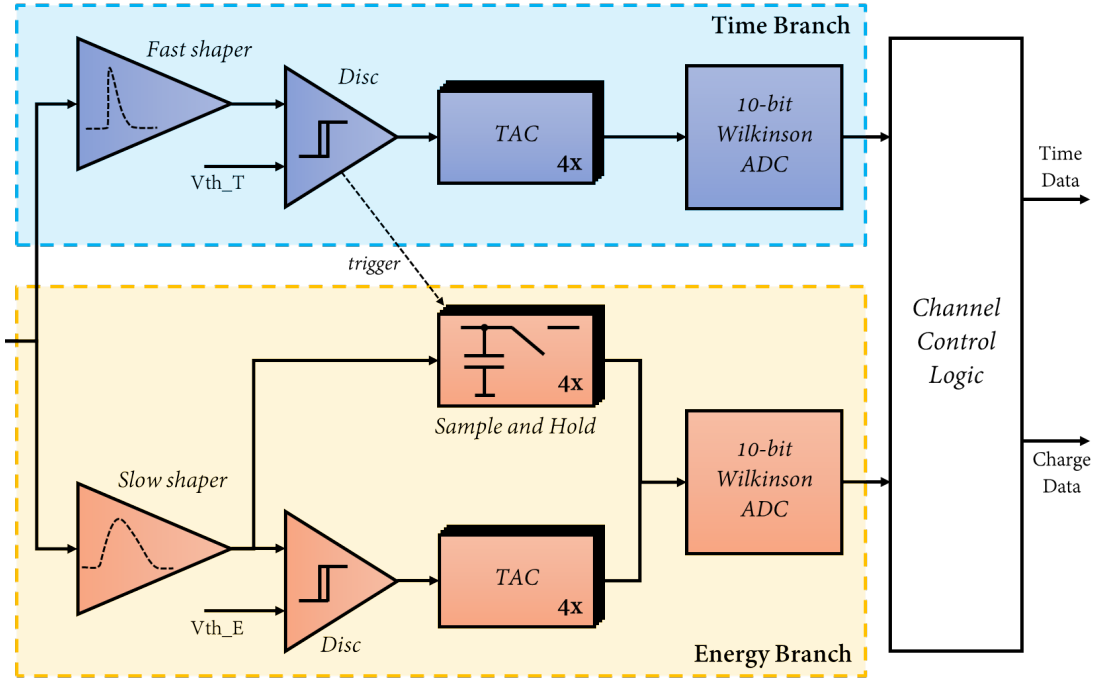
1. CSA pre-amplifier
   - Q_{in} = 2 - 50 fC
   - input transistor bias current set by 6-bit DAC (1.5 – 4.5 mA)
   - ENC target < 2000 e^- @ C_{in} = 100 pF
2. Time-branch
   - Simple CR-RC shaper
   - 60 ns peaking time for low-jitter timing measurement
3. Energy-branch
   - 4 complex-conjugate poles shaper for a more gaussian signal shape to reduce pile-up probability
   - 170 ns peaking time for signal-to-noise ratio optimization

- BLH to lock the shapers output DC to an external reference value (V_{BL} = 350 mV)

➢ Total gain ≈ 12 mV/fC

Trigerless Readout

- LE discriminators with 6-bit DAC programmable thresholds and 3-bit DAC hysteresis
- Data-push readout architecture: each signal above the selected threshold is taken as a good event, digitized and sent off-chip (no external trigger)



Time and Charge Measurement

- Coarse time measurement from the chip master clock counter
- Fine time measurement with low-power analogue TDCs based on time interpolation (I.F. = 128)
  - 50 ps time binning @ 160 MHz
  - Quad-buffered TACs for event de-randomization
  - TAC buffers with refresh scheme to avoid off-chip correction algorithm for leakage
- Charge measurement with S/H circuit sampling the E-branch shaper output
  - Programmable sampling time targeting the signal peak
  - Digitization with Wilkinson ADC shared with the TDC
  - Quad-buffered sampling capacitors for event de-randomization
- Charge measurement from ToT information by operating both branches in TDC mode (backup solution)