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The SAMPA Chip

A continuous read-out FE ASIC

(but it can be triggered, too)

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For the SAMPA Team

Meetings of the DAQ and electronics WG for the EIC Yellow report

19th June, 2020

The SAMPA ASIC, a bit of history

Starting from Run3, ALICE will operate at higher rate, aquiring all MB events

Goal: 50kHz in Pb-Pb (~10nb^{-1} in Run3 and Run4)

Upgrade detectors and electronics during Long Shutdown 2 ("now")

➢ Time Projection Chamber (TPC)

- GEM readout plane, high rate capability, continuous readout.

TPC electronics used till 2018 was not made to amplify negative charge input (as GEMs provides) and cannot cope with the higher rate and with the continuous readout operation planned

➢ Muon Chamber (Forward muon spectrometer)

- Higher rate capability, new acquisition electronics chain in ALICE

new electronics needed, too

TPC required a new readout, MCH too.

A common project to design a new ASIC: SAMPA

SAMPA Design Specifications Summary

SAMPA is an ASIC developed for the readout of ALICE TPC and MCH detectors:

GEM MWPC

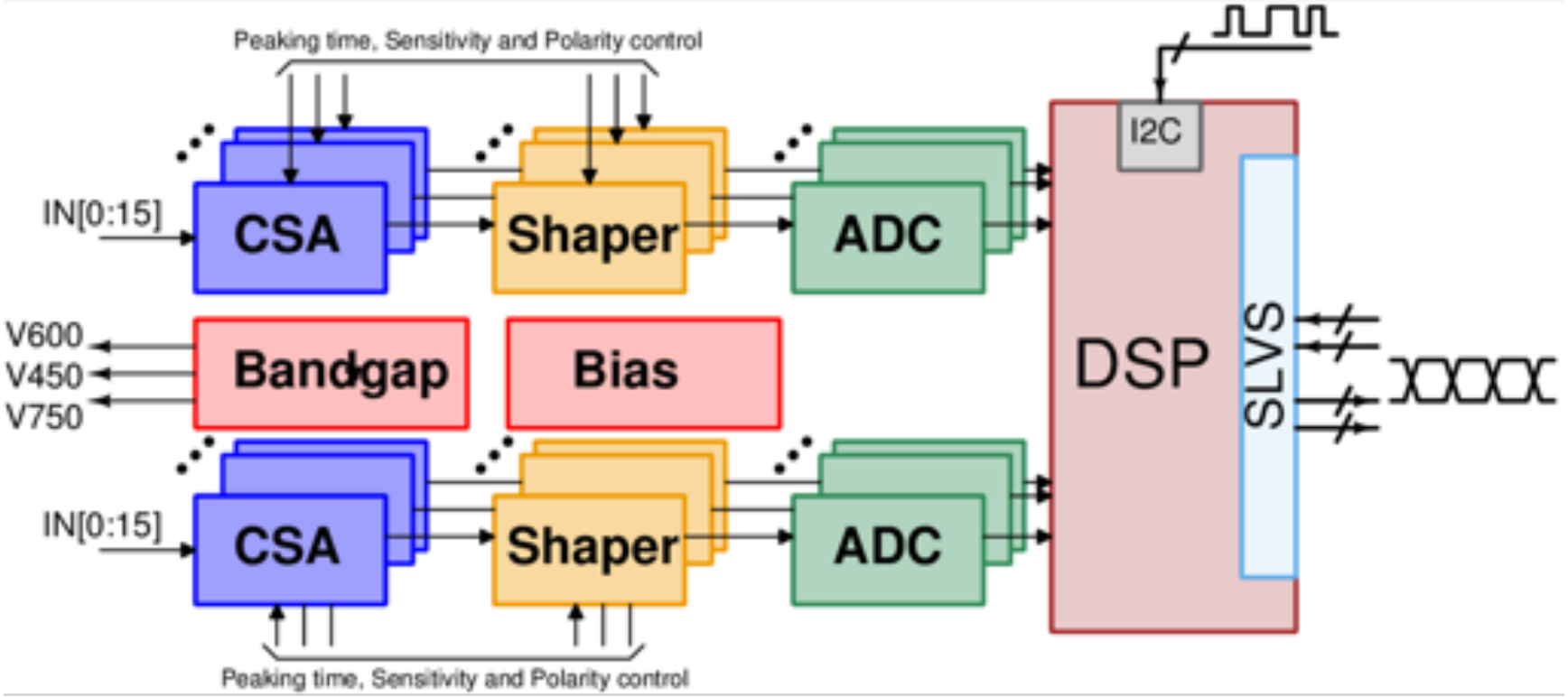
- TSMC CMOS 130 nm, 1.25V technology
- 32 channels, Front-end + ADC + DSP
- package size ≤15x15mm^2 (total footprint)
- ADC: 10-bit resolution, 10MS/s, ENOB>9.2
  (Alice TPC is eventually using: 5MS/s, to keep BW requirement in the readout chain lower)
- DSP functions: pedestal removal, baseline shift corrections, zero-suppression
- Data transmission: up to 11 e-link at 320 Mbps to GBTx, SLVS I/O
- Power < 32 mW/channel (Front End + ADC) V4, typical configuration, usually 20mW/ch or less.

TPC Mode	MCH Mode
▪ Negative Input charge	▪ Positive input charge
▪ Sensor capacitance: 12 – 25 pF	▪ Sensor capacitance: 40–80 pF
▪ Sensitivity: 20mV/fC & 30mV/fC	▪ Sensitivity: 4mV/fC
▪ Noise: ENC ≤ 580 e^- @ 18.5pF	▪ Noise: ENC ≤ 950 e- @ 40pF 1600 e- @80pF
▪ Peaking time: ~160 ns	▪ Peaking time: ~300 ns
▪ Baseline return: <500 ns	▪ Baseline return: <550 ns

In addition, a modified version with 80/160 ns shaping, 20/30 mV/fC gain, 20MSps ADC, has been designed, fabricated and validated, and is presently in production for sPHENIX TPC.

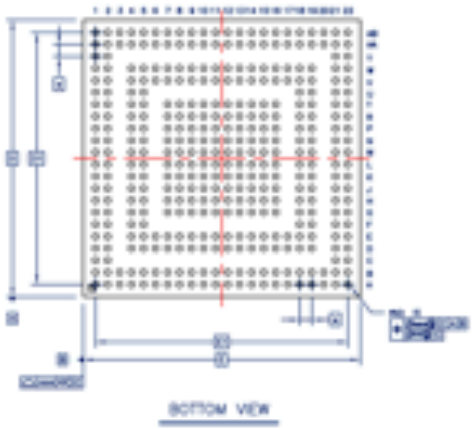
SAMPA Block Diagram

CONF	CSA	x	Shaper/Buffer	x	ADC	=	FullChip
”conf20”	1mV/fC		20mV/mV		~1ADU/2.15mV		~9.3ADU/fC
”conf30”	1mV/fC		30mV/mV		~1ADU/2.15mV		~14ADU/fC
“conf4”	0.5mV/ fC		8mV/mV		~1ADU/2.15mV		~1.9ADU/fC



SAMPA Package

- die size 9534µm x 8944µm
- TFBGA package
- 15 mm x 15 mm body size
- 1.2 mm thickness
- 0.65 mm ball pitch.
- 372 balls
- 4-substrate layers
- QR (unique identifier)

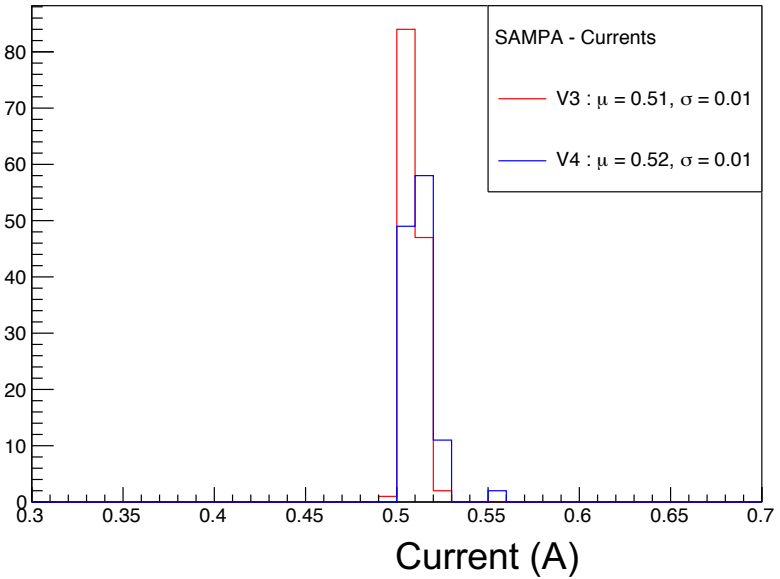


Performance

Some results from SAMPA qualification

Power Consumption (exp. results)

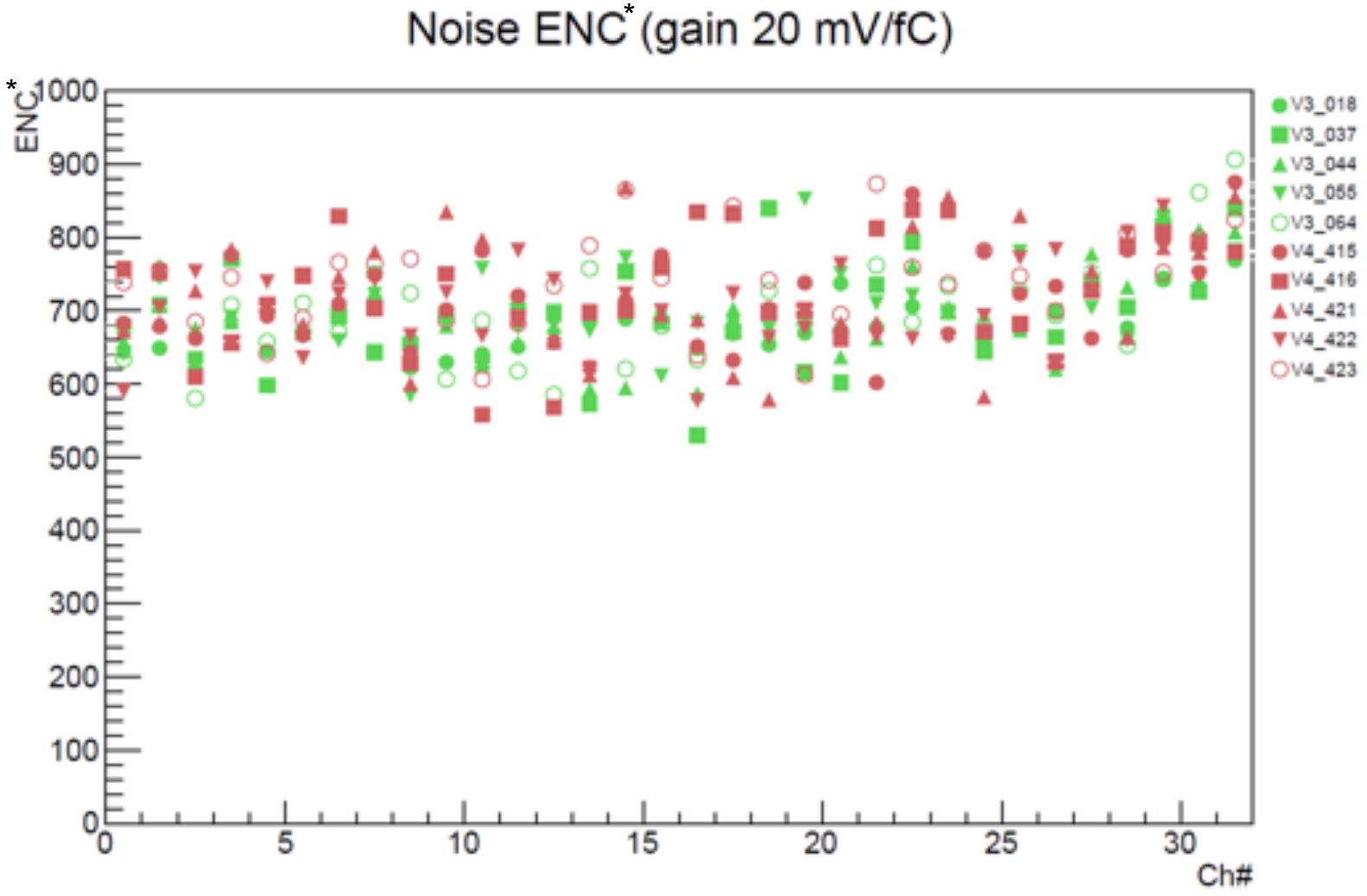
- **320 / 10 MHz operation mode**
- Current consumption from Power Supply (1.7V) **including regulators - Average of 10 Samples**:
  - All serial out enable (11) **without Data Acquisition**: **500 mA**
  - **Acquiring data** with 11 serial out enabled: **520 mA**
- Digital current increase with # of serial out enabled:
  - **4 serial out@ 480mA**
  - **11 serial out@ 502mA**



SAMPA is powered at ~1.25 V
In this configuration: **~ 20mW/ch**

Noise

Noise
(example of inside chip distribution)



*) ENC calculated using nominal FE gain (20mV/fC) and nominal ADC conversion factor (2.15 mV/ADU)

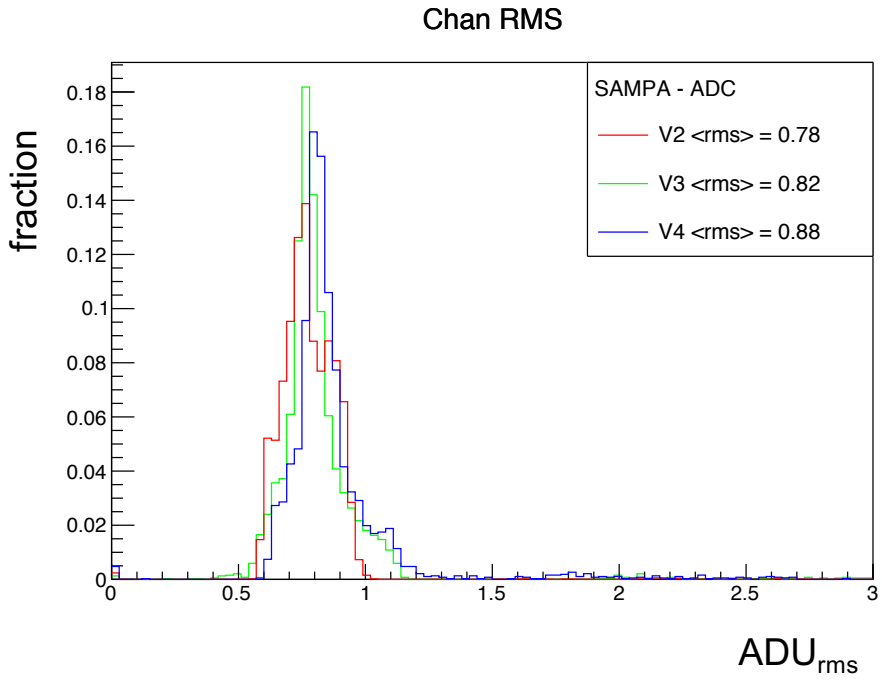
Noise (many chips)

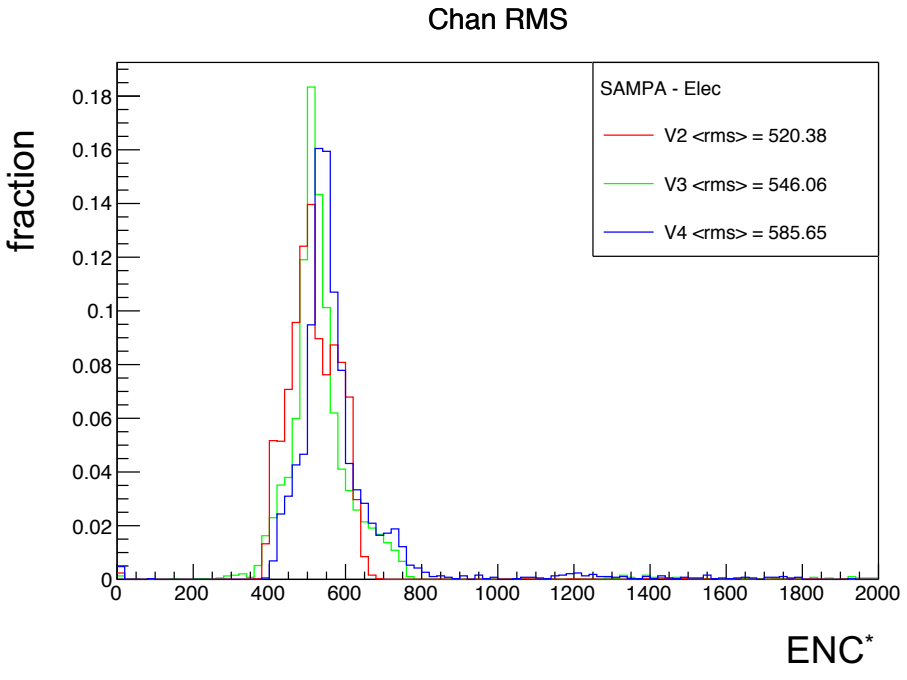
Experimental conditions:

C_{det}=0 (no added capacitance on the CSA input)

R_s=0 (external ESD-protection series resistor not present)

20N160



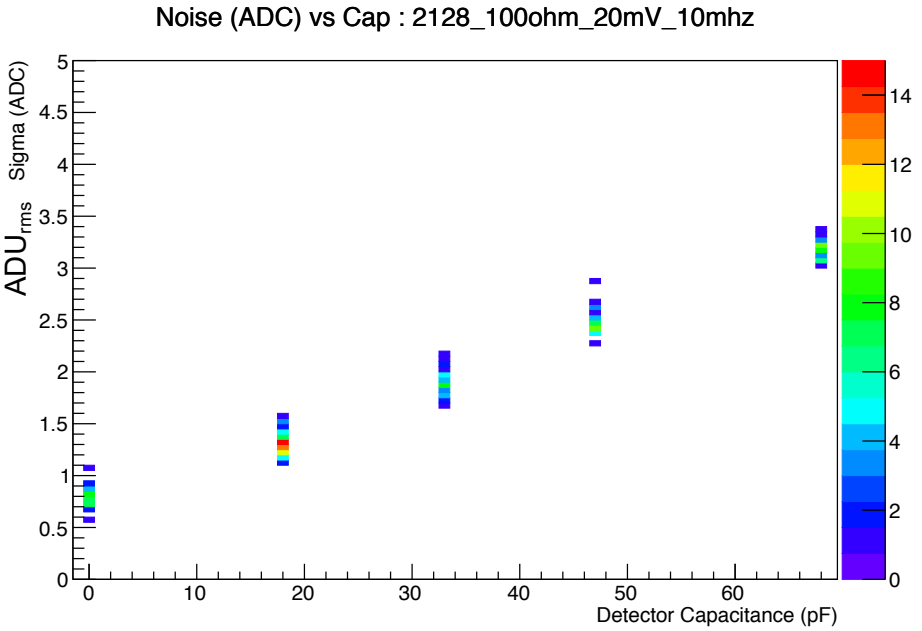


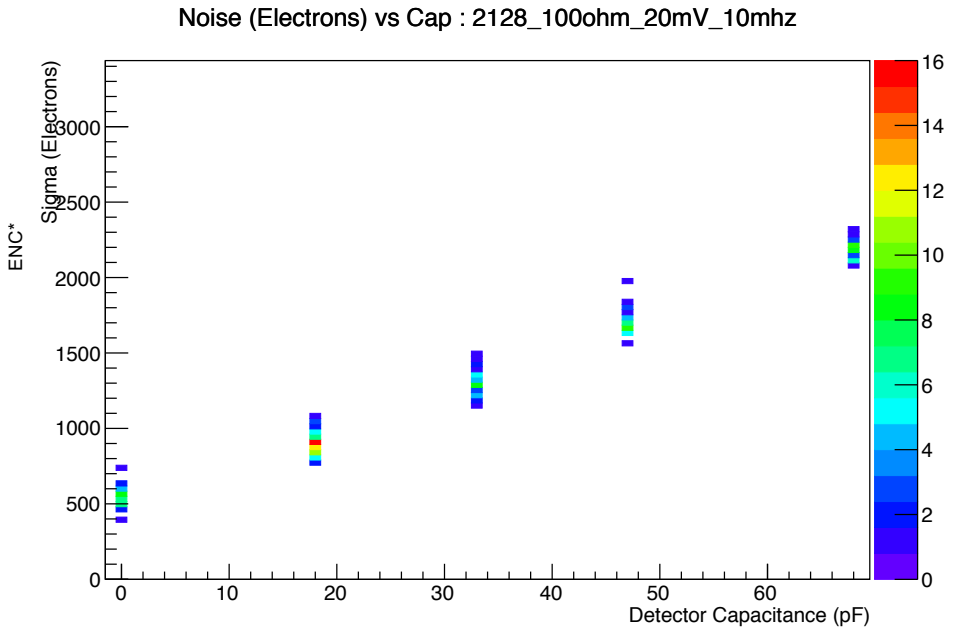
*) ENC calculated using nominal FE gain (20mV/fC) and nominal ADC conversion factor (2.15 mV/ADU)

Noise vs C_{det} (V3, 20N160)

Experimental conditions:
C_{det} scan
R_s=100Ω

20N160, chip V3 #2128



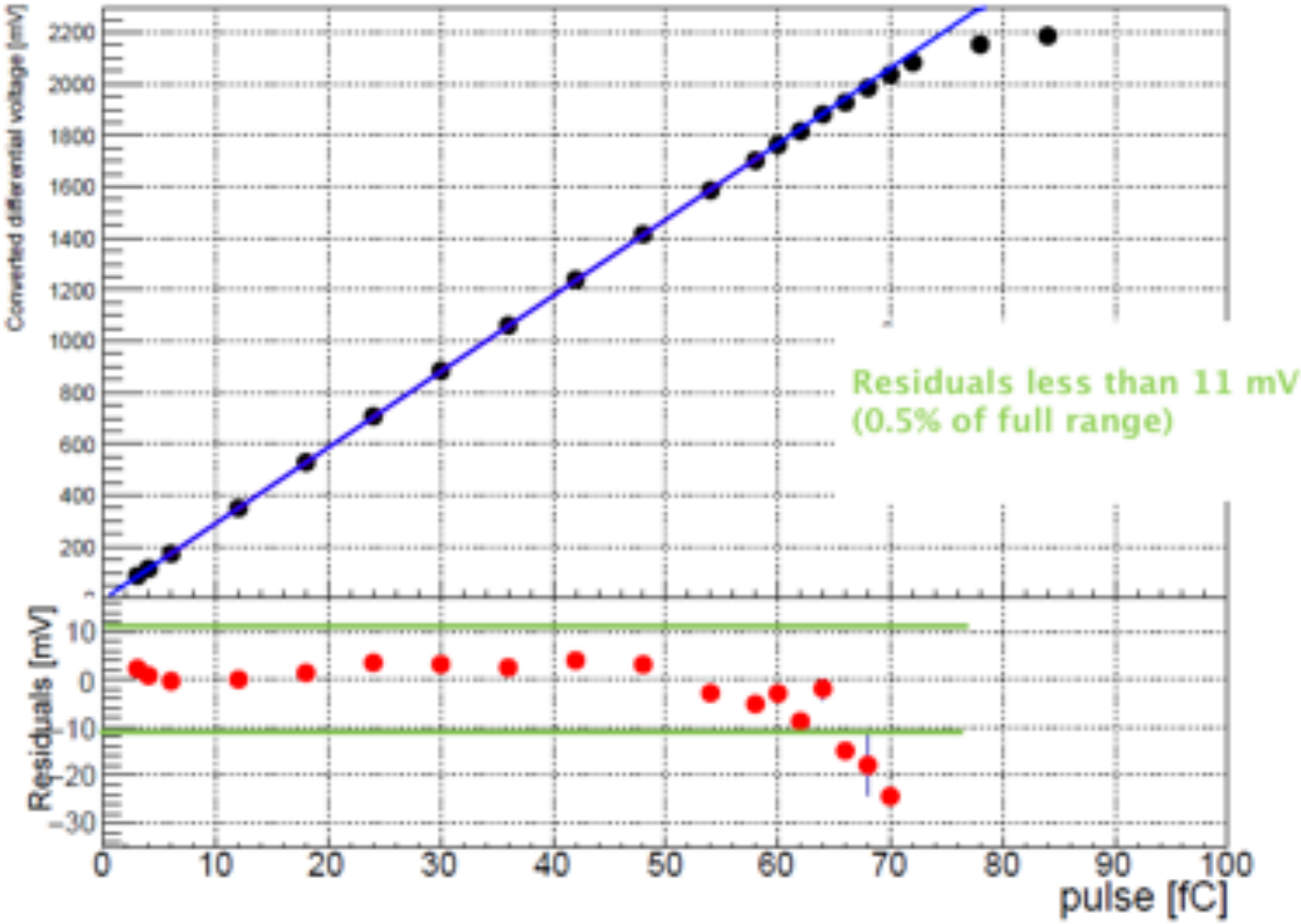


*) ENC calculated using nominal FE gain (20mV/fC)
and nominal ADC conversion factor (2.15 mV/ADU)

Sensitivity (gain)

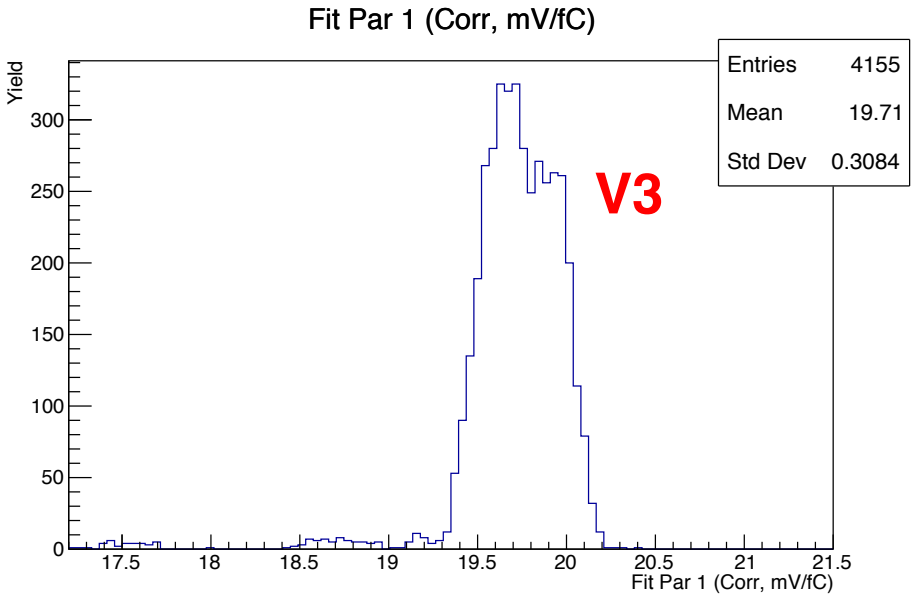
Linearity and Residual – an example

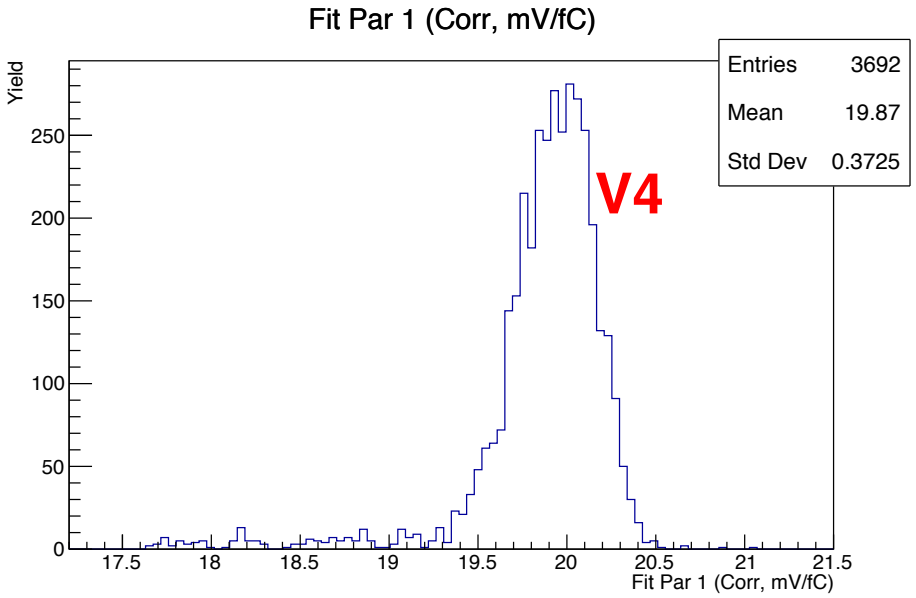
30N160



Gain (many chips)

Higher statistics for 20N160 configuration





Post layout simulations

SAMPA V3	15.8mV/fC (SFFS_80C)	18.4mV/fC	20.5mV/fC (FSSF_40C)
SAMPA V4	16.35mV/fC (SFFS_80C)	19.01mV/fC	21.17mV/fC (FSSF_80C)

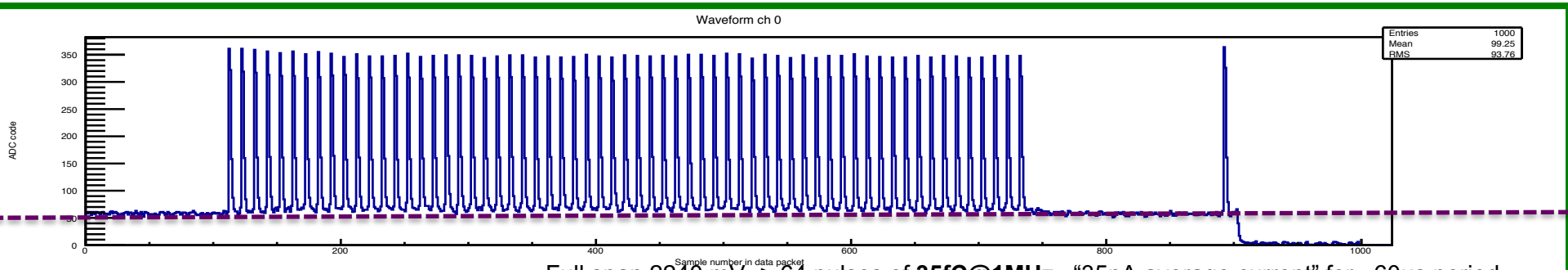
Linearity range, overview

- A calibration curve was performed for all channels of several chips
- The residuals* are very small (<10mV), for all channels, for a consistent part of the operational range:
  - 20N160: until ~95 fC ⇔ 1900 mV (>85% of the full range)
  - 30N160: until ~63 fC ⇔ 1900 mV (>85% of the full range)
  - 4P300: until ~480 fC ⇔ 1900mV (>85% of the full range)

* The curve used to calculate the residuals is the result of a linear fit in the central range (~15%-75%)

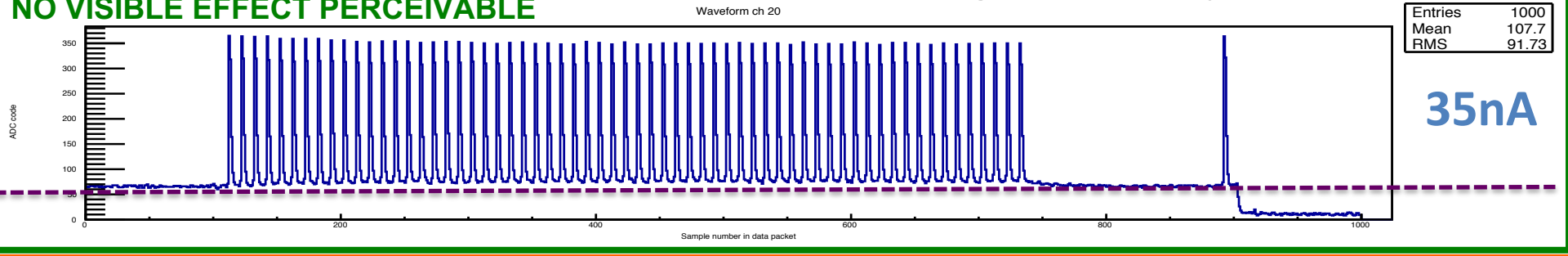
CSA robustness against Pile Up in SAMPA V4

Pile-up testing of a V4 chip

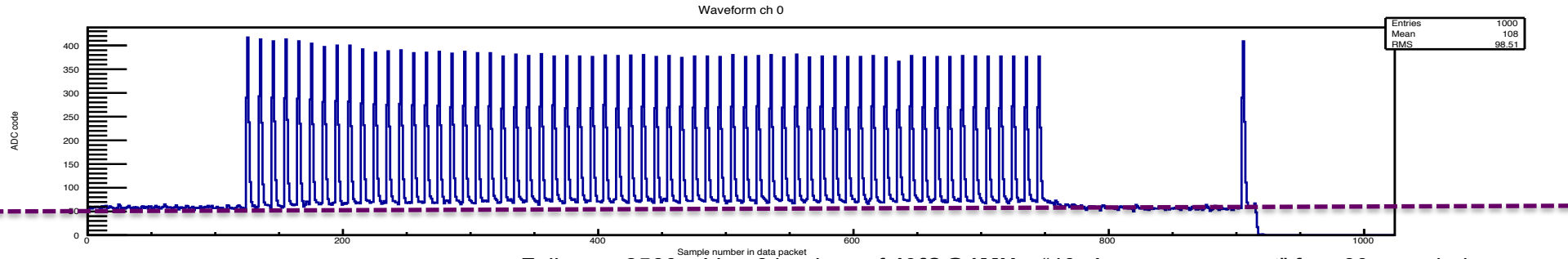


Full span 2240 mV -> 64 pulses of **35fC@1MHz**, “35nA average current” for ~60µs period

NO VISIBLE EFFECT PERCEIVABLE

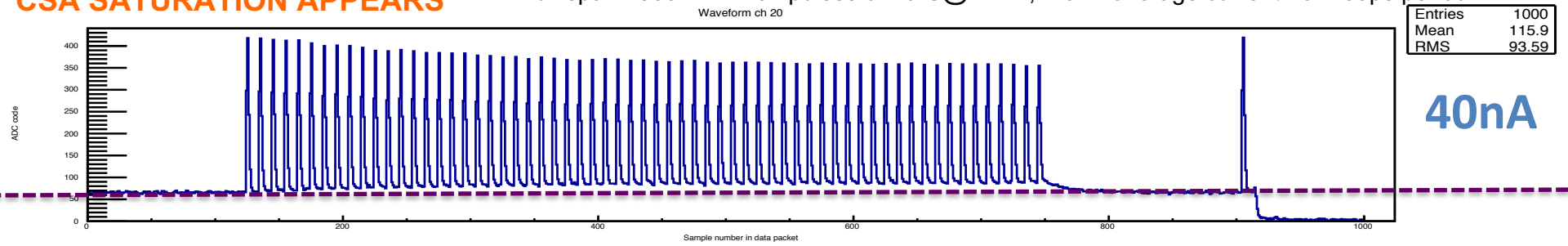


35nA



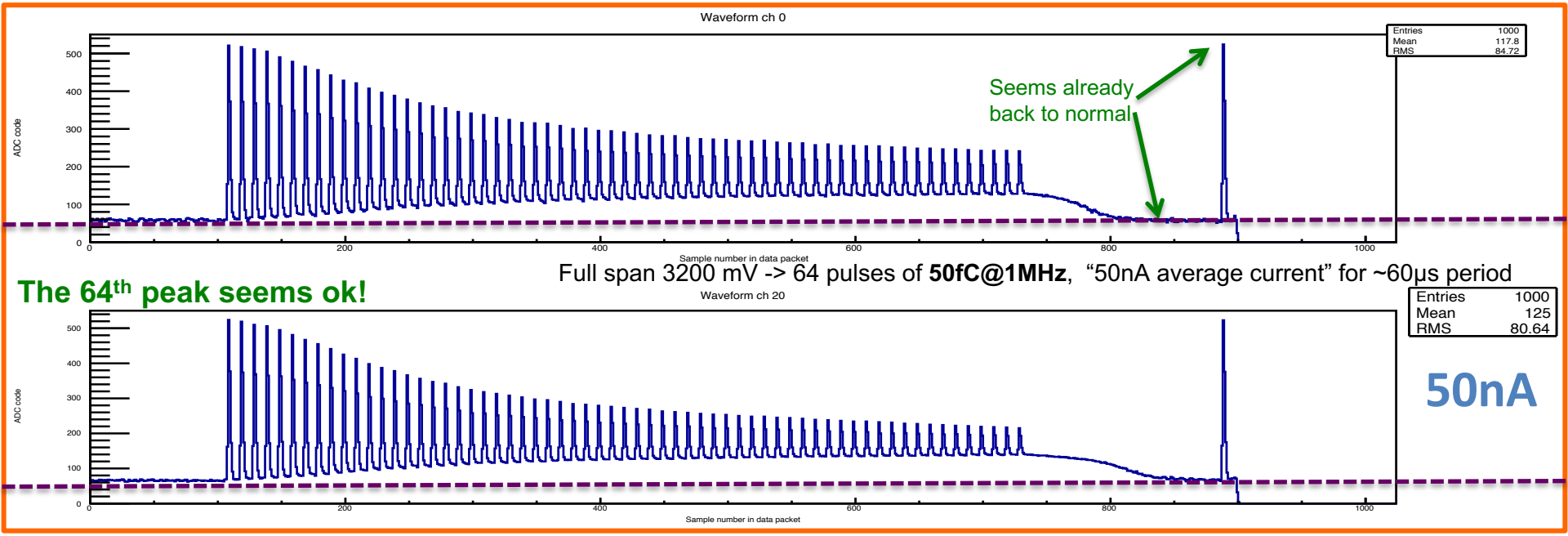
CSA SATURATION APPEARS

Full span 2560 mV -> 64 pulses of **40fC@1MHz**, “40nA average current” for ~60µs period



40nA

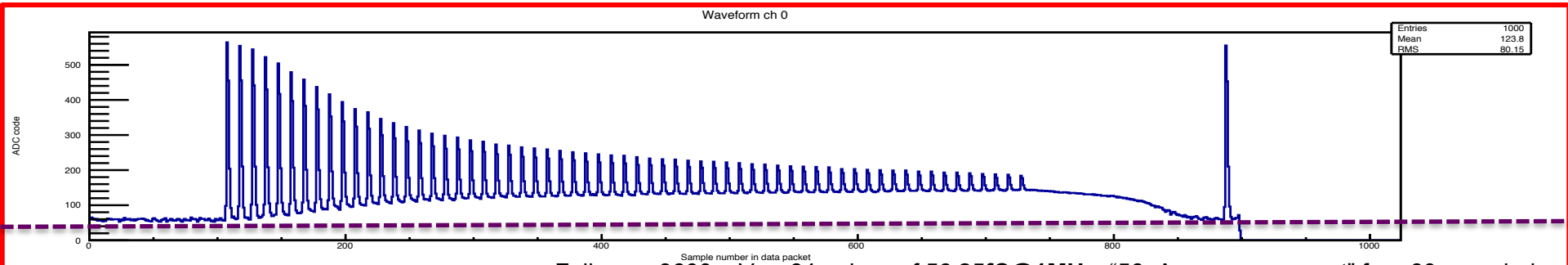
Going on: now really stressing a V4 chip



Full span 3200 mV -> 64 pulses of **50fC@1MHz**, "50nA average current" for ~60µs period

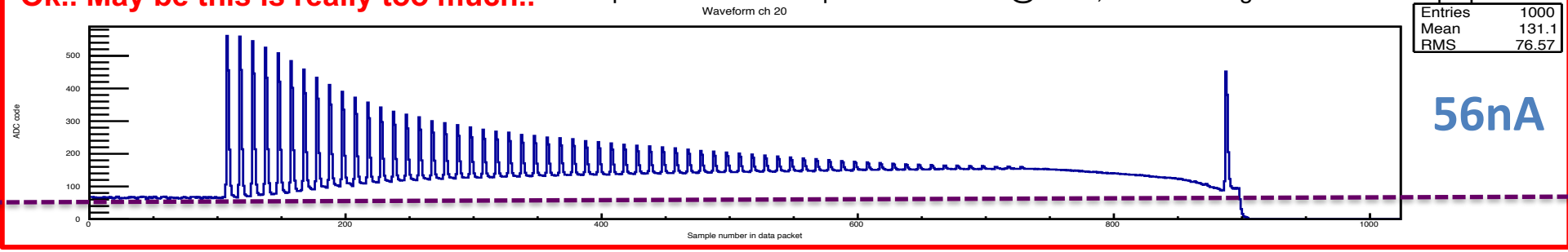
The 64th peak seems ok!

50nA



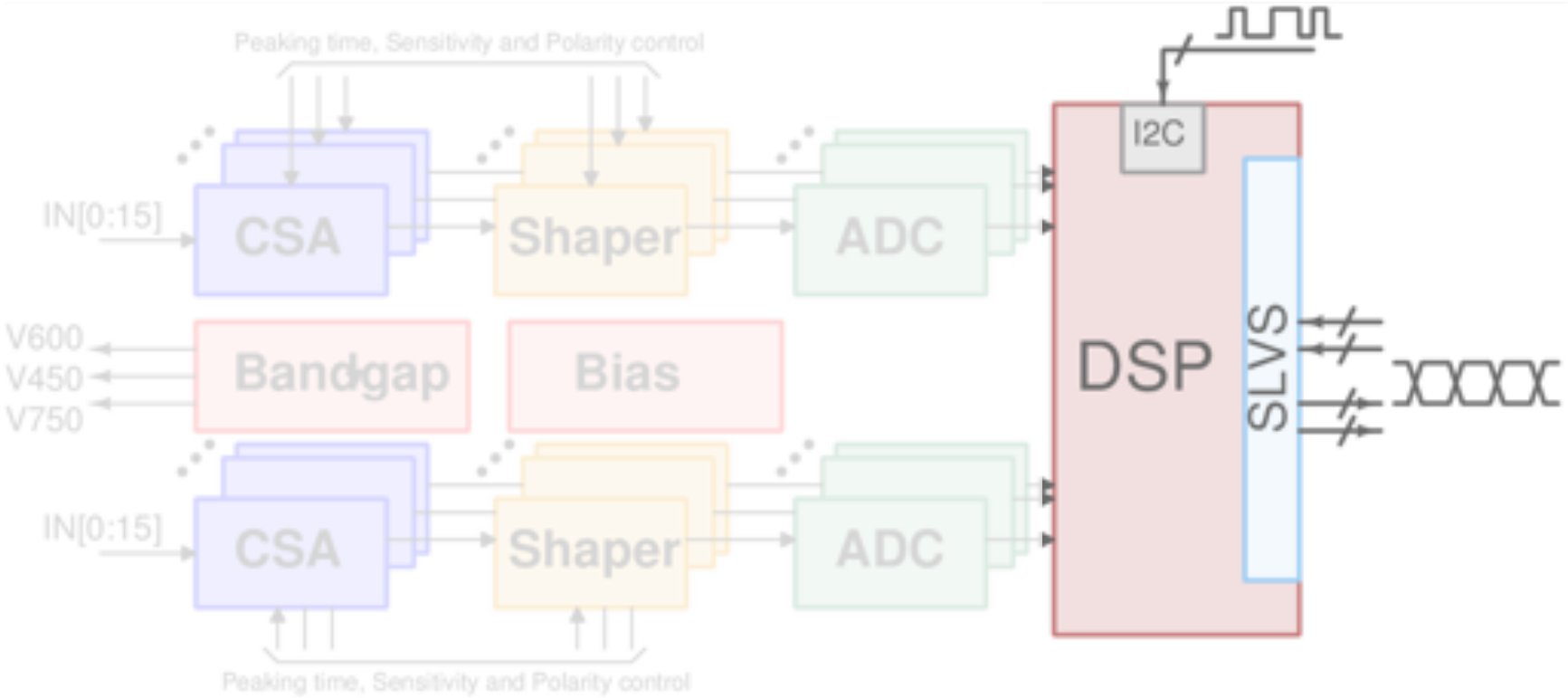
Ok.. May be this is really too much..

Full span 3600 mV -> 64 pulses of **56.25fC@1MHz**, "56nA average current" for ~60µs period



56nA

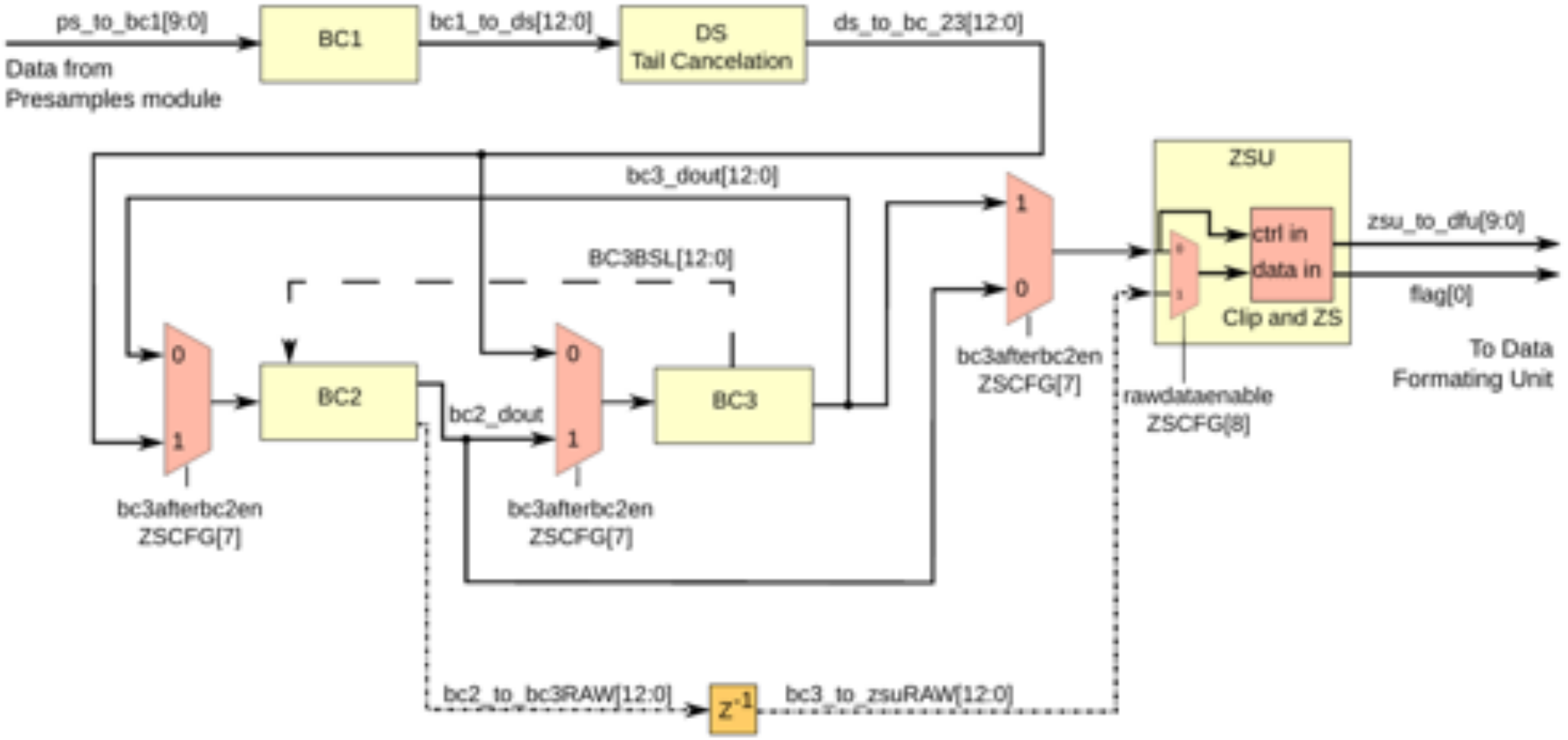
DSP


Peaking time, Sensitivity and Polarity control
IN[0:15]
CSA
Shaper
ADC
V600
V450
V750
Bandgap
Bias
IN[0:15]
CSA
Shaper
ADC
Peaking time, Sensitivity and Polarity control
I2C
DSP
SLVS

Top Level Functionality

- 4 primary filter blocks
  - Individual correction per channel
  - Baseline correction
    - 1 FIR filter
    - 1 Slope based filter
    - 1 IIR filter
    - Lookup table correction (Pedestal Memory) f(t);f(din)
    - Conversion f(din)
    - Fixed correction
  - Tail cancellation
    - 1 IIR filter

SAMPA Digital Filters Block Diagram



Top Level Functionality

- Compression
  - Zero suppression with run length encoding
    - Forward linked list for easier decoding
  - Cluster sum
    - Uses zero suppression with run length encoding , but sums cluster into 20bit word
  - Huffman
    - Differential encoded data
    - Programmable table of codes for +17 to -17
    - Values outside table have special Huffman code prepended to raw 10bit value

Top Level Functionality

- Configuration
  - –Configurable through I2C
  - –1 global register unit, 32 sets of channel registers
- Design for test
  - –JTAG boundary scan
  - –Built in memory tester
  - –Scan chain (on >98% of digital block flops)
- Strategies against to mitigate radiation effects
  - –TMR on almost all flip-flops
    - •except on part of data path
  - –Hamming protected headers

Readout

- Selectable number of serial links up to 11
  - 320/160/80Mbps
  - Channels distributed among links, no load sharing
  - Which channel goes to which link and in which order can be selected
  - Data is packet based (header + payload)
    - One packet per channel per event
- Event modes
  - Triggered
  - **Continuous**
  - Selectable event length up to 1024 samples
  - 192 pre-trigger samples

Readout

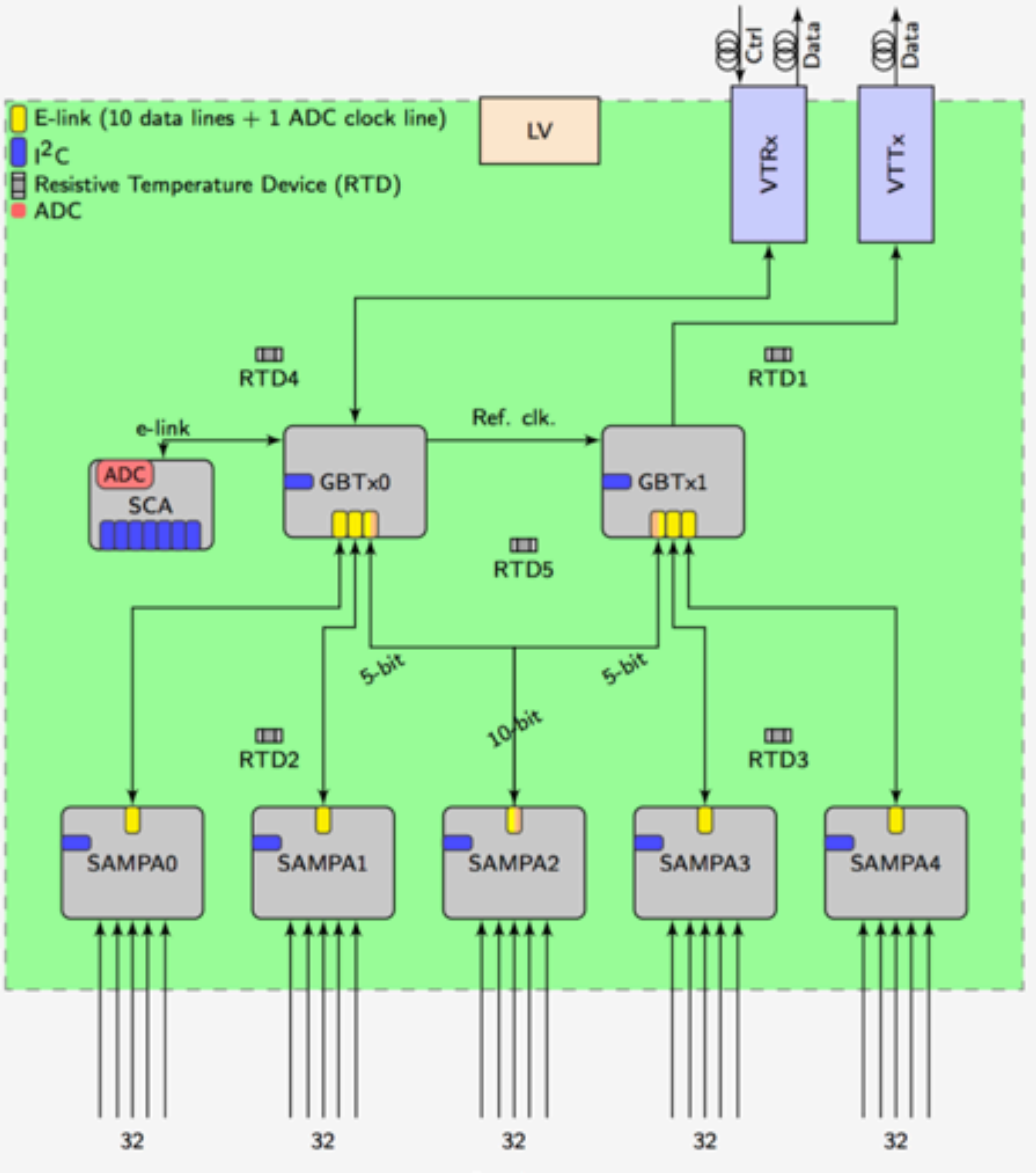
- Event buffer per channel
  - –6144(6K) words of compressed samples
  - –256 words of headers
  - –Header still created if data memory goes full (but data discharged)
- Daisy chain
  - –Multiple devices can share a single serial link to readout unit
  - –2K word buffer in the receiving side

Readout

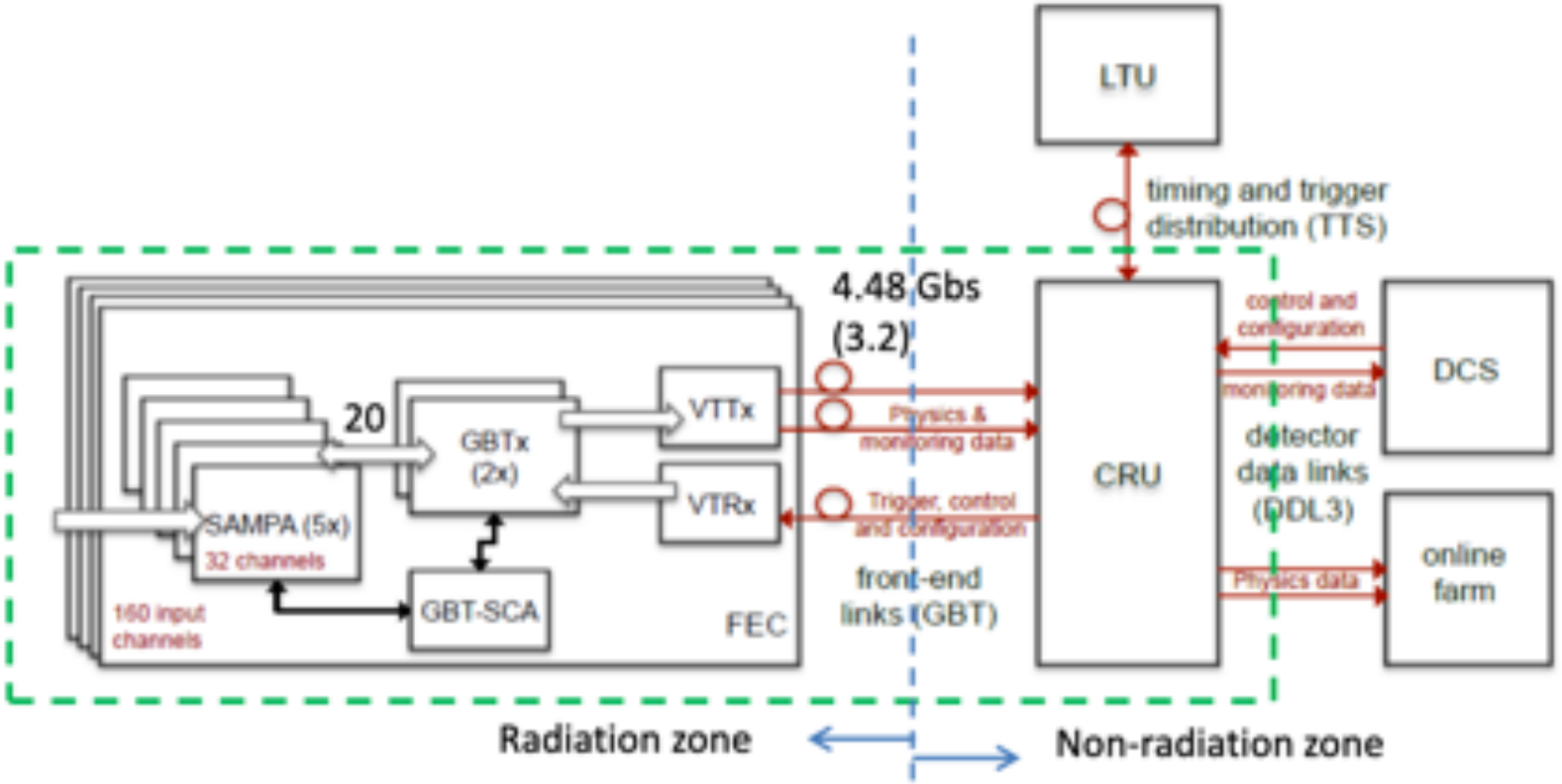
- Direct ADC serialization
  - Data serialized directly from ADC at 320Mbps rate over 10 links
  - Raw data, no filtering, no headers
  - Sync pattern on startup, receiver should maintain sync after that
  - Two modes
    - 10 bits is sent consecutively for channel 0-31 each 32xADC cycle
    - 5 lower bits, then 5 higher bits consecutively for channels 0-15 is sent on link 0-4 and for channels 16-31 on link 5-9
  - Clockgate the rest of the system to save power

SAMPA, how it is used: ALICE TPC

- 1 FrontEndCard reads 160 chs: 5 SAMPAs/FEC
- 2 GBTx chips to manage the communication (data multiplexing)
- Direct Serialization mode used



SAMPA, how it is used: ALICE TPC



FEC – Front End Card (160 ch / FEC)

CRU – Common Readout Unit (12 FECs / CRU = 1920 ch / CRU

DCS – Detector Control System

LTU – Local Trigger Unit

SAMPA ASIC overview summary

- SAMPA design was ALICE TPC/MCH driven
  - ASIC for gas detector readout (either “GEM-like”, electron collection, or “MWPC-like”, induced charge collection)
  - 4/20/30 mV/fC gain (500/100/66 fC range) provided
  - Digitalization @10MS/s

  Version V5: 80ns and 20MSps-optimized ADC developed & fabricated for sPHENIX, where configuration 4mV/fC & 300ns shaping was removed
- Several readout options available by the embedded DSP:
  - “raw data” (DSP-bypassed, no trigger, continuous read-out) possible up to ~10MSps
  - **Continuous** or triggered readout, framed data (DSP)
    - Filters available for baseline correction
    - Either ZeroSuppression or Huffman coding for data reduction
    - Possibility of Cluster_sum output and DaisyChain
    - I/O via I2C (settings) and up to eleven 320Mbps LVDS links
- Used in STAR TPC (in operation), ALICE TCP&MCH (in pre-commissioning), MPD@NICA TPC (advanced development), sPHENIX TPC (in construction), …

Future

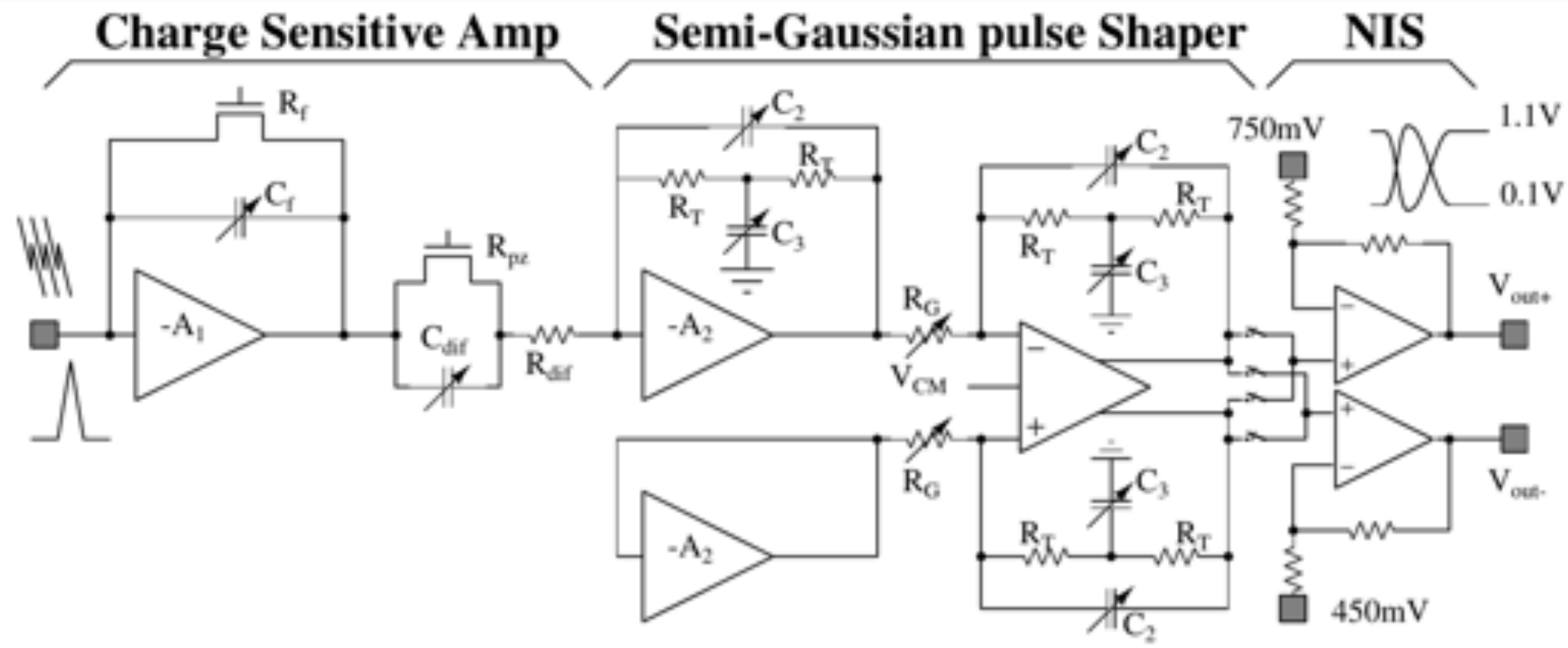
- Short term
  - Slightly modified SAMPA versions to better attend experiment specific needs (as recently done for sPHENIX) can be developed on request
- Continuous
  - Academic research about basic blocks for HE experiment ASICS
    - Different topologies and/or optimization for CSA, shaper, amplifier, ADC , TDC, ..
    - Studying the migration to more advanced processes
- Middle term
  - Physicists of the local group are interested in LGAD sensors, so, having a R&D for electronics to be coupled do this type of sensor is presently being discussed in the SAMPA team.
- Always
  - Part of the team is project-based, so we need a continuous flux of projects to keep the team together
  - Therefore, open to new challenges and collaborations/partnerships

Thanks!

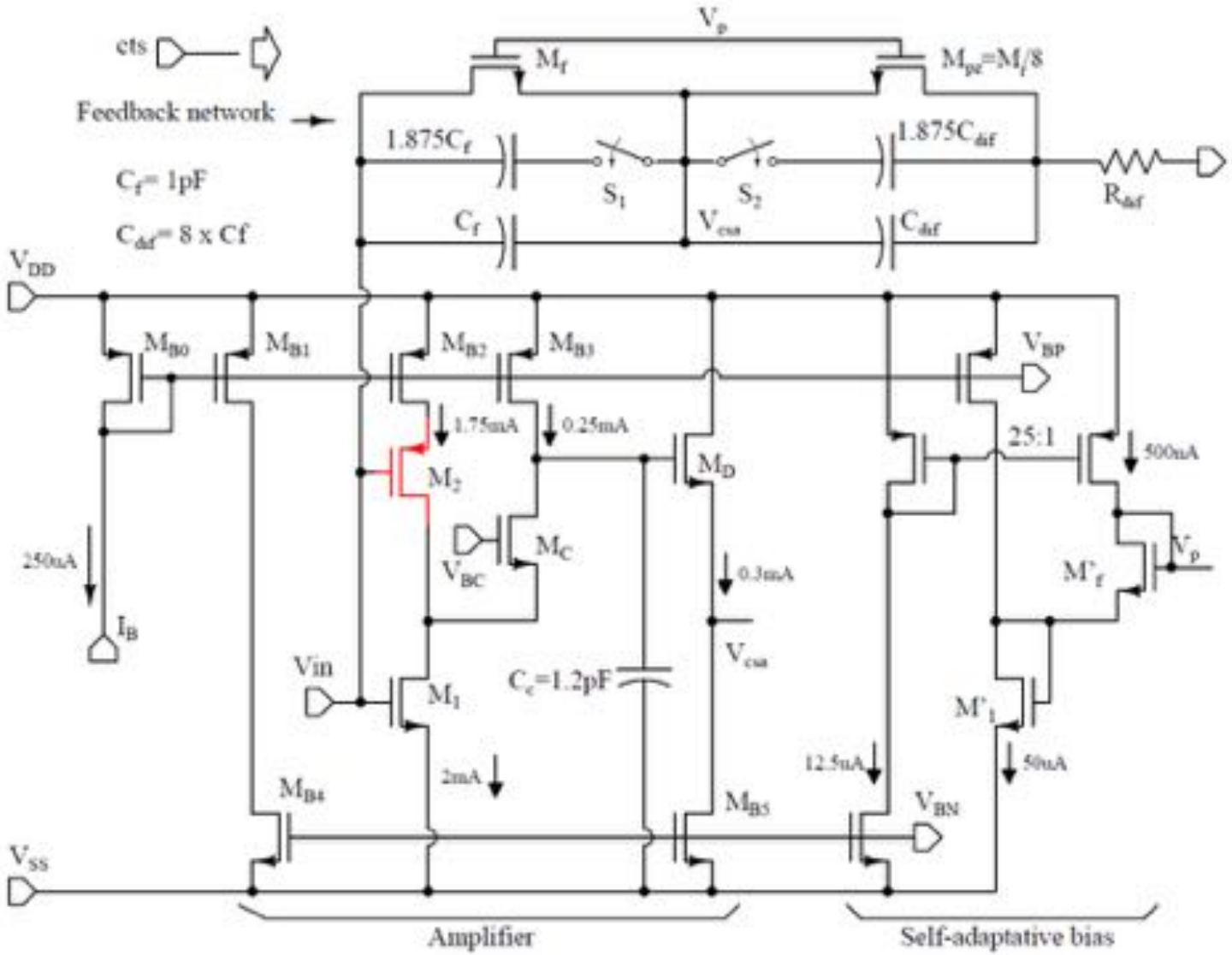
More information

BackUp Slides

SAMPA : CSA + Shaper

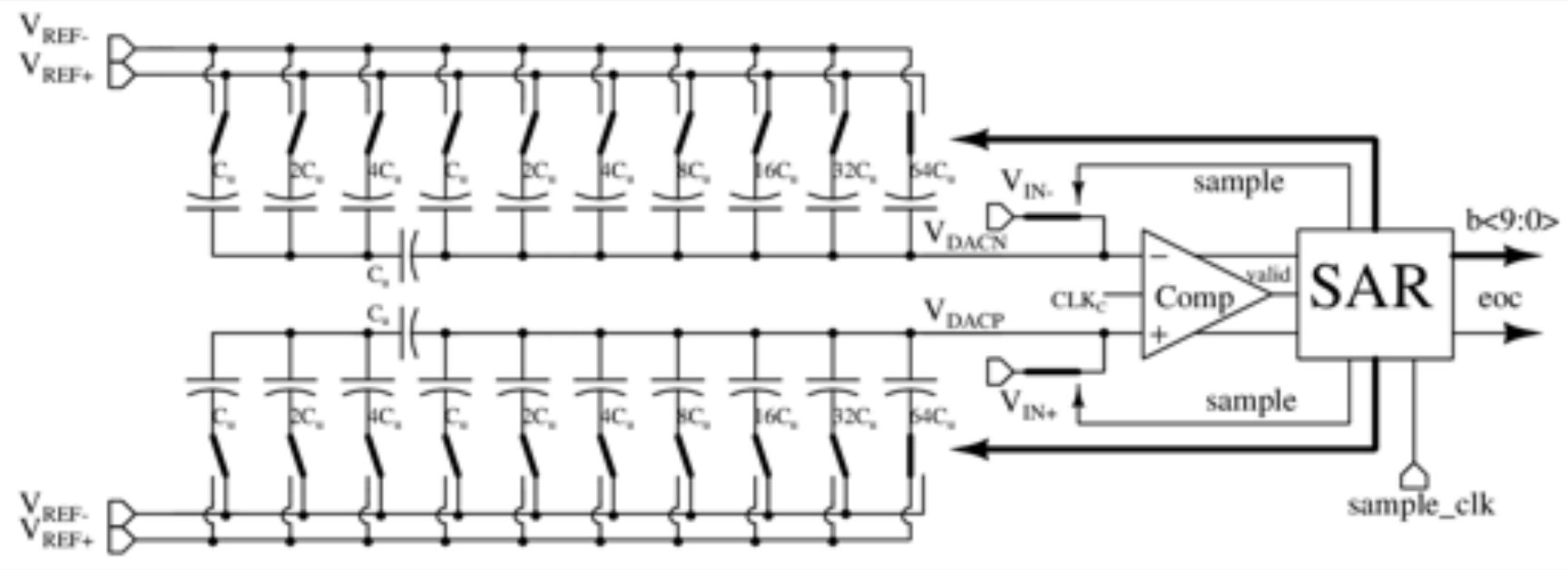


Transistor level schematic of the CSA



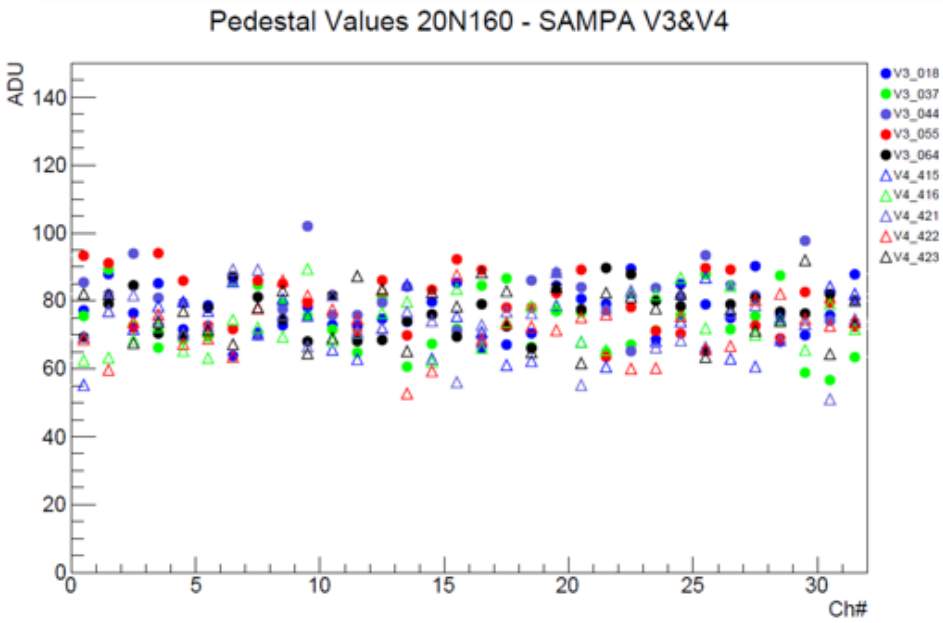
SAMPA : ADC

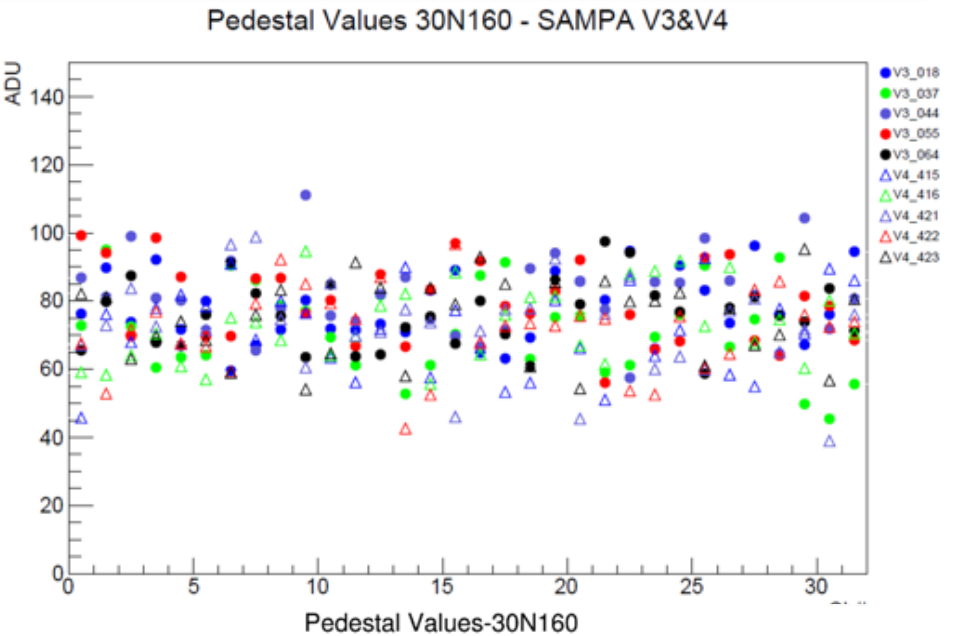
- SAR ADC: 80MHZ (Conversion clock) and 10MHz (Sampling Clock)

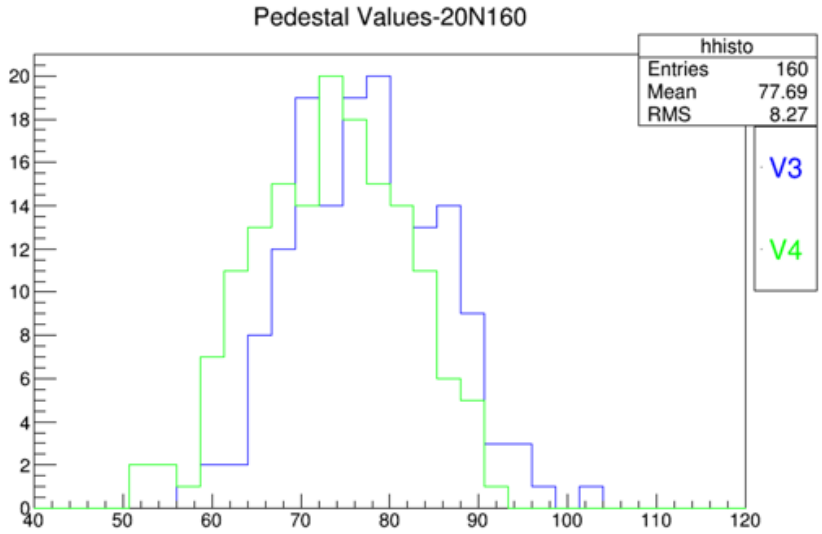


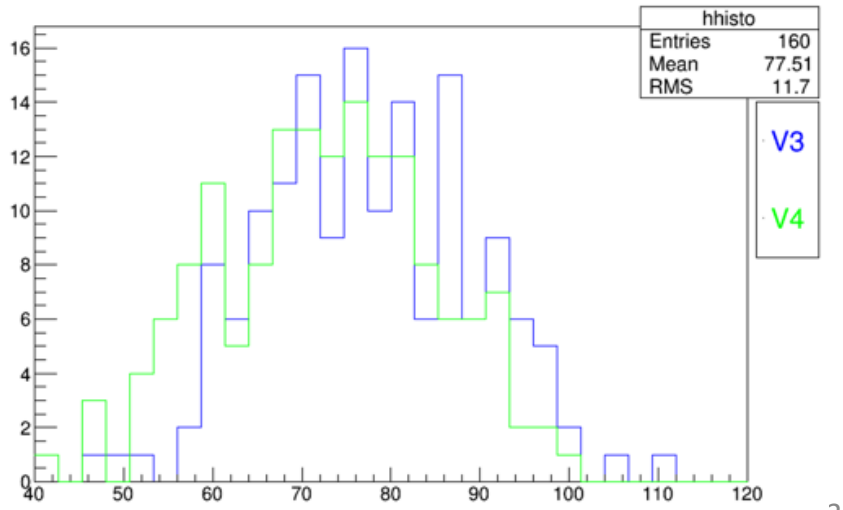
Pedestal (baseline)

SAMPA V3/V4 Baseline Measurements





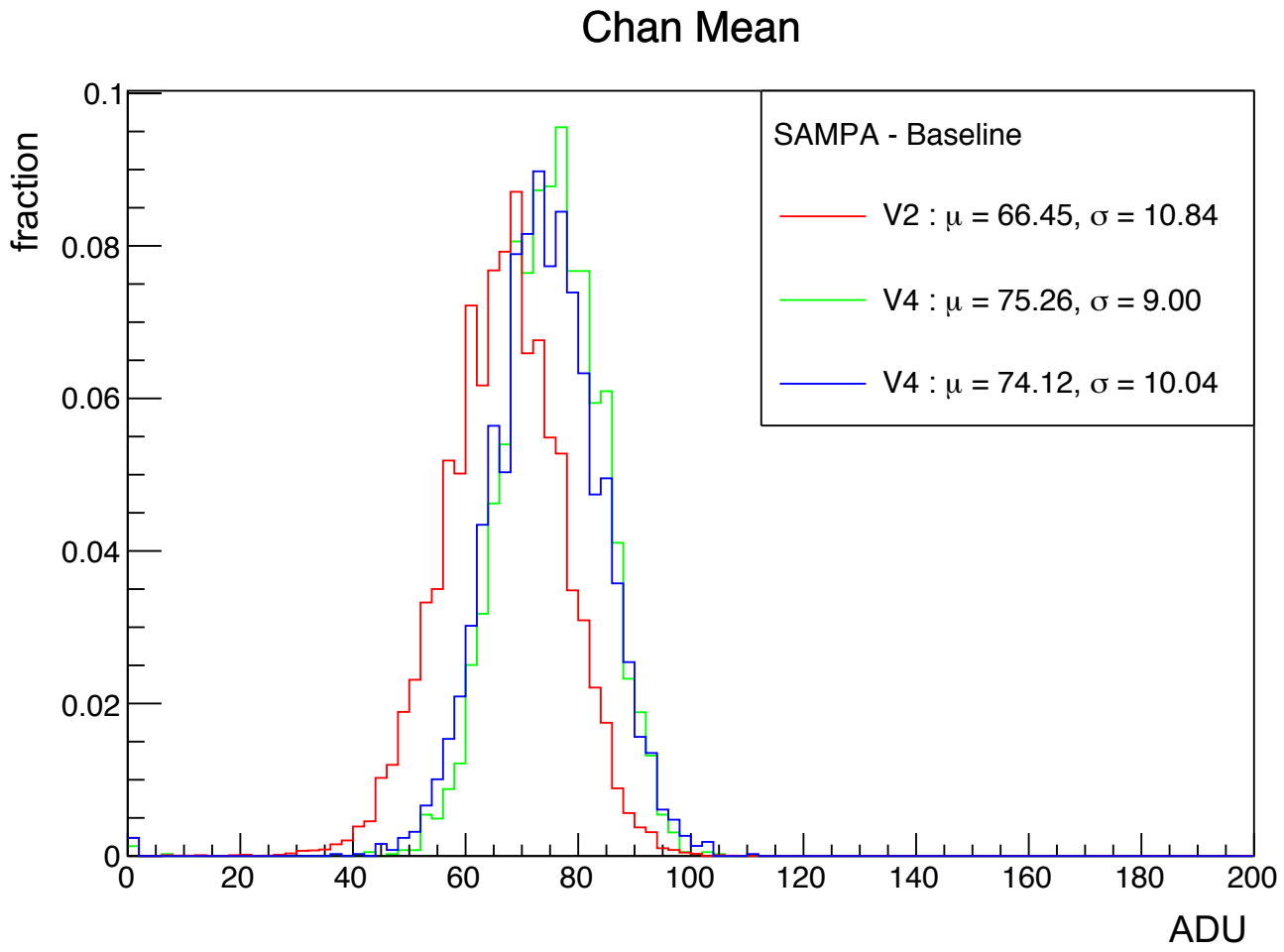




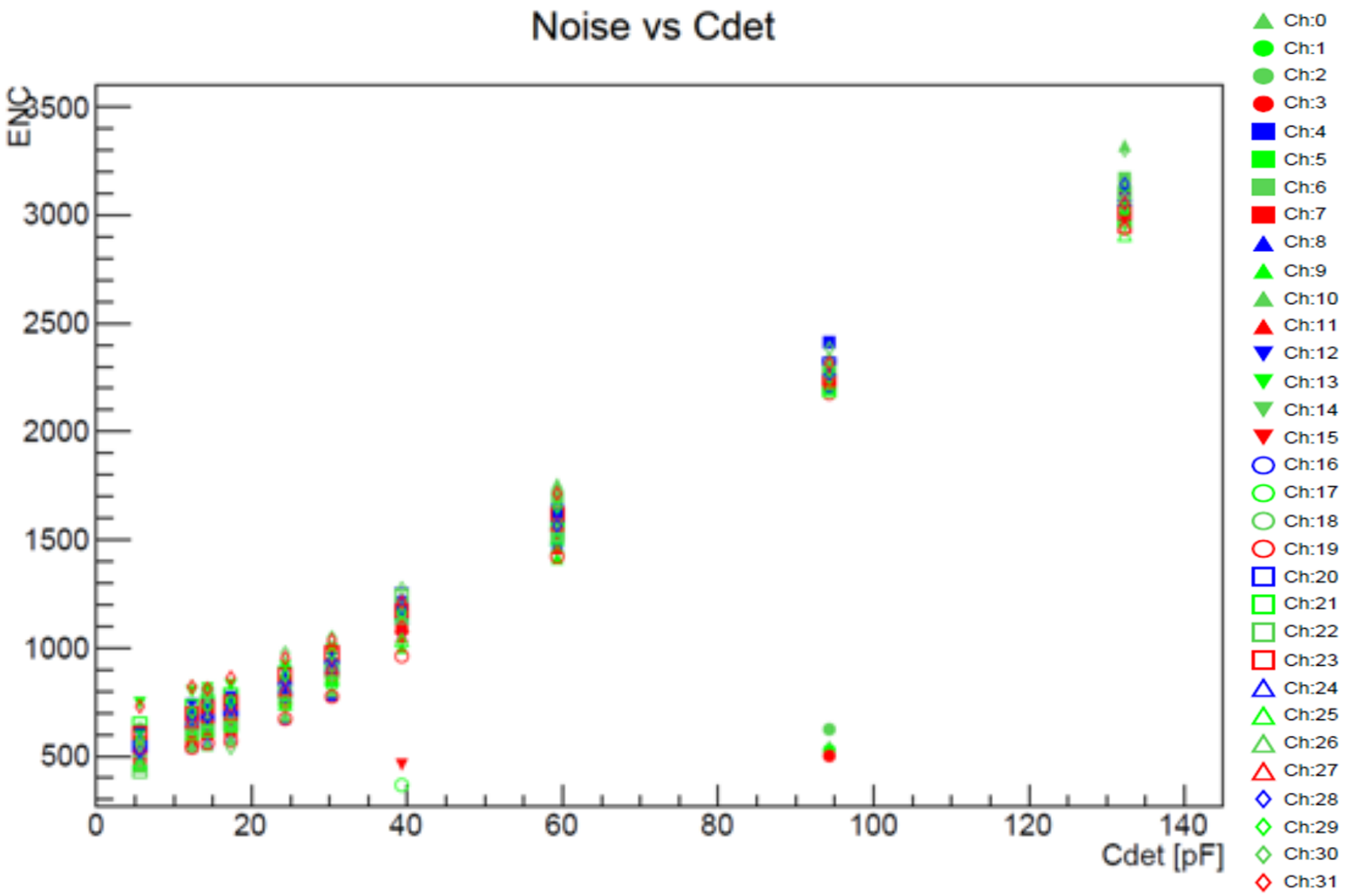
Baseline (many chips)

Baseline values for all channels for many V2 and V3 and V4 chips (at 0 pF and 0 Ohm):

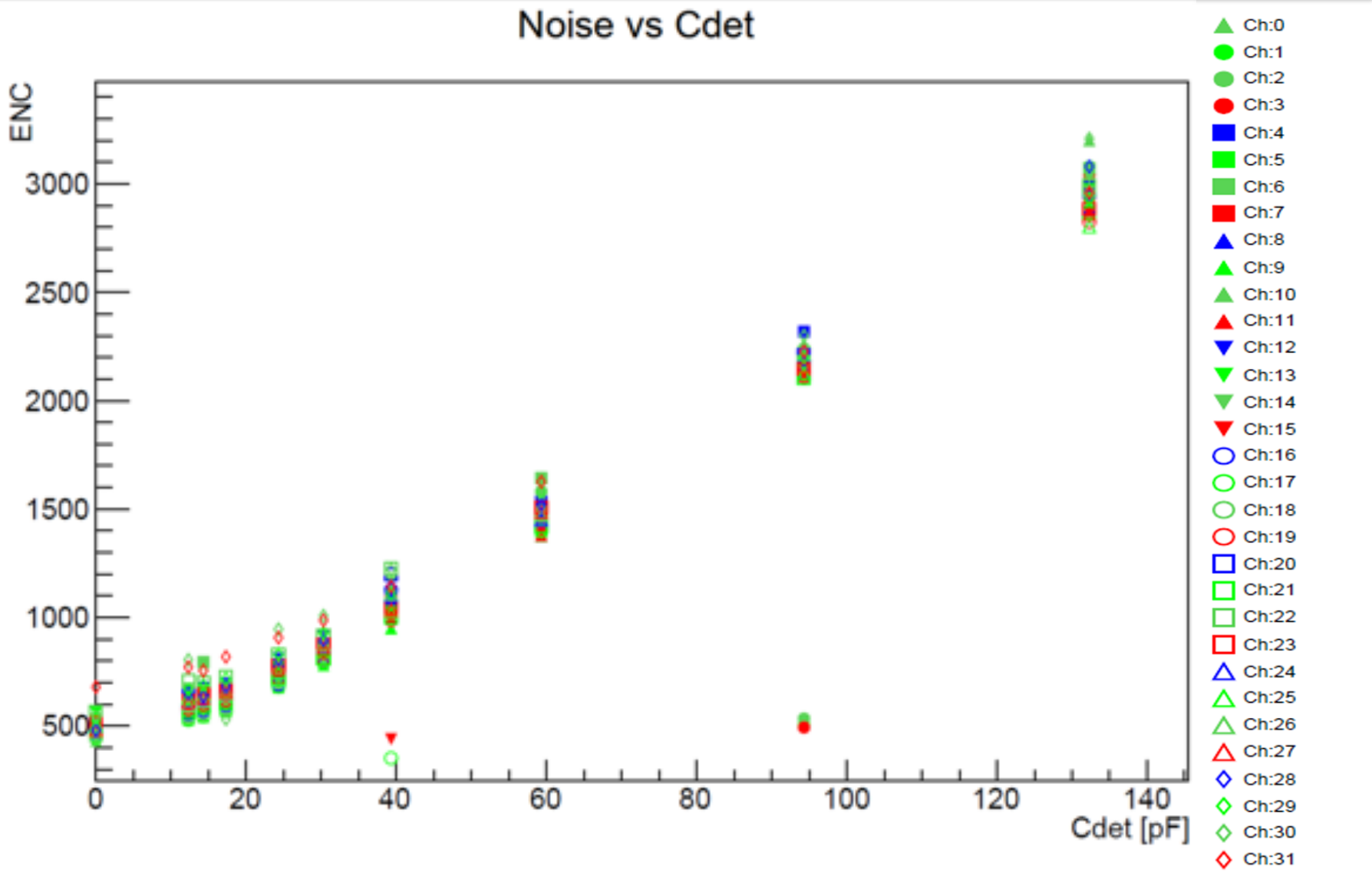
20N160



Noise, TPC 20N160 - SAMPLE 057



Noise, TPC 30N160 - SAMPLE 057



How to emulate a burst of charge pulses

”stairs-shaped waveform”, 63 steps, 1µs apart, + a last one after ~16µs, applied via series C_{inj}