



sPHENIX INTT

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First real module in Taiwan



2020/06/04

First real module assembled by TW-sPHENIX : pre-production 001



To do list : encapsulated glue

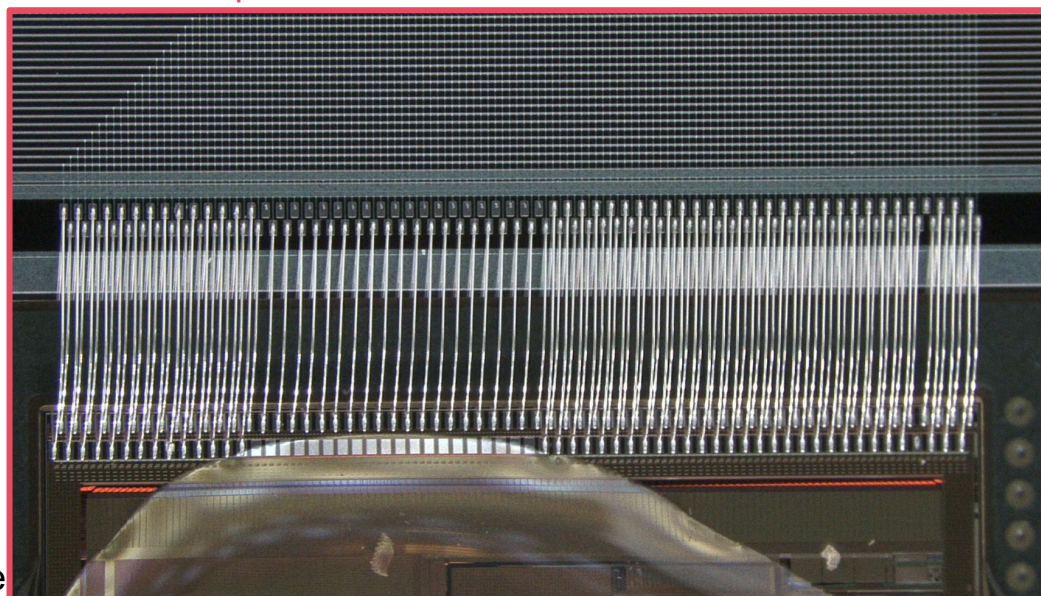
U2 : 21 error pads

20 channels are covered by glue

17 channels can not be bonded

Total : 37 error pads

Bonding performance : 98.9%



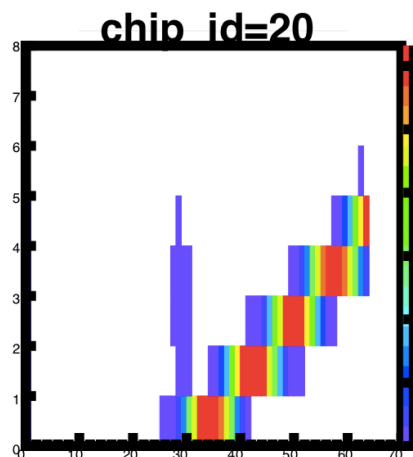
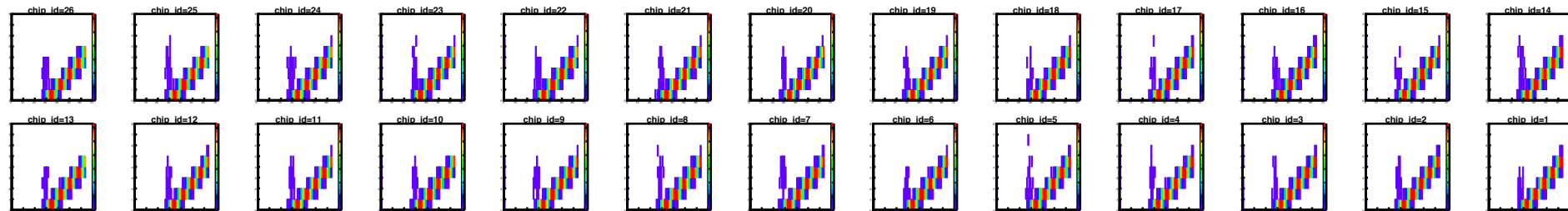
Bonding pads overlapped with glue



Calibration test : pre-production 001



(only 26 chips and pre -production HDI)
without bias voltage (data : fphx_raw_20200601-1214_0.dat)



Zoom in example

Gsel : 2

The threshold setting on the GUI in NCU TestBench

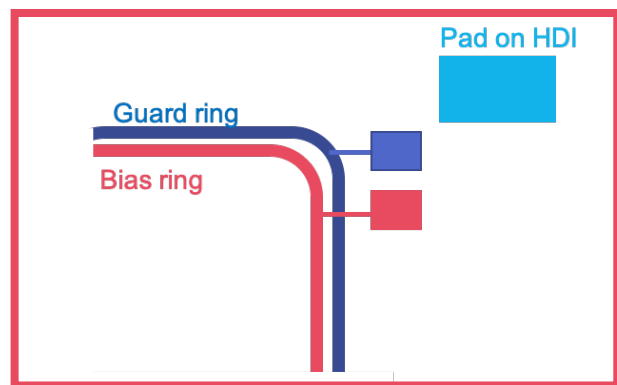
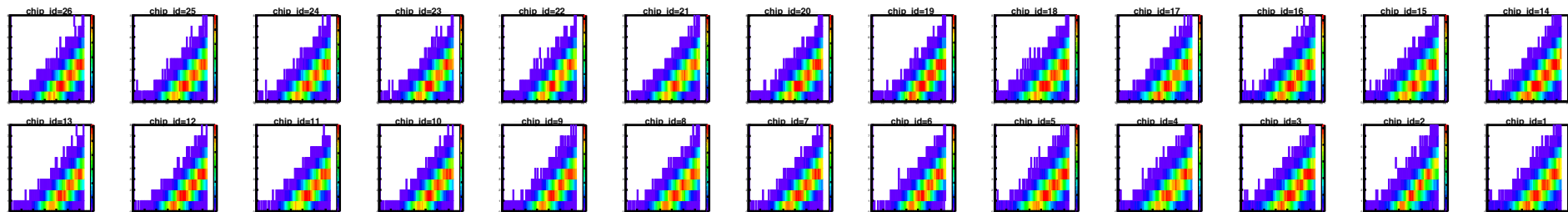
DAC0	20	Read	Write	Set	Reset	Default
DAC1	25	Read	Write	Set	Reset	Default
DAC2	30	Read	Write	Set	Reset	Default
DAC3	35	Read	Write	Set	Reset	Default
DAC4	40	Read	Write	Set	Reset	Default
DAC5	45	Read	Write	Set	Reset	Default
DAC6	50	Read	Write	Set	Reset	Default
DAC7	55	Read	Write	Set	Reset	Default



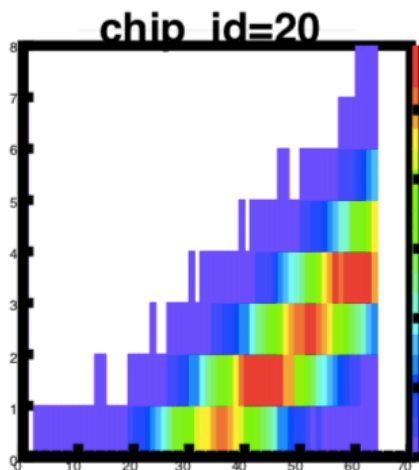
Calibration test : pre-production 001



(sensor type A and B, 26 chips and pre-production HDI)
without bias voltage (data : fphx_raw_20200608-1733_0.dat)



Bonding missing



Zoom in example

Gsel : 2

The threshold setting on the GUI in NCU TestBench

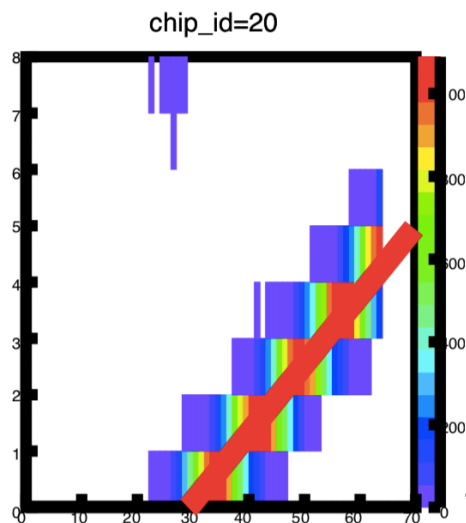
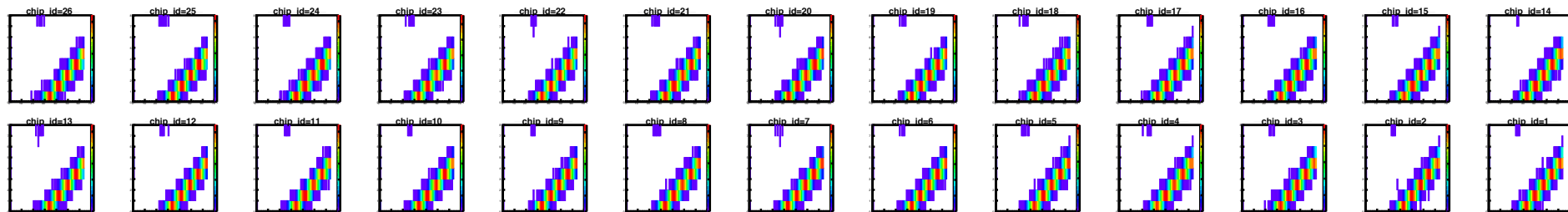
DAC0	20	Read	Write	Set	Reset	Default
DAC1	25	Read	Write	Set	Reset	Default
DAC2	30	Read	Write	Set	Reset	Default
DAC3	35	Read	Write	Set	Reset	Default
DAC4	40	Read	Write	Set	Reset	Default
DAC5	45	Read	Write	Set	Reset	Default
DAC6	50	Read	Write	Set	Reset	Default
DAC7	55	Read	Write	Set	Reset	Default



Calibration test : pre-production 001



(sensor type A and B, 26 chips and pre -production HDI)
 With bias voltage (+50V) (data : fphx_raw_20200609-2023_0.dat)



Zoom in example

Gsel : 2

The threshold setting on the GUI in NCU TestBench

DAC0	20	Read	Write	Set	Reset	Default
DAC1	25	Read	Write	Set	Reset	Default
DAC2	30	Read	Write	Set	Reset	Default
DAC3	35	Read	Write	Set	Reset	Default
DAC4	40	Read	Write	Set	Reset	Default
DAC5	45	Read	Write	Set	Reset	Default
DAC6	50	Read	Write	Set	Reset	Default
DAC7	55	Read	Write	Set	Reset	Default

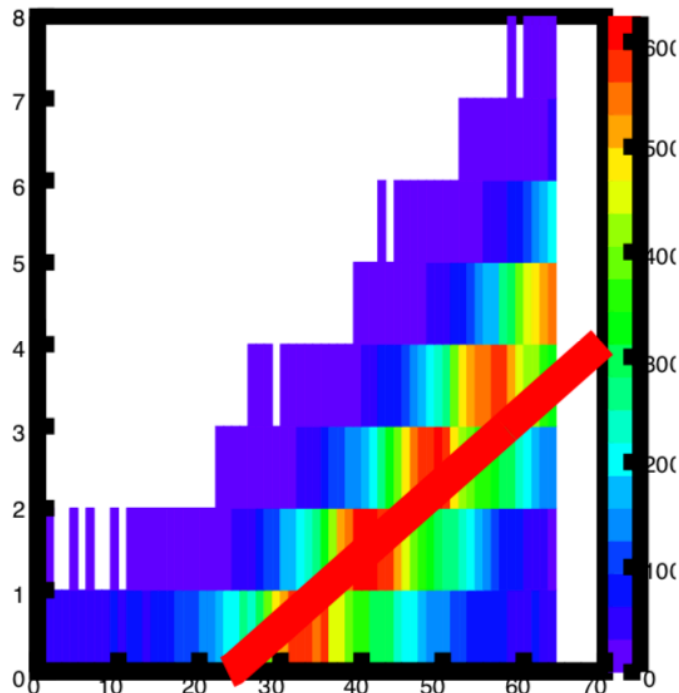


Calibration test, slope comparison: pre-production 001



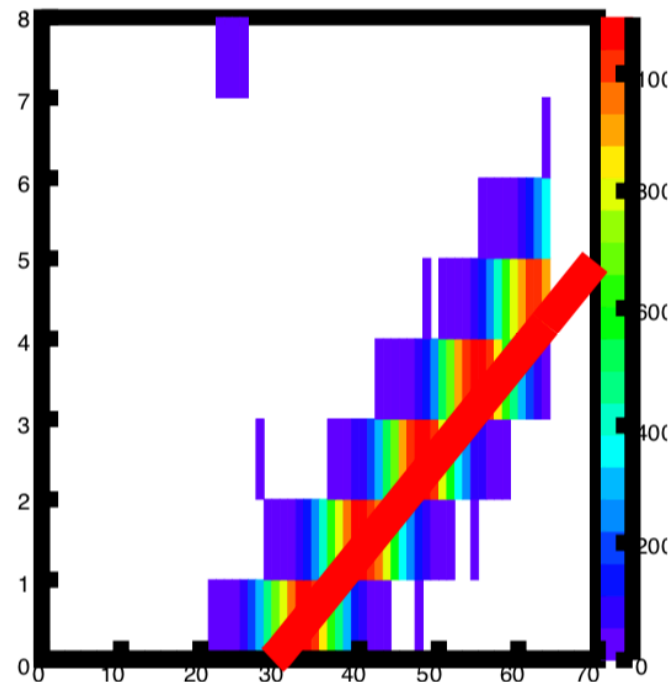
Gsel : 2

Without bias voltage
chip_id=2



slope : **0.0827**,
offset : -1.632,
chi2/NDF : 167.29

With bias voltage (+50 V)
chip_id=2



slope : **0.1304**,
offset : -3.663,
chi2/NDF : 81.64

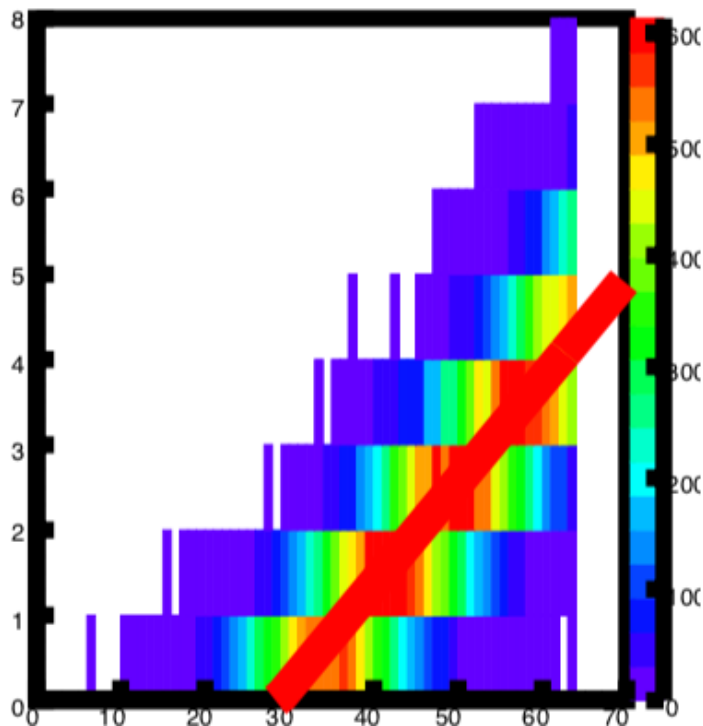


Calibration test, slope comparison: FVTX (B295)



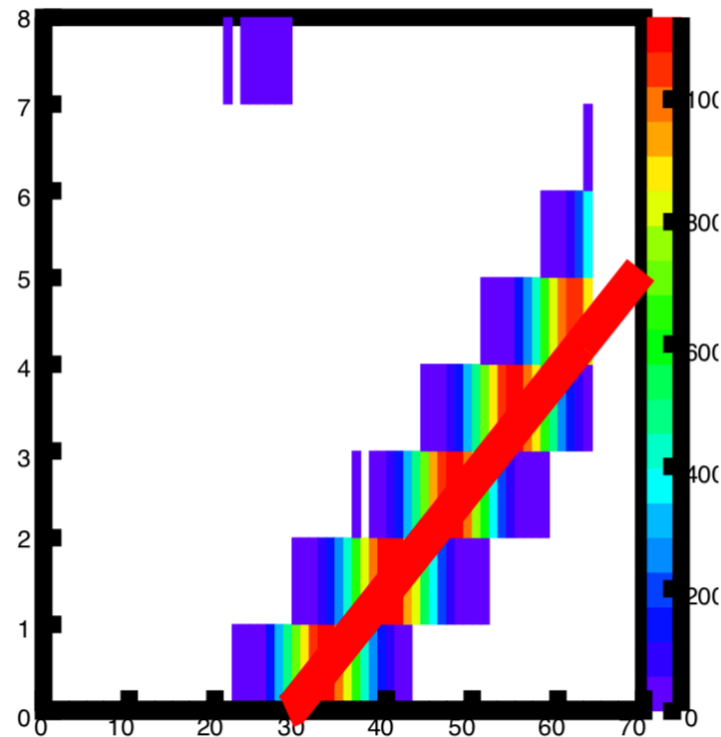
Gsel : 2

Without bias voltage
chip_id=2



slope : **0.1066**,
offset : -2.700,
chi2/NDF : 127.11

With bias voltage (+50 V)
chip_id=2



Slope : **0.1298**,
offset : -3.627,
chi2/NDF : 102.60

The slope of FVTX and INTT module with the bias voltage seems to be similar



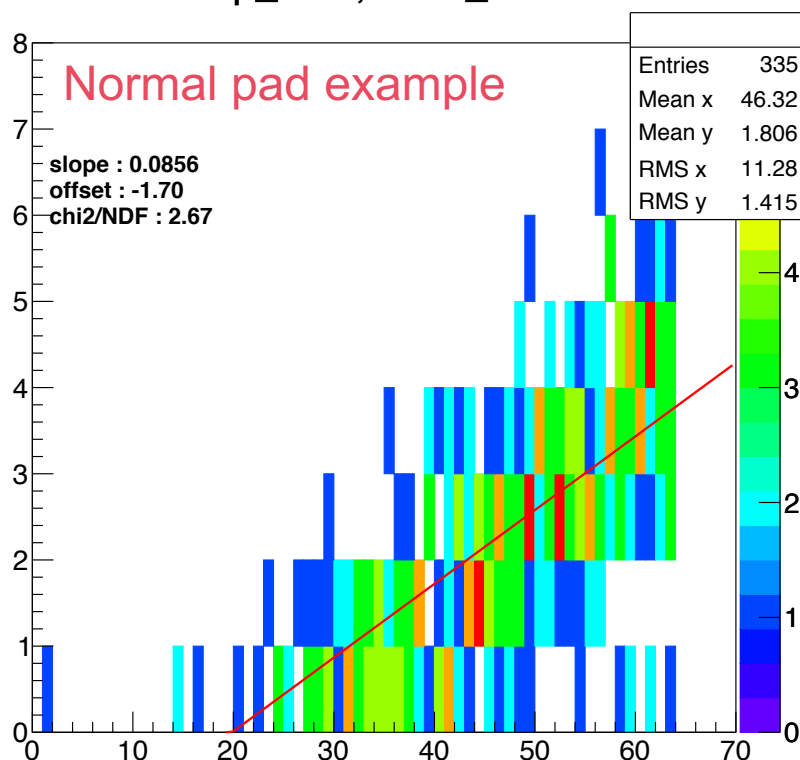
Assembly performance check : pre-production 001



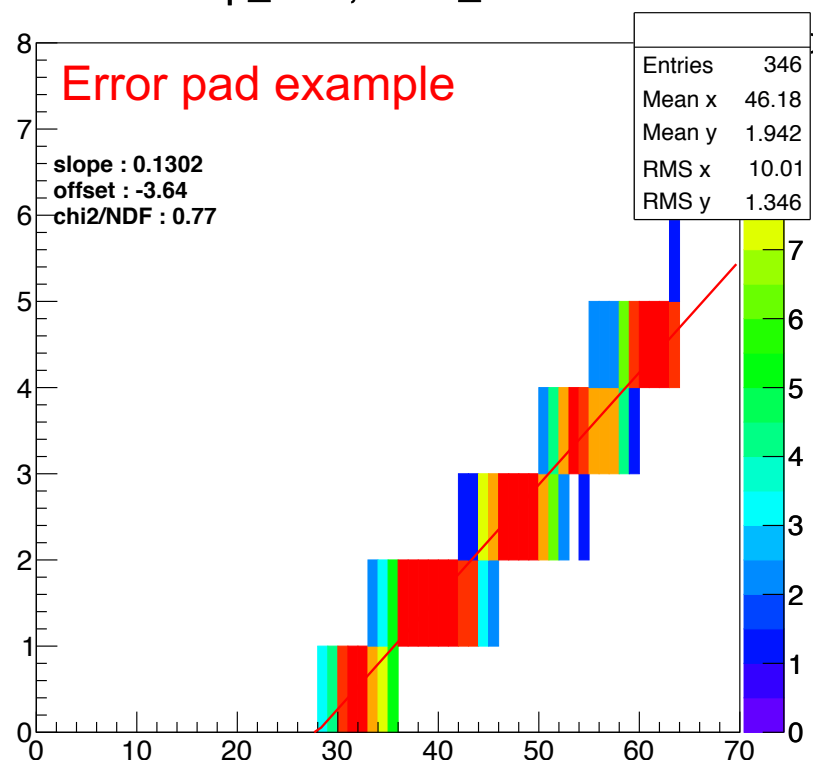
Without bias voltage

Ampl - ADC check, channel to channel

chip_id=2, chan_id = 0



chip_id=2, chan_id = 28



Error pad check : self - comparison



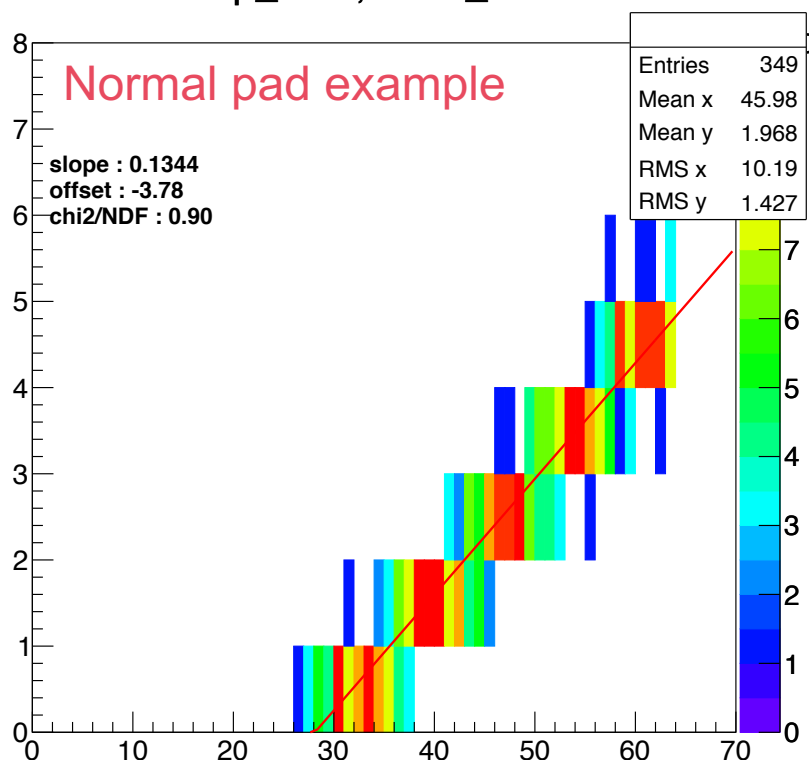
Assembly performance check : pre-production 001



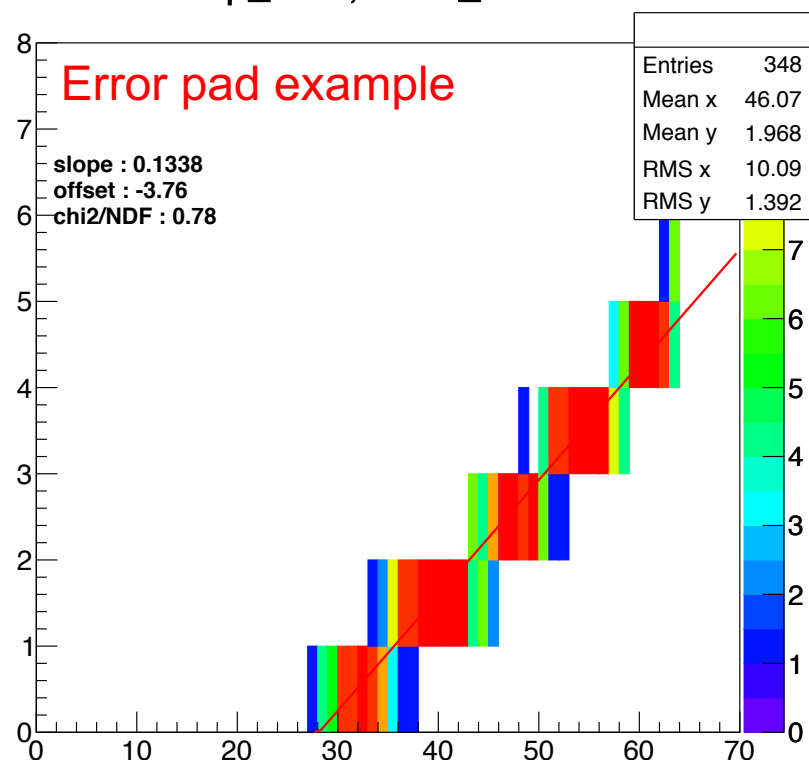
With bias voltage (+50V)

Ampl - ADC check, channel to channel

chip_id=2, chan_id = 0



chip_id=2, chan_id = 28



Error pad check : slope subtraction

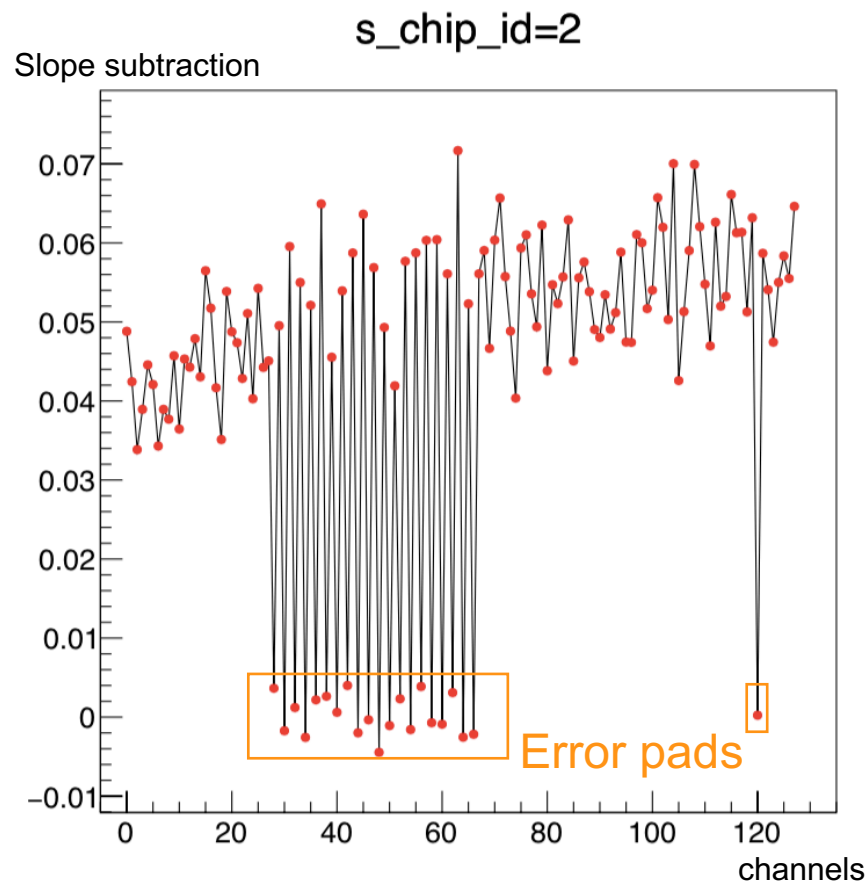
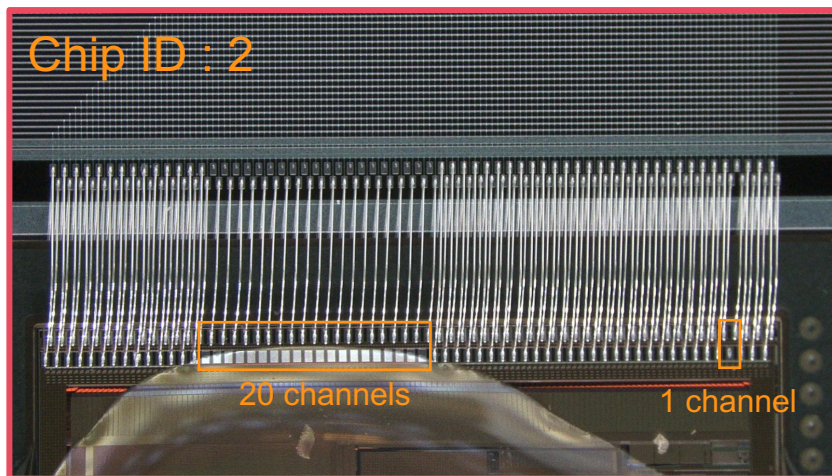


Assembly performance check : pre-production 001



U2 : 21 error pads

	error pad		error pad
U1		U14	79
U2	68,95~114	U15	
U3		U16	22,111
U4		U17	3,99,102
U5		U18	
U6		U19	
U7		U20	
U8		U21	
U9	76,96,115	U22	40,115,116,118
U10		U23	42,109
U11		U24	76
U12		U25	
U13		U26	

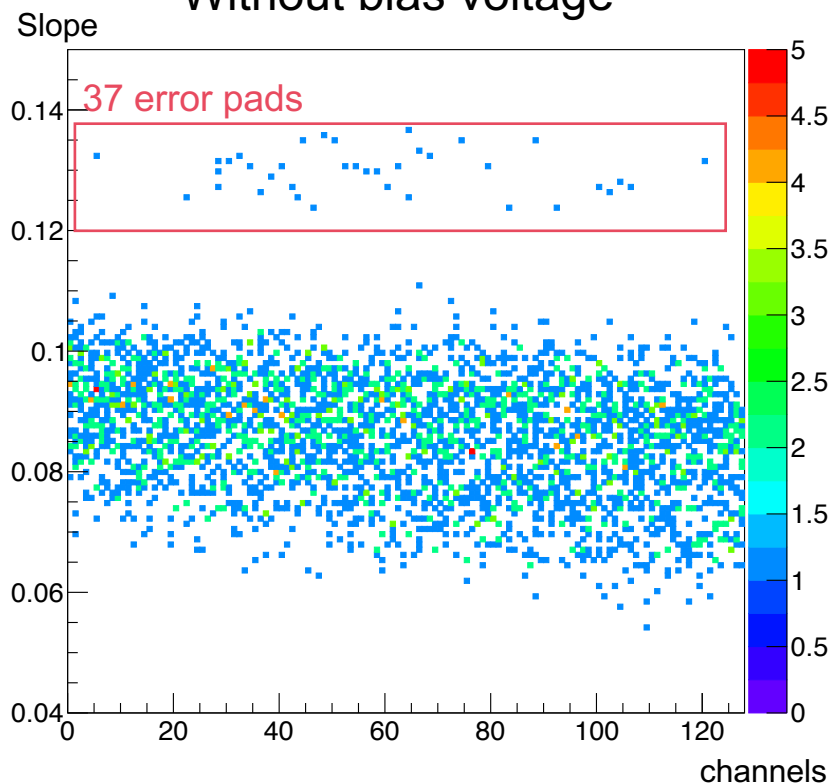




Assembly performance check : pre-production 001

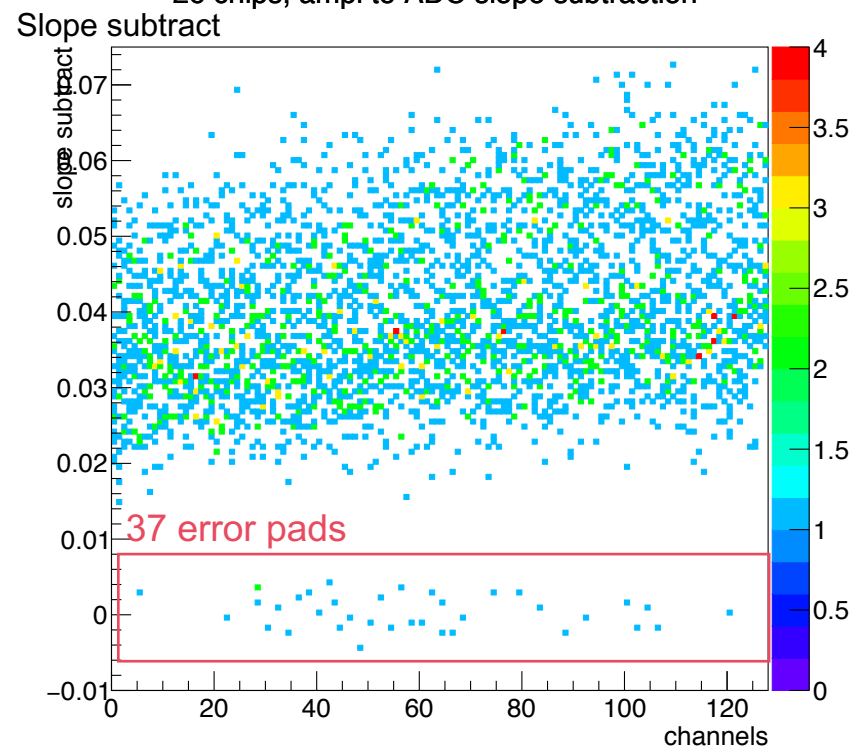


Self-comparison,
Without bias voltage



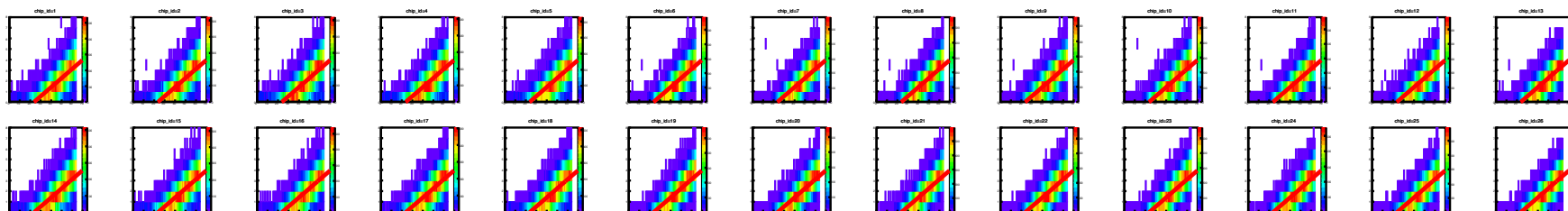
w/ and w/o bias voltage comparison

26 chips, ampl to ADC slope subtraction

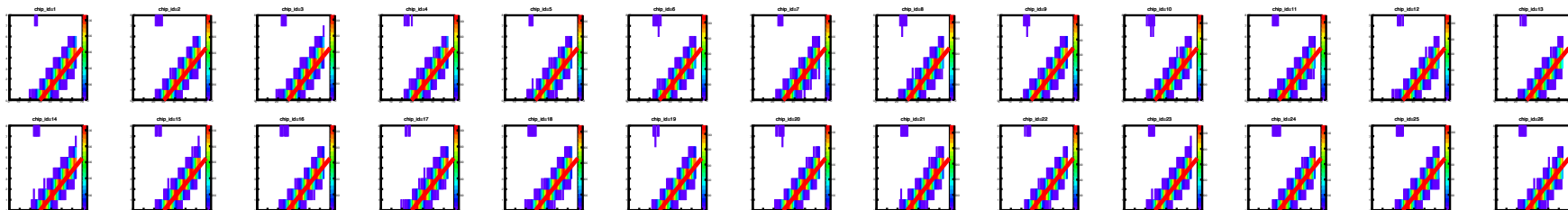




Second Module assembly in Taiwan. Pre - production 002



Without bias voltage



With bias voltage (+50V)

Placing error (measured by OGP)

Type A -> X : 120 μm , Y : 6 μm

Type B -> X : 48 μm , Y : 44 μm

Rotate error:

Type A -> 0.0373°

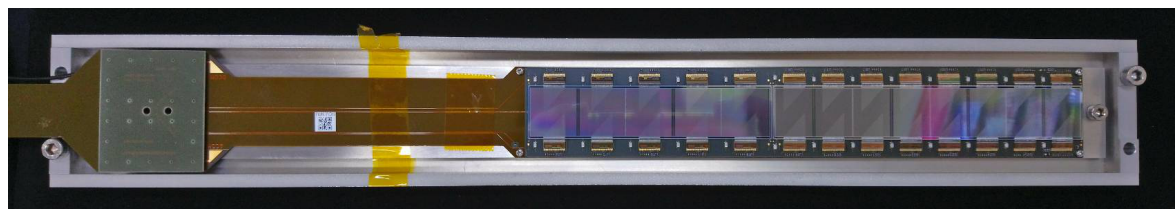
Type B -> 0.0469°

Bonding Condition:

18 pads can not be bonded in the beginning,

Tried to rebond them.

-> all channels were bonded in the end.

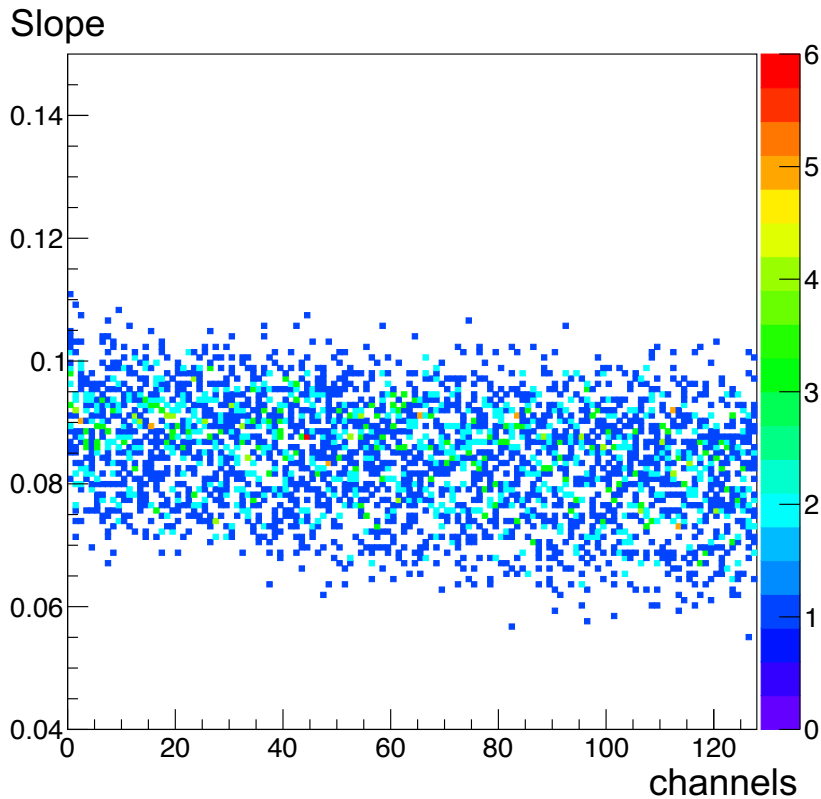




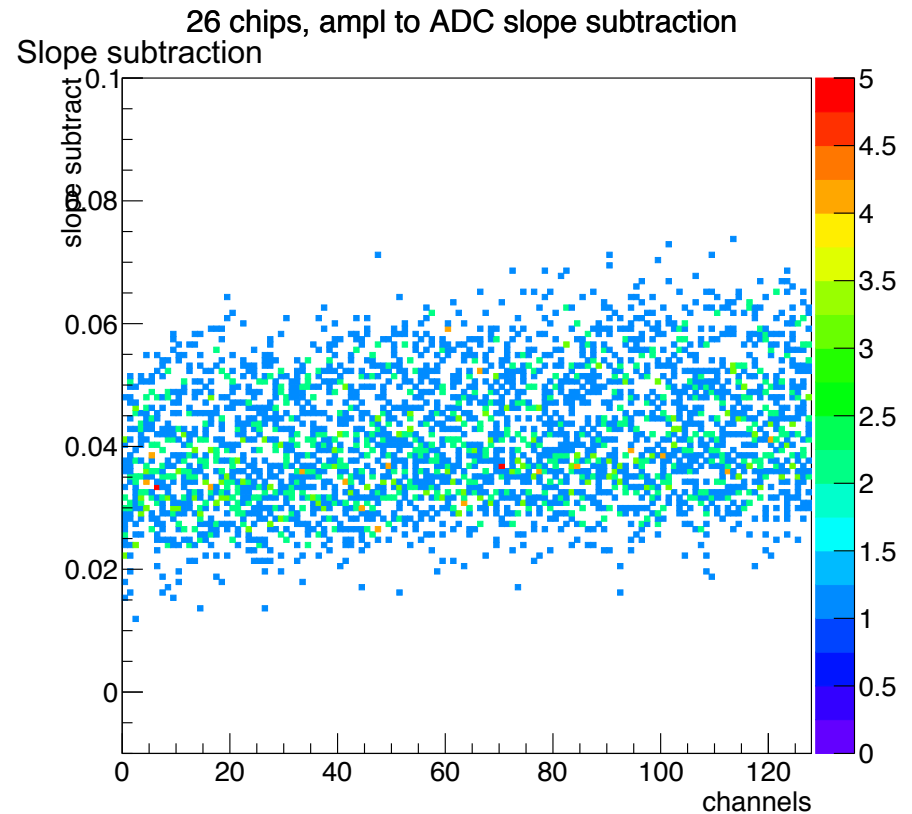
Assembly performance check : Pre - production 002



Self-comparison,
Without bias voltage



w/ and w/o comparison



All chips and all channels are functional



To do list

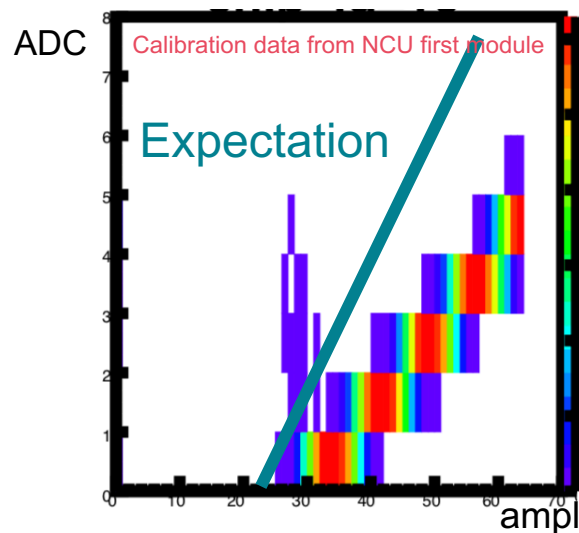


- ~~Produce first two real modules ASAP~~
- R&D the encapsulated glue apply.
- Gsel test
- I-V and noise level – V test
- Pedestal test
- Cosmic ray test
- Modify the assembly tools -> massive production

Back up



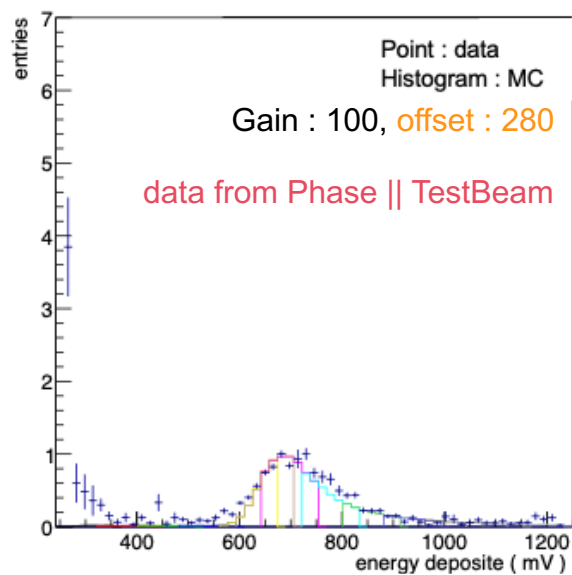
Testbench problems



The threshold setting on GUI in NCU TestBench

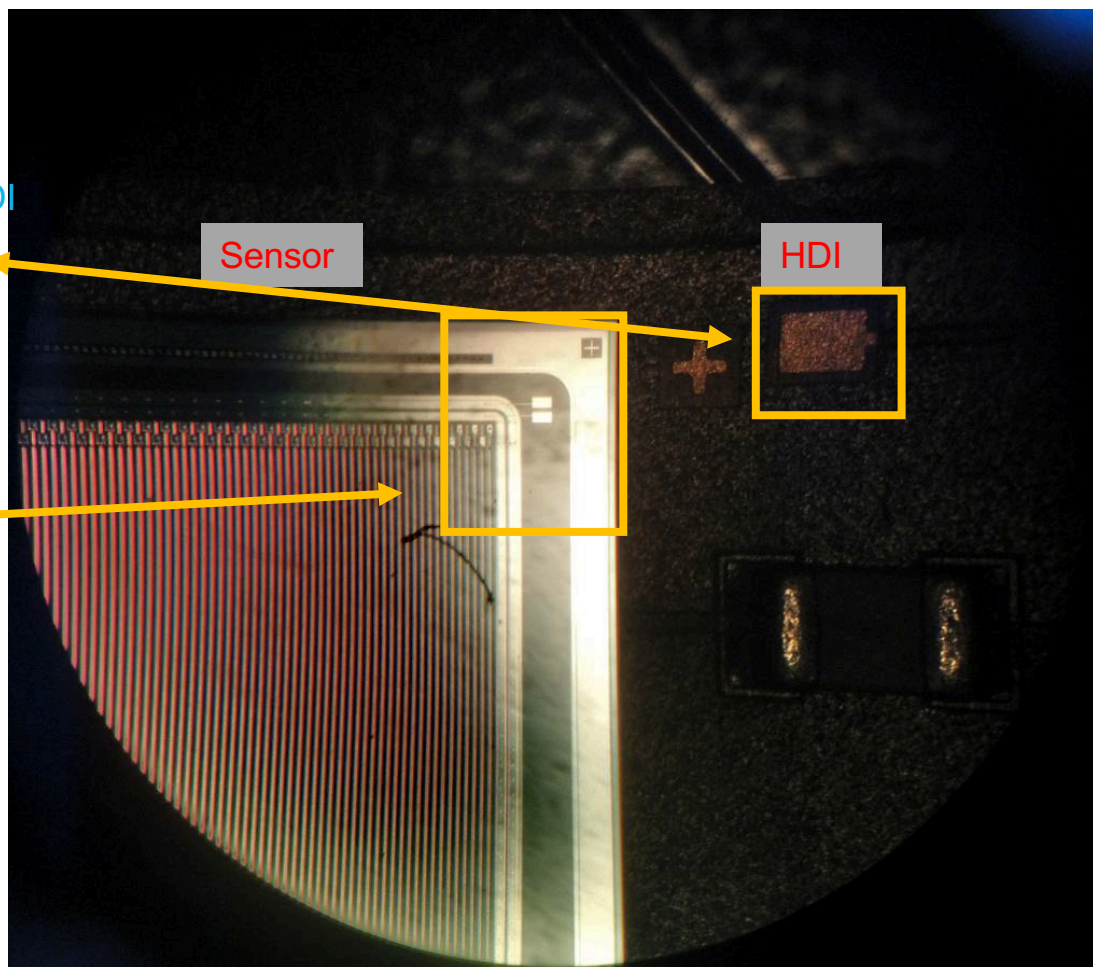
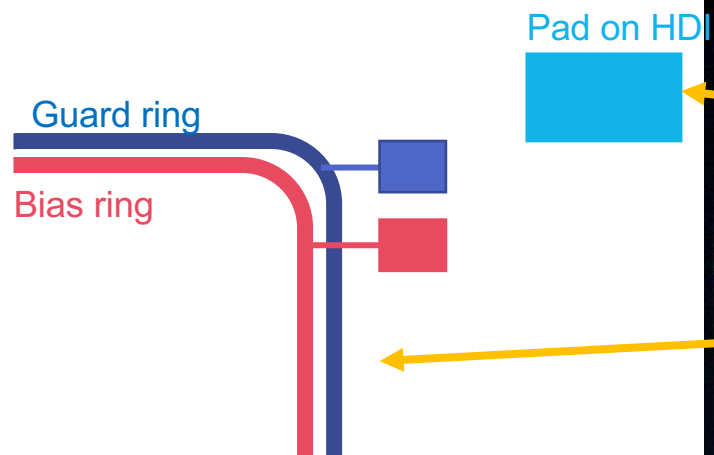
DAC0	20	Read	Write	Set	Reset	Default
DAC1	25	Read	Write	Set	Reset	Default
DAC2	30	Read	Write	Set	Reset	Default
DAC3	35	Read	Write	Set	Reset	Default
DAC4	40	Read	Write	Set	Reset	Default
DAC5	45	Read	Write	Set	Reset	Default
DAC6	50	Read	Write	Set	Reset	Default
DAC7	55	Read	Write	Set	Reset	Default

Energy deposit





Module bonding question



Do Bias ring pad and Guard ring pad both need to bond onto the HDI pad?



Calibration data, pre production 001 ampl to ADC, fitting detail



Without bias voltage

chip_id=1,	slope : 0.0794,	offset : -1.478,	chi2/NDF : 172.44
chip_id=2,	slope : 0.0827,	offset : -1.632,	chi2/NDF : 167.29
chip_id=3,	slope : 0.0760,	offset : -1.374,	chi2/NDF : 177.48
chip_id=4,	slope : 0.0771,	offset : -1.419,	chi2/NDF : 167.82
chip_id=5,	slope : 0.0765,	offset : -1.455,	chi2/NDF : 173.00
chip_id=6,	slope : 0.0941,	offset : -2.241,	chi2/NDF : 135.01
chip_id=7,	slope : 0.0936,	offset : -2.201,	chi2/NDF : 138.96
chip_id=8,	slope : 0.0914,	offset : -2.127,	chi2/NDF : 138.09
chip_id=9,	slope : 0.0924,	offset : -2.173,	chi2/NDF : 138.20
chip_id=10,	slope : 0.0912,	offset : -2.152,	chi2/NDF : 135.61
chip_id=11,	slope : 0.0907,	offset : -2.158,	chi2/NDF : 132.15
chip_id=12,	slope : 0.0912,	offset : -2.146,	chi2/NDF : 135.19
chip_id=13,	slope : 0.0877,	offset : -2.085,	chi2/NDF : 131.36
chip_id=14,	slope : 0.0783,	offset : -1.474,	chi2/NDF : 173.80
chip_id=15,	slope : 0.0768,	offset : -1.440,	chi2/NDF : 172.10
chip_id=16,	slope : 0.0760,	offset : -1.400,	chi2/NDF : 168.64
chip_id=17,	slope : 0.0762,	offset : -1.449,	chi2/NDF : 166.96
chip_id=18,	slope : 0.0749,	offset : -1.397,	chi2/NDF : 164.77
chip_id=19,	slope : 0.0916,	offset : -2.160,	chi2/NDF : 134.80
chip_id=20,	slope : 0.0913,	offset : -2.133,	chi2/NDF : 133.54
chip_id=21,	slope : 0.0919,	offset : -2.164,	chi2/NDF : 138.87
chip_id=22,	slope : 0.0915,	offset : -2.167,	chi2/NDF : 131.36
chip_id=23,	slope : 0.0914,	offset : -2.150,	chi2/NDF : 133.42
chip_id=24,	slope : 0.0893,	offset : -2.108,	chi2/NDF : 133.09
chip_id=25,	slope : 0.0872,	offset : -2.059,	chi2/NDF : 134.02
chip_id=26,	slope : 0.0877,	offset : -2.084,	chi2/NDF : 133.49



Calibration data, pre production 001 ampl to ADC, fitting detail



With bias voltage (+50 V)

chip_id=1,	slope : 0.1301,	offset : -3.733,	chi2/NDF : 61.20
chip_id=2,	slope : 0.1305,	offset : -3.771,	chi2/NDF : 59.13
chip_id=3,	slope : 0.1298,	offset : -3.781,	chi2/NDF : 61.21
chip_id=4,	slope : 0.1289,	offset : -3.761,	chi2/NDF : 62.24
chip_id=5,	slope : 0.1279,	offset : -3.800,	chi2/NDF : 62.83
chip_id=6,	slope : 0.1273,	offset : -3.795,	chi2/NDF : 61.00
chip_id=7,	slope : 0.1266,	offset : -3.727,	chi2/NDF : 61.44
chip_id=8,	slope : 0.1265,	offset : -3.753,	chi2/NDF : 61.77
chip_id=9,	slope : 0.1264,	offset : -3.755,	chi2/NDF : 62.37
chip_id=10,	slope : 0.1268,	offset : -3.797,	chi2/NDF : 61.91
chip_id=11,	slope : 0.1259,	offset : -3.804,	chi2/NDF : 63.09
chip_id=12,	slope : 0.1264,	offset : -3.770,	chi2/NDF : 64.04
chip_id=13,	slope : 0.1235,	offset : -3.723,	chi2/NDF : 67.74
chip_id=14,	slope : 0.1289,	offset : -3.736,	chi2/NDF : 58.97
chip_id=15,	slope : 0.1288,	offset : -3.791,	chi2/NDF : 63.35
chip_id=16,	slope : 0.1285,	offset : -3.792,	chi2/NDF : 62.07
chip_id=17,	slope : 0.1272,	offset : -3.767,	chi2/NDF : 64.12
chip_id=18,	slope : 0.1265,	offset : -3.768,	chi2/NDF : 62.56
chip_id=19,	slope : 0.1252,	offset : -3.739,	chi2/NDF : 65.50
chip_id=20,	slope : 0.1260,	offset : -3.770,	chi2/NDF : 65.42
chip_id=21,	slope : 0.1261,	offset : -3.760,	chi2/NDF : 62.11
chip_id=22,	slope : 0.1238,	offset : -3.694,	chi2/NDF : 60.72
chip_id=23,	slope : 0.1253,	offset : -3.735,	chi2/NDF : 64.41
chip_id=24,	slope : 0.1243,	offset : -3.737,	chi2/NDF : 61.38
chip_id=25,	slope : 0.1239,	offset : -3.745,	chi2/NDF : 65.26
chip_id=26,	slope : 0.1233,	offset : -3.702,	chi2/NDF : 63.97



Calibration data, FVTX (B295) ampl to ADC, fitting detail



Without bias voltage

chip_id=1,	slope : 0.1065,	offset : -2.681,	chi2/NDF : 128.18
chip_id=2,	slope : 0.1066,	offset : -2.700,	chi2/NDF : 127.11
chip_id=3,	slope : 0.1102,	offset : -2.789,	chi2/NDF : 125.65
chip_id=4,	slope : 0.1102,	offset : -2.847,	chi2/NDF : 125.83
chip_id=5,	slope : 0.1116,	offset : -2.905,	chi2/NDF : 122.24
chip_id=6,	slope : 0.1126,	offset : -2.981,	chi2/NDF : 118.84
chip_id=7,	slope : 0.1133,	offset : -2.992,	chi2/NDF : 112.96
chip_id=8,	slope : 0.1158,	offset : -3.088,	chi2/NDF : 111.88
chip_id=9,	slope : 0.1169,	offset : -3.116,	chi2/NDF : 111.79
chip_id=10,	slope : 0.1185,	offset : -3.213,	chi2/NDF : 106.05
chip_id=11,	slope : 0.1197,	offset : -3.287,	chi2/NDF : 105.81
chip_id=12,	slope : 0.1205,	offset : -3.354,	chi2/NDF : 100.95
chip_id=13,	slope : 0.1219,	offset : -3.402,	chi2/NDF : 94.95
chip_id=14,	slope : 0.1032,	offset : -2.542,	chi2/NDF : 129.11
chip_id=15,	slope : 0.1053,	offset : -2.637,	chi2/NDF : 127.69
chip_id=16,	slope : 0.1084,	offset : -2.731,	chi2/NDF : 128.99
chip_id=17,	slope : 0.1084,	offset : -2.784,	chi2/NDF : 126.53
chip_id=18,	slope : 0.1099,	offset : -2.877,	chi2/NDF : 121.15
chip_id=19,	slope : 0.1111,	offset : -2.988,	chi2/NDF : 118.81
chip_id=20,	slope : 0.1135,	offset : -3.014,	chi2/NDF : 116.71
chip_id=21,	slope : 0.1142,	offset : -3.043,	chi2/NDF : 112.71
chip_id=22,	slope : 0.1158,	offset : -3.116,	chi2/NDF : 112.08
chip_id=23,	slope : 0.1149,	offset : -3.162,	chi2/NDF : 105.74
chip_id=24,	slope : 0.1177,	offset : -3.245,	chi2/NDF : 102.34
chip_id=25,	slope : 0.1179,	offset : -3.313,	chi2/NDF : 97.46
chip_id=26,	slope : 0.1198,	offset : -3.425,	chi2/NDF : 92.42



Calibration data, FVTX (B295) ampl to ADC, fitting detail



With bias voltage (+50 V)

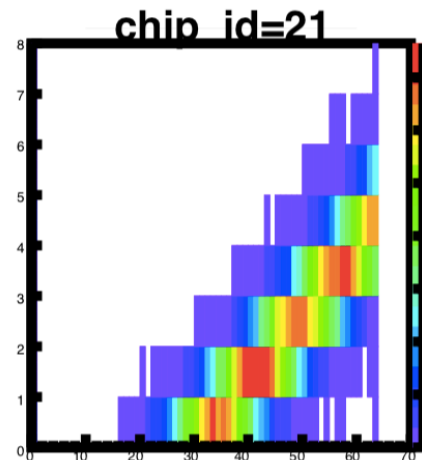
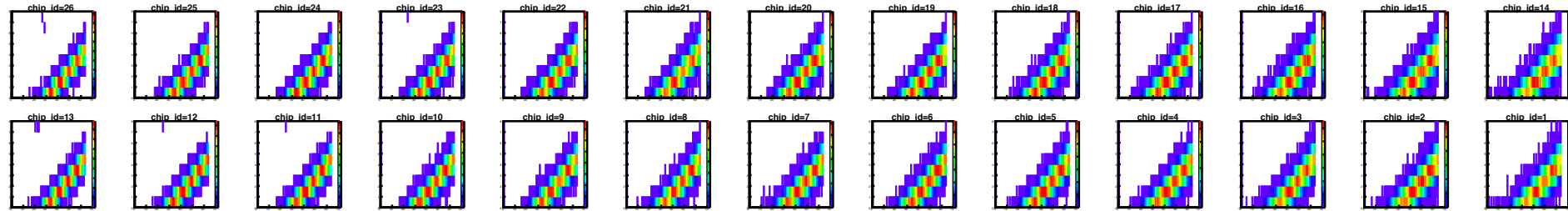
chip_id=1,	slope : 0.1315,	offset : -3.684,	chi2/NDF : 99.49
chip_id=2,	slope : 0.1298,	offset : -3.627,	chi2/NDF : 102.60
chip_id=3,	slope : 0.1311,	offset : -3.616,	chi2/NDF : 109.00
chip_id=4,	slope : 0.1299,	offset : -3.633,	chi2/NDF : 104.44
chip_id=5,	slope : 0.1291,	offset : -3.600,	chi2/NDF : 102.63
chip_id=6,	slope : 0.1284,	offset : -3.604,	chi2/NDF : 103.04
chip_id=7,	slope : 0.1285,	offset : -3.593,	chi2/NDF : 104.24
chip_id=8,	slope : 0.1293,	offset : -3.614,	chi2/NDF : 110.87
chip_id=9,	slope : 0.1275,	offset : -3.532,	chi2/NDF : 110.51
chip_id=10,	slope : 0.1284,	offset : -3.597,	chi2/NDF : 114.46
chip_id=11,	slope : 0.1277,	offset : -3.584,	chi2/NDF : 112.84
chip_id=12,	slope : 0.1269,	offset : -3.583,	chi2/NDF : 110.44
chip_id=13,	slope : 0.1270,	offset : -3.574,	chi2/NDF : 111.88
chip_id=14,	slope : 0.1294,	offset : -3.606,	chi2/NDF : 103.08
chip_id=15,	slope : 0.1301,	offset : -3.651,	chi2/NDF : 93.55
chip_id=16,	slope : 0.1311,	offset : -3.657,	chi2/NDF : 99.08
chip_id=17,	slope : 0.1287,	offset : -3.608,	chi2/NDF : 96.50
chip_id=18,	slope : 0.1269,	offset : -3.564,	chi2/NDF : 106.52
chip_id=19,	slope : 0.1274,	offset : -3.641,	chi2/NDF : 93.75
chip_id=20,	slope : 0.1294,	offset : -3.661,	chi2/NDF : 93.81
chip_id=21,	slope : 0.1277,	offset : -3.588,	chi2/NDF : 107.23
chip_id=22,	slope : 0.1277,	offset : -3.593,	chi2/NDF : 107.15
chip_id=23,	slope : 0.1256,	offset : -3.592,	chi2/NDF : 99.95
chip_id=24,	slope : 0.1270,	offset : -3.610,	chi2/NDF : 103.51
chip_id=25,	slope : 0.1249,	offset : -3.573,	chi2/NDF : 110.01
chip_id=26,	slope : 0.1246,	offset : -3.587,	chi2/NDF : 110.86



Calibration test : FVTX (B295)



without bias voltage (data : fphx_raw_20200608-1004_0.dat)



Zoom in example

Gsel : 2

The threshold setting on the GUI in NCU TestBench

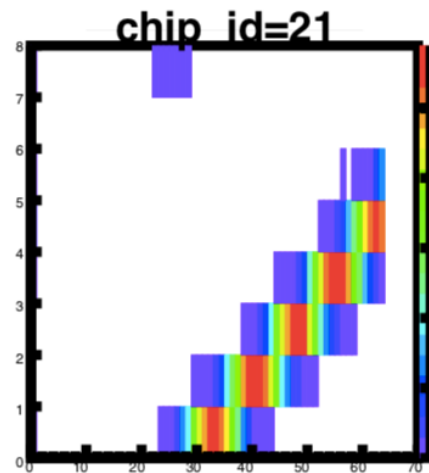
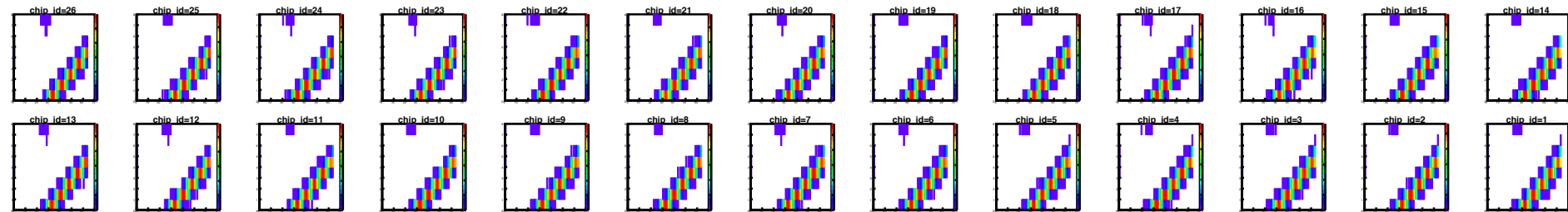
DAC0	20	Read	Write	Set	Reset	Default
DAC1	25	Read	Write	Set	Reset	Default
DAC2	30	Read	Write	Set	Reset	Default
DAC3	35	Read	Write	Set	Reset	Default
DAC4	40	Read	Write	Set	Reset	Default
DAC5	45	Read	Write	Set	Reset	Default
DAC6	50	Read	Write	Set	Reset	Default
DAC7	55	Read	Write	Set	Reset	Default



Calibration test : FVTX (B295)



with bias voltage (+50V) (data :fphx_raw_20200609-0035_0.dat)



Zoom in example

Gsel : 2

The threshold setting on GUI in NCU TestBench

DAC0	20	Read	Write	Set	Reset	Default
DAC1	25	Read	Write	Set	Reset	Default
DAC2	30	Read	Write	Set	Reset	Default
DAC3	35	Read	Write	Set	Reset	Default
DAC4	40	Read	Write	Set	Reset	Default
DAC5	45	Read	Write	Set	Reset	Default
DAC6	50	Read	Write	Set	Reset	Default
DAC7	55	Read	Write	Set	Reset	Default