LSST Raft Electronics

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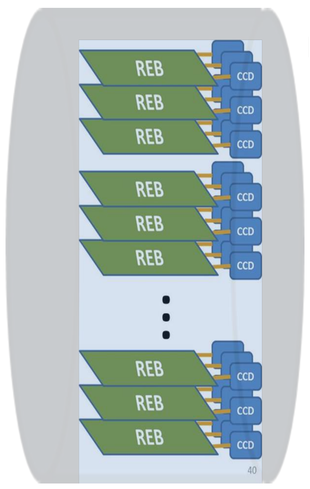
ABSTRACT

Compared to previous astronomical camera electronics, LSST's readout is highly parallelized and the entire readout chain is housed in the sensor cryostat vacuum, making compactness and low power critical. LSST readout electronics is organized as a set of 63 Readout Electronics Boards (REBs), each serving three science CCDs. Custom CMOS ASICs provide the key functions of video processing and clock/bias generation. The focal plane is made up of 21 raft modules, each containing 9 CCDs and three REBs for a total video channel count of 3024. Prototype sensors and electronics have been evaluated in a vertical slice test and the performance of the integrated signal chain meets requirements for low noise and crosstalk.

OVERVIEW

In LSST, 189 science CCDs are organized into 21 "rafts" of 9. Each raft is served by a trio of Raft Electronics Boards (REBs) which provide all electronic functions to control and readout the nine CCDs.



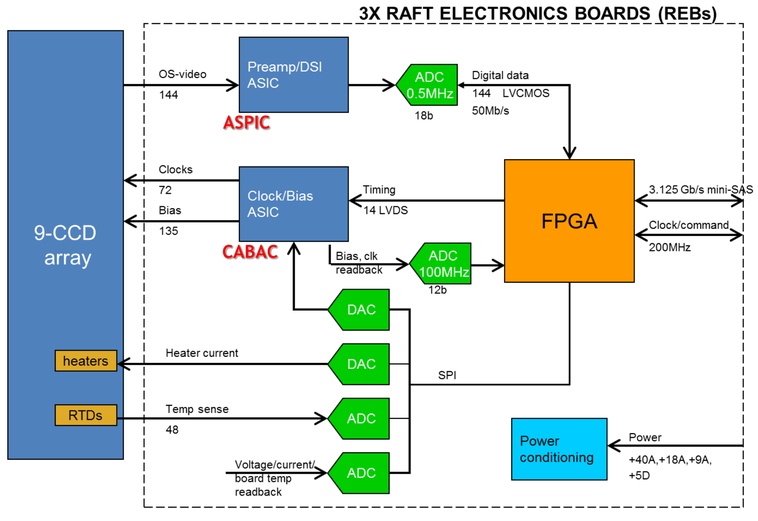
Key design decisions :

- High level of parallelism to maintain low read noise while sustaining 1.5Gpixels/s aggregate rate
- Entire readout chain in cryostat, in "shadow" of CCD array, to provide tight CCD-FEE coupling and manage vacuum feedthrough count

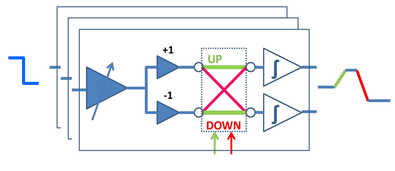
REQUIREMENTS

Requirement	Value	Rationale
Number of CCDs	3 per REB	Raft tower organization
Pixel rate	550kpix/s	Achieve 2s frame readout time
Read noise	9 e^-	Stay below sky noise in grizy
Dynamic range	86dB	Match CCD
Electronic crosstalk	0.2%	Limit of software pipeline
Video gain drift	0.1%/hr	Photometric calibration requirement
Digital output bandwidth	0.5Gbps	18b/pixel × 550kpix/s × 48 channels + overheads for CCD data
Power dissipation	16.7W	Refrigeration system capacity
CCD temperature resolution	0.05°C	Photometric calibration in y
Raft makeup heat	670mW	Maintain CCD temperature

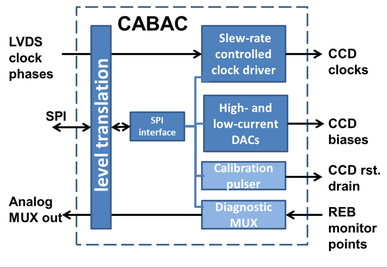
BLOCK DIAGRAM



Implementation relies on two 0.35μm CMOS ASICs (developed by LPNHE/LAL groups)

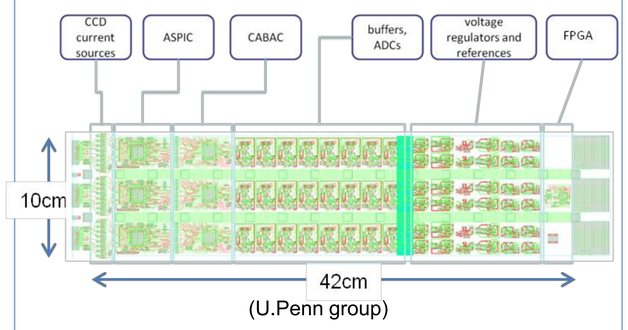


ASPIC: preamplifier, dual-slope integrator, differential driver



CABAC: clock switches, bias DACs, multiplexer

RAFT ELECTRONICS BOARD LAYOUT



(U.Penn group)

The REB is divided into five sections:

- Three identical "stripes" each servicing a single CCD. These stripes contain the clock and video ASICs, and the digitizers;
- A common power conditioning and reference generation section;
- An FPGA for control and I/O (currently implemented as a daughter board).

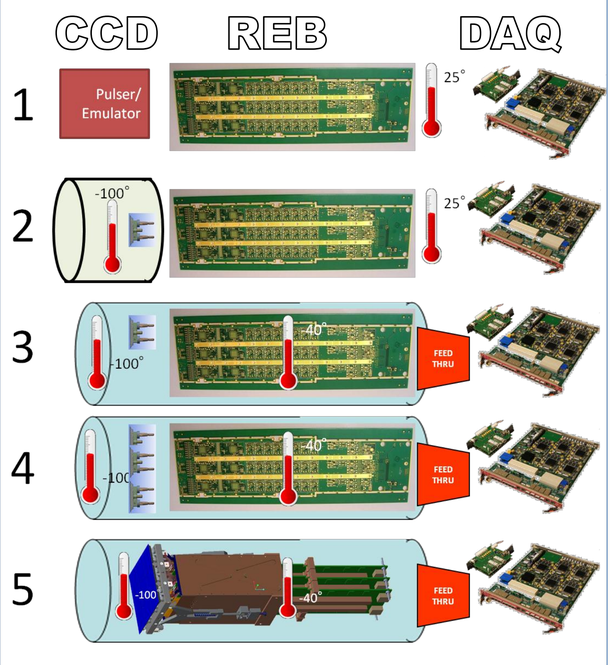
Each REB processes 48 CCD channels.

INTEGRATED TESTING

A vertical slice test bench has been developed to:

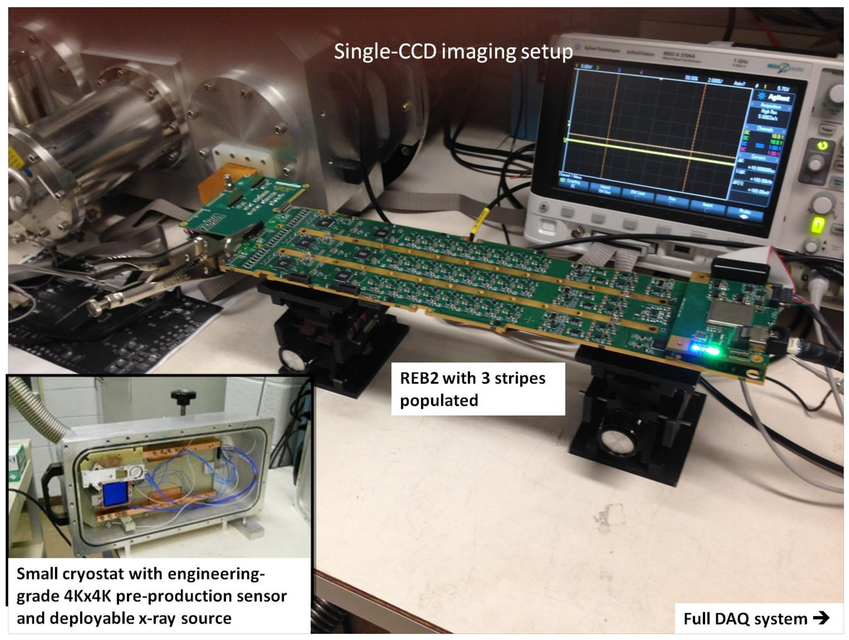
- Ensure that the ensemble of raft electronic components (CCDs, ASICs, digitizers, clock switches, DAQ, and power system) meets requirements;
- Monitor potential performance degradations from scale-up;
- Provide a test bed for control software development;
- Monitor the thermal behavior of electronics components;
- Prototype the Raft Acceptance Test Stand (TS8) and the LSST Commissioning Camera (ComCam)

Testing has been divided into phases which build up in stages to the final fully-integrated science raft:

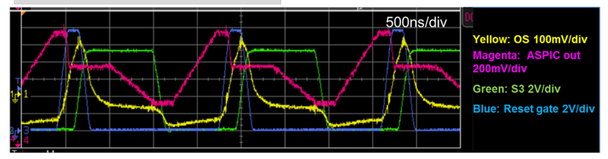


Note that between Stage 2 and Stage 3, the cable connecting the CCD to the REB goes from ~300mm to ~60mm, greatly reducing the channel-to-channel crosstalk.

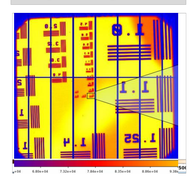
TEST SETUP (STAGE 2 AND 3) AND RESULTS



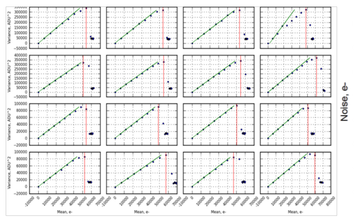
CCD and ASIC waveforms



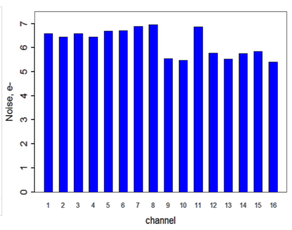
Target image



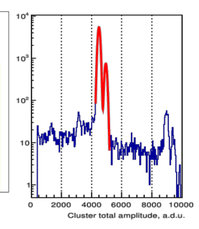
Photon transfer curves



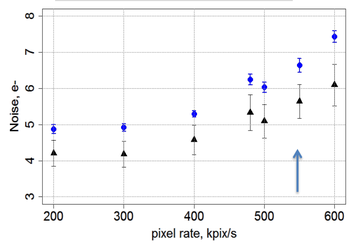
Read noise (550kpix/s)



^{55}Fe spectrum

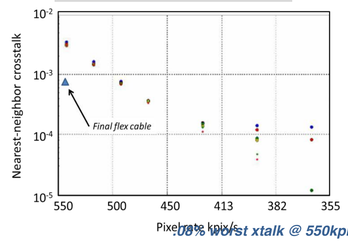


Read noise vs. pixel rate



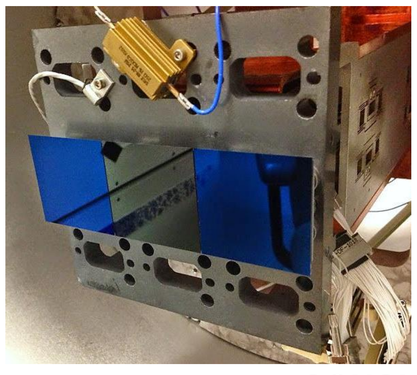
5.6 ±0.5 e^- noise @ 550kpix/s

Crosstalk vs. pixel rate



-88% worst xtalk @ 550kpix/s

TEST SETUP (STAGE 4)



Photograph of 3 prototype CCDs installed in raft baseplate.

CONCLUSION

A powerful test bed for raft electronics characterization and optimization has been developed, featuring:

- Close emulation of final cryostat environment
- Full signal chain from optical input through DAQ
- Instrumented for flexible electronic, thermal, and optical configuration
- Hardware debugging and software development platform

At the level of a single CCD with complete electronics chain, performance requirements are met.

System will be scaled up to 3, then 9 CCDs.