# The VMM ASIC

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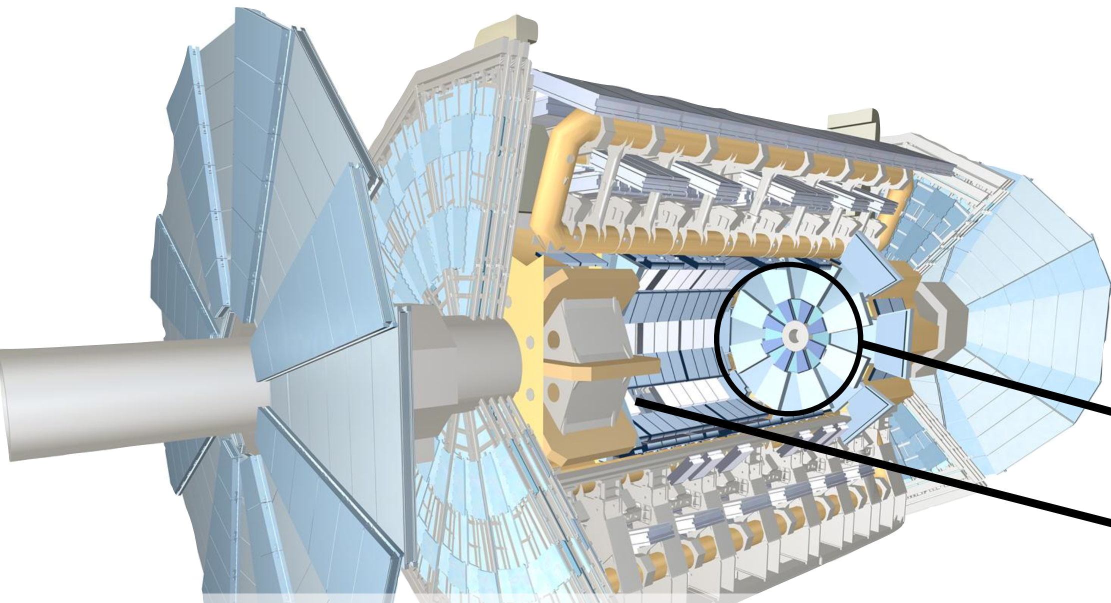
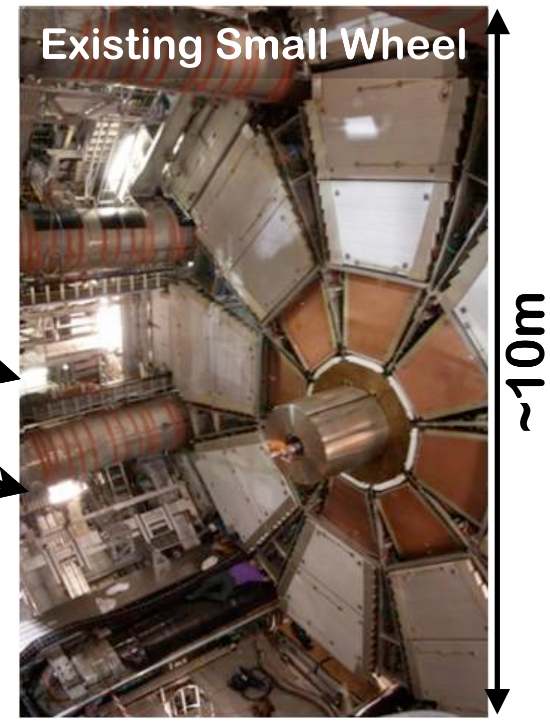
# The ATLAS New Small Wheel(s) Upgrade

- The motivation of developing the VMM ASIC was the ATLAS NSW upgrade at CERN
- Biggest MPGD development and most complex part of the muon spectrometer ever built

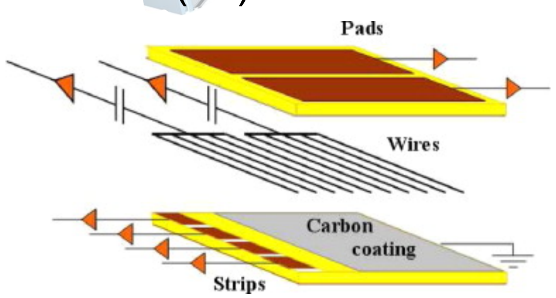




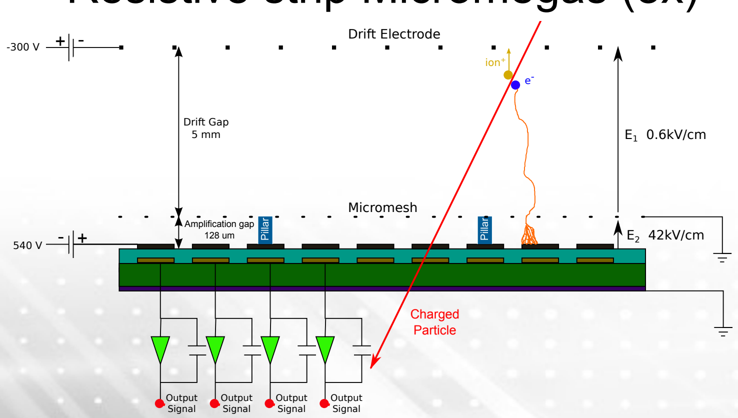


<u>New Small Wheels (16 sensitive layers)</u>

- sTGC (8x)



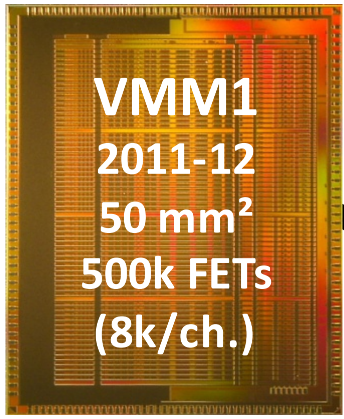

- Resistive strip Micromegas (8x)




<u>Front-end Electronics Requirements (need of custom ASIC)</u>

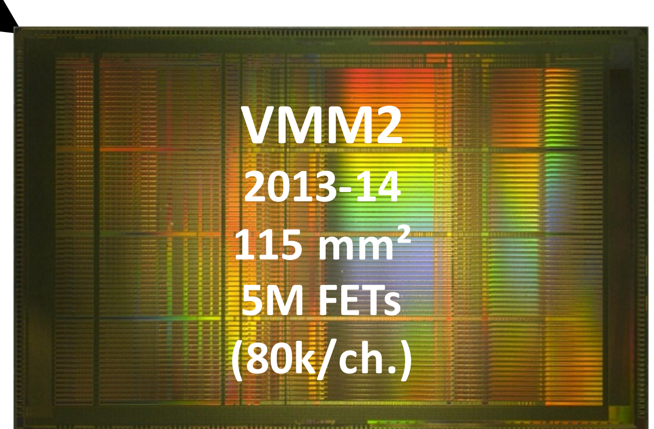
- Challenge of this Project - <u>More than 2.4 million</u> channels total (2.1M for Micromegas and 300k for sTGC) <u>(full MS of ATLAS ~1.6M channels)</u>
- Operate with both charge polarities
- Sensing element capacitance 50-200pF (sTGC Pad up to 2nF)
- Charge measurements up to 2pC @ < 1fC RMS(6pC for sTGC pads)
- Time measurements ~ 100ns @ < 1ns RMS
- Multiple Trigger primitives, complex logic
- Digitisation included, Low power, programmable
- Space requirements on the detector
- Radiation tolerant

# The VMM front-end ASIC - **Evolution**




- **Mixed-signal**
- 2-phase readout with external ADC
- **peak** and **timing** information
- neighbouring readout
- sub-hysteresis **discrimination**
- few timing outputs

- Mixed-signal
- **Continuous** readout
- Current-output peak detector
- **Increased** range of **gains**
- **Three ADCs** per channel
- FIFOs, **serialised data with DDR**




- Serialised ART with DDR
- Additional timing modes
- **64 timing outputs**
- Additional functions and fixes

- **LVL0 pipeline** and buffering for ATLAS
- **SEU-tolerant logic**
- **Revised front-end** for high charge and capacitance (2nF, 50pC, fast recovery)
- SLVS signals
- Reset controls
- **Timing at threshold**
- Timing ramp optimisation
- Ion **tail suppressor** (fast recovery)
- Int. Pulser range extension
- ART synchronisation to BC clock
- additional functions and fixes
- **VMM3a fixed open bugs** from VMM3 and introduce some stability fixes on the ADCs and Front-end

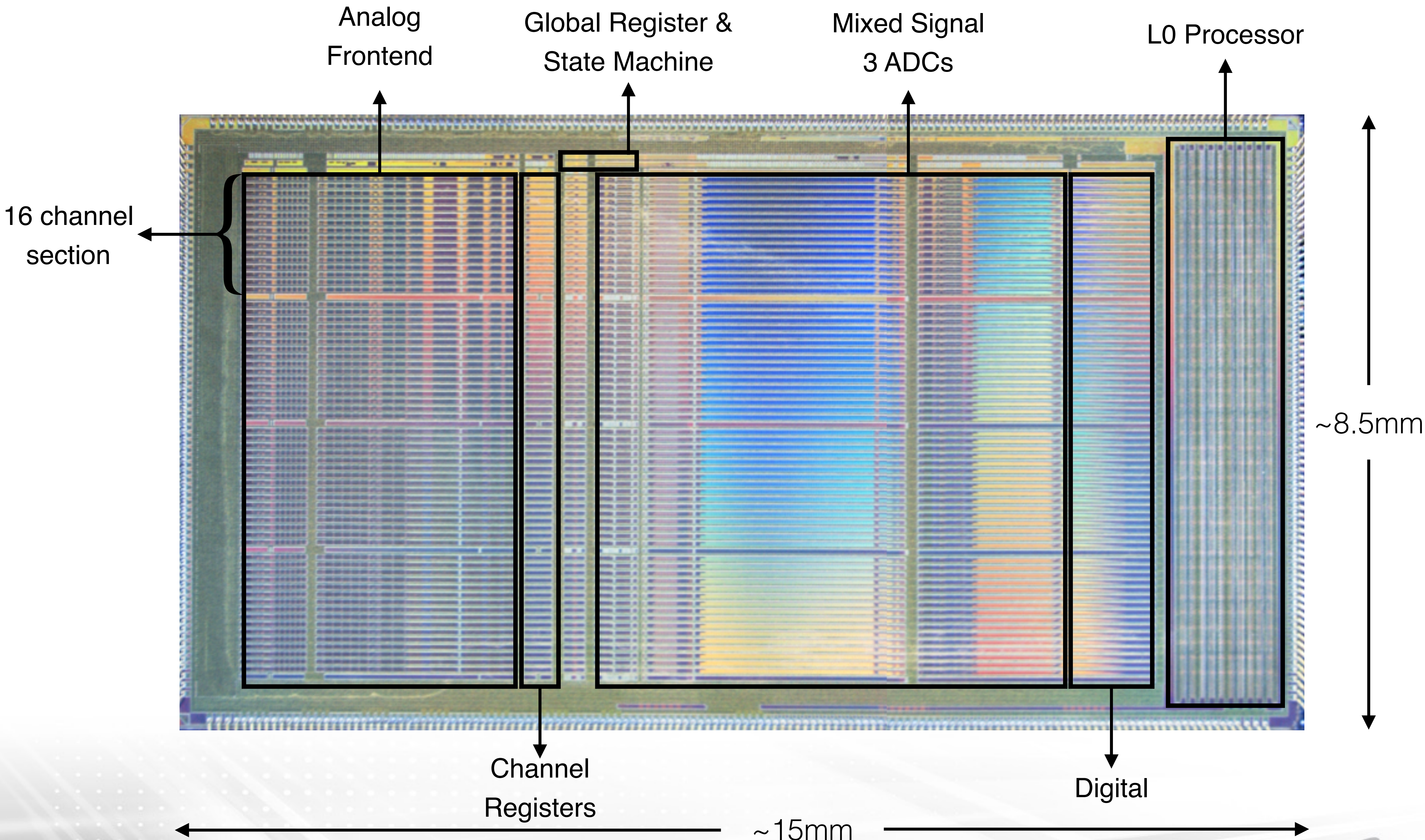
**VMM3a - Production Version !**


~10mW/channel

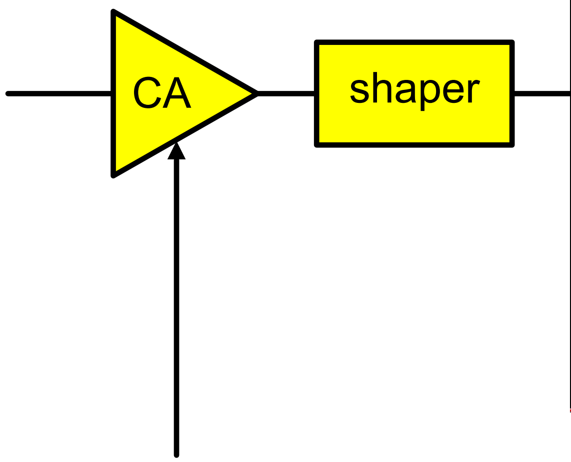
- ***The VMM was designed at BNL in collaboration with IFIN-HH***
- ***It is fabricated in the 130nm Global Foundries 8RF-DM process (former IBM 8RF-DM)***

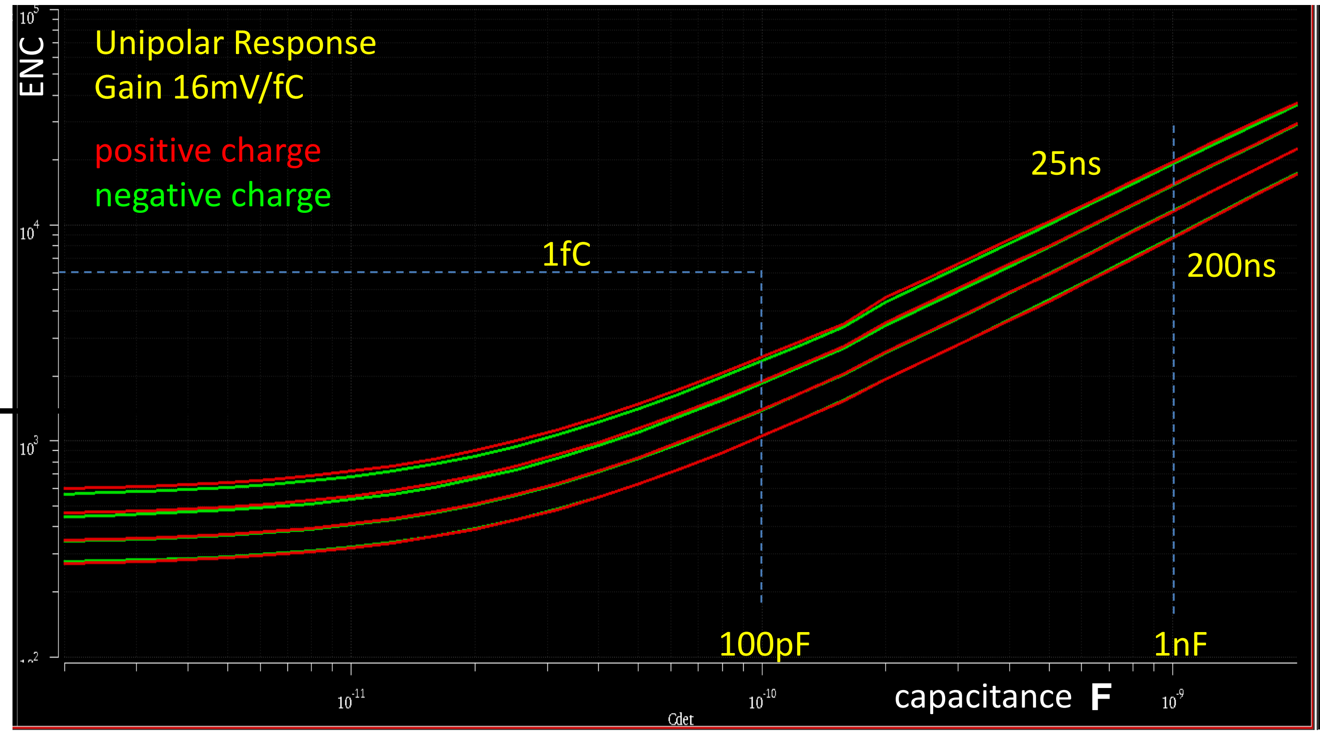
# An actual photo of the ASIC

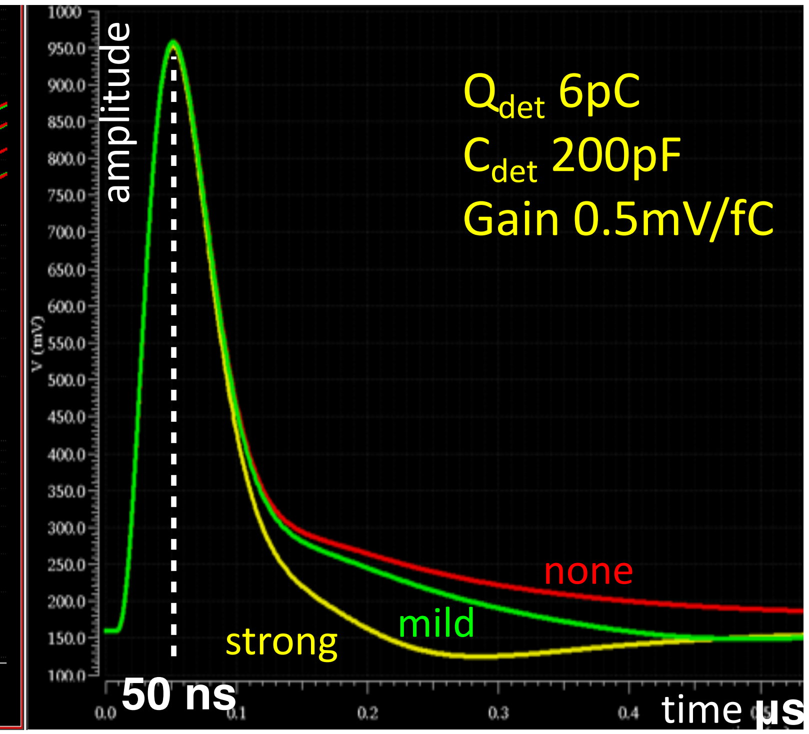
- The ASIC features **64 channels** that extend along the size of the die. At the end the L0 section (explained in later slides) is separated to isolate the noise from the digital activity



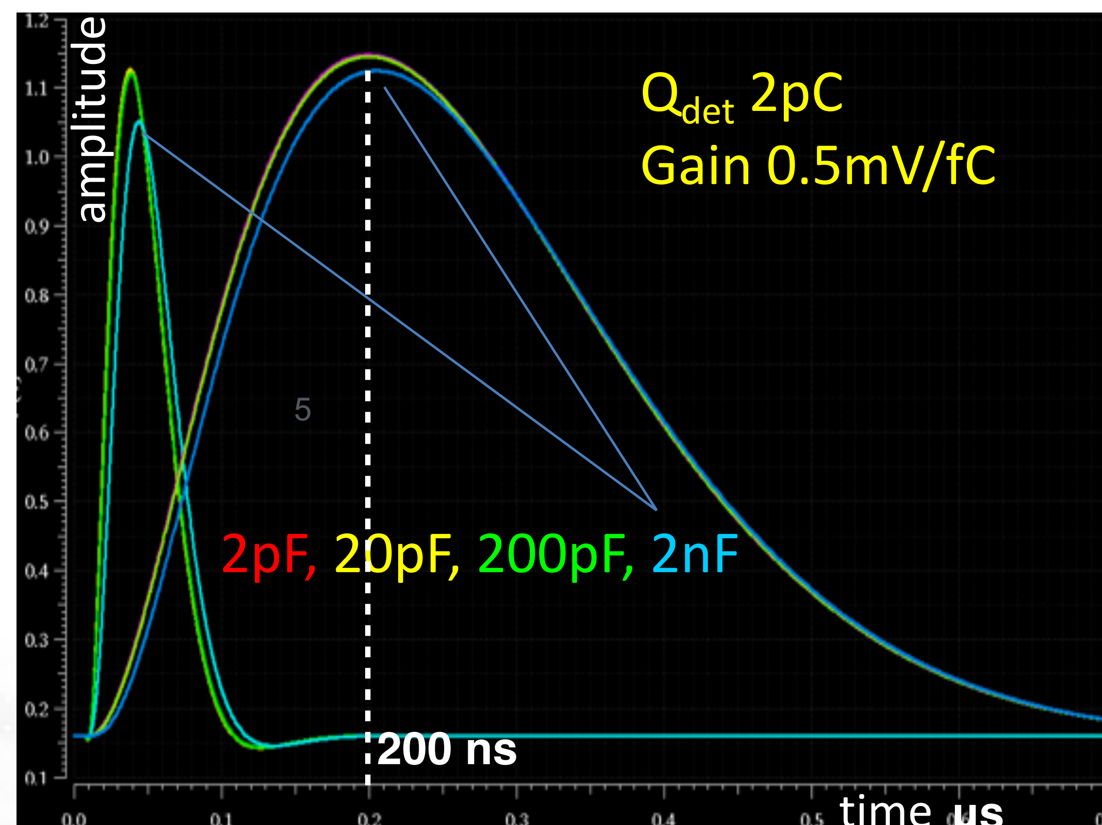
# VMM3a **Amplifier & Shaper**




- Input transistor: **PMOS,** 3 stage amplifier,
  - 2 stages used for **adjustable gain**: 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC
  - last stage for **charge inversion (**positive or negative)
- Input **capacitance**: can operate from sub-pF to several nF
- Maximum **charge**: 2 pC in **linear range**, **fast recovery** from 50 pC
- Semi gaussian DDF c-**shaper 3rd order**
  - **Configurable** ion tail **suppression**: none, mild or strong
  - **Adjustable peaking** time: 25, 50, 100, 200 ns
  - Leakage-adaptive, **BGR-stabilised baseline**

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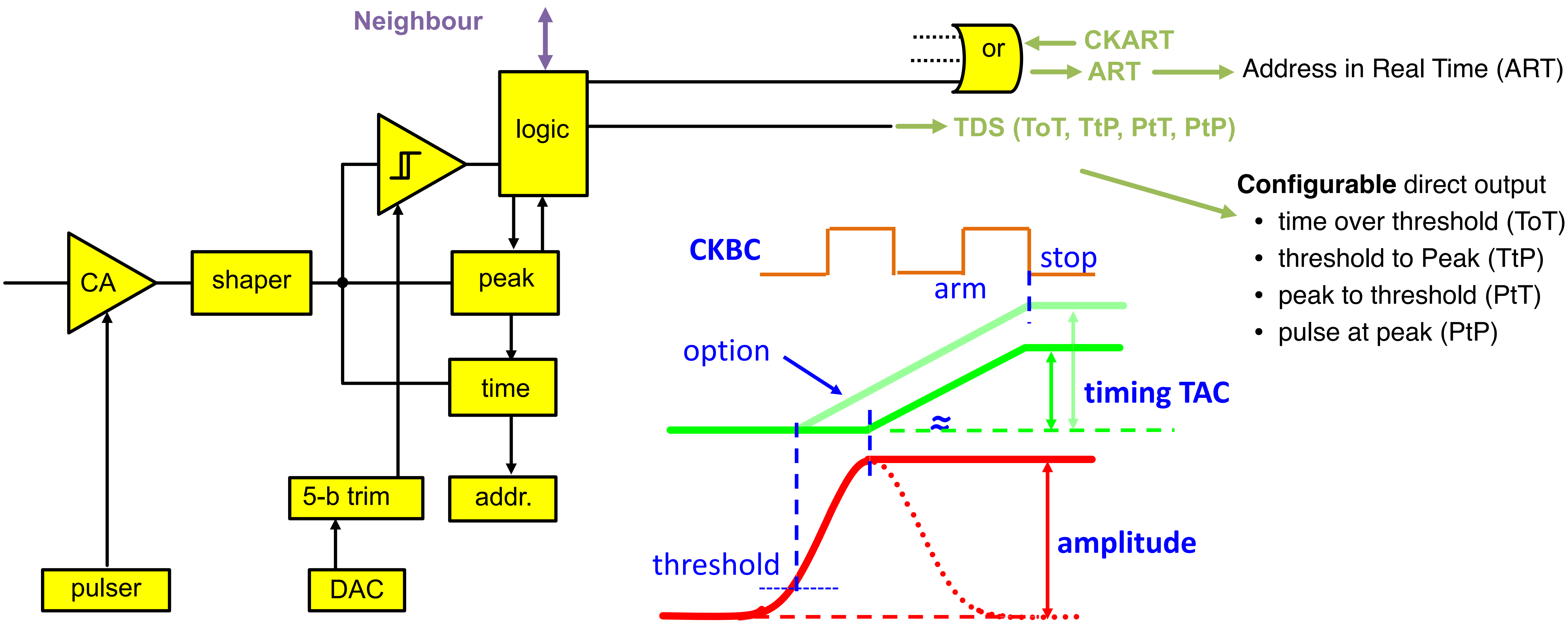
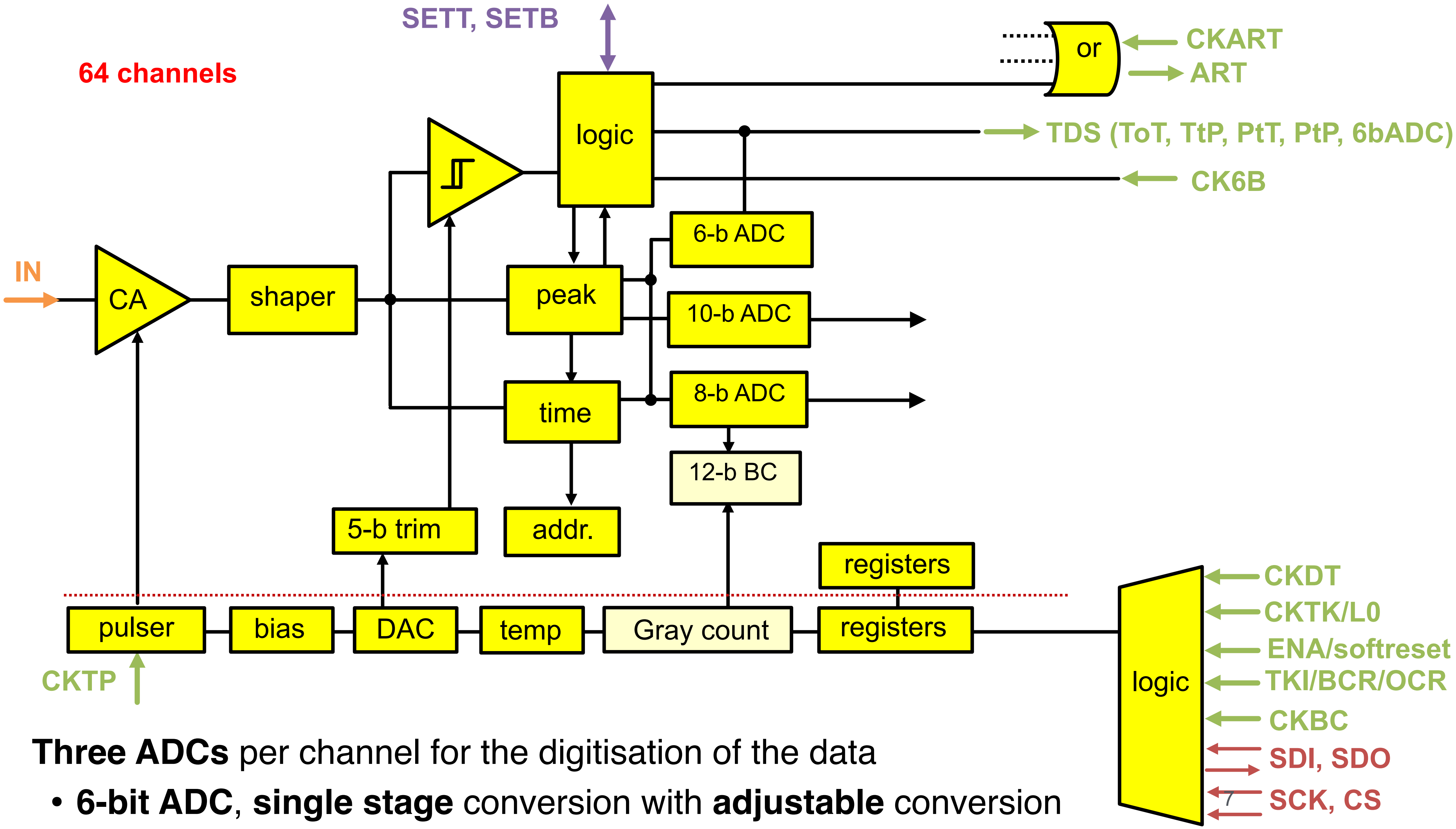
# VMM3a **Discrimination, Charge and Time**




- Global 10-bit DAC for adjusting the **threshold** - **Discrimination** with sub-hysterisis (effective 2mV)
- Adjustable **5-bit discrimination** threshold **per channel** to adjust at ~mV level
- **Neighbour** logic to trigger sub-threshold channels with inter-chip communication
- Configurable **direct output** per channel and serial fast output of address as an OR of all channels
- **Peak detection**: measurement of peak **amplitude** and storage in analog memory
- **Time detection**: measurement of **peak/threshold** timing through a configurable time to amplitude converter (**TAC**: 60, 100, 350, 650 ns) and storage in analog memory
  - Clock working mode on **synchronous** machines but also as strobe for **asynchronous** operations

# VMM3a **ADCs**

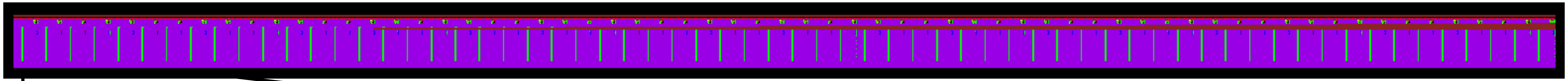



**Three ADCs** per channel for the digitisation of the data

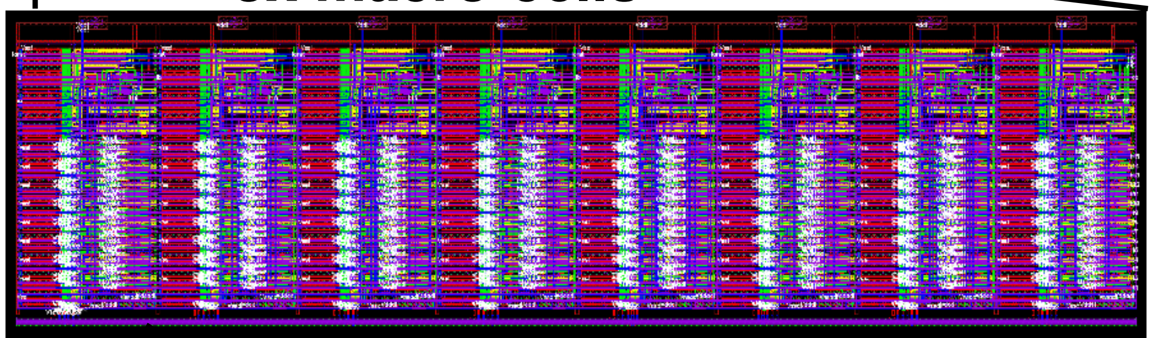
- **6-bit ADC**, **single stage** conversion with **adjustable** conversion **time** and **offset**, completes within **25 ns from peak**
- **10-bit ADC**, **200 ns adjustable** conversion time/offset, for peak **amplitude** conversion
- **20-bit timing information** with 8-bit ADC, **100 ns** conversion time + 12-bit Gray-code counter, BC clock
- **2 step mode conversion for 10-bit & 8-bit ADCs** - First stage the comparison identifies one of the macro-cells and at the second stage the micro-cell is identified, possibility to jump through macro-cells

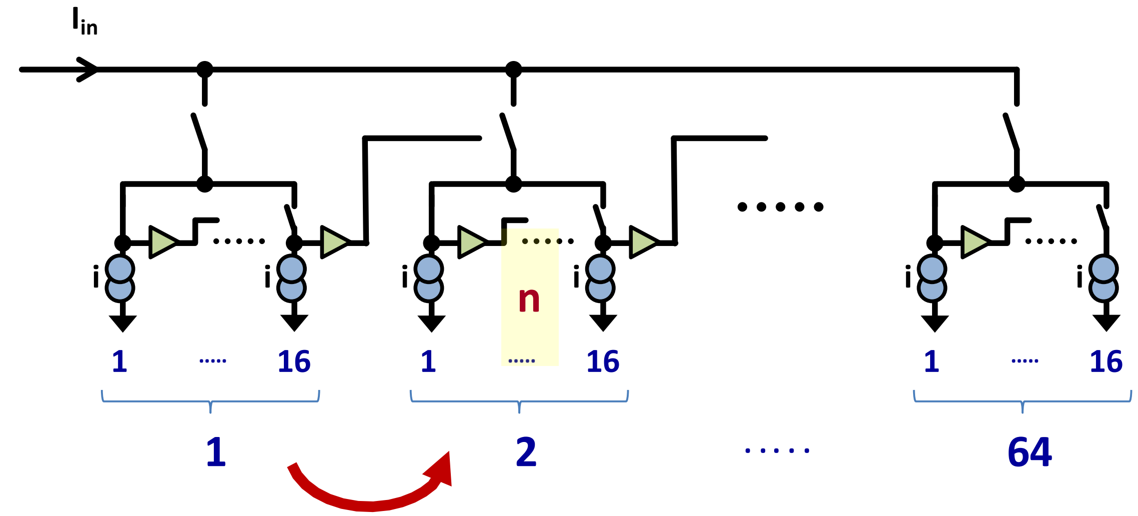
# 10-bit Current-Mode Domino **ADC** - Functionality

**ADC Cells**

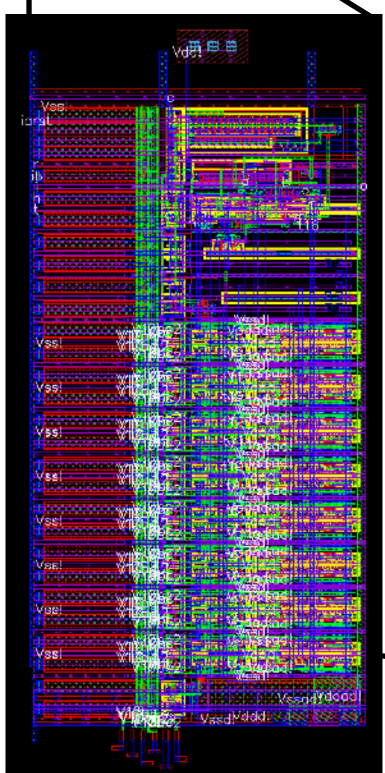


**8x macro-cells**






**1 macro-cell**

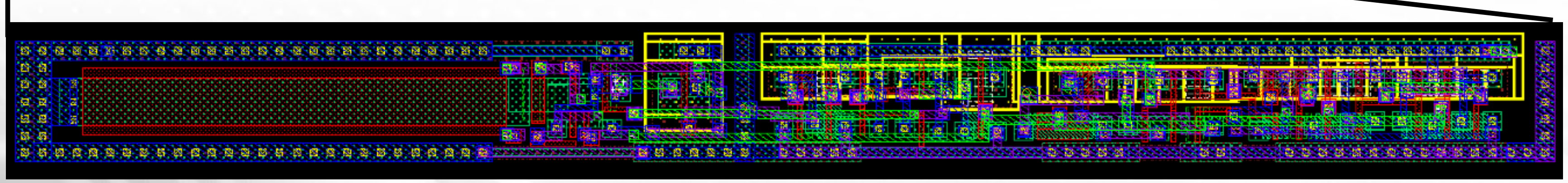


**16x micro-cells**

**<u>ADC Core (per channel)</u>**

- **1024** current sources (similar to a digital thermometer)
- **64** macro-shells (6 upper bits xxxxxx0000), **16** micro-shells (4 lower bits 000000xxxx)
- **2 step mode** - First the comparison identifies one of the 64 macro-cells Then on second step the lower 4 bits are identified (250ns adj conversion time)
- **8 bit ADC** is build in the similar way (5+3)
- **6 bit ADC** is a **single stage conversion** similar to the 64 macro shells with fast digitisation (50ns)

**1x micro-cell**



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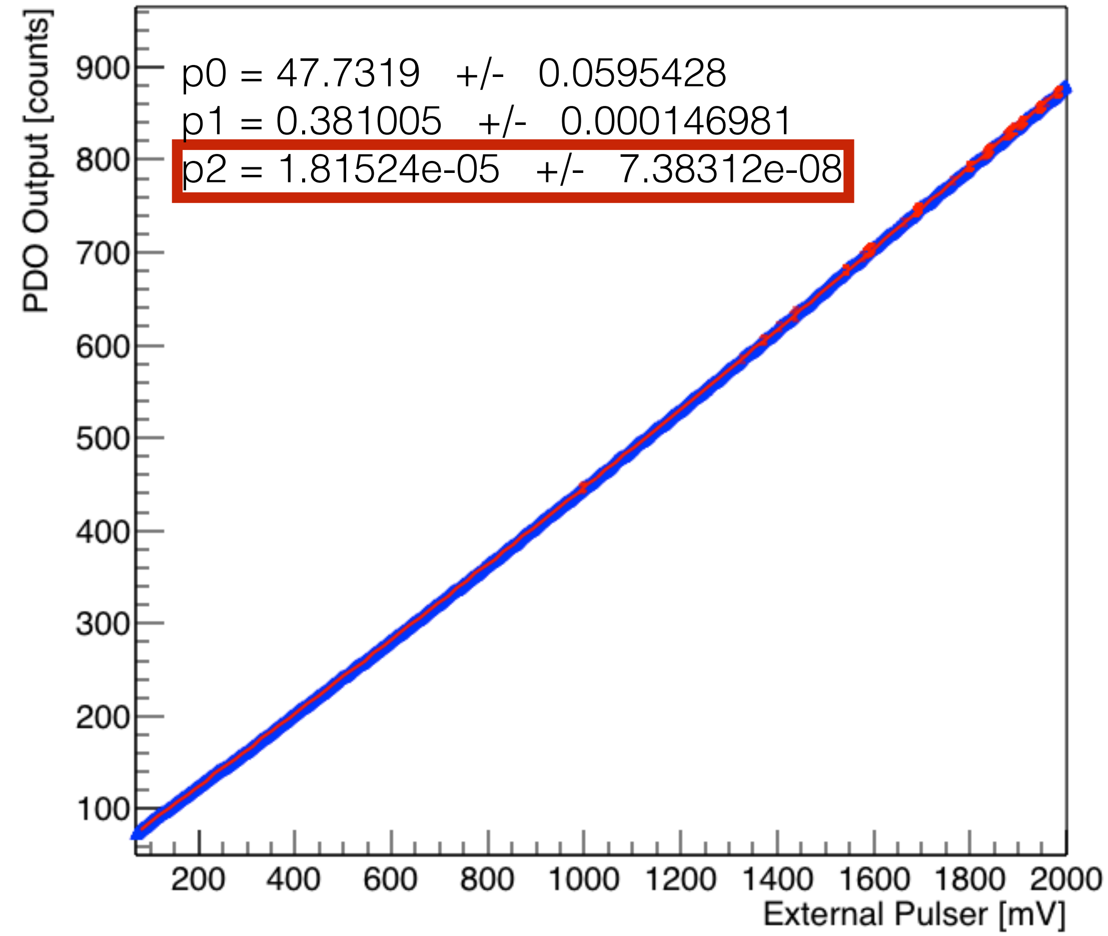
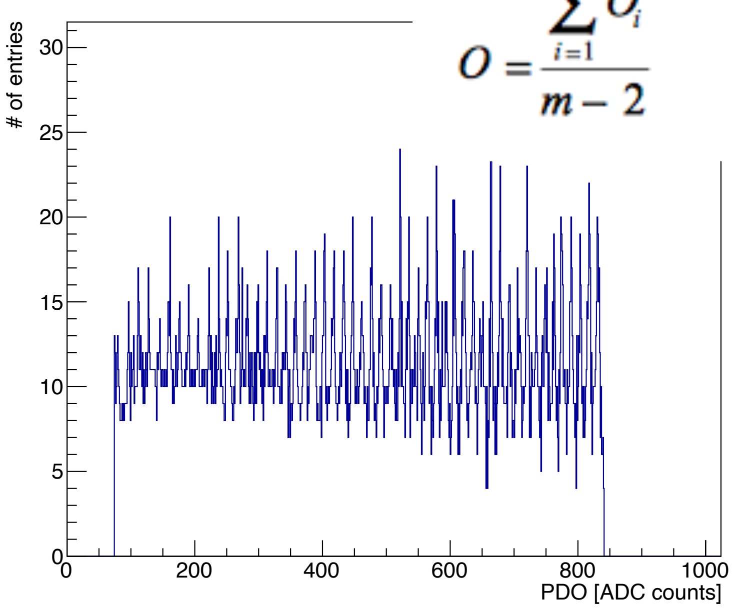
# ADC Performance - 10bit example

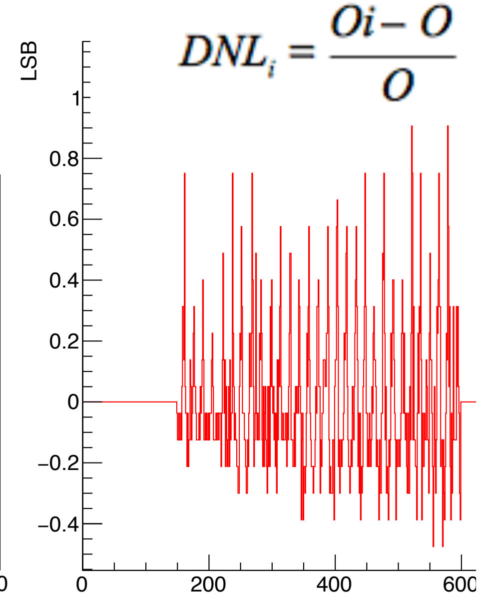
- In order to evaluate the ADC performance, **a full scan** with fine step was performed
- The ADC cannot be driven with a sinusoidal waveform for accurate estimation of its “noise” from the FFT
- In that sense the **DNL** and **INL** is calculated and used to estimate the **ENOB** of the 10-bit ADC
- The non-linearity introduced by the ADC is of the order of $\mathbf{2x10^{-5}}$
- **Equivalent number of bits ~8 (noise free)** for the 10-bit ADC



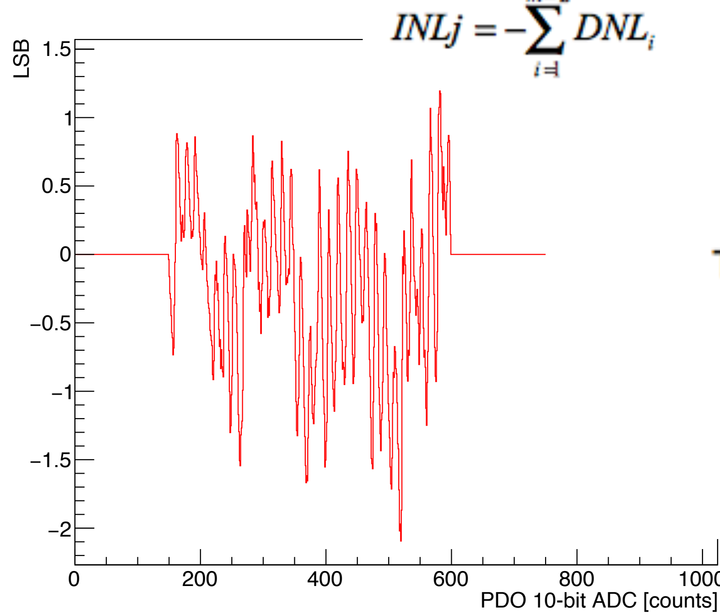

$$O = \frac{\sum_{i=1}^{m-2} O_i}{m-2}$$




$$DNL_i = \frac{Oi - O}{O}$$




$$INLj = -\sum_{i=1}^{m-2} DNL_i$$

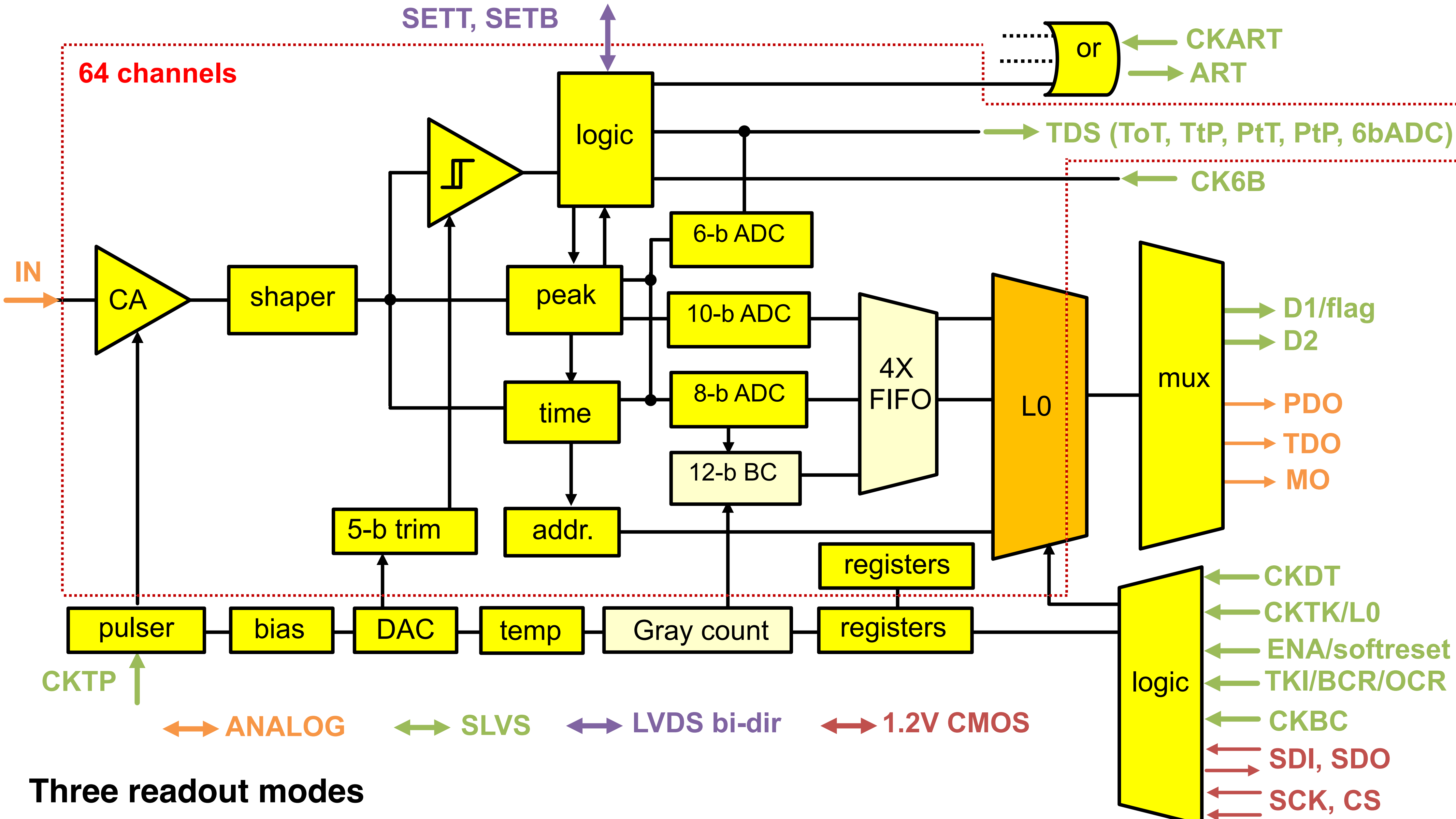



$$\sigma_c = \sqrt{\frac{1}{12} + \frac{1}{m-2}\sum_{i=1}^{m-2} INL_i^2}$$

Then, ENOB can be calculated as

$$ENOB = \log_2 \frac{m}{\sigma_c \sqrt{12}}$$

# VMM3a Readout & Overall **Architecture**



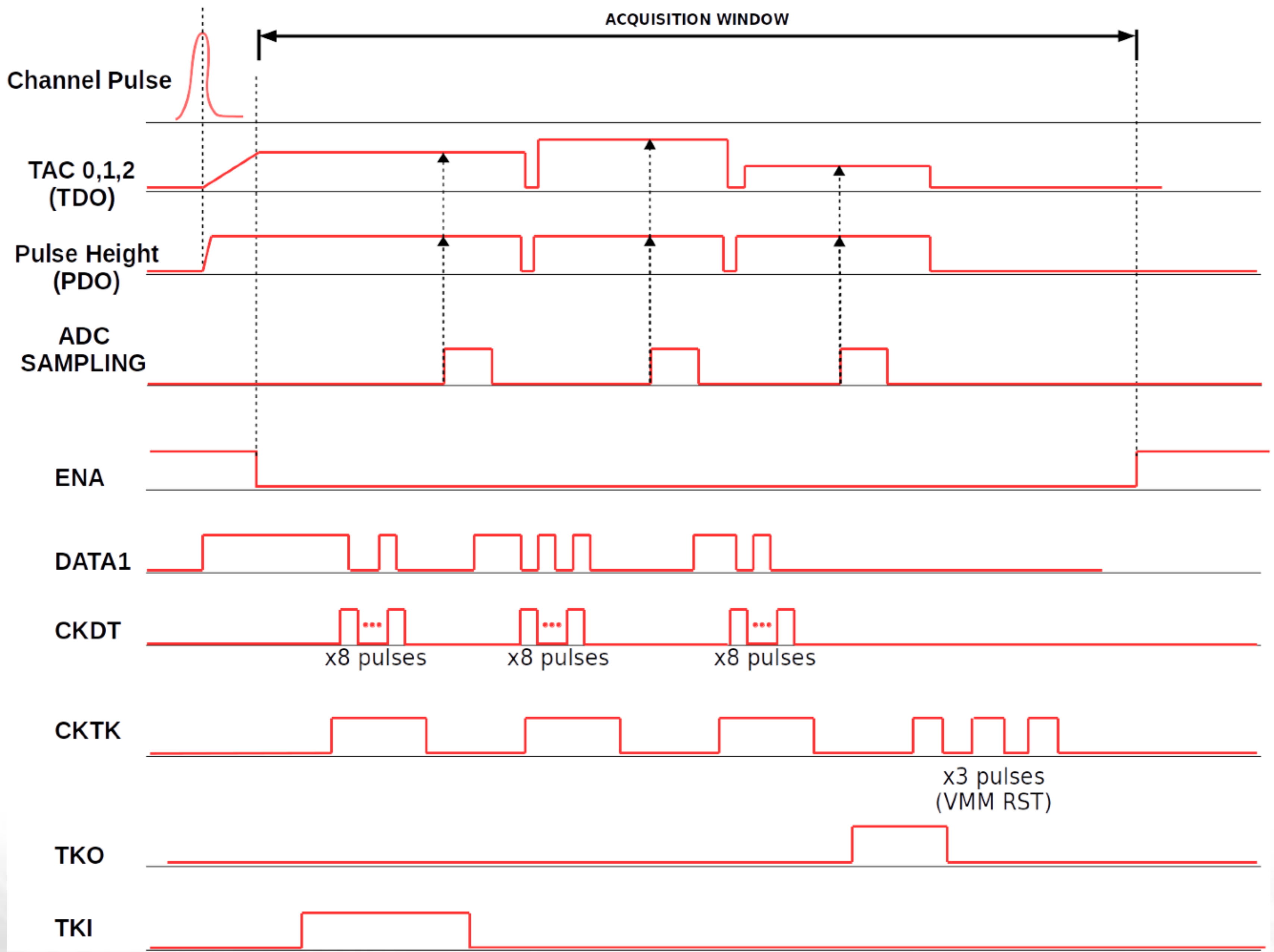

| | |
|---|---|
| flg | 1-bit |
| thr | 1-bit |
| addr | 6-bit |
| ampl | 10-bit |
| time | 8-bit |
| BC | 12-bit |

**Three readout modes**

- **Mixed** mode with peak & time analog output + address **(external ADCs)**
- **Digital continuous** with **internal ADCs** and 38-bit data at 2 outputs with 200MHz DDR, **trigger-less** or with **external trigger** and auto reset
- **Level-0** processor **external trigger mode** with 64-deep latency FIFO programmable acceptance windows with 8b/10b encoding. Each channel could achieve 4MHz, total latency 16us

# Modes of operation - Analog

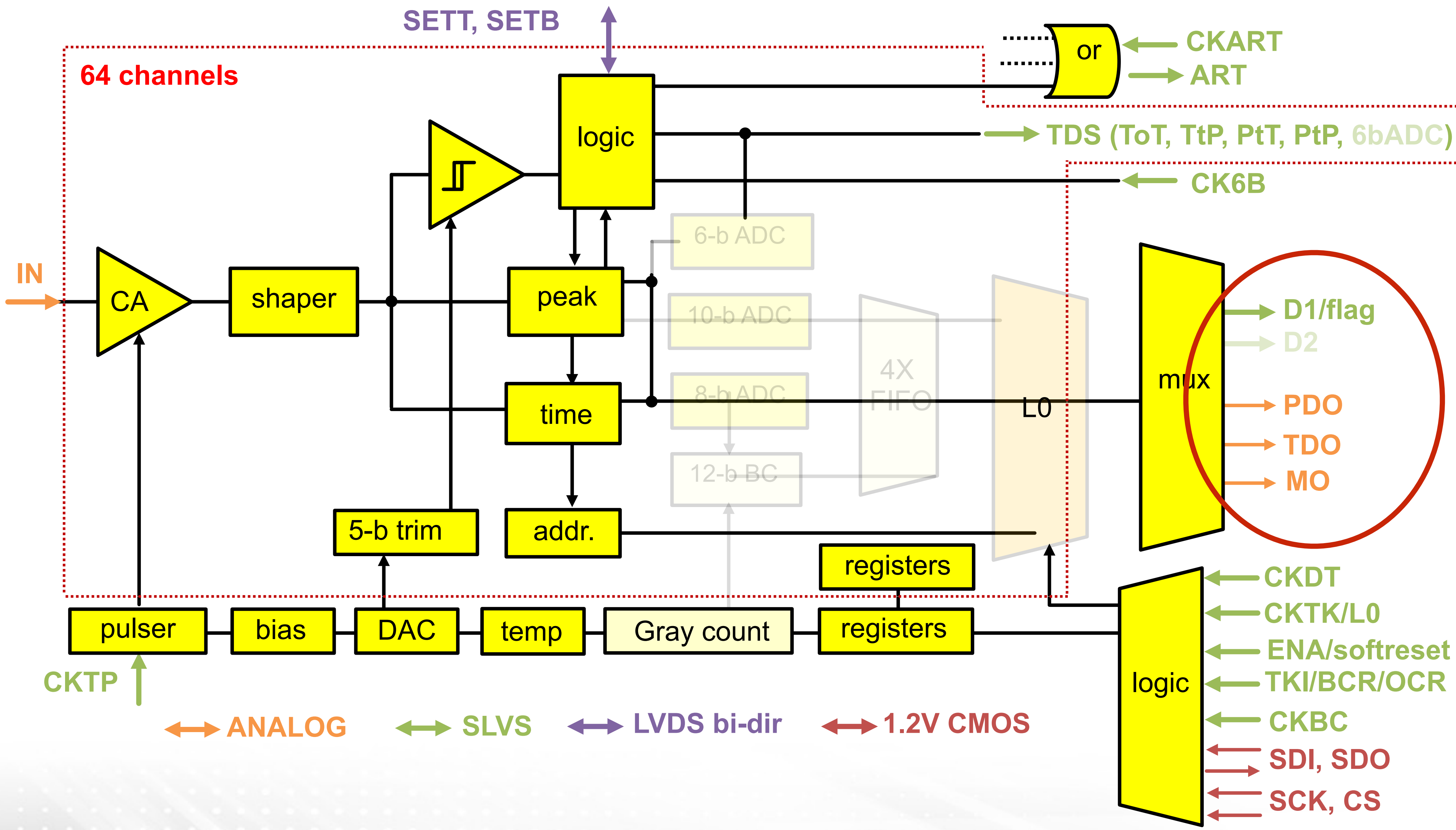
- In two-phase (analog) mode which is the mode originally implemented in the VMM1, the ASIC operates in two separate phases: **acquisition** and **readout** - During the acquisition phase the events are processed and stored in the **analog memories** of the **peak and time detectors**. As soon as a first event is processed, a flag is raised at the digital output.




- Once the process is complete the **ASIC can be switched readout phase**. The first set of amplitude and time voltages is made available at the **analog outputs**. The **address of the channel is serialised** and made available at the digital output using **six data clocks**.

# Modes of operation - Analog

- In this mode all **analog buffers are multiplexed** in the analog outputs
- Lengthy operation since each analog signal needs to be sampled while the address is read out serially

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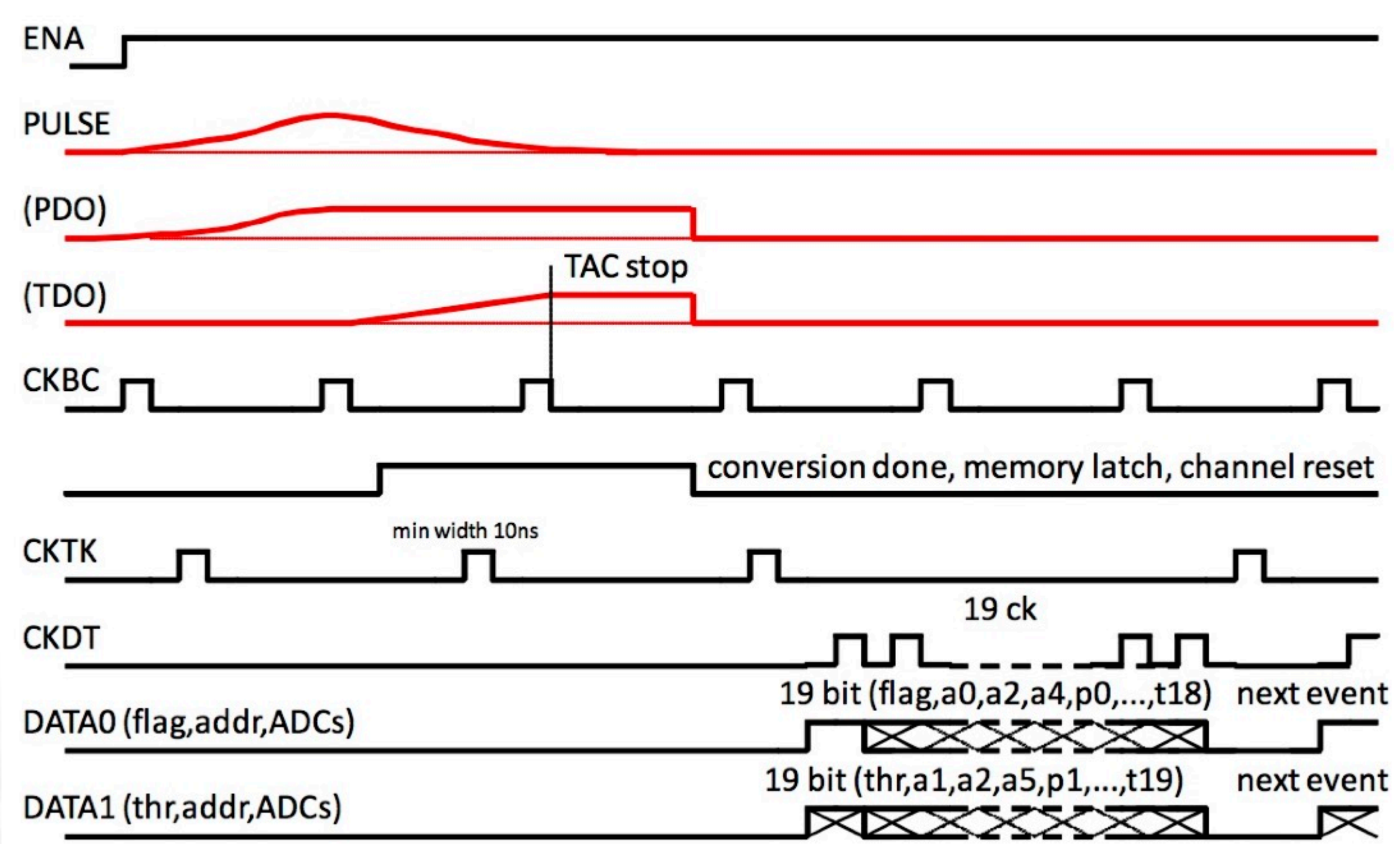
# Modes of operation - Continuous

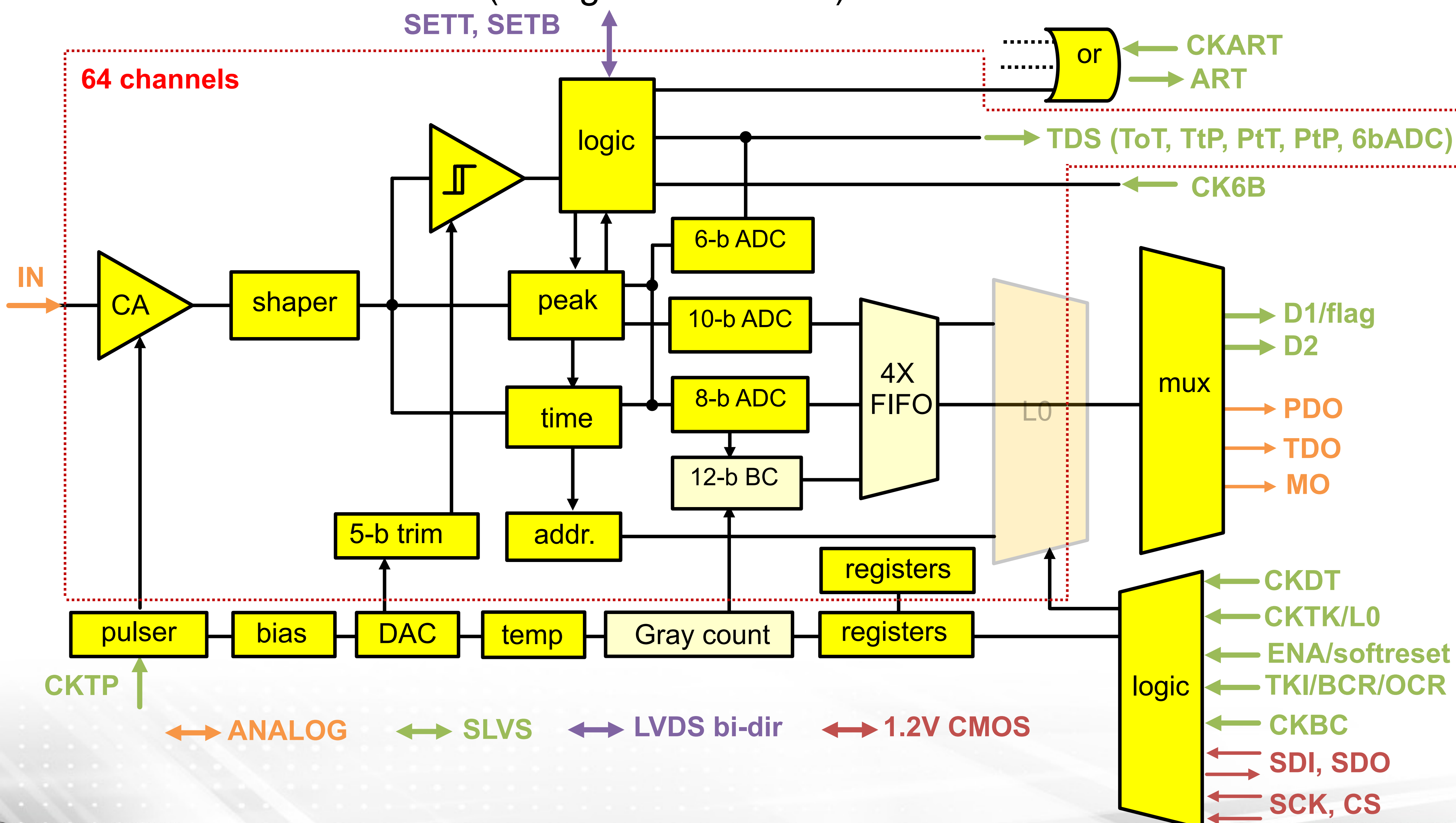
- Trigger-less mode with **peak and time detectors convert the voltages into currents** routed to the **6/10-bit ADC and 8-bit ADC respectively**.
- The 10-bit ADC provides a **high resolution** A/D conversion of the peak amplitude
- The 8-bit ADC provides the A/D conversion of the **timing (measured using the TAC peak** or the **threshold to a stop signal). Time associated with global 12-bit** counter.
- In the continuous mode the **64 channel direct outputs** are available as well providing time-over-threshold (ToT), threshold-to-peak (TtP), peak-to-threshold (PtT), or a 10 ns pulse occurring at peak (PtP) or the 6-bit ADC. The **channel self resets** at the end of the timing pulse, thus providing continuous and **independent operation of all 64-channels.**




| | |
|---|---|
| flg | 1-bit |
| thr | 1-bit |
| addr | 6-bit |
| ampl | 10-bit |
| time | 8-bit |
| BC | 12-bit |

# Modes of operation - Continuous

- This mode provides **continuous trigger-less readout**
- All the outputs and inputs are active and **independent**
- 6bit ADC conversion within 25ns (configurable + reset)
- 10bit ADC conversion at 200ns (configurable + reset) ← Leading dead-time per channel
- 8bit ADC conversion at 100ns (configurable + reset)

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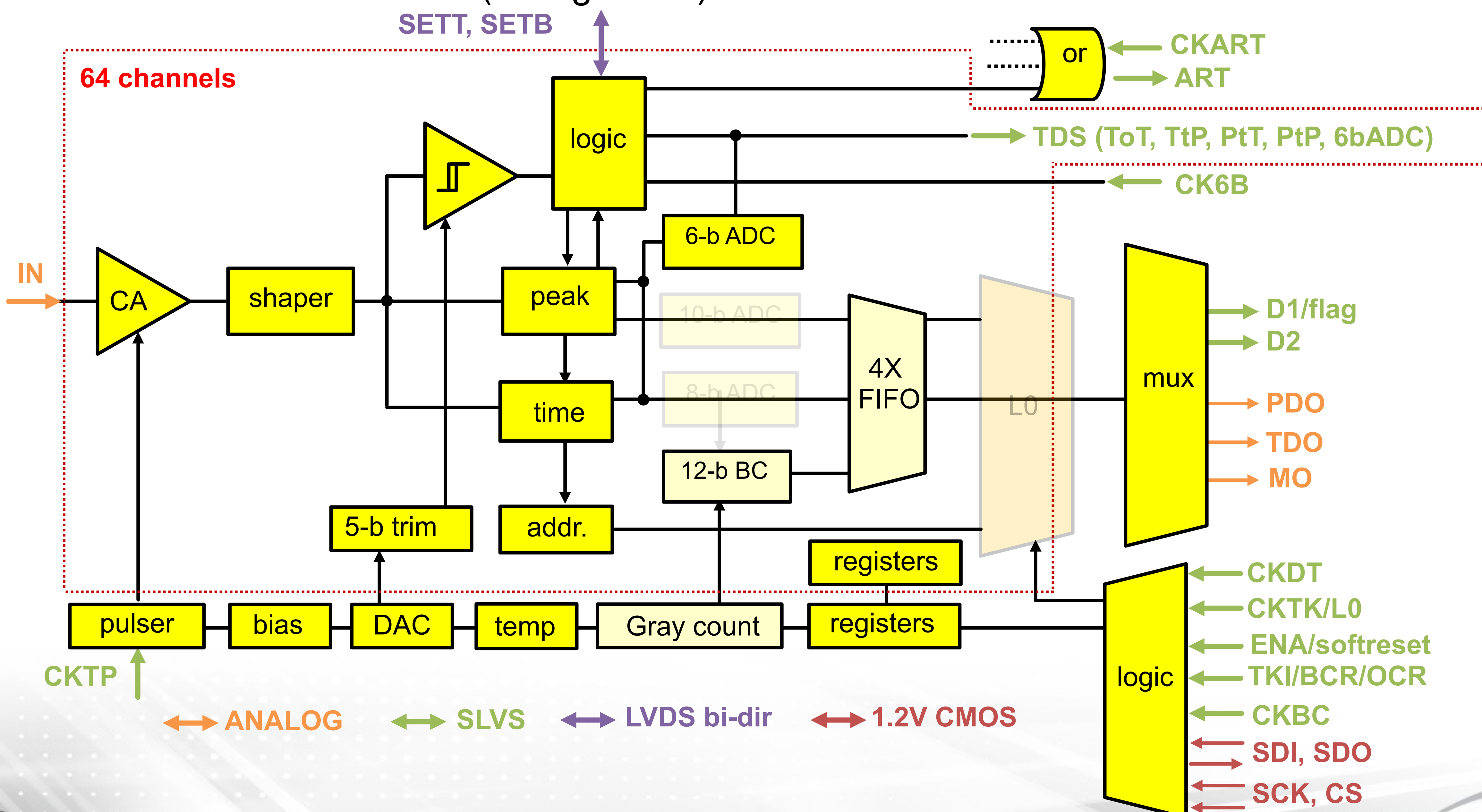
# Modes of operation - Direct output

- This mode provides **continuous trigger-less readout**
- All the outputs and inputs are active and **independent**
- 6bit ADC conversion within 25ns (configurable)
- 10bit ADC conversion at 200ns (configurable)
- 8bit ADC conversion at 100ns (configurable)

Enabling sfrst, channel resets after 6bit conversion ~ 50ns dead-time

~~Leading dead-time per channel~~

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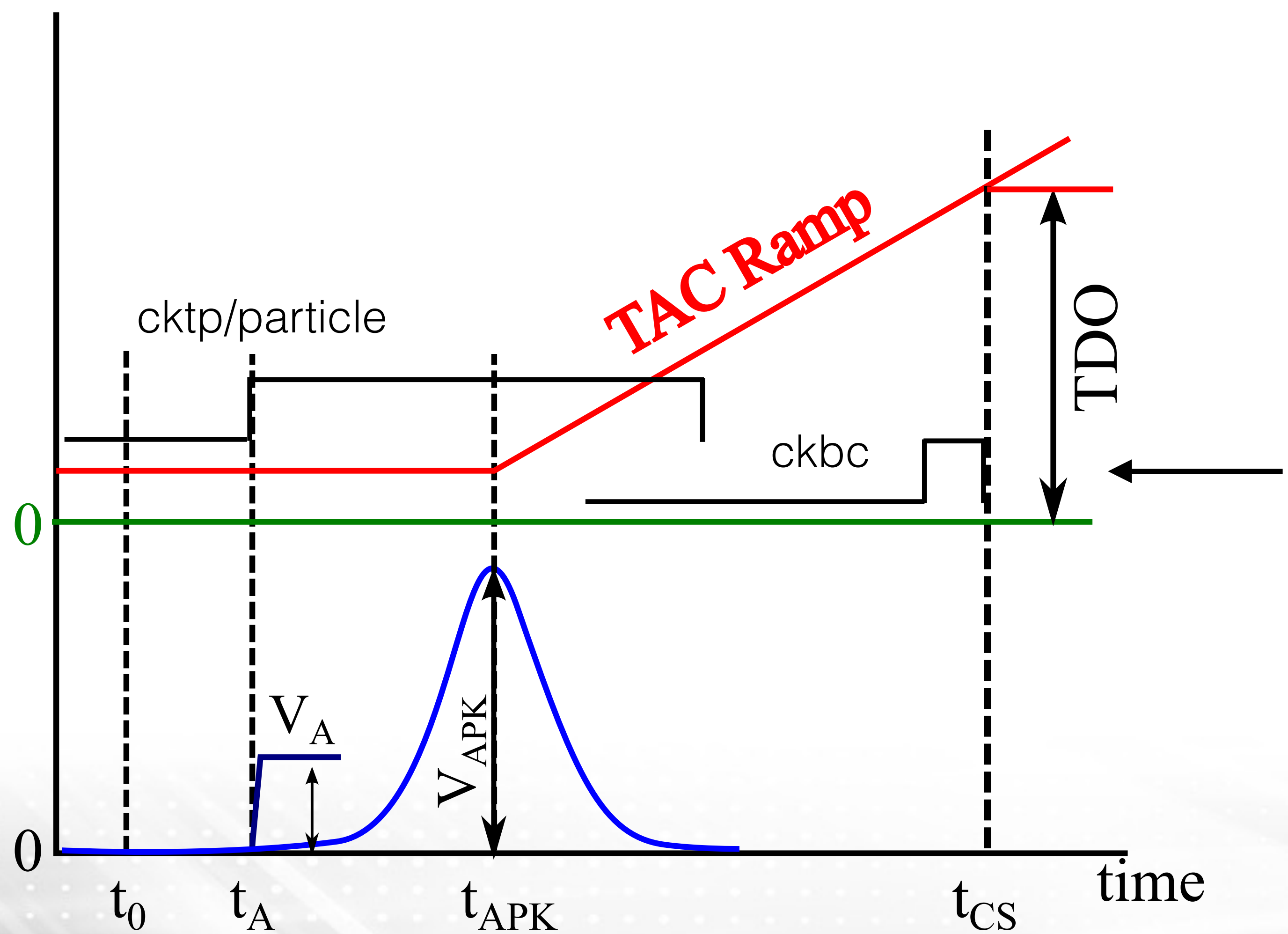
# Modes of operation - Continuous + ext trigger

- VMM design targets **synchronous** machines hence can be difficult to use in an environment like a **test beam where asynchronous operation** is needed but **precise timing** is needed to be measured (drift time)
- Most chips designed for synchronous machine **suffer from time jitter in such environment**
- On **VMM a mode was foreseen** to do such measurement where the **ckbc** can be used as a **strobe** and **not like a real clock**
- It can be **send as a trigger signal** with a **fixed latency** achieving precise time measurements




- Trigger signal from **external source**
- Can be combined with **register stcr** where **channel resets** if stop signal not occurs within the **TAC ramp**
- **Implies that trigger is propagated** within the TAC ramp up time (**60ns-650ns**)
- The **longer the TAC** though the **lower the resolution** on 8-bit information from the ADC
- Highly correlated trigger readout and noise subtraction

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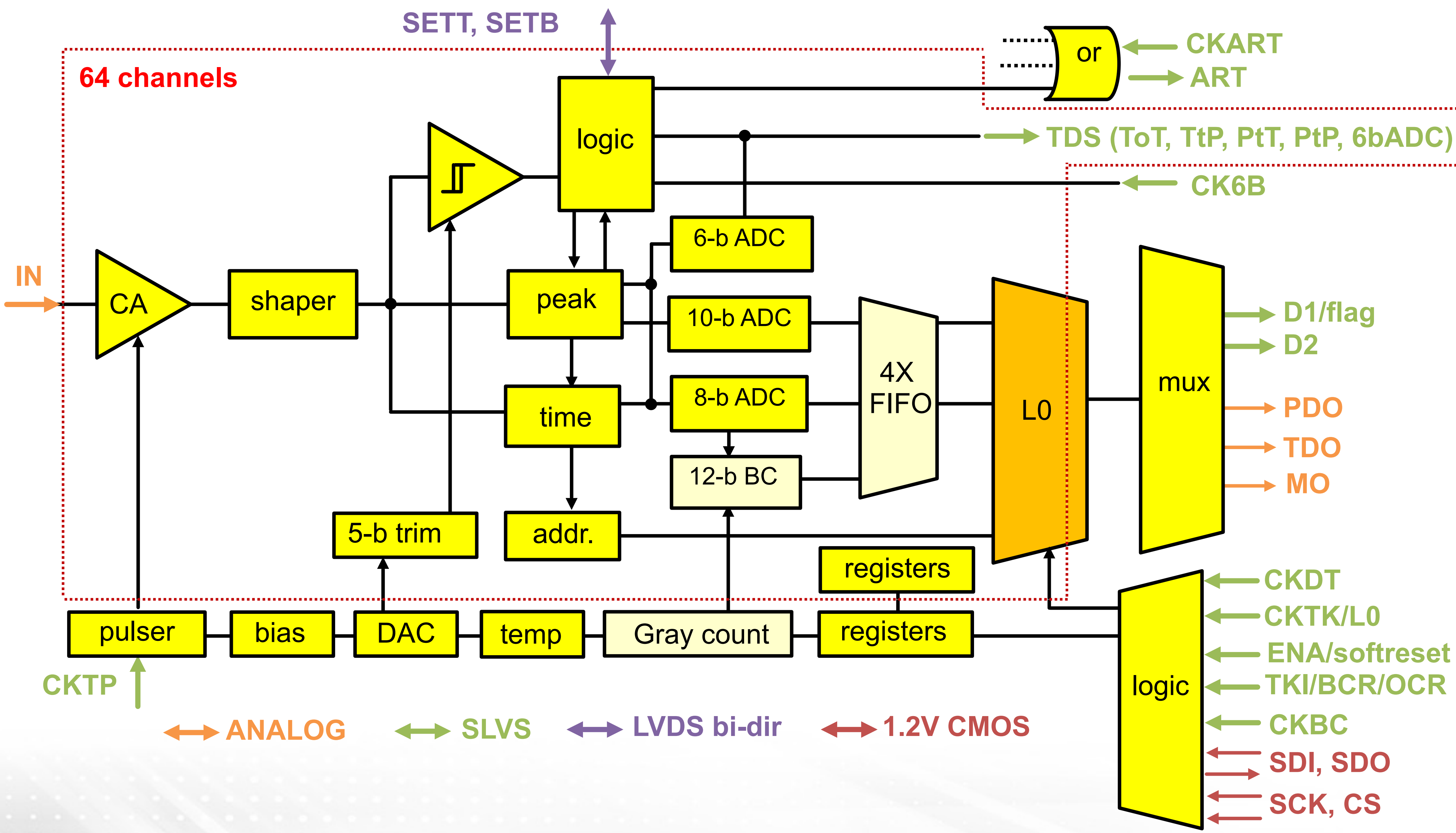
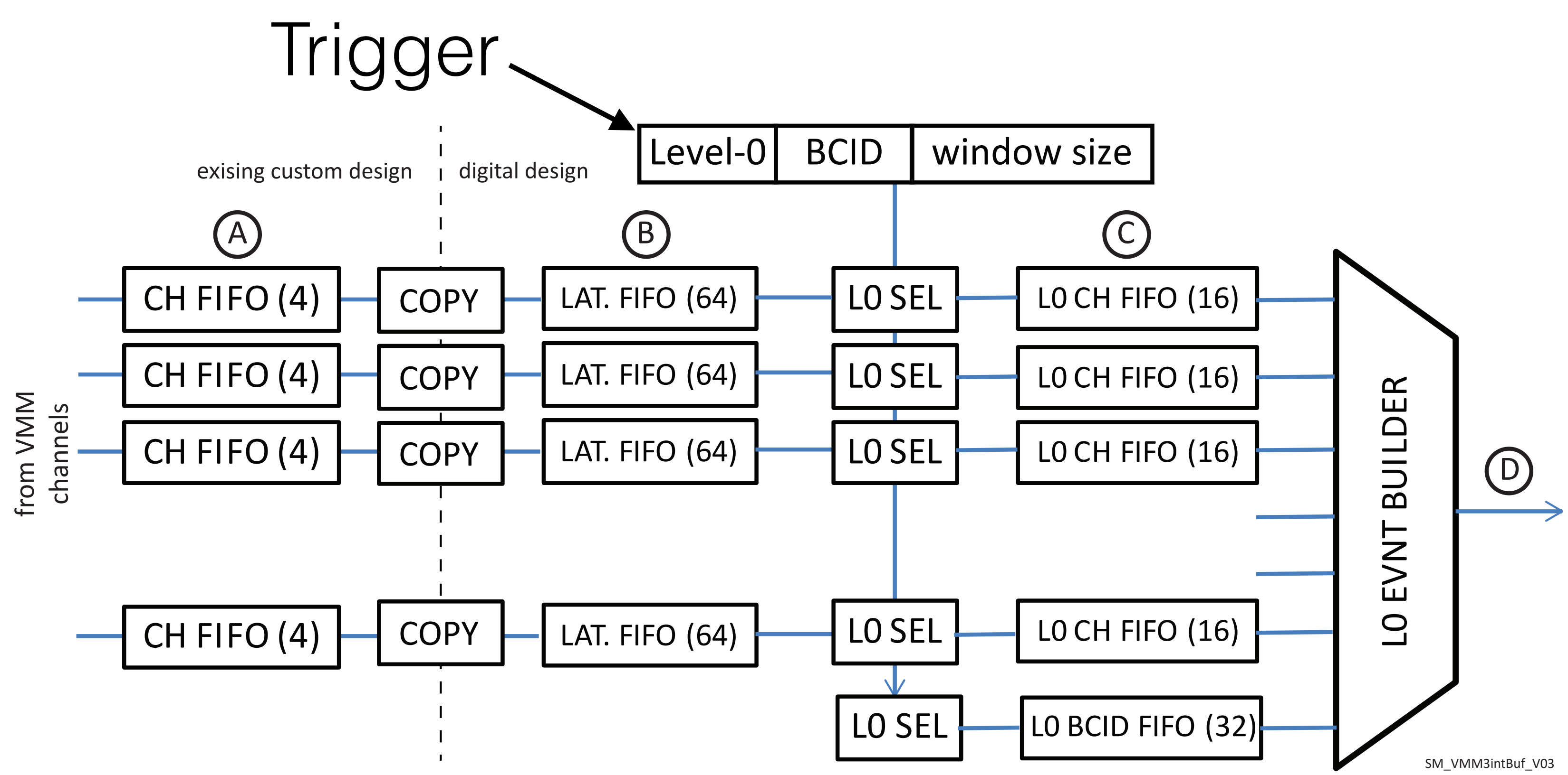
# Modes of operation - L0

- The **signal processing** is done in the **same way** but the **readout is different.**
- This is an **externally triggered operation** for **synchronous** machines



# Modes of operation - L0

- **Each channel has a Level-0 Selector** circuit which is **connected to the output** of the channel's latency FIFO.
- The **selector finds events within the BCID window** (maximum size of 8 BC clocks) of a Level-0 Accept and **copies them to the L0 Ch FIFO**. The data are available in the output which is running on **IDLE K28.5** in two data lines and can be readout **DDR at a speed of 640Mbps** (160MHz clock tested, effective bandwidth 560Mbps due to 8b/10b encoding).

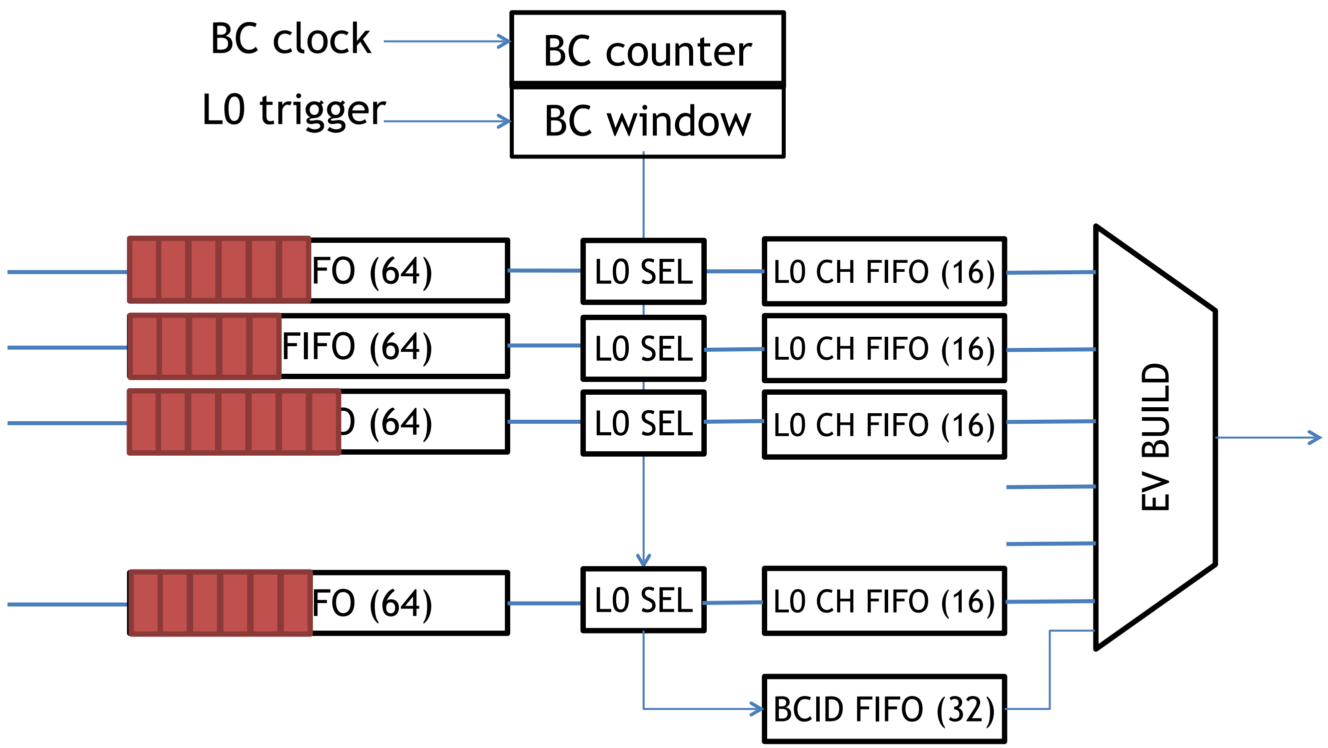



- VMM will build the event with common BCID +relative for each hit
- Header is sent out once no data found

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| header | V | P | orb | | BCID (12) | | | | | | | | | | | | 1st word after comma | | | | | | | | | | | | | | | |
| hit data | 1 | P | *R* | T | Chan# (6) | | | | | | ADC (10) | | | | | | | | | | TDC (8) | | | | | | | | N | rel BCID | | |

LL_format_VMM3out_V04

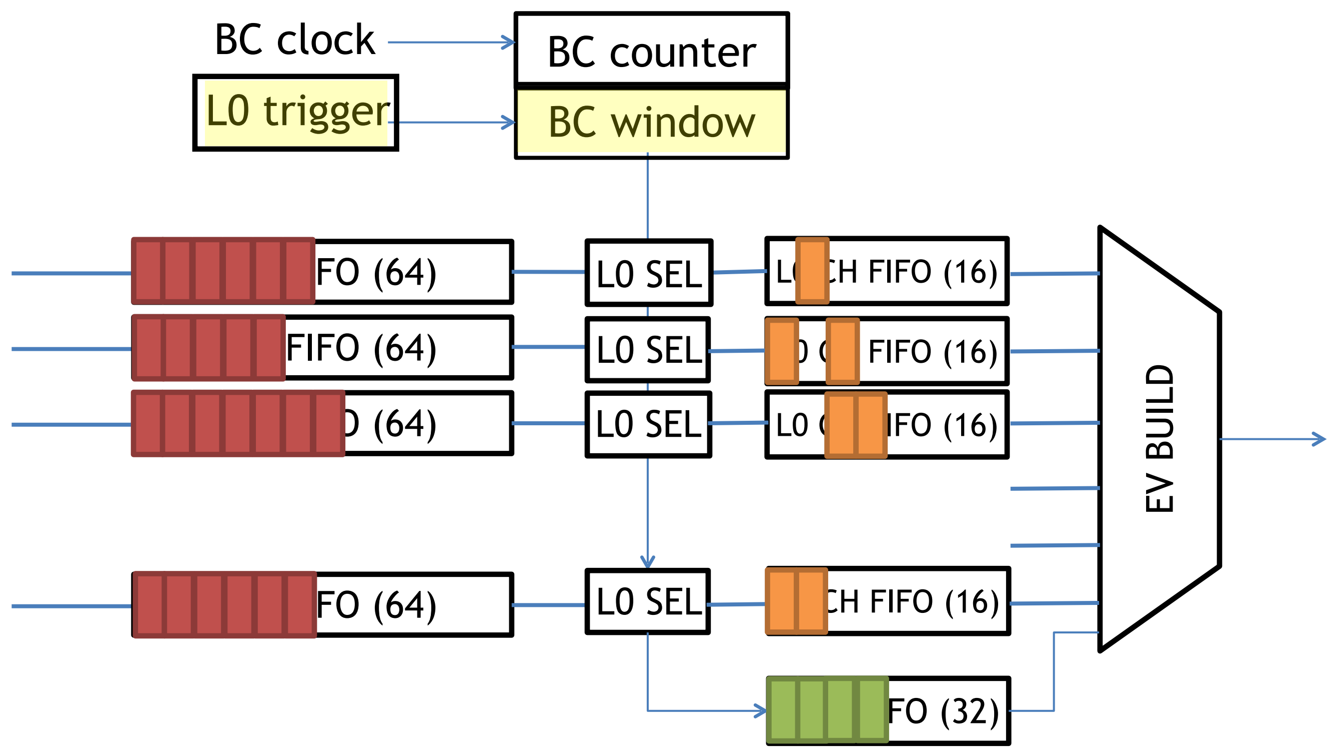
# Modes of operation - L0




**Latency FIFO** takes data from the mixed-signal front-end

- FIFO designed to accommodate 4 MHz data in a 10 μs latency window
- 20-bit data: threshold, amplitude (ADC), timing (ADC)

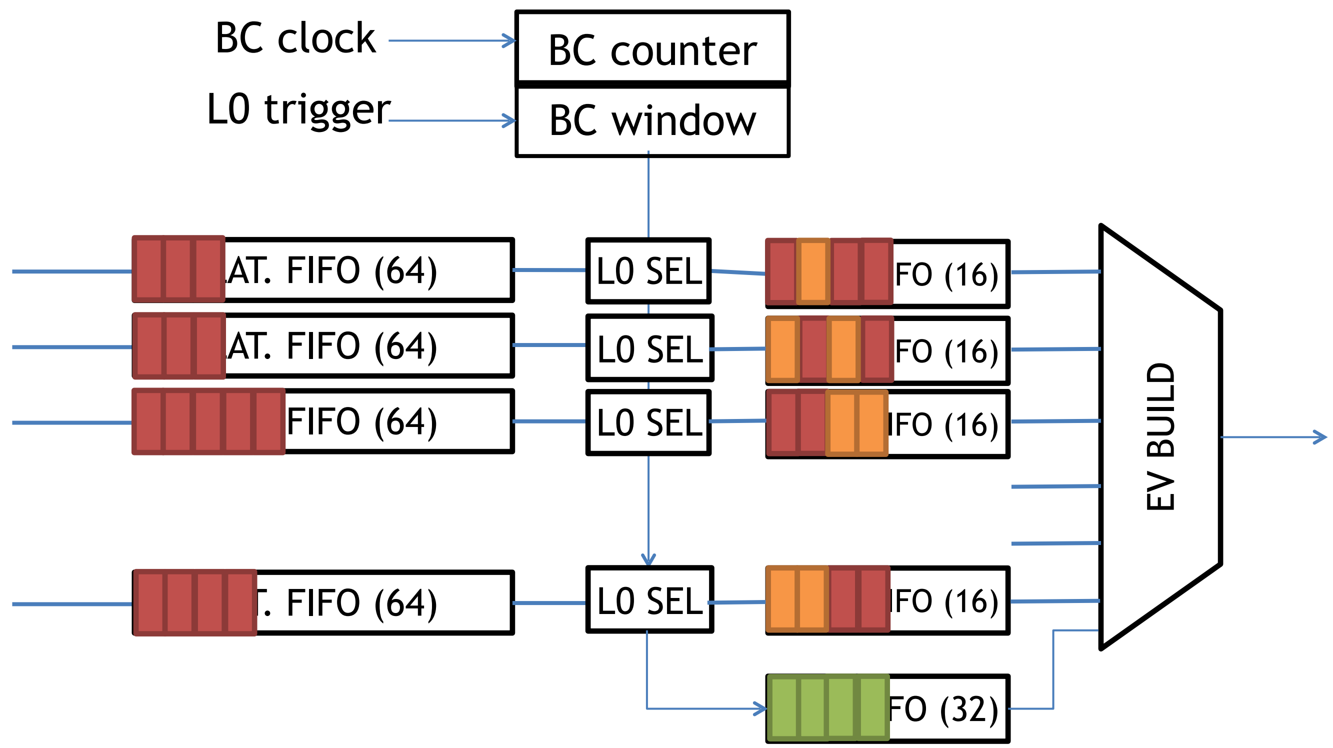
# Modes of operation - L0




At **L0 trigger** builds BC trigger window and **selects data** for the L0 CH FIFO

- flushes old data
- fills non-valid data as needed (for simultaneous overflow)
- builds BCID FIFO

# Modes of operation - L0



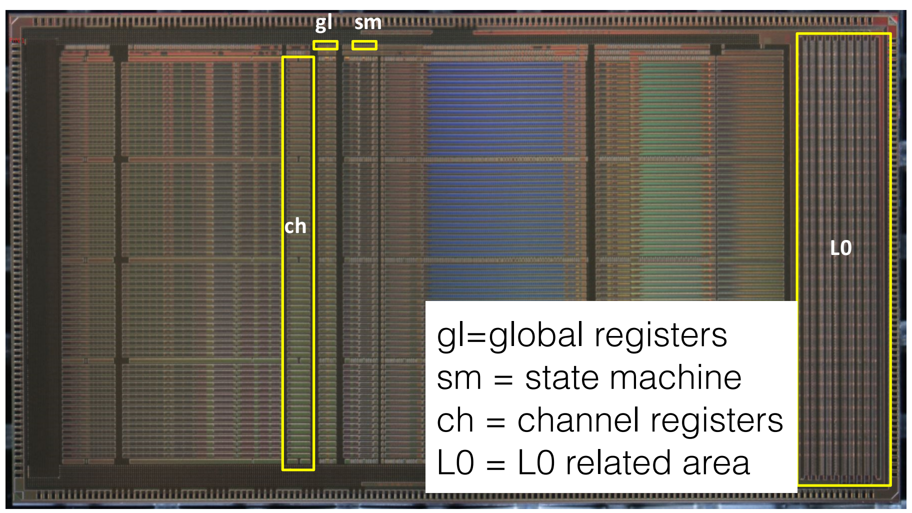

**Builds event**

- BCID followed by valid data with address
- header
- event built in < 1μs

**Sends data** through two data links (DDR, 640MB/s)`

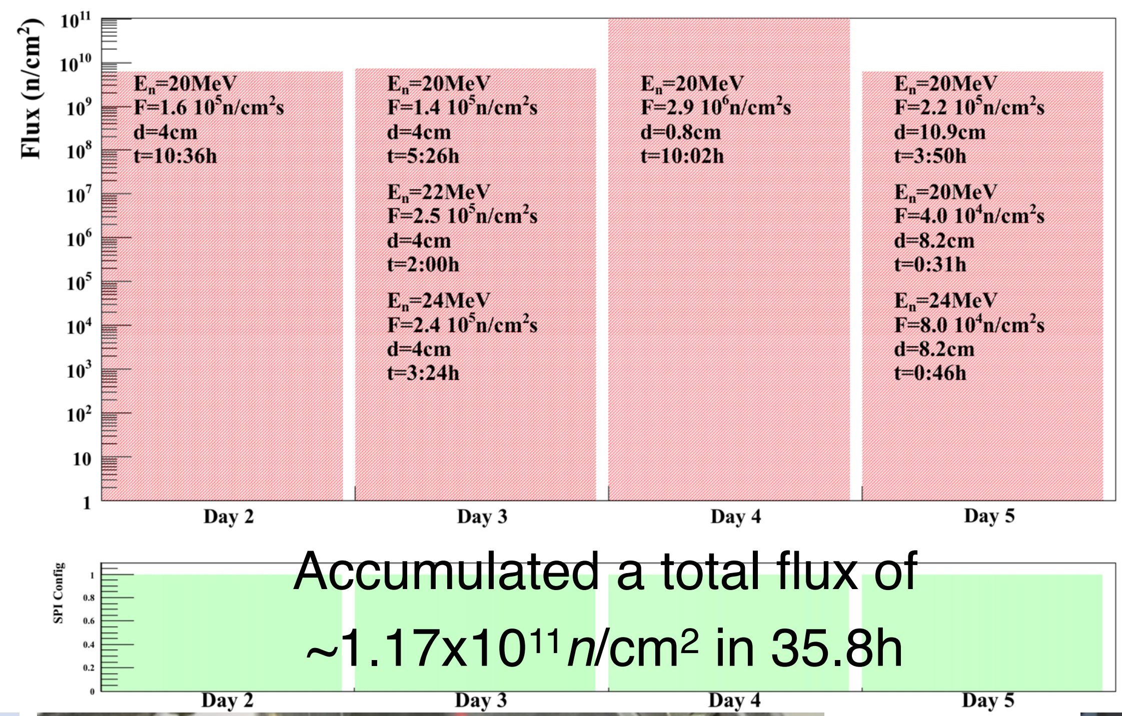
# Single Event Upset & Total Ionisation Dose

- In the VMM3a there are **three types of storage elements** that require SEU protection, the **configuration registers**, the **state machine** control logic and the **L0 logic**
- To mitigate for SEU two techniques are used:
  - **Dual Interlocked Cells** (DICE) for the protection of the configuration registers
  - **Triple Modular Redundancy** (TMR) for the state machines and the L0 Logic blocks
- L0 Data
  - Single-bit faults on data are flagged by a **parity bit**
  - The **parity** is registered in the FIFOs and **transmitted** outside

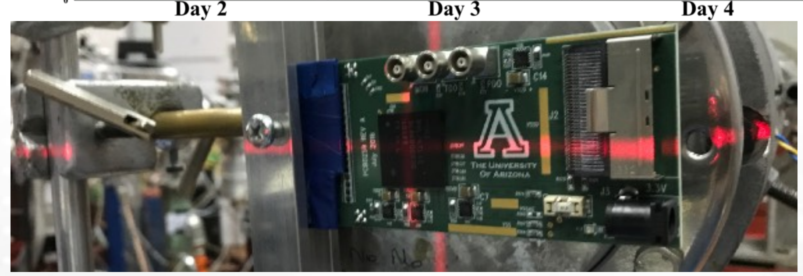



| Block | Method |
|---|---|
| BC counter | TMR |
| Latency FIFO CTRL | Parity on FIFO pointer, FIFO resets if parity err |
| L0 FIFOs Control | TMR |
| Event Builder | TMR |
| L0A register/Nskip circuit | TMR |

L0 block protection




Accumulated a total flux of ~$1.17 \times 10^{11}$ $n$/cm$^2$ in 35.8h

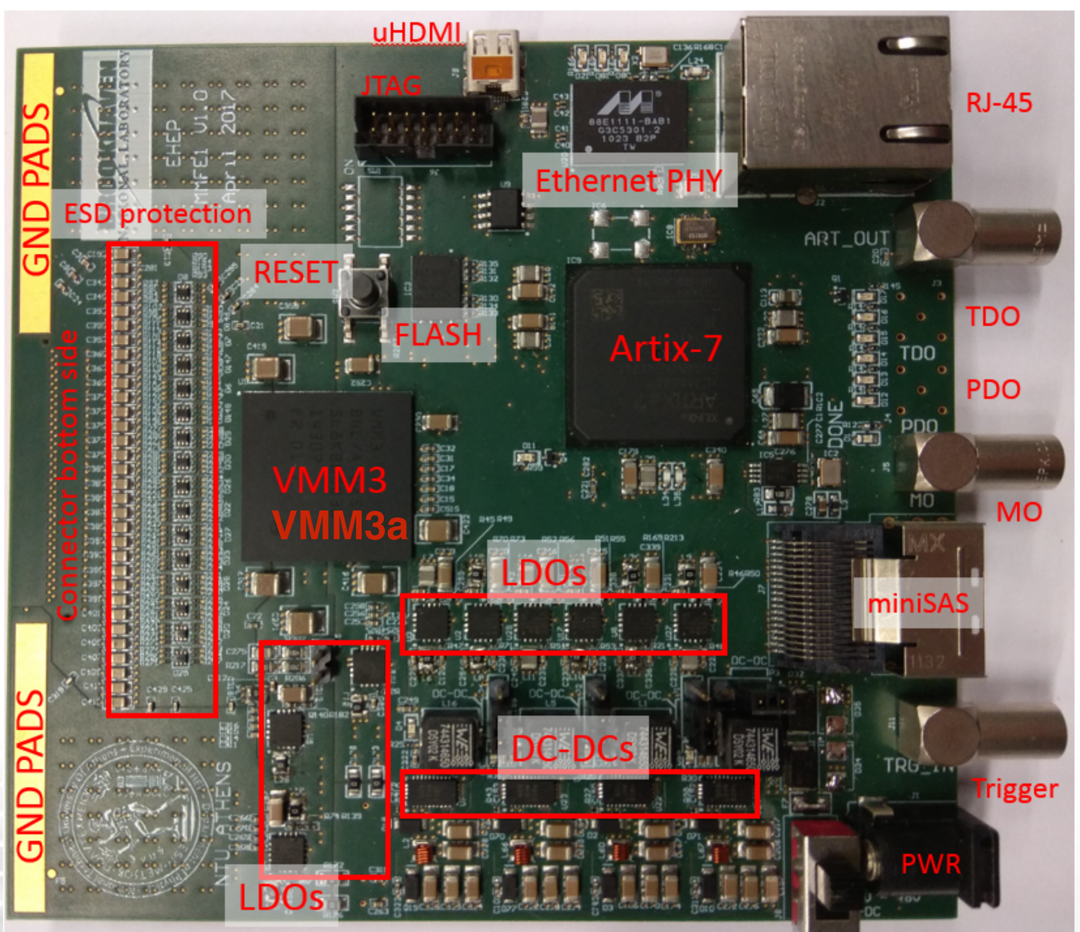


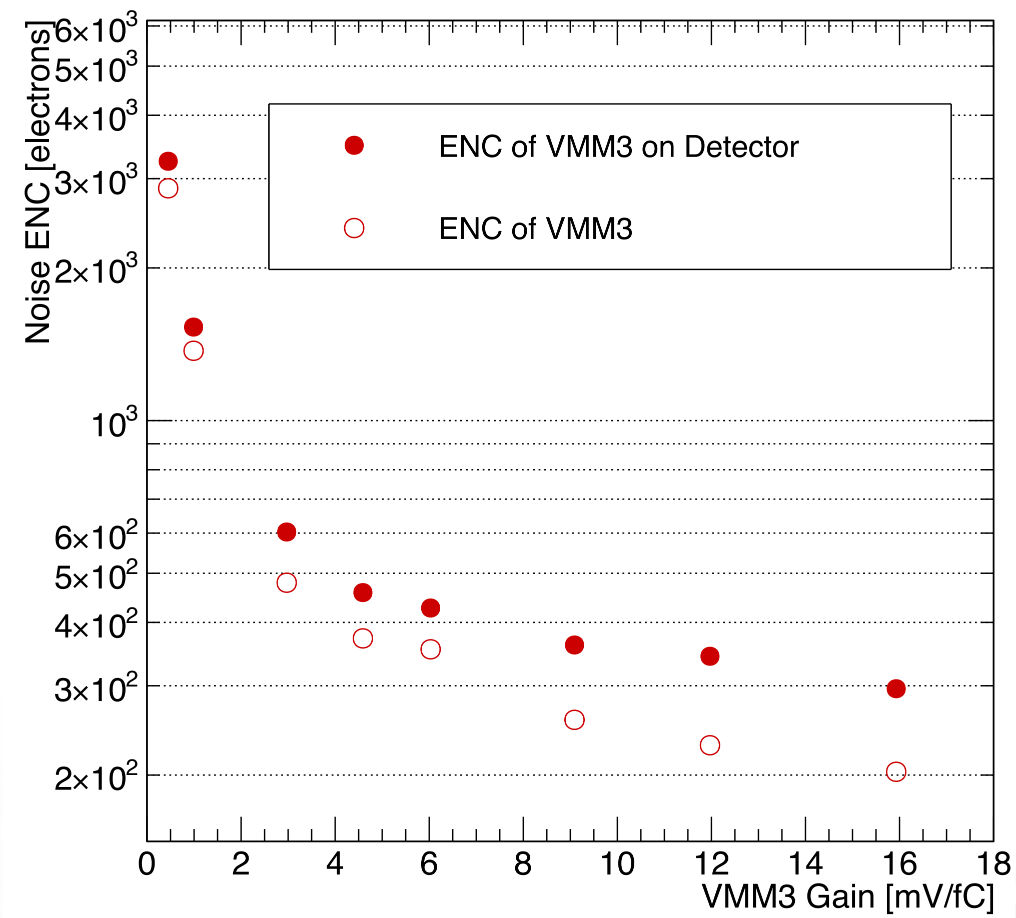
4 VMM3a were irradiated at the $^{60}$Co

# **Test Beams** with **Resistive - Micromegas** prototypes



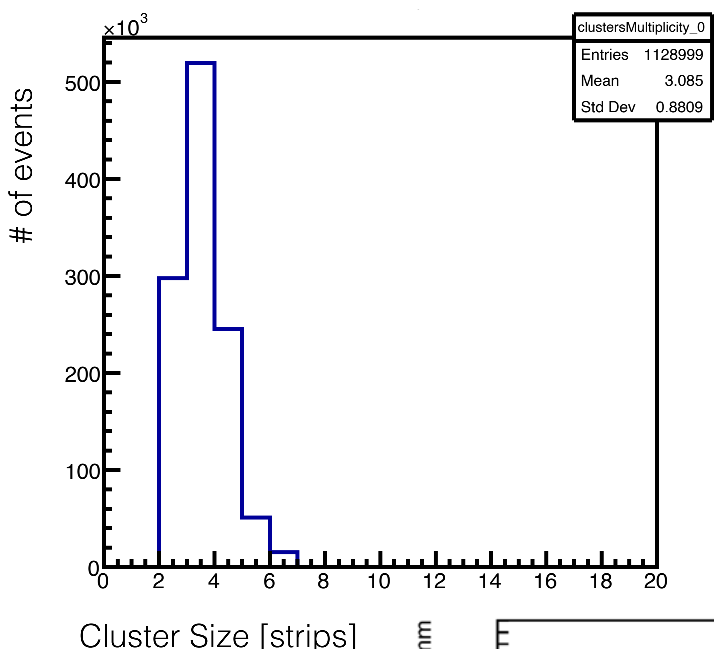
- **Setup** of of 2x MMFE1s on 2x Resistive Micromegas chambers (Ar+7%$CO_2$ 400µm pitch, 5mm drift)
- Custom made **firmware** and **software** was developed allowing to **trigger** with scintillator system
  - Mode to control the CKBC externally
- **High** data **rate** ~20KHz/channel (VMM can reach 4MHz), arrived at the limit of Gbps UDP connection
- **Noise** levels of 300 $e^-$ ENC at gain 9mV/fC, 200ns

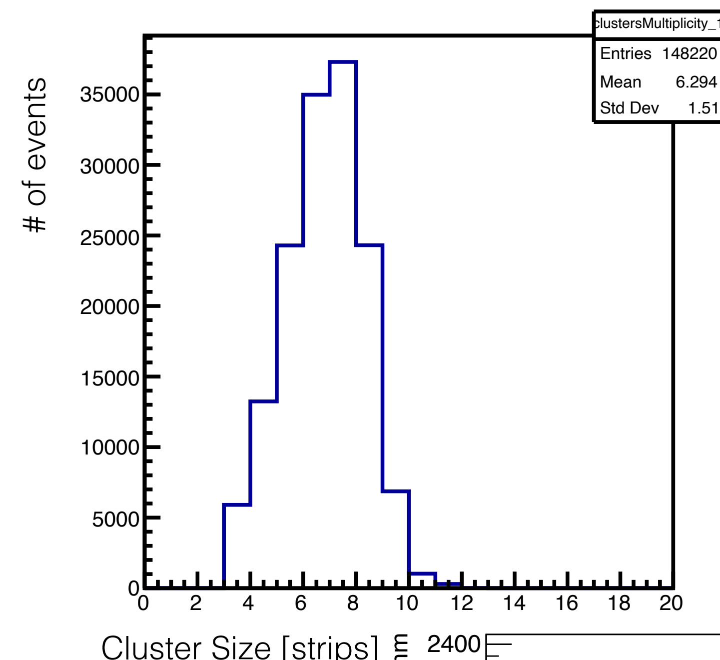


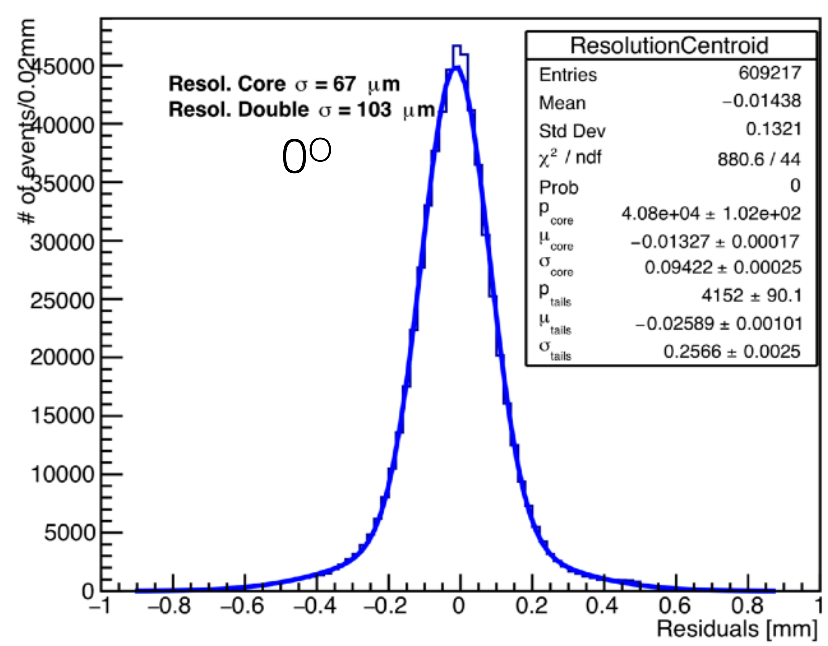



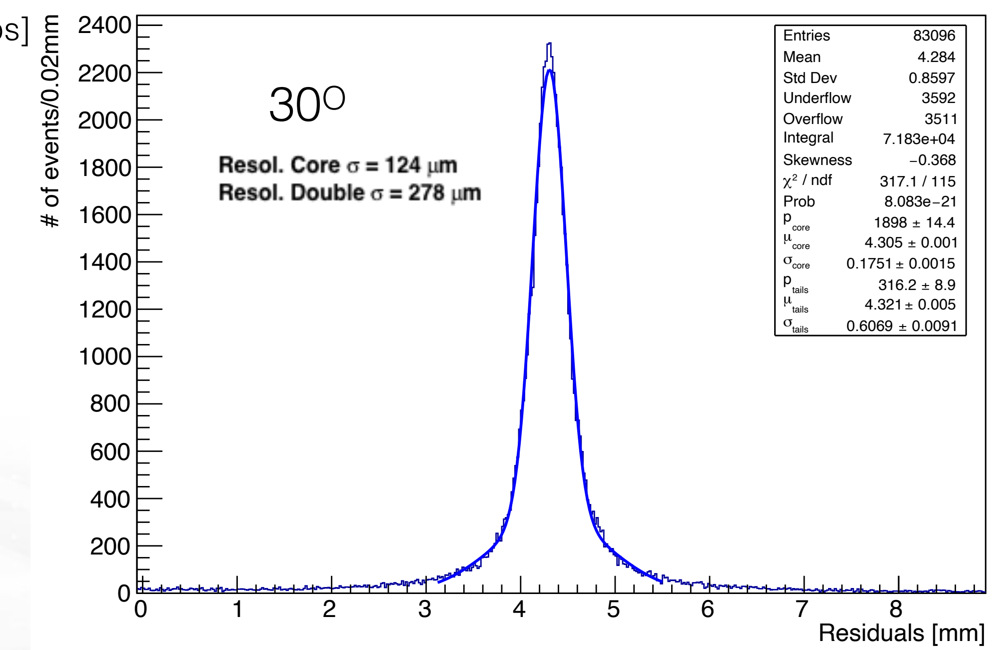
# Test Beams with Micromegas prototypes

- To form **clusters** of strips per particle hit **charge centroid** was used for perpendicular tracks and **μTPC** for tracks under an angle with a pattern recognition filter
- After **forming the clusters** the position **resolution** is measured by **subtracting** the space point reconstructed in different layers (identical layers)
- The spatial performance of the detectors is **satisfactory** for the NSW application



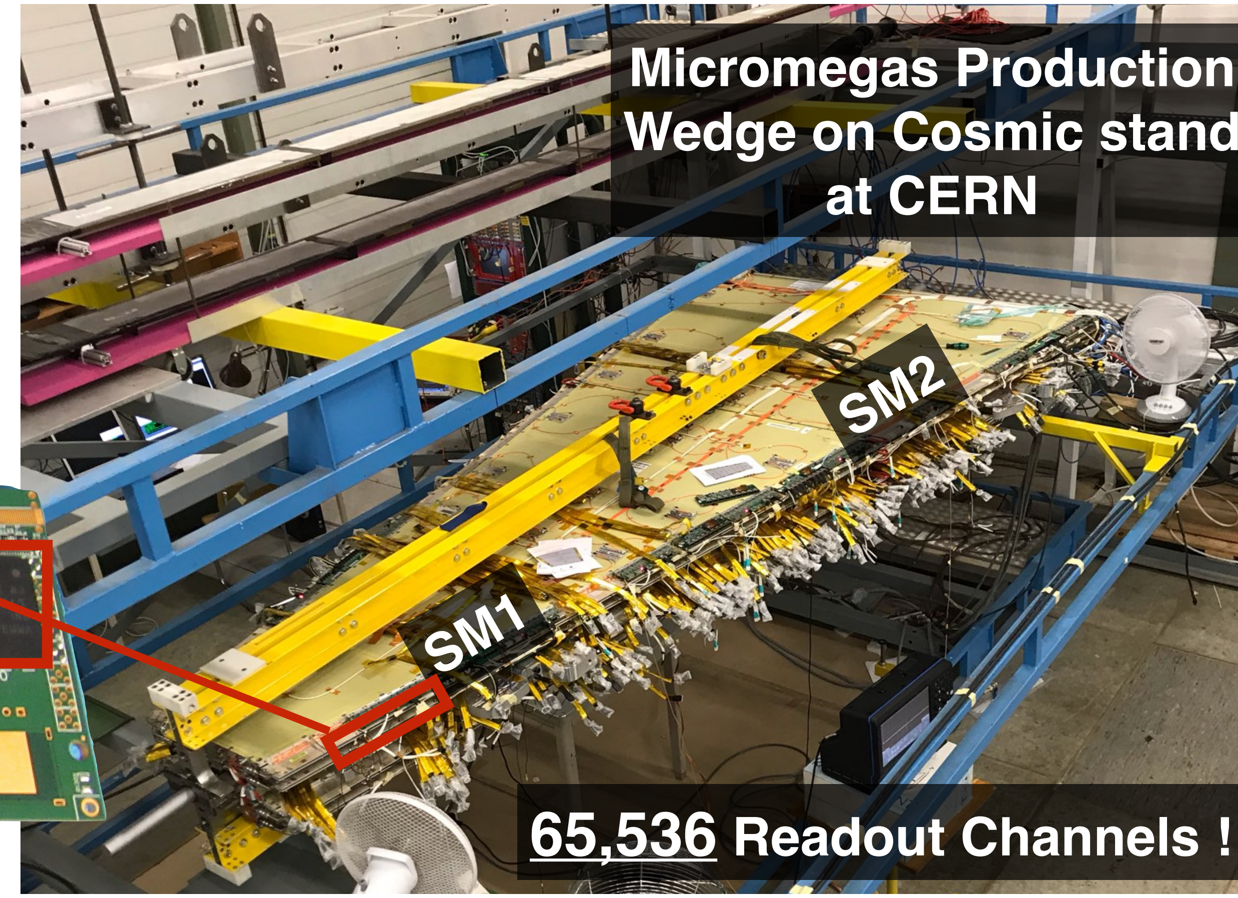



# **Integration** with Micromegas **Production** modules

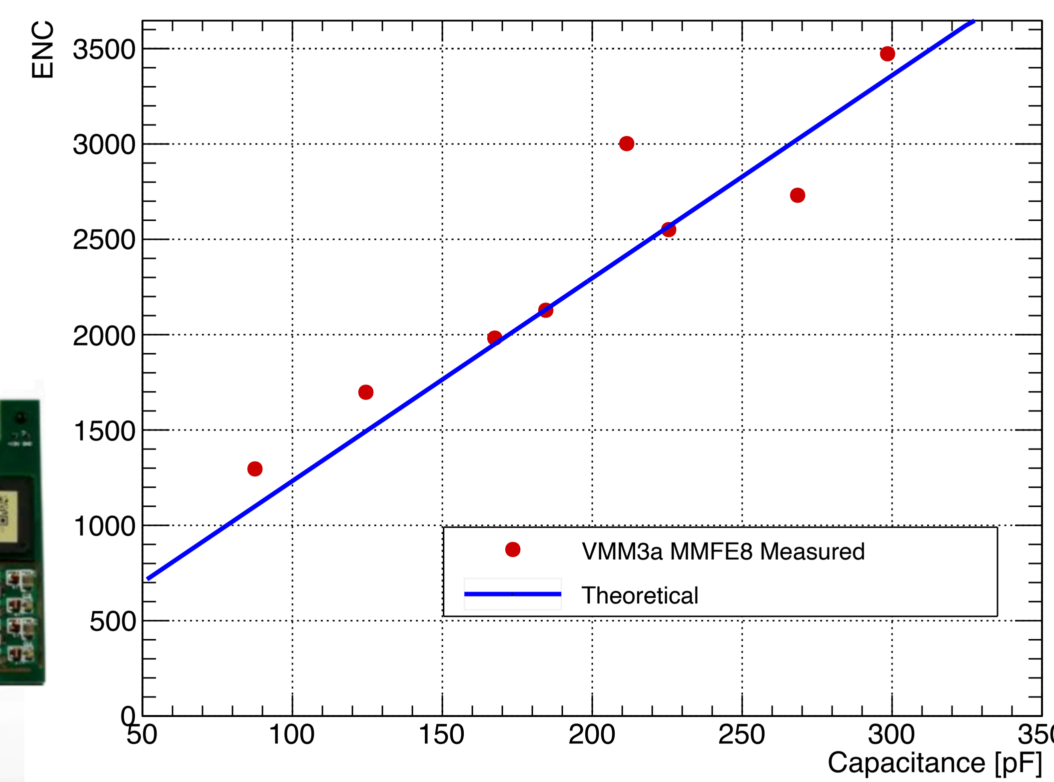
- **Micromegas** & sTGC Production modules at CERN integrating the VMMs
- All the FE boards are readout through custom made 4.8Gbit serialiser boards with fibres
- Water Cooling is a must in these applications




400-pin
21 x 21 mm²
BGA
1mm pitch



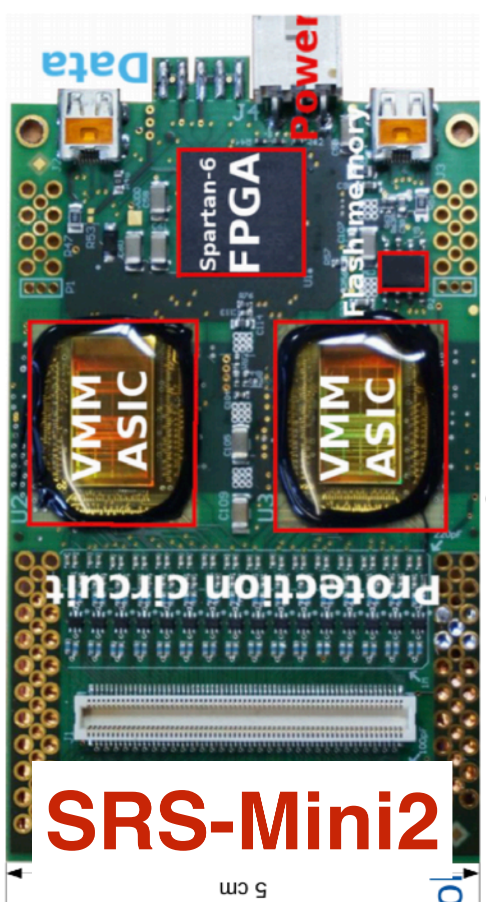




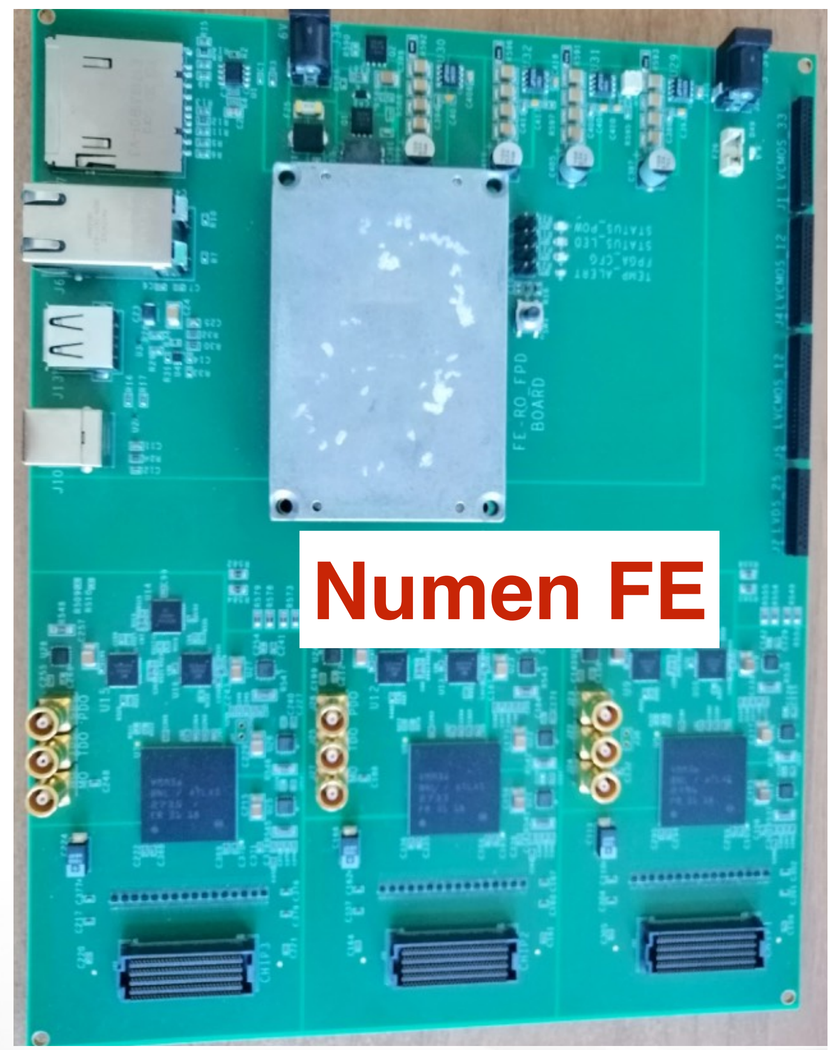
# Example of applications

**VMM** has been as well **of interest** and in some cases **already** made it in the following other than NSW applications:

- Focal Plane Detector for NUMEN
- Interest from n_TOF at CERN
- Mu2e at Fermilab
- DUNE Near Detector at Fermilab
- CERN RD51 SRS system (replace APV hybrids) which is a hub for **many other applications**




GPVMM

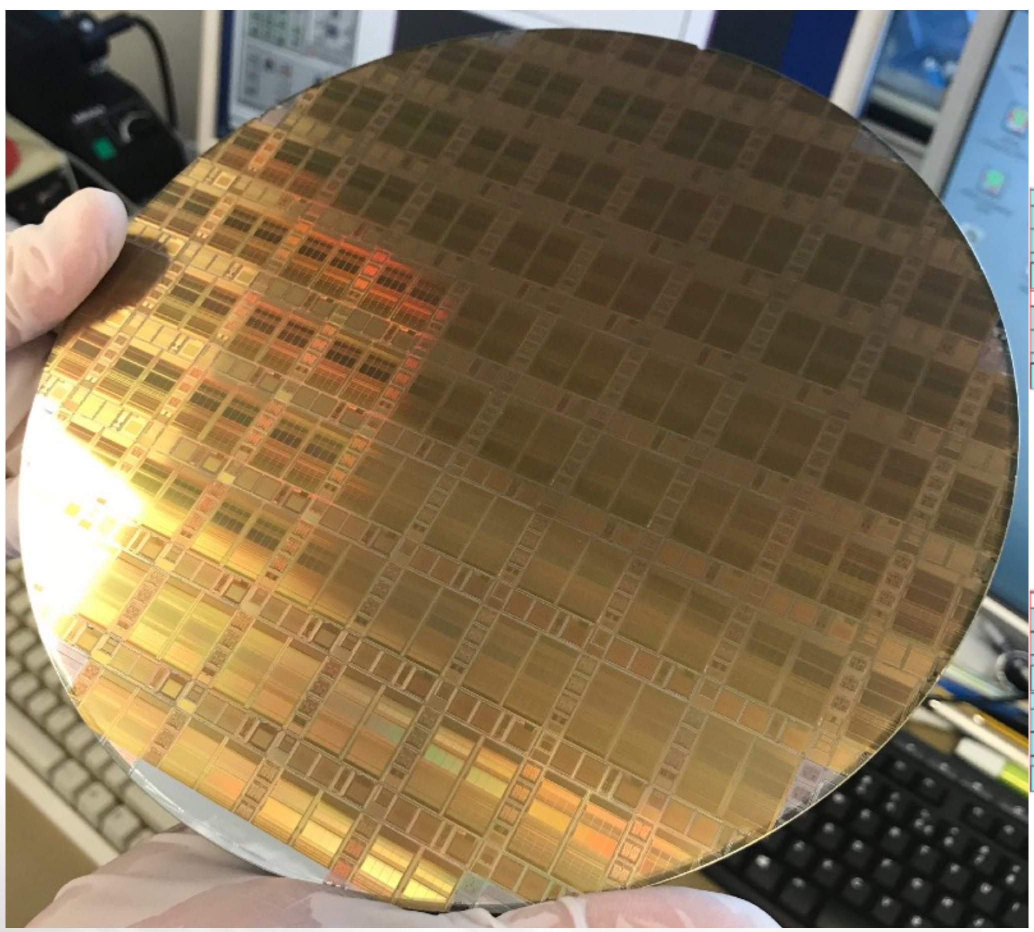


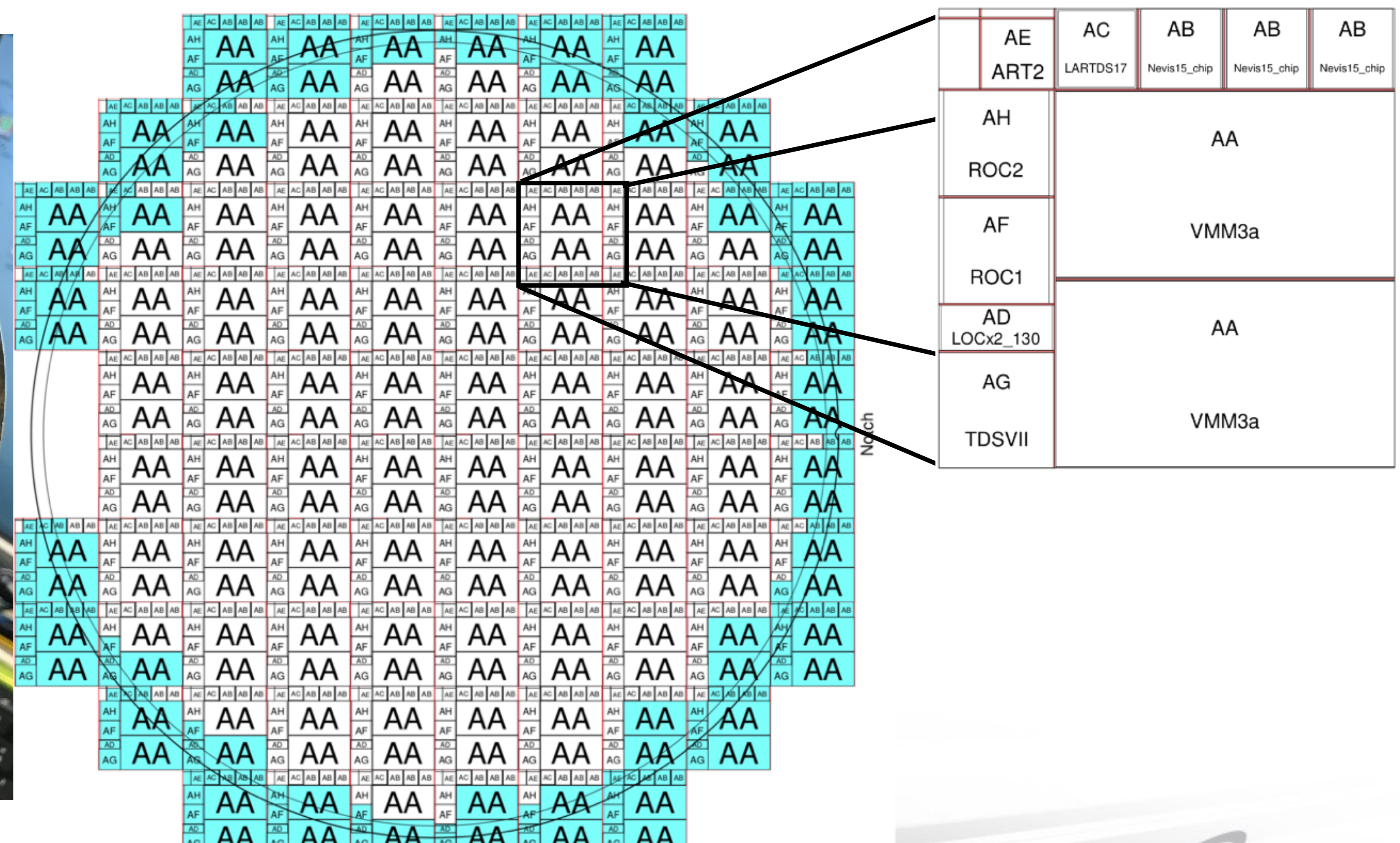

# Applications - Future SRS VMM users / interested

| Group | Application | VMM hybrids | Contact |
|---|---|---|---|
| ESS Lund / BrightnESS | NMX instrument @ ESS | 164 | Dorothea PFEIFFER |
| University of Science and Technology of China | RICH R&D for future colliders in China (CEPC and STCF) | 156 | LUI Jianbei |
| Bonn University | BASTARD neutron detector | 71 | Jochen KAMINSKI<br>Markus KÖHLI |
| Mainz University | MAGIX experiment @ MESA* | 211 | Stefano CAIAZZA |
| Budker Institute of Nuclear Physics, Novosibirsk | µWell MPGD R&D | 22 | Lev I. SHEKHTMAN |
| INFN Tieste | Generic R&D | 10 | Silvia DALLA TORRE |
| Tsukuba University | ALICE FoCal, Si Pads | 50 | CHUJO Tatsuya |
| GDD group CERN | Generic R&D | 16 | Eraldo OLIVERI |
| Peking University | CMS GEM upgrade | 52 | Dayong WANG |
| LMU Munich | Ion Tomography with Micromegas | 16 | Felix KLITZNER |
| LMU Munich | Medical physics with MPGDs, Si | 48 | Jona BORTFELDT |
| ETH Zurich | GBAR experiment @ CERN | ≈40 | Gianluca JANKA |
| CERN | BGV(Beam Gas Vertex) beam monitor* | 200 | Robert KIEFFER |
| University of Virginia, Charlottesville | EIC tracker @ RHIC* | Not known yet | Kondo GNANVO |

# VMM Production

- The **VMM** is **produced** in a 8” **wafer** with 2 copies of the chip in a reticle, **total 113 chips per wafer**. In the same floor-plan other ATLAS ASICs are included
- ATLAS has already produced and package **<u>70,000 Chips</u>** (RD51 another 3k chips)
- Many iterations with experts from Global Foundries to improve the yield (currently ~72% due to damage on the Baseline stabiliser circuit). Already got indications on issues in their processes
- Current experience shows yield of ~80% mainly due to BLH probably getting damaged during the process or over etching in some lines (already investigated that with GF)
- In ATLAS we had no time to further investigate the issue and moved forward to production





# VMM Future ?

- Clearly VMM is a state of the art ASIC for physics applications
- There is a big demand from several applications and experiments which clearly needs high support. I have though quite a lot of responsibilities in ATLAS as of now which limits me from providing support
- BNL has looked into how to support demands and EIC (if VMM is needed) maybe be a good opportunity to have this support (instrumentation of BNL is already quite expert in VMM)
- The main designer, G. de Geronimo resigned from BNL since VMM3 release but through these years was engaged with specific contract to advance VMM to the state that we have it today

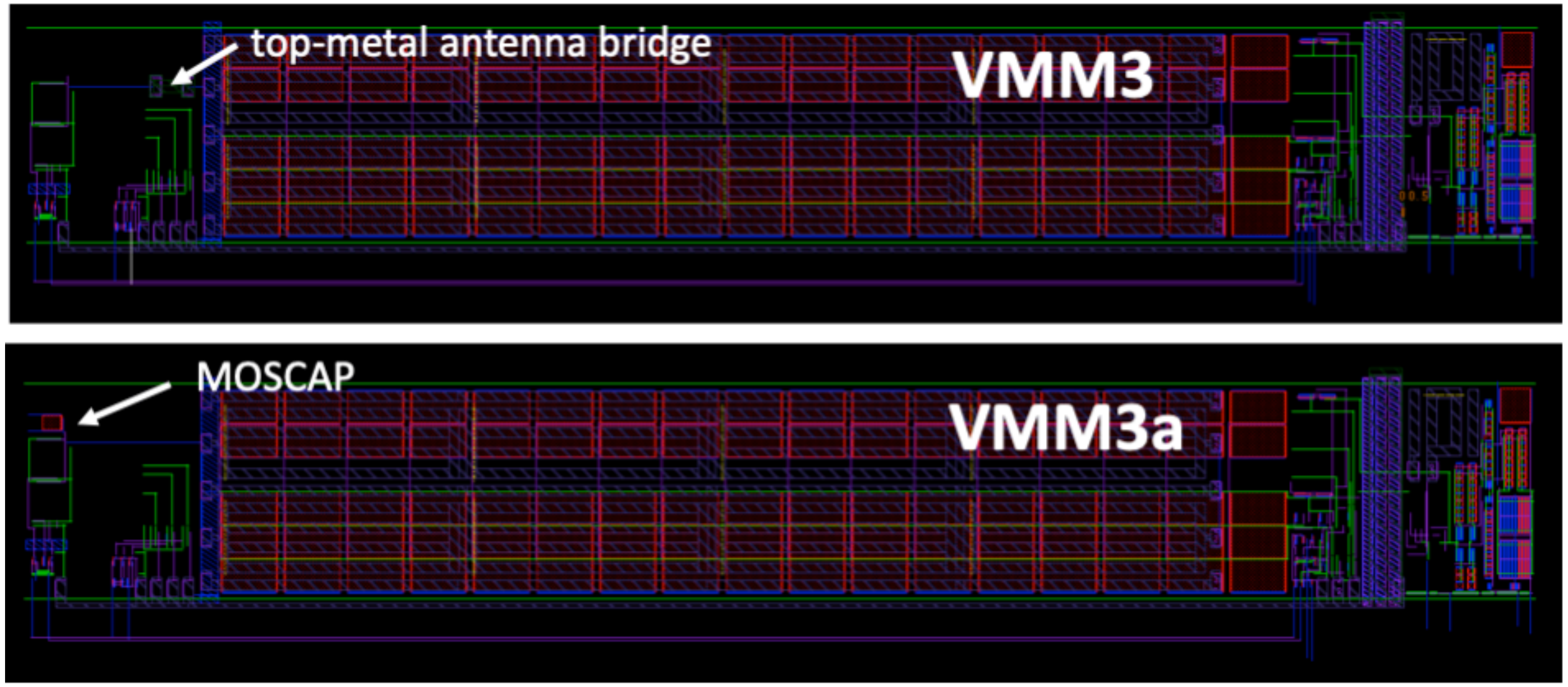
- Clearly 130nm will be around for some years but VMM could become even more attractive
  - Move it to TSMC 65nm technology, much more reliable (many users go away from GF, CERN as well)
  - A point which has been proven difficult in VMM was the implementation of the ADCs. Clearly this is an area of improvement or maybe something from the market can be employed
  - ADC deadtime is what limits the VMM as of now to 4MHz per channel. I imagine that this can be improved if applications need it, implementing more data lines as well for more throughput

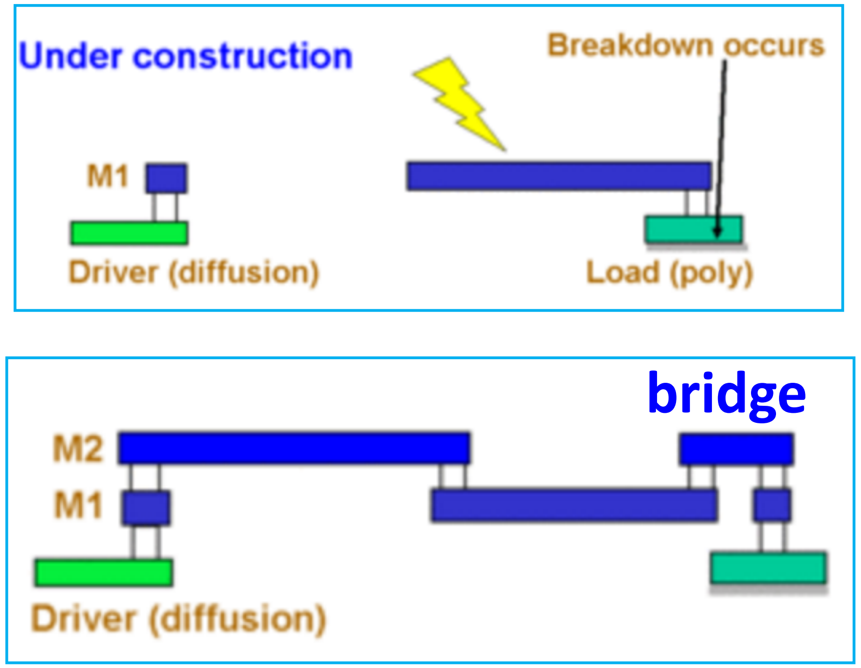
➡Clearly though those are my thoughts… probably I should hear yours now !

*backup*

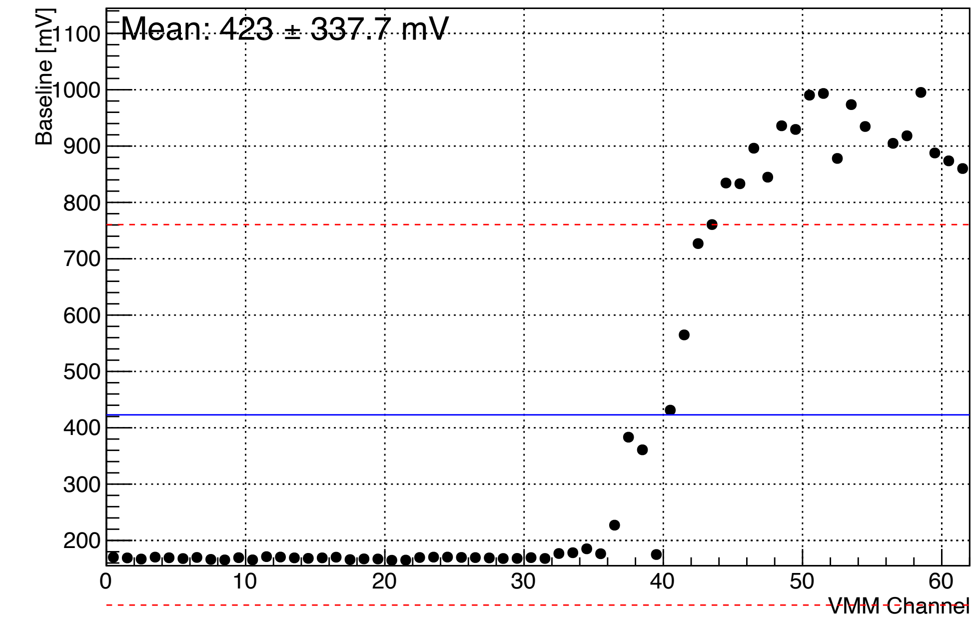
# VMM BLH

- On VMM3a, under the suspicion of antenna damage, the bridge of the top layer was replaced by a MOSCAP
- **Just to note that both designs are satisfying the DRC for antenna damage**




- The issue cannot be explained from simulation: Points to damage of the gate, or degradation of it



# The Shaper

## The VMM Shaper

The VMM "semi-Gaussian" shaper responds to an event with an analog pulse, the peak amplitude of which is proportional to the event charge. The time needed to return to baseline after the peak, depends on the the time constants and the configuration of poles. The VMM facilitates a 3rd order c-shaper with the combination of one real and two conjugate poles. The transfer function $T(s)$ for such shaper is given by the following expression:

$$T(s) = \frac{1}{(s+p_1)\prod_{i=2}^{(n+1)/2}\left[(s+r_i)^2+c_i^2\right]} = \frac{1}{(s+p_1)\left[(s+r_2)^2+c_2^2\right]}, \quad n=3$$

where $n$ is the order of the shaper, and $r_i, c_i$ are the real and imaging parts. The roots are:

$$(s+r_2)^2+c_2^2=0 \Rightarrow s+r_2=\pm jc_2 \Rightarrow s=-r_2\pm jc_2$$

so the transfer function can be written with the simple fractions like :

$$T(s) = \frac{K_1}{(s+p_1)} + \frac{K_2}{(s+r_2-jc_2)} + \frac{K_3}{(s+r_2+jc_2)} \tag{1}$$

where one real pole, $\text{pole}_\emptyset = -p_1$ and the two complex poles, $\text{pole}_1 = -r_2+jc_2$ and $\text{pole}_2 = -r_2-jc_2 = p_1^*$, $\Re\text{pole}_1 = -r_2$, $\Im\text{pole}_1 = c_2$. The coefficients $K_i$ are :

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# VMM **Registers**

| Global bits (defaults are 0) | Description |
|---|---|
| sp | input charge polarity ([0] negative, [1] positive) |
| sdp | disable-at-peak |
| sbmx | routes analog monitor to PDO output |
| sbft [0 1], sbfp [0 1], sbfm [0 1] | analog output buffers, [1] enable (TDO, PDO, MO) |
| slg | leakage current disable ([0] enabled) |
| sm5-sm0, scmx | monitor multiplexing.<br>• Common monitor: scmx, sm5-sm0 [0 000001 to 000100], pulser DAC (after pulser switch), threshold DAC, band-gap reference, temperature sensor)<br>• channel monitor: scmx, sm5-sm0 [1 000000 to 111111], channels 0 to 63 |
| sfa [0 1], sfam [0 1] | ART enable (sfa [1]) and mode (sfam [0] timing at thresh-old, [1] timing at peak) |
| st1,st0 [00 01 10 11] | peaktime (200, 100, 50, 25 ns ) |
| sfm [0 1] | enables full-mirror (AC) and high-leakage operation (enables SLH) |
| sg2,sg1,sg0 [000:111] | gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC) |
| sng | neighbor (channel and chip) triggering enable |
| stot [0 1] | timing outputs control 1 (s6b must be disabled)<br>• stpp,stot[00,01,10,11]: TtP,ToT,PtP,PtT<br>• TtP: threshold-to-peak<br>• ToT: time-over-threshold<br>• PtP: pulse-at-peak (10ns) (not available with s10b)<br>• PtT: peak-to-threshold (not available with s10b) |
| sttt [0 1] | enables direct-output logic (both timing and s6b) |
| ssh [0 1] | enables sub-hysteresis discrimination |
| stc1,stc0 [00 01 10 11] | TAC slope adjustment (60, 100, 350, 650 ns ) |
| sdt9-sdt0 [0:0 through 1:1] | coarse threshold DAC |
| sdp9-sdp0 [0:0 through 1:1] | test pulse DAC |
| sc010b,sc110b | 10-bit ADC conv. time (increase subtracts 60 ns) |
| sc08b,sc18b | 8-bit ADC conv. time (increase subtracts 60 ns) |
| sc06b, sc16b, sc26b | 6-bit ADC conversion time |
| s8b | 8-bit ADC conversion mode |
| s6b | enables 6-bit ADC (requires sttt enabled) |
| s10b | enables high resolution ADCs (10/8-bit ADC enable) |
| sdcks | dual clock edge serialized data enable |
| sdcka | dual clock edge serialized ART enable |
| sdck6b | dual clock edge serialized 6-bit enable |
| sdrv | tristates analog outputs with token, used in analog mode |
| stpp [0 1] | timing outputs control 2 |
| slvs | enables direct output IOs |
| stcr | enables auto-reset (at the end of the ramp, if no stop occurs) |
| ssart | enables ART flag synchronization (trail to next trail) |

| Global bits (defaults are 0) | Description |
|---|---|
| s32 | skips channels 16-47 and makes 15 and 48 neighbors |
| stlc | enables mild tail cancellation (when enabled, overrides sbip) |
| srec | enables fast recovery from high charge |
| sbip | enables bipolar shape |
| srat | enables timing ramp at threshold |
| sfrst | enables fast reset at 6-b completion |
| slvsbc | enable slvs 100 Ω termination on ckbc |
| slvstp | enable slvs 100 Ω termination on cktp |
| slvstk | enable slvs 100 Ω termination on cktk |
| slvsdt | enable slvs 100 Ω termination on ckdt |
| slvsart | enable slvs 100 Ω termination on ckart |
| slvstki | enable slvs 100 Ω termination on cktki |
| slvsena | enable slvs 100 Ω termination on ckena |
| slvs6b | enable slvs 100 Ω termination on ck6b |
| sL0enaV | disable mixed signal functions when L0 enabled |
| reset reset | Hard reset when both high |
| sL0ena | enable L0 core / reset core & gate clk if 0 |
| l0offset_i0:11 | L0 BC offset |
| offset_i0:11 | Channel tagging BC offset |
| rollover_i0:11 | Channel tagging BC rollover |
| window_i0:2 | Size of trigger window |
| truncate_i0:5 | Max hits per L0 |
| nskip_i0:6 | Number of L0 triggers to skip on overflow |
| sL0cktest | enable clocks when L0 core disabled (test) |
| sL0ckinv | invert BCCLK |
| sL0dckinv | invert DCK |
| nskipm_i | magic number on BCID - 0xFE8 |
| slh, slxh | increases bias current at input node from nominal 1nA to 15nA or 300nA respectively |
| stgc | extreme charge handling compensation |

**There are two banks of 96 global registers**
**Each channel has a configuration of 24 bits**

# VMM **Connectivity on the BGA (NSW)**

| Name, Position | Con-nection | In, Out or I/O | Type of Signal or Max/Min | Description |
|---|---|---|---|---|
| sett A19-20 | VMM | I/O | Custom LVDS Bi-directional | Channel 0 force-neighbor signal |
| setb Y19-20 | VMM | I/O | Custom LVDS Bi-directional | Channel 63 force-neighbor signal |
| ckbc (BCclk) C15-16 | ROC | In | SLVS | Bunch crossing clock of 40 MHz / External trigger signal |
| cktp (Test Pulse) B15-16 | ROC | In | SLVS | Test pulse clock |
| cktk (Level-0) D13-14 | ROC | In | SLVS | Token clock / L0 (digital NSW mode) |
| ckdt (ROclk) E15-16 | ROC | In | SLVS | Data clock |
| ckart (ARTclk) D19-20 | ROC | In | SLVS | ART clock |
| sdi B17 | SCA | In | CMOS | Configuration data input |
| sdo B18 | | Out | CMOS | Configuration data output (not used, HiZ state in NSW) |
| cs B19 | SCA | In | CMOS | Chip Select, active low |
| sck B20 | SCA | In | CMOS | Input SPI clock |
| t0-t63 E17-W20 | TDS | Out | SLVS | Direct digital outputs |
| mo C9 | SCA | Out | 0-1 V | Analog output for calibration |
| tki (BCR/OCR) C13-14 | ROC | In | SLVS | Token input (an. mode) / (BCR-OCR) / acceptance window in non-L0 cont. mode |
| tko B13-14 | | Out | SLVS | Token output (analog mode, not used in NSW) |
| ena (ENA/Soft Reset) C17-18 | ROC | In | SLVS | Acquisition start/stop |
| ck6b C19-20 | TDS | In | SLVS | 6-bit ADC Clock |
| art E13-14 | ART2GBT | Out | SLVS | Address in Real Time |
| data0 D15-16 | ROC | Out | SLVS | data line |
| data1 D17-18 | ROC | Out | SLVS | data line first bit, flag in cont. |

Inter chip communication (sett, setb)

Can use different frequencies (ckbc)

should be longer that the peaking (cktp)

Trigger on L0, data finder on Continuous (cktk)

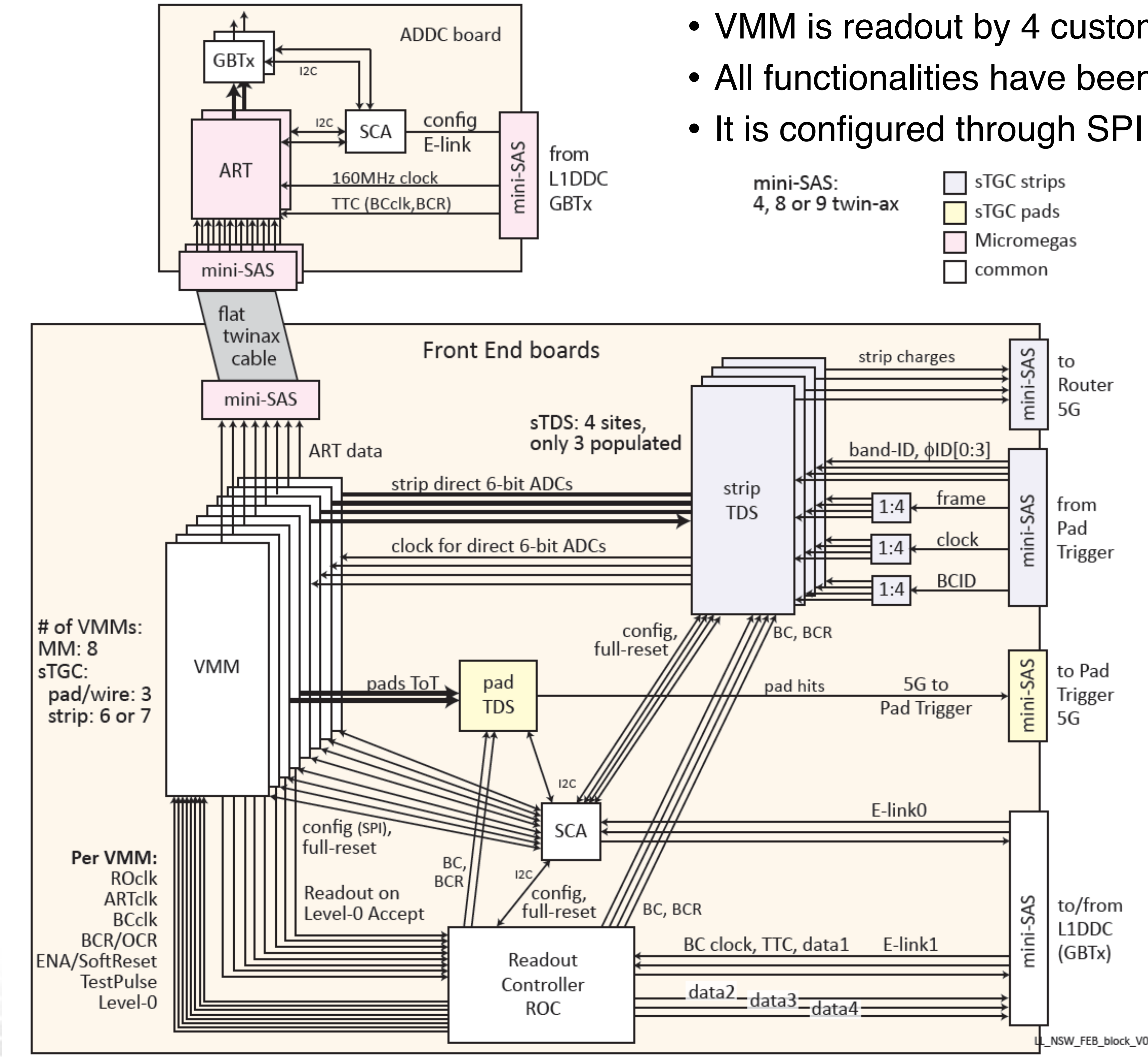
Configuration (sdi, sdo, cs, sck)

64 outputs - one per channel (t0-t63)

Analog output - Can see the actual waveform but also threshold DAC, pulser DAC, temperature, BGR (mo)

Data (data0, data1)

# VMM3a connectivity at NSW application

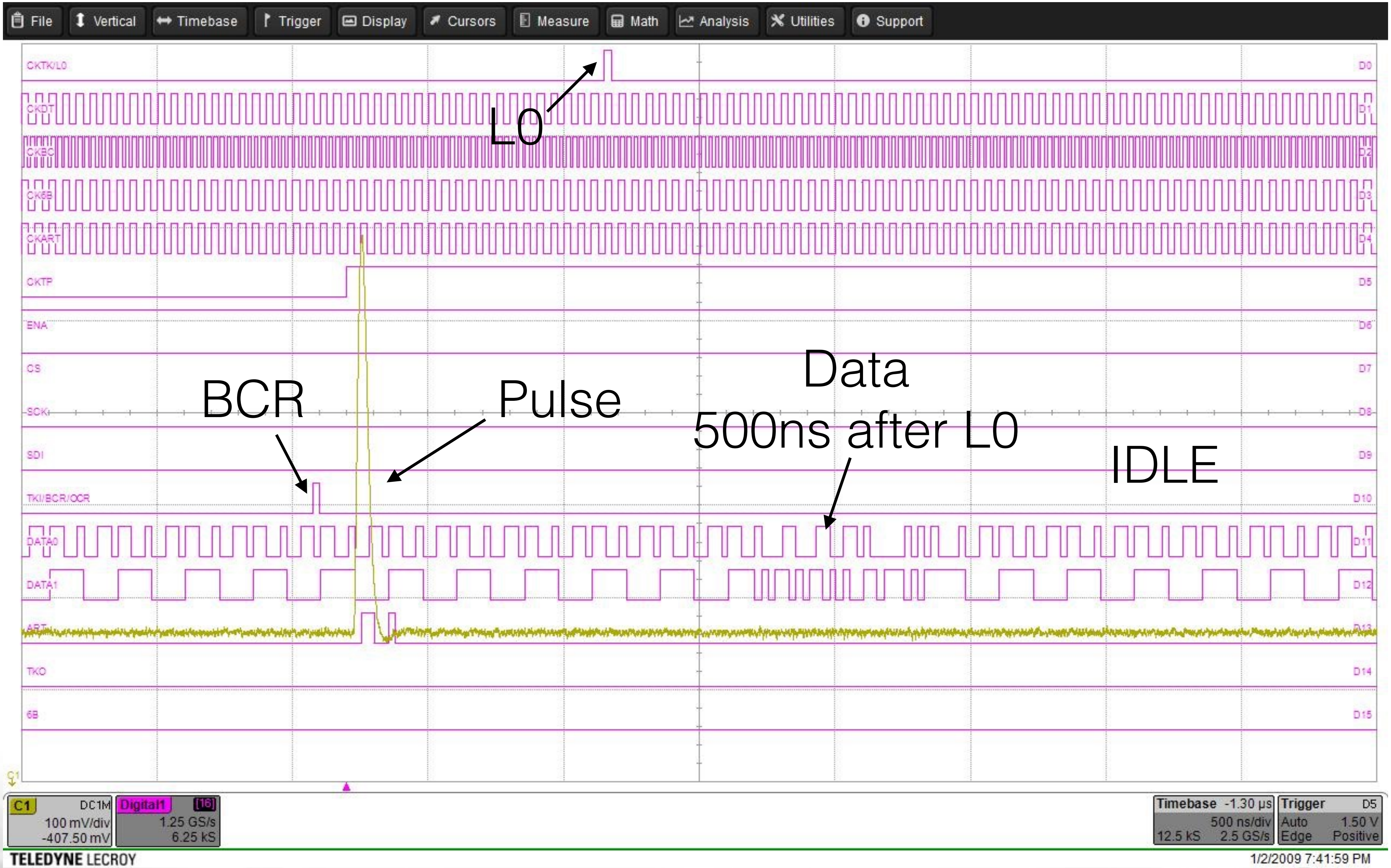



- VMM is readout by 4 custom ASICs at NSW
- All functionalities have been extensively validated
- It is configured through SPI protocol (CERN SCA ASIC)

mini-SAS:
4, 8 or 9 twin-ax

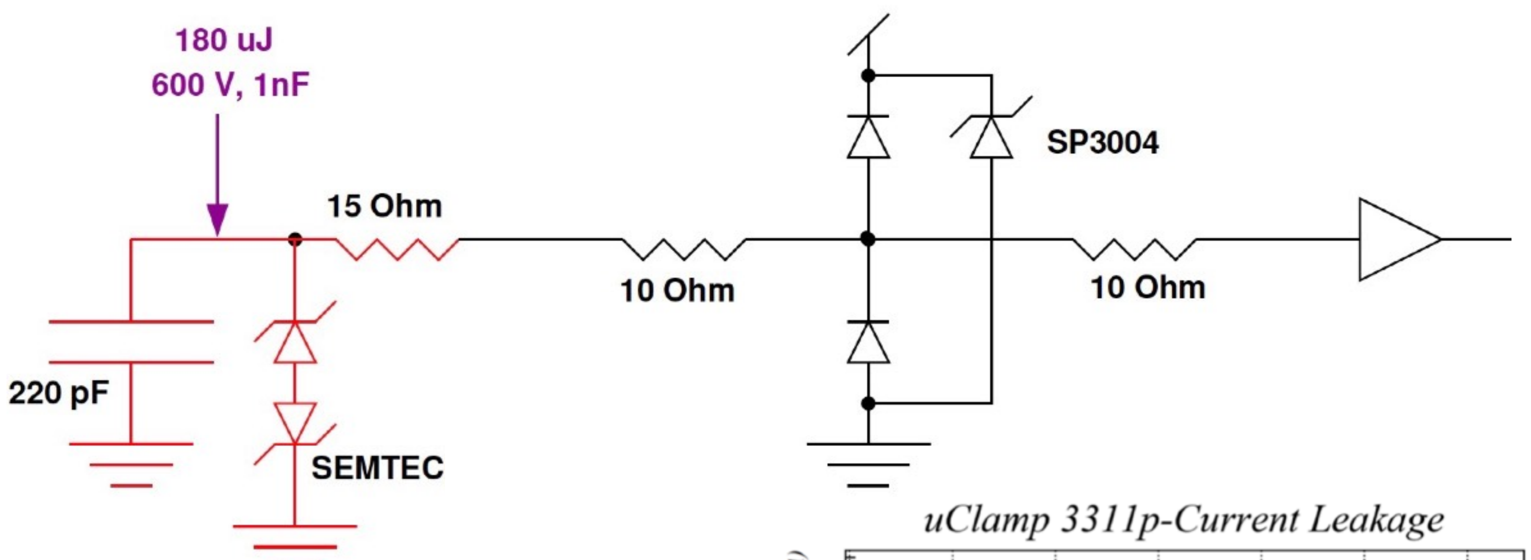
- sTGC strips
- sTGC pads
- Micromegas
- common

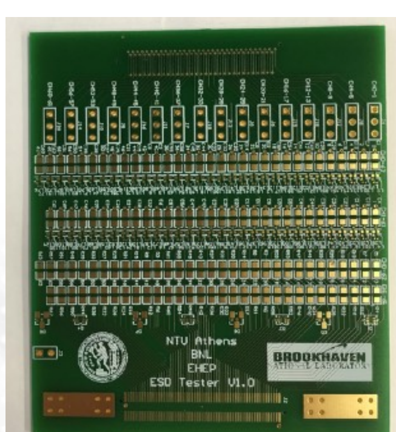
# Modes of operation - L0

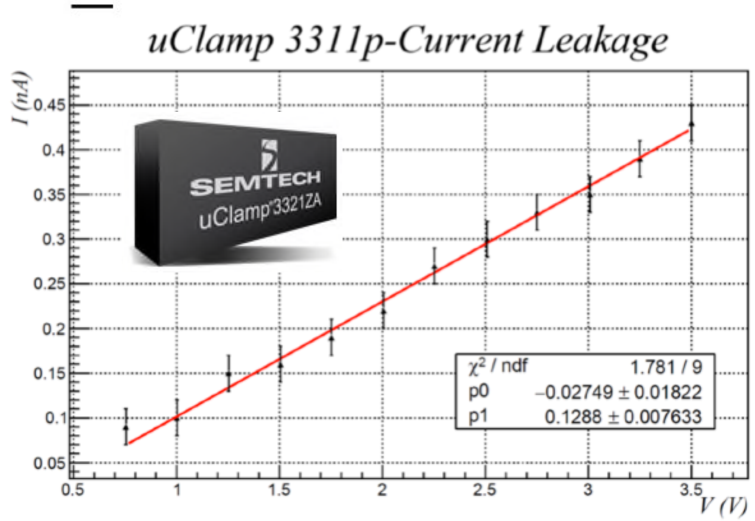


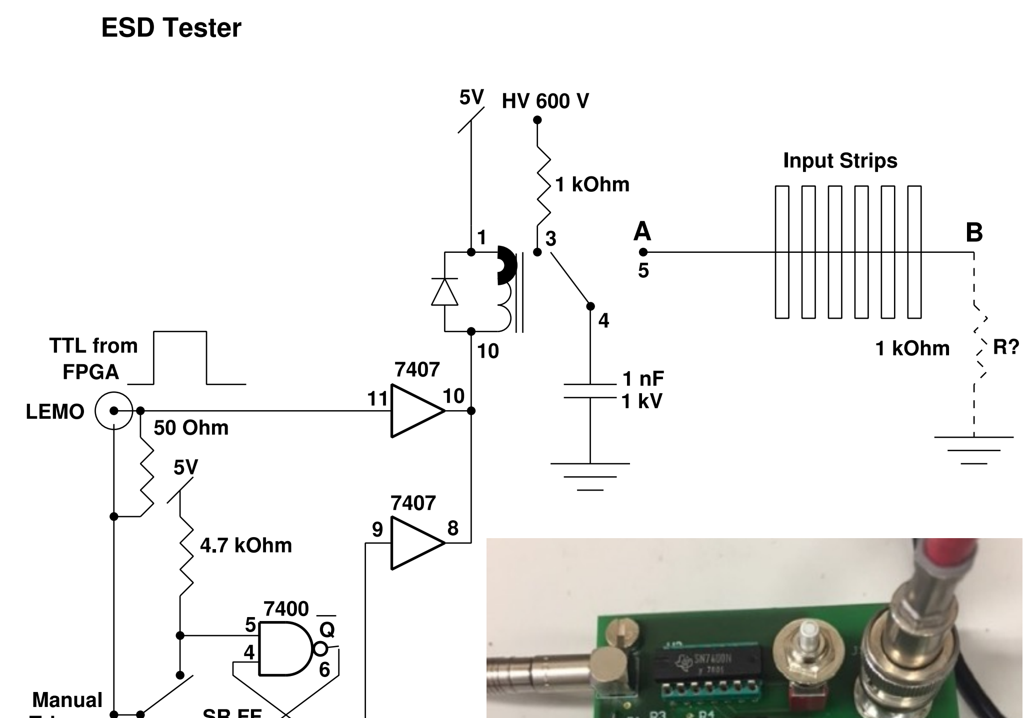
# Input protection schema

- Since the VMM2, we have experience major channel (initial NUP4114 issue). Moving to **130nm technology** made the requirements on **input protection higher**. Current protection scheme based on the SP3004 seems inadequate to protect the VMM front ends
- A **dedicated ESD testing procedure** was lunched allowing a systematic test of the VMM input.
- A VMM board (MMFE1) with Panasonic connector and a VMM socket was developed to perform systematic tests. On top a Panasonic based connector daughter-board was built to test different protection schemes and different footprints.
- 220 pF capacitor emulates typical MM strip capacitance, a channel like this survived repeated discharges while without protection is dead after a single discharge. Then **survived zapping overnight (>30,000 discharges)**



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# Temperature monitoring

The IBM CMOS8RF Design Manual specifies the operating temperature range to be from -55 °C to 125 °C. However device life time degrades rapidly at high temperatures. The case temperature should be kept below 50°C and preferably in the range 30–40 and should be verified and compared to the junction temperature provided by the VMM ASIC. The VMM includes a temperature sensor which can be read out by appropriately programming the monitor output and digitized by the SCA setting (in configuration mode) scmx = 0, sm5–sm0 = 000100 (see Table 6). The die temperature is approximately given by:

$$^\circ\mathrm{C} = \frac{725 - V_{\mathrm{sensor}}}{1.85}$$

where $V_{\mathrm{sensor}}$ is the temperature sensor reading in mV. The case temperature of a single-chip

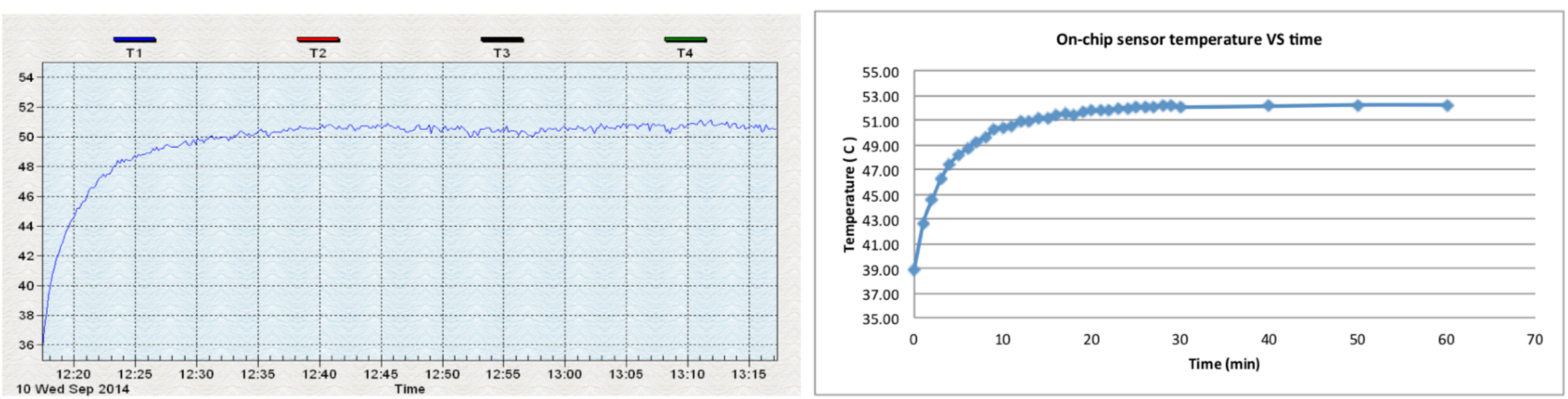
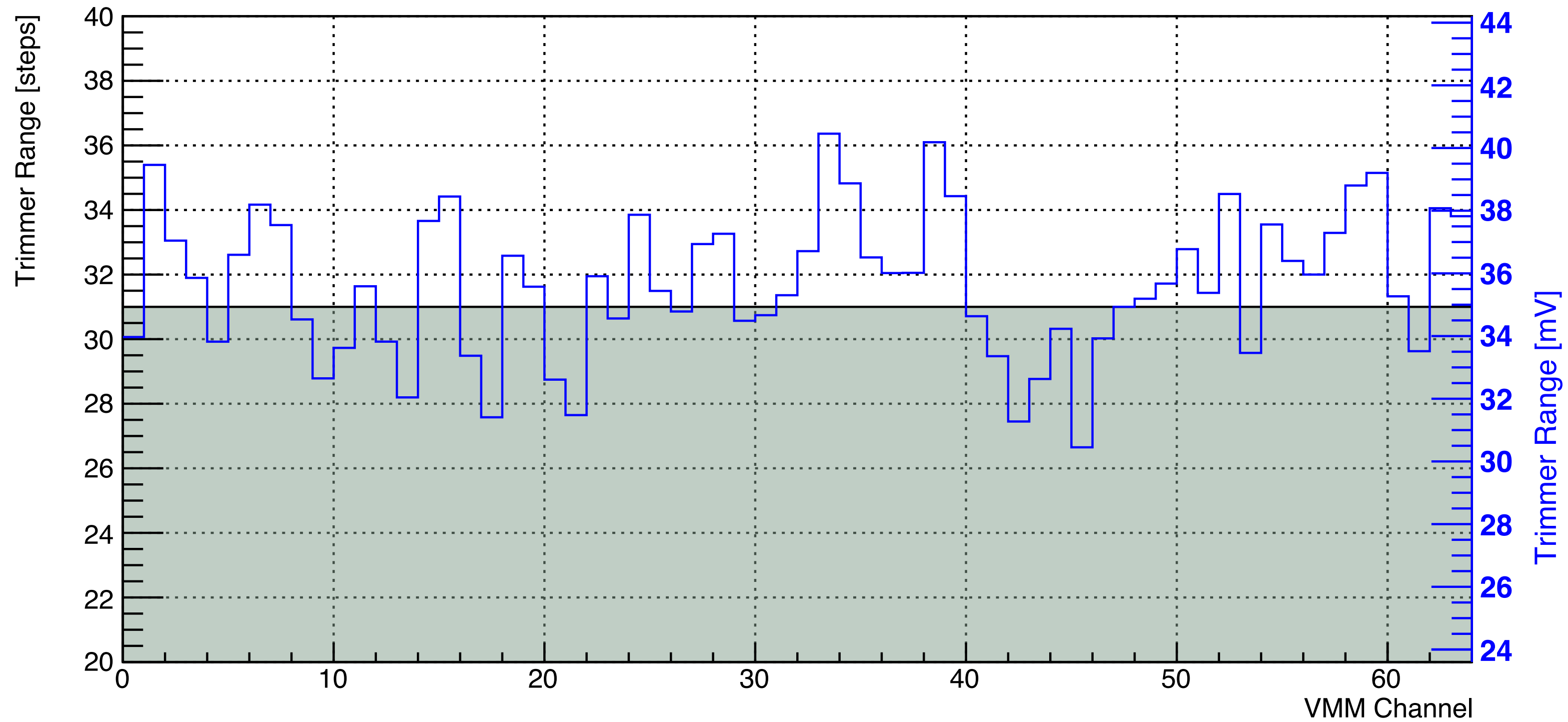
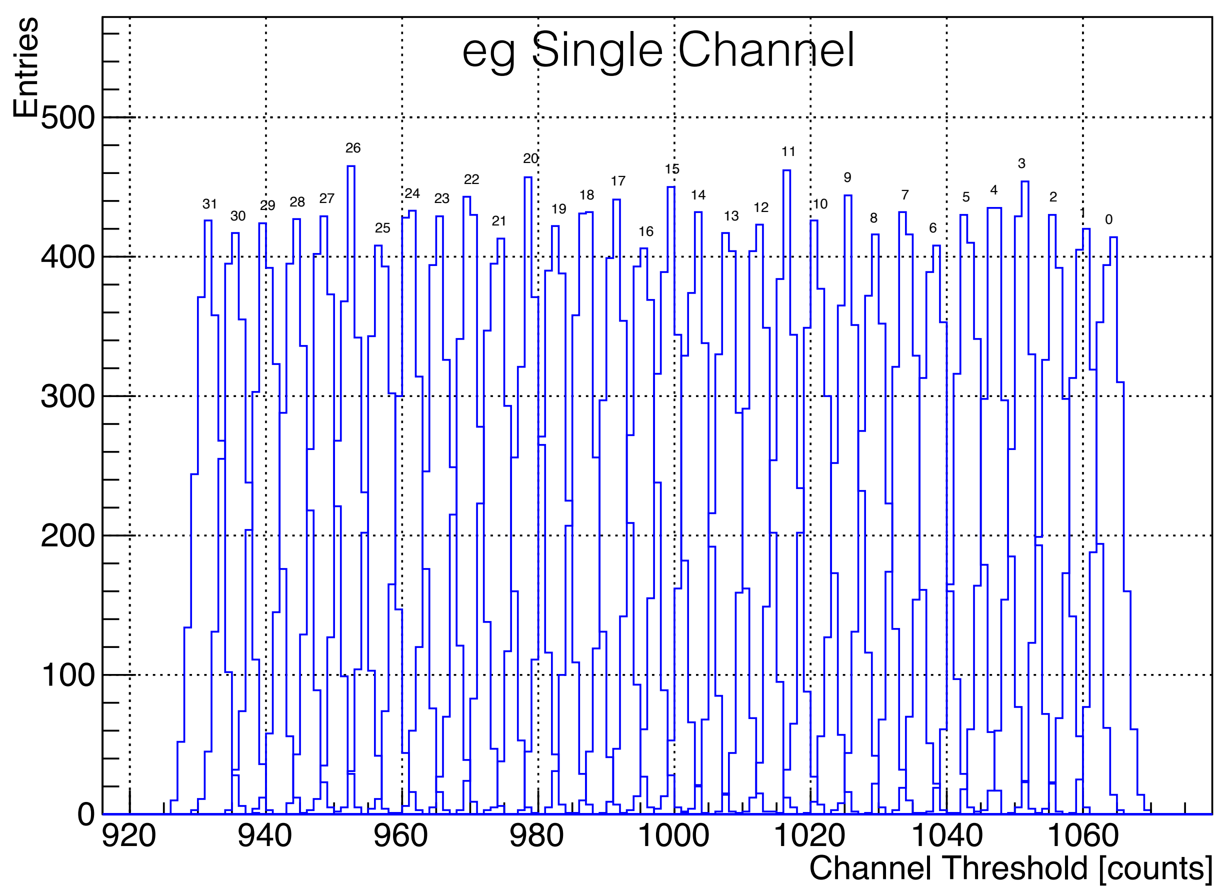


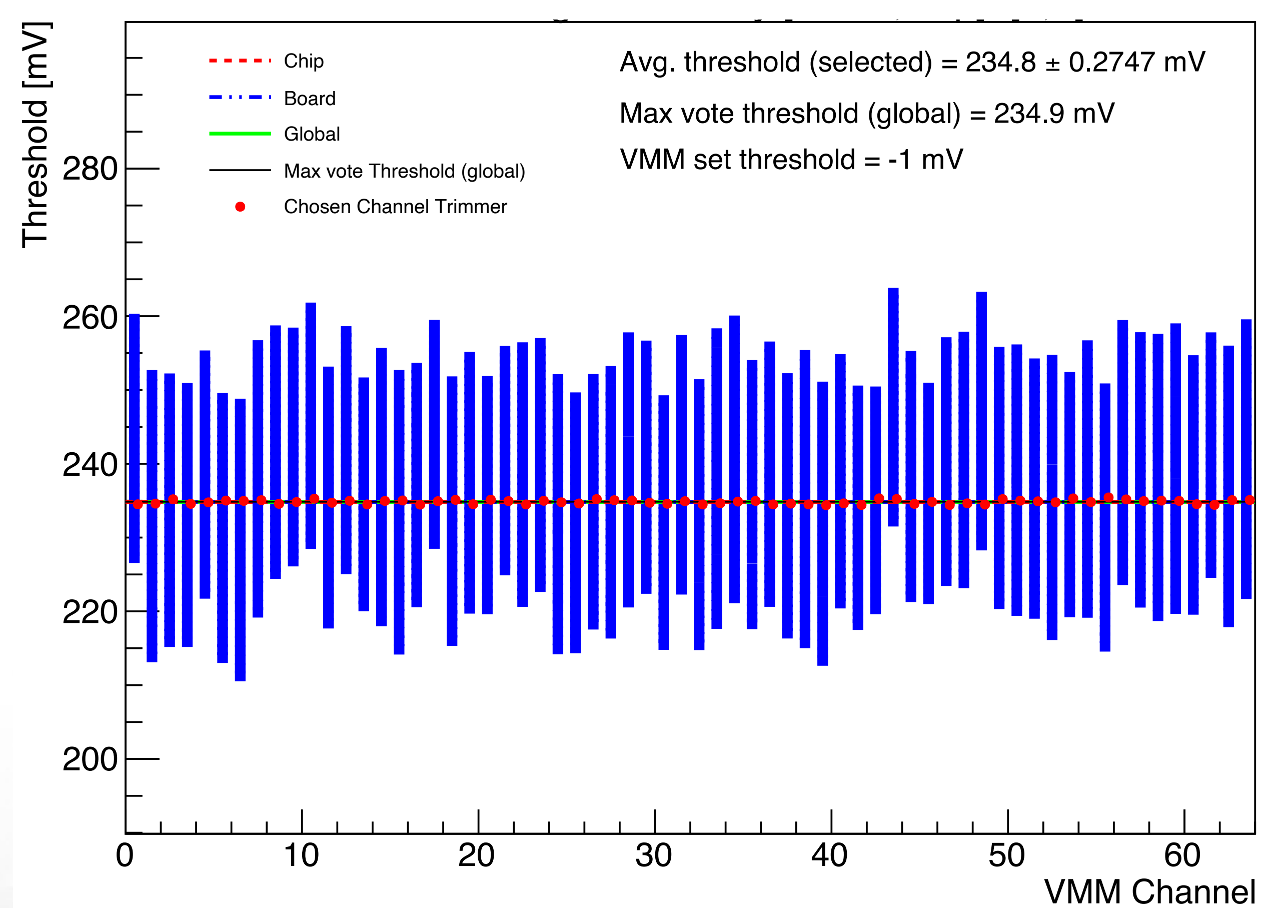

Figure 8: Left plot, the VMM case temperature. Right plot, the junction temperature as a function of time after turn-ON

# Calibration - channel trimming

- Full scan performed on the channel **trimmers** across full threshold range
- Found that the **full range** of 31 counts shows normal behaviour
- Minimum range of 30mV across all channels, **good uniformity**.
- **Equalisation** can be performed easily

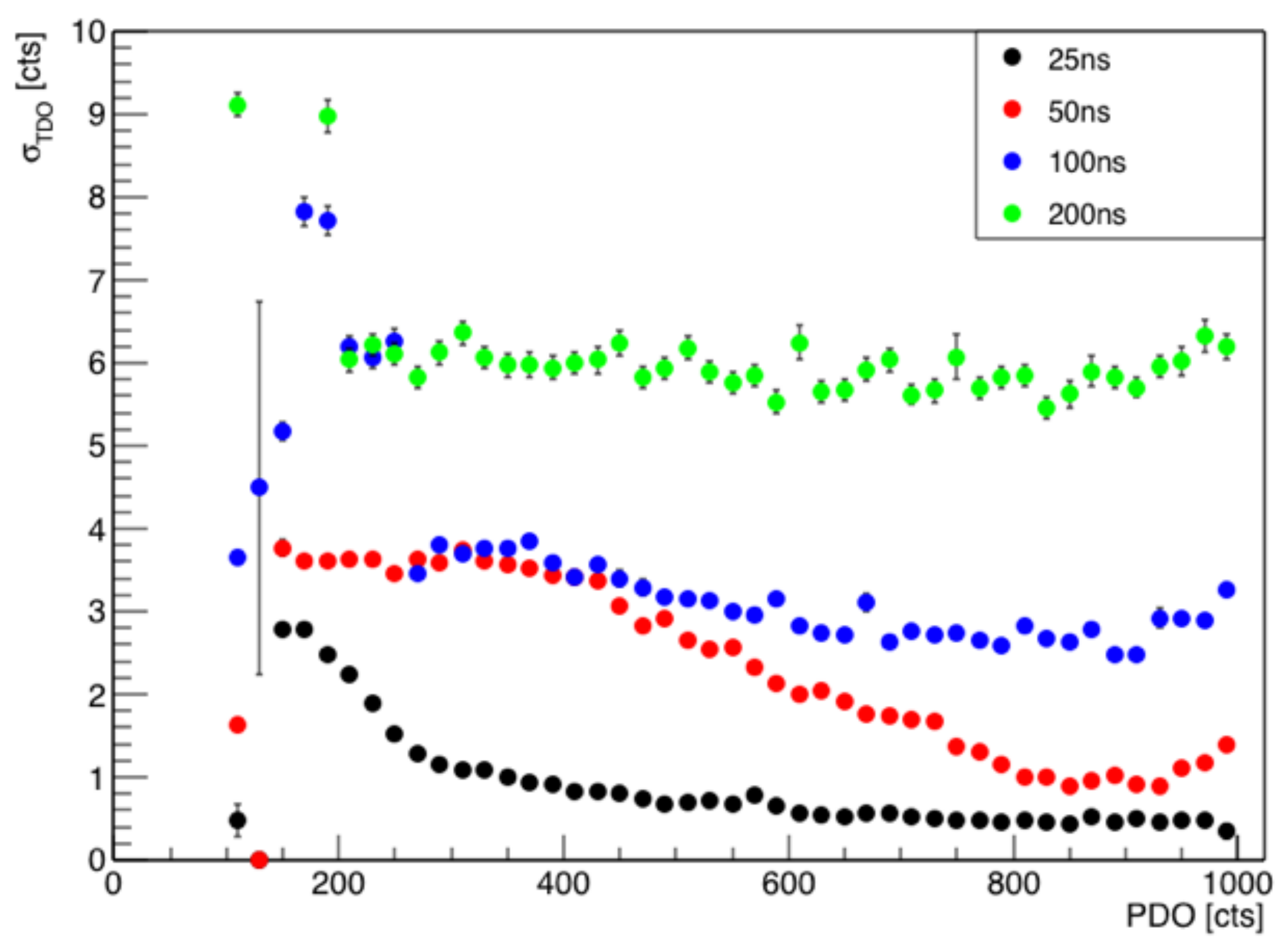


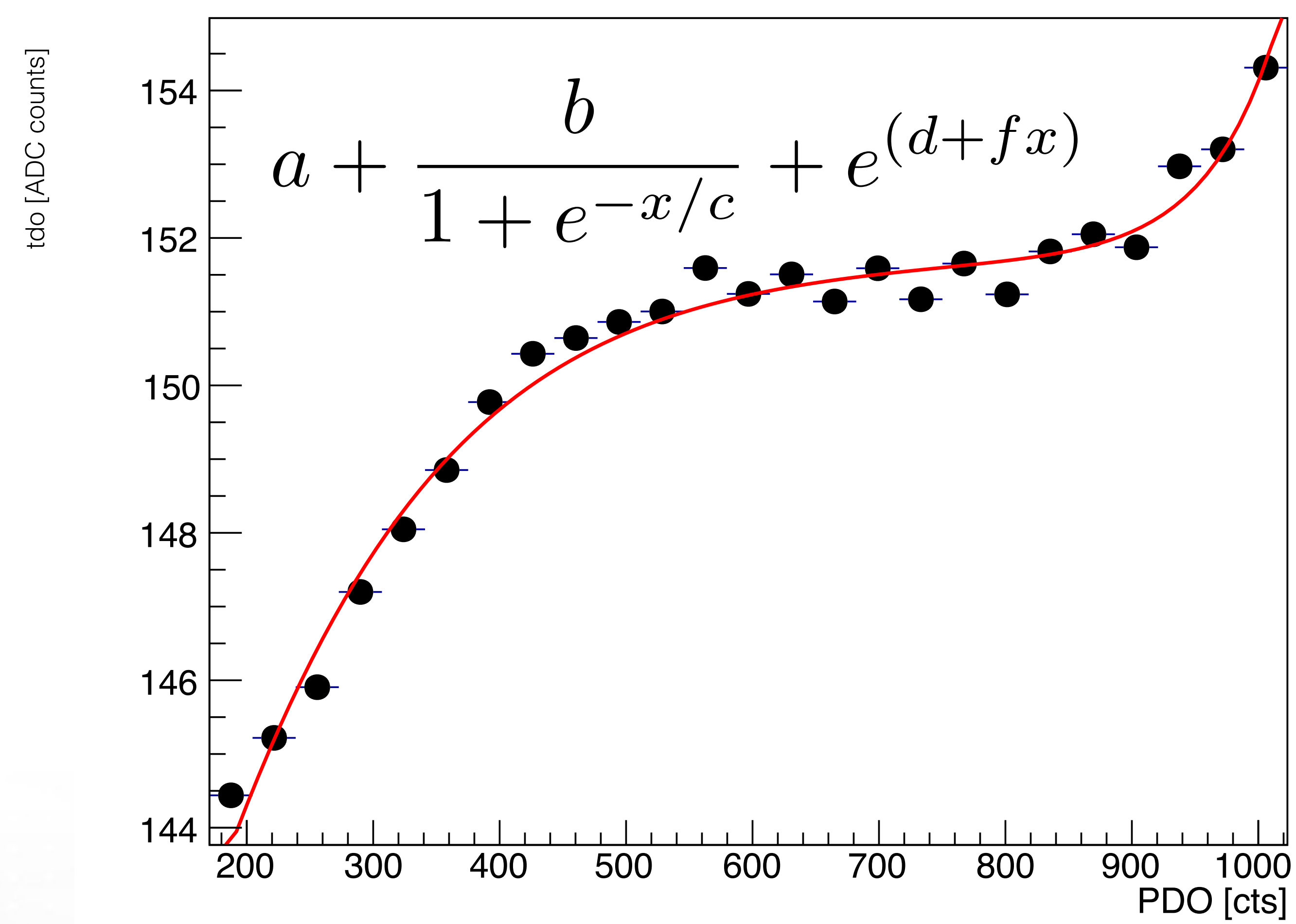



# Calibration - channel time walk and resolution

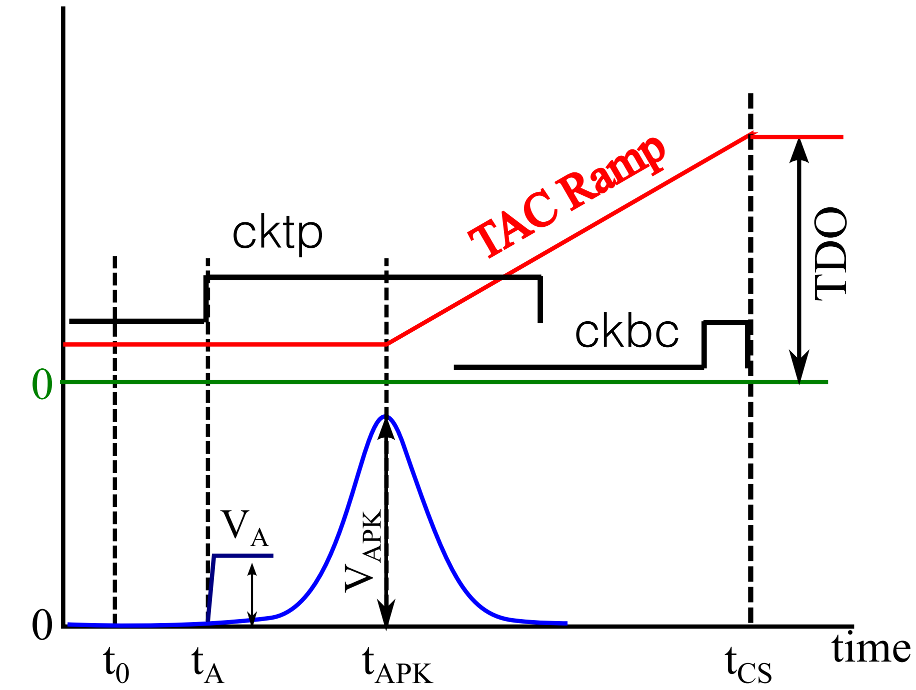
- Calibration of the following:
  - **Timing resolution along amplitude**: This is taking into account on the fitting of the event as an error. Other errors like the longitudinal diffusion is negligible with respect this.
  - **Time walk**: There is a dependance of the time finding (peak or threshold) from the signal amplitude. This is a correction applied on the timing reconstruction. Fitting the full distribution will improve more the results. To be done.

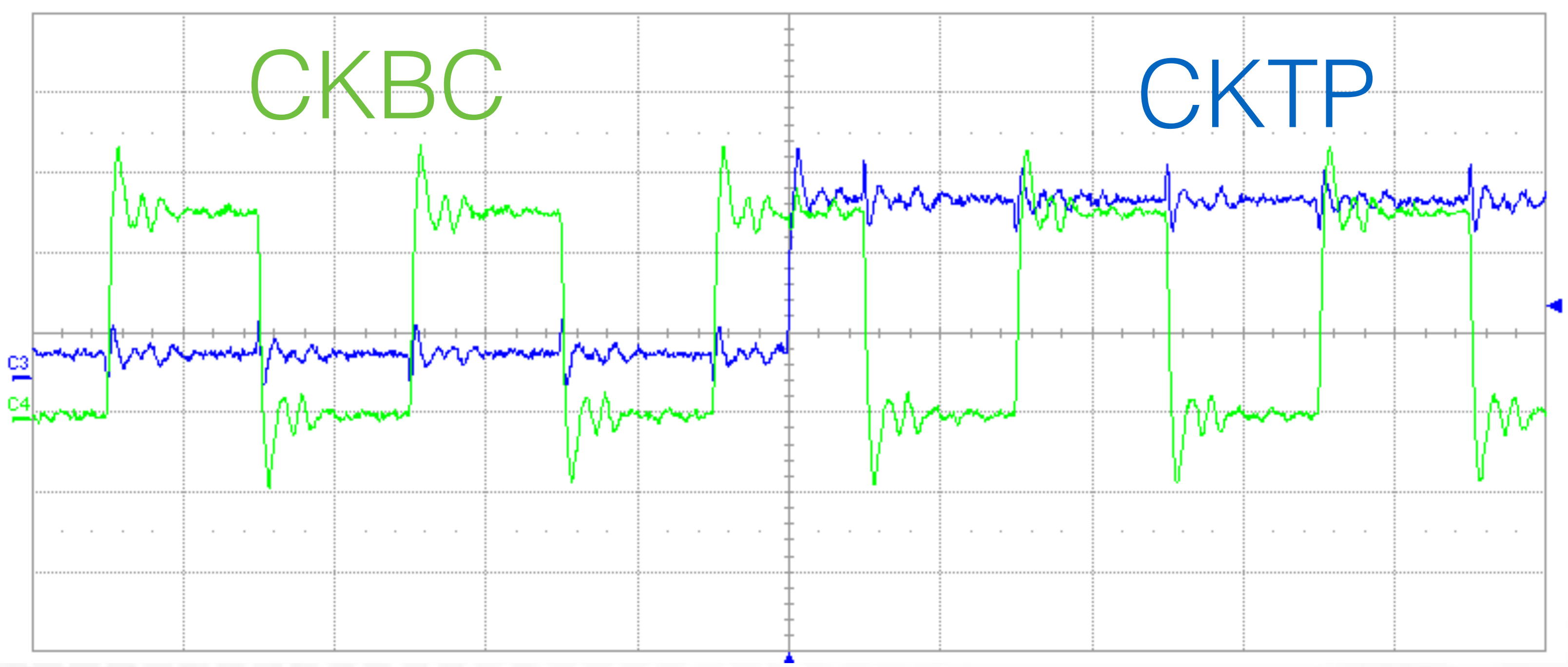


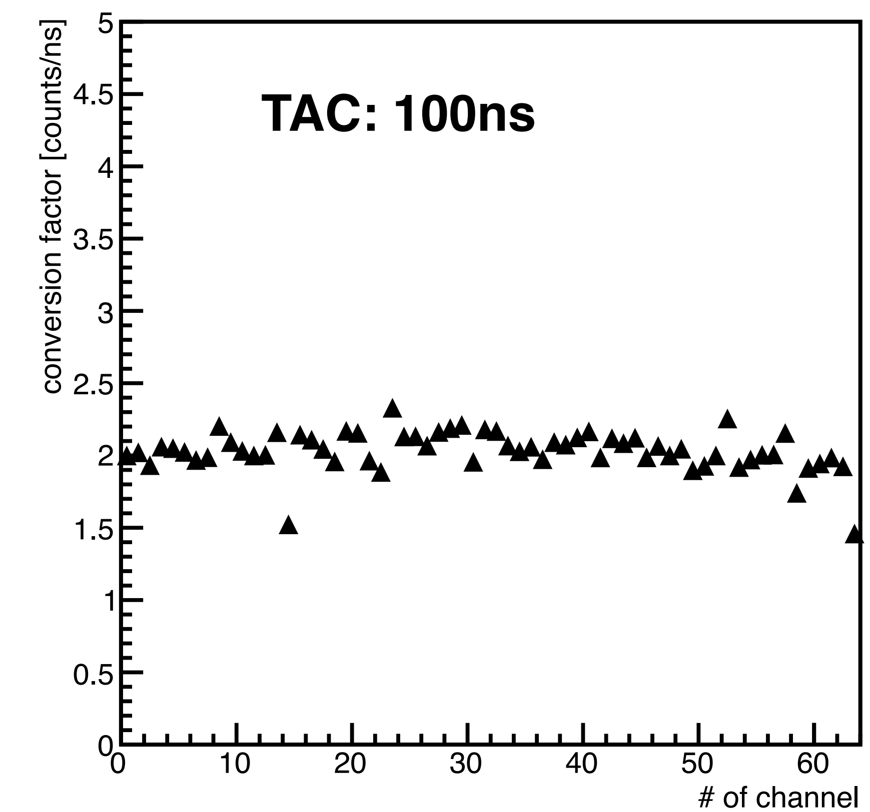



# Calibration - TAC

- **Calibration of the TAC** for different ramps was automatically performed. Skewing clocks method (NSW mode, VMM3/3a) and latency method (Not NSW VMM3) were used to extract the ramping rate and pedestal.
- Uniformity is good, the extracted **constants were used in analysis** to convert from ADC counts to ns



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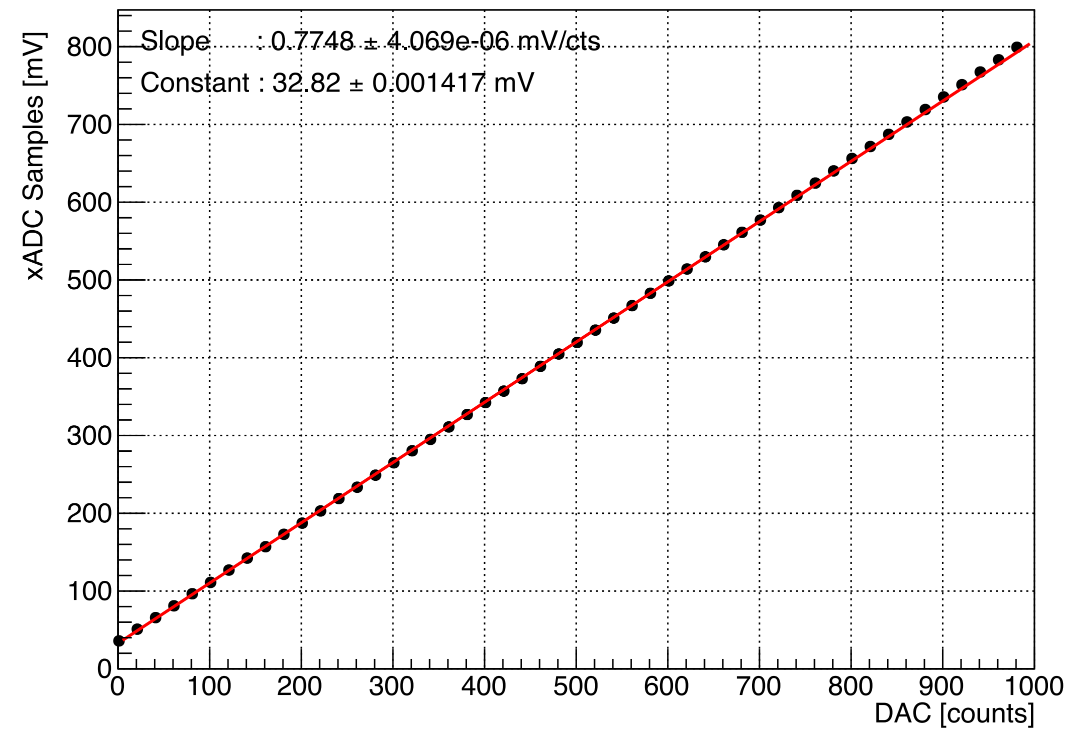
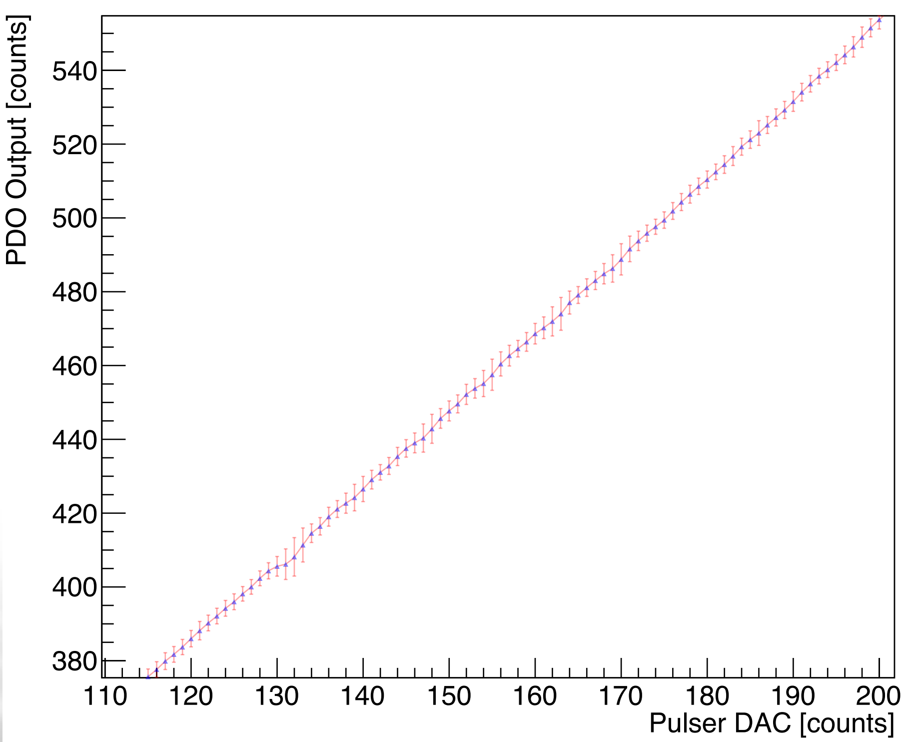
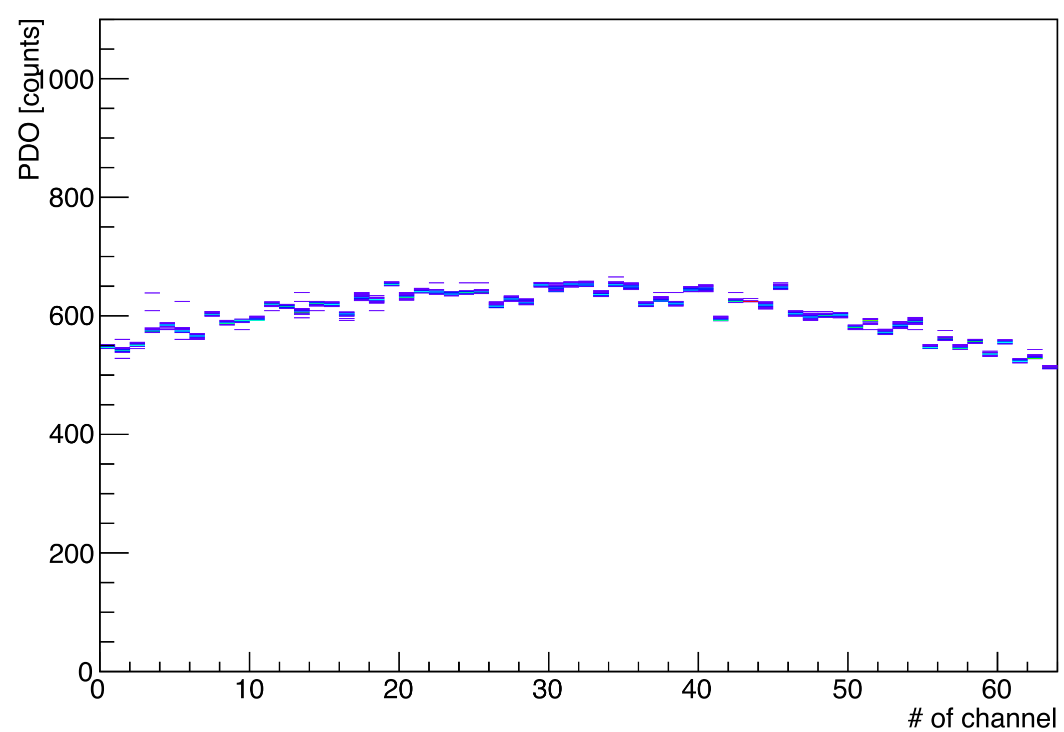
# Calibration - Charge

- VMM features as well an **internal pulser** which can cover the full range on all the gain settings
- Varying the input and **measuring the PDO**, a charge/gain **calibration can be done for each channel**

| Channel bits (defaults are 0) | Description |
|---|---|
| sc [0 1] | large sensor capacitance mode ([0] <~200 pF , [1] >~200 pF ) |
| sl [0 1] | leakage current disable [0=enabled] |
| st [0 1] | 300 fF test capacitor [1=enabled] |
| sth [0 1] | multiplies test capacitor by 10 |
| sm [0 1] | mask enable [1=enabled] |
| sd0-sd4 [0:0 through 1:1] | trim threshold DAC, 1 mV step ([0:0] trim 0 V , [1:1] trim -29 mV ) |
| smx [0 1] | channel monitor mode ( [0] analog output, [1] trimmed threshold)) |
| sz010b, sz110b, sz210b, sz310b, sz410b | 10-bit ADC zero |
| sz08b, sz18b, sz28b, sz38b | 8-bit ADC zero |
| sz06b, sz16b, sz26b | 6-bit ADC zero |



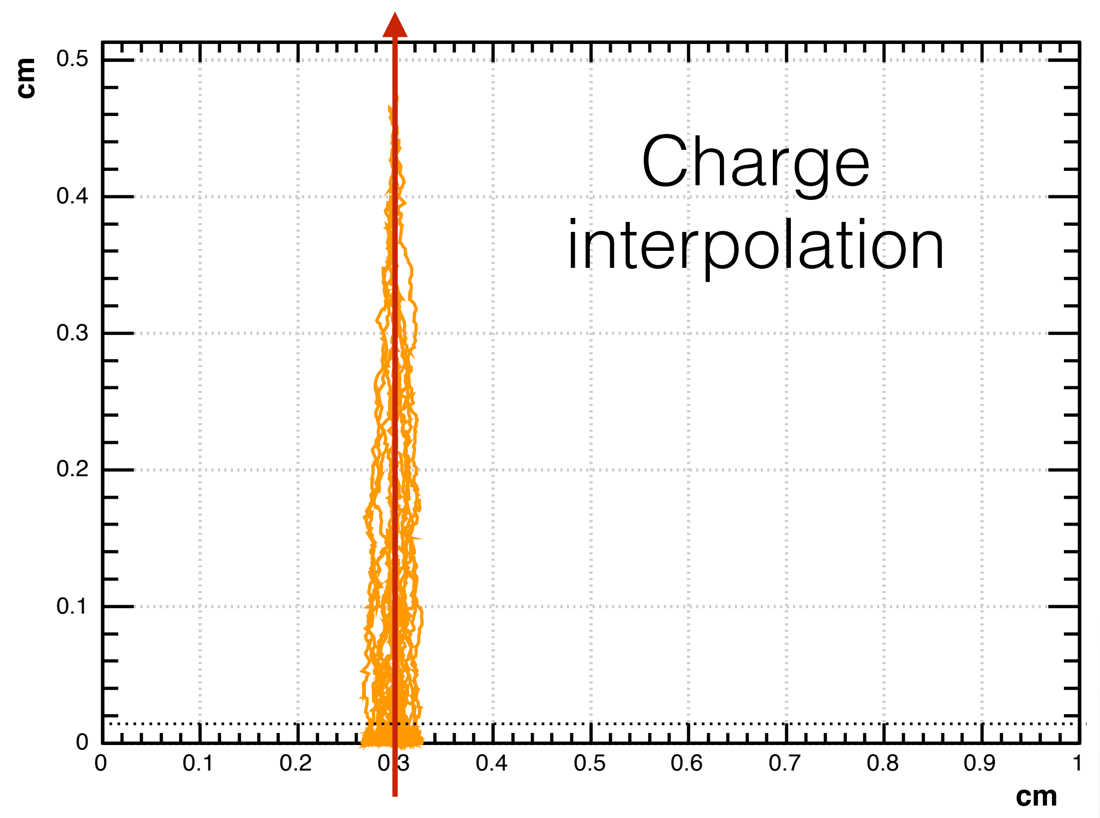



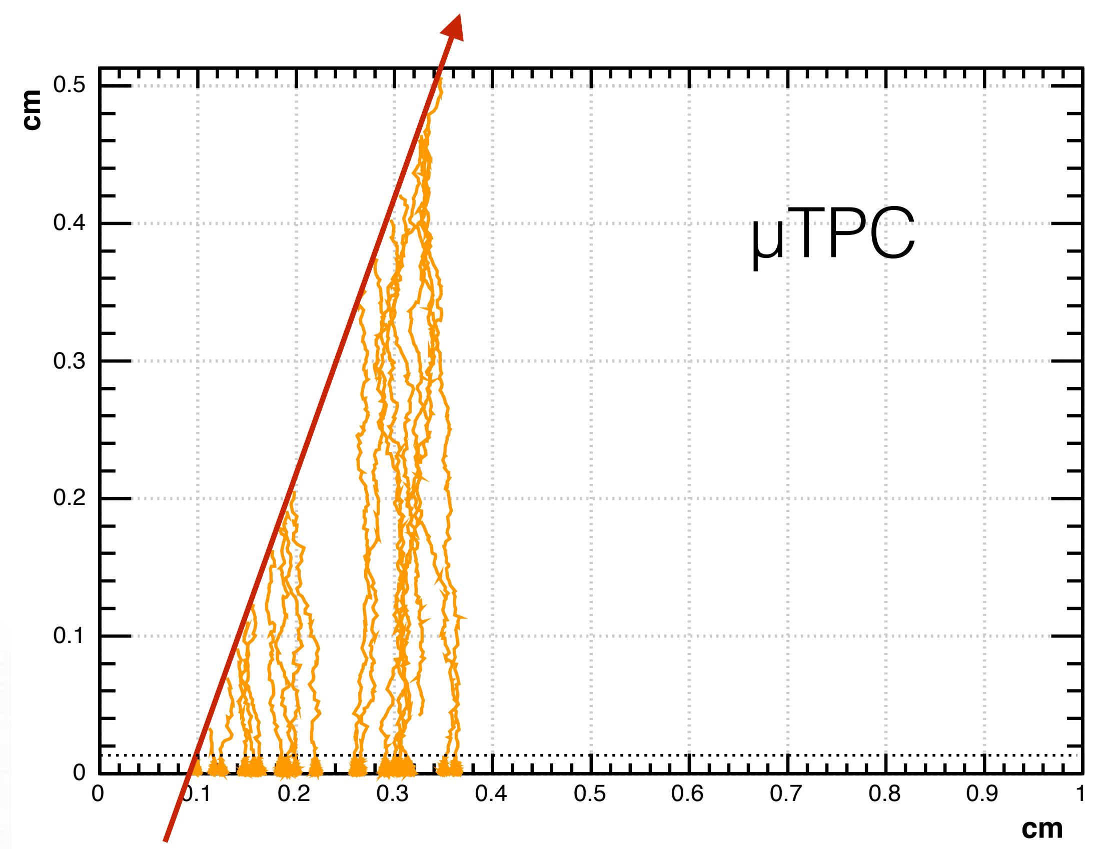




- In the effort of improving the ADCs a gain difference was introduced to the channels,
- Not big effect for adjacent channels
- Small loss of dynamic range

# µTPC - The concept

- In the NSW the **track range** is 5º-28º for the tracks originated from the IP
- It is mandatory to be able to **reconstruct the position** of a particle that transversed the detector under an angle **with high resolution**
- The **charge centroid method** is proven **not to be able to provide** good resolution for tracks over 5º.
- Instead a **new method** was implemented in the Micromegas called the **µTPC**
- This method implies on **measuring with high accuracy** (<3ns) **the arrival time** of the primary ionisation above a strip.

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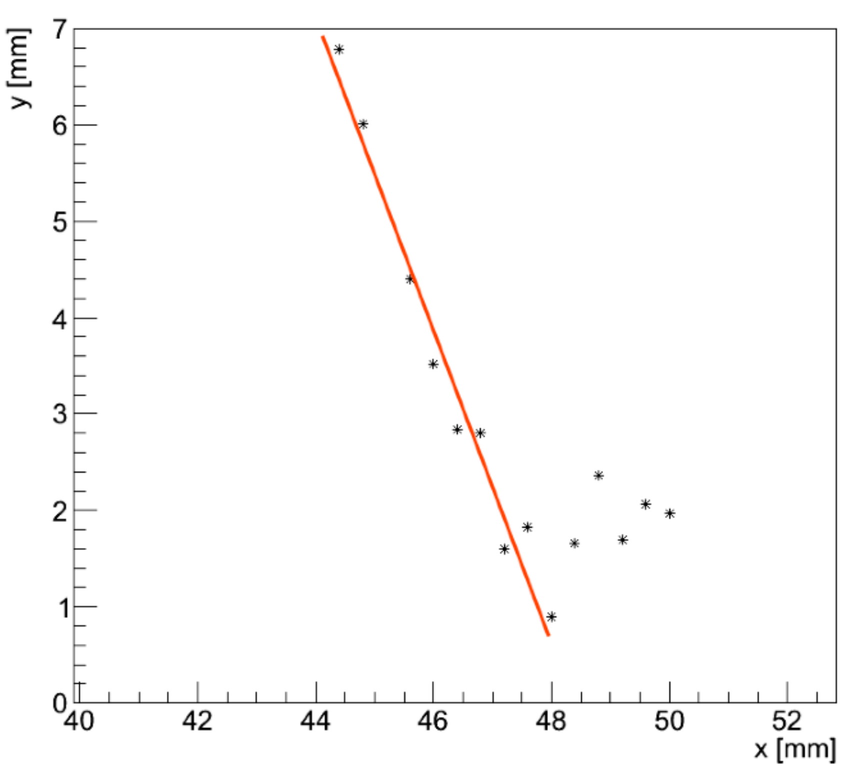
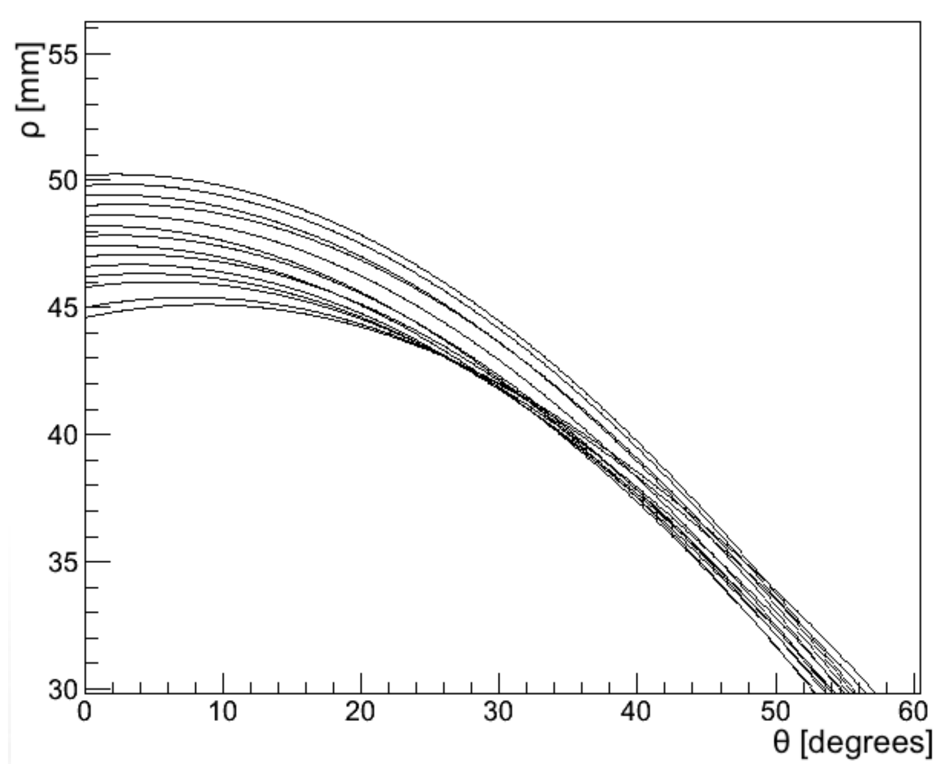
# µTPC - **Clustering** under an angle

- **Clustering** strips for **inclined tracks** is a challenging task due to:
  - Ionisation statistics, there are **fluctuations** on **primary** cluster generation that can give "holes" in between a cluster of strips **depending on the incident track angle**
  - Generation of **delta electrons**
  - **Multiple** track events
  - **Noise** in the system
- For this reason, a **pattern recognition technique** including the **Hough** Transform is used as a **filter** efficiently removing noise, delta electrons, separating double track events

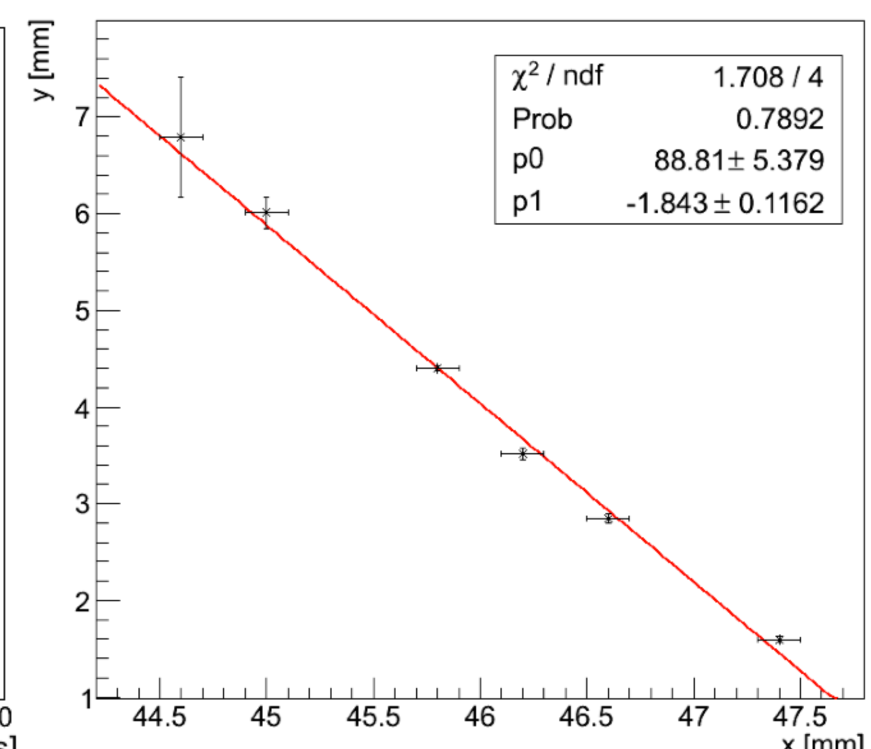
Hough line




Hough Space




Linear fit after filter



# VMM Embedded Readout Software (VERSO)

- For the test-beams, a **DAQ + control software** was **developed** allowing operations like configuration and calibration. Highly configurable, multi-threaded and reliable (VMM electronics)
- The applications is developed in Qt and C++ based on a UDP handshake protocol