The VMM ASIC

George lakovidis

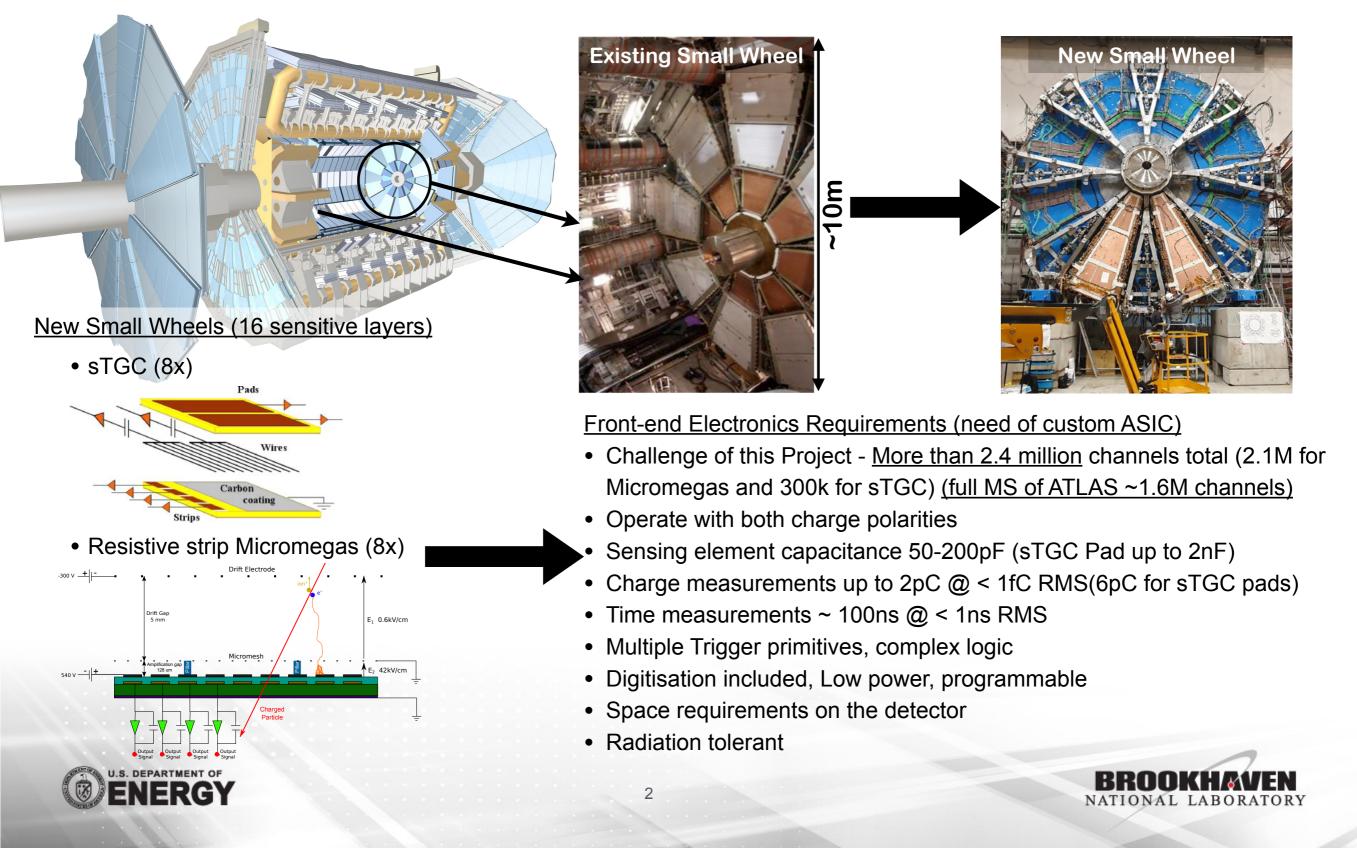




BROOKHAVEN SCIENCE ASSOCIATES

The ATLAS New Small Wheel(s) Upgrade

- The motivation of developing the VMM ASIC was the ATLAS NSW upgrade at CERN
- Biggest MPGD development and most complex part of the muon spectrometer ever built



The VMM front-end ASIC - Evolution



- Mixed-signal
- 2-phase readout with external ADC
- ✓ peak and timing information

Information

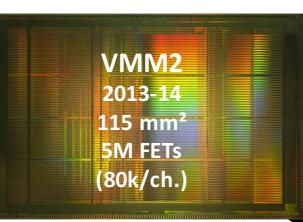
reighbouring readout

🗹 sub-hysteresis

discrimination

few timing outputs

- Mixed-signal
- Continuous readout
- Current-output peak detector
- ✓ Increased range of gains
- ✓ <u>Three ADCs</u> per channel
- FIFOs, serialised data with DDR



- Serialised ART with DDR
- Additional timing modes
- 64 timing outputs
- Additional functions and fixes

The VMM was designed at BNL in collaboration with IFIN-HH
 It is fabricated in the 130nm Global Foundries 8RF-DM
 process (former IBM 8RF-DM)



- ✓ LVL0 pipeline and buffering for ATLAS
- **SEU-tolerant logic**
- Revised front-end for high charge

and capacitance (2nF, 50pC, fast recovery)

- ✓ SLVS signals
- Reset controls
- Timing at threshold
- Timing ramp optimisation
- ✓ Ion tail suppressor (fast recovery)
- Int. Pulser range extension
- ART synchronisation to BC clock
- additional functions and fixes
- VMM3a fixed open bugs from
 - VMM3 and introduce some stability fixes on the ADCs and Front-end

VMM3a - Production Version !

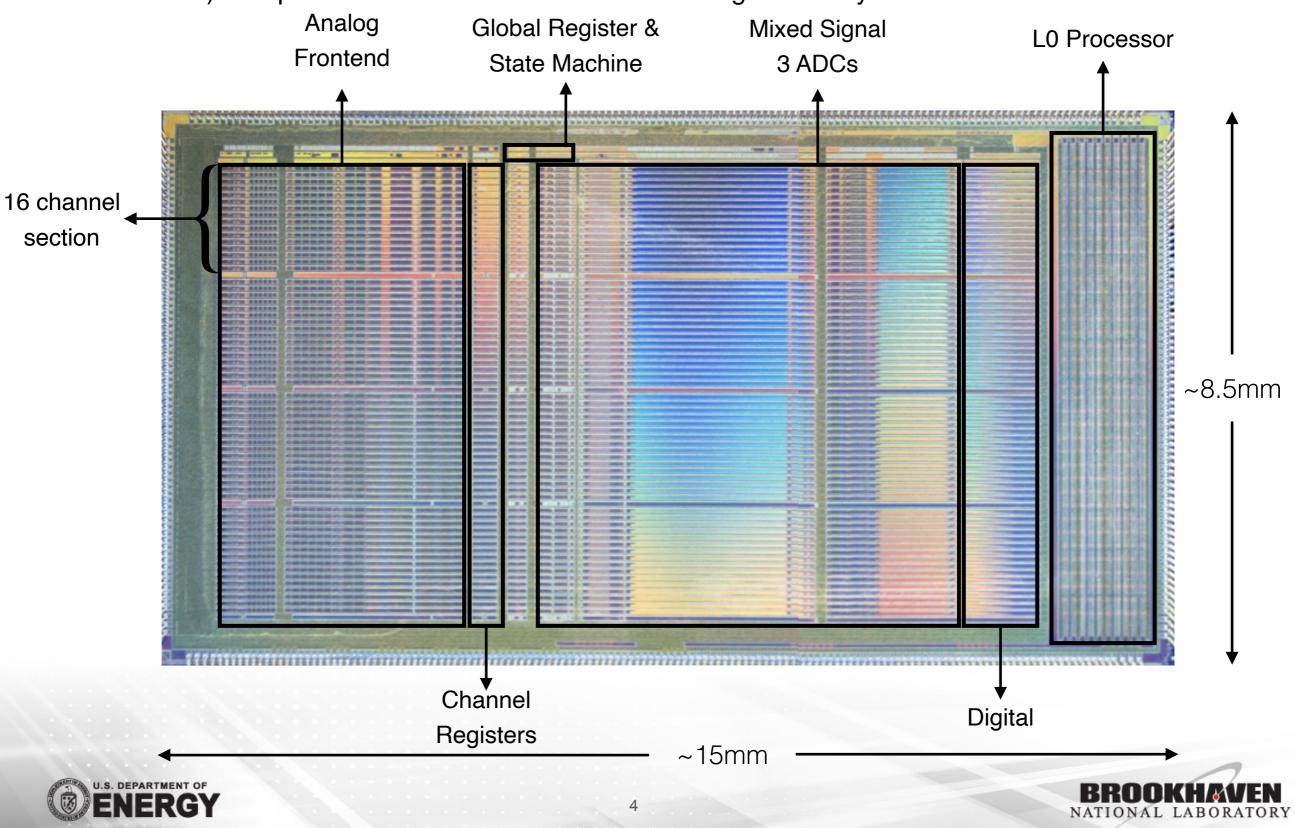
VMM3/3a 2015-2017 130mm² 10M FETs (160k/ch.)

~10mW/channel

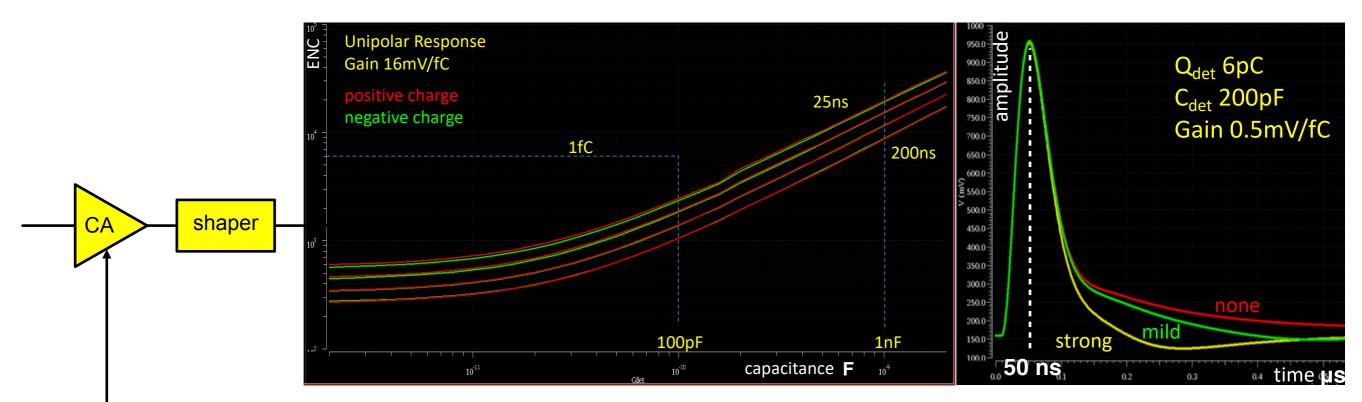


An actual photo of the ASIC

• The ASIC features **64 channels** that extend along the size of the die. At the end the L0 section (explained in later slides) is separated to isolate the noise from the digital activity

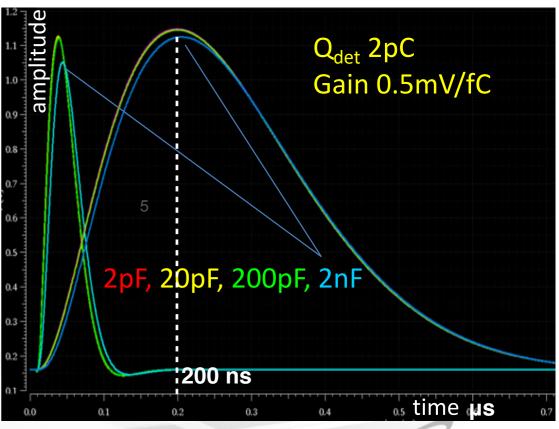


VMM3a Amplifier & Shaper



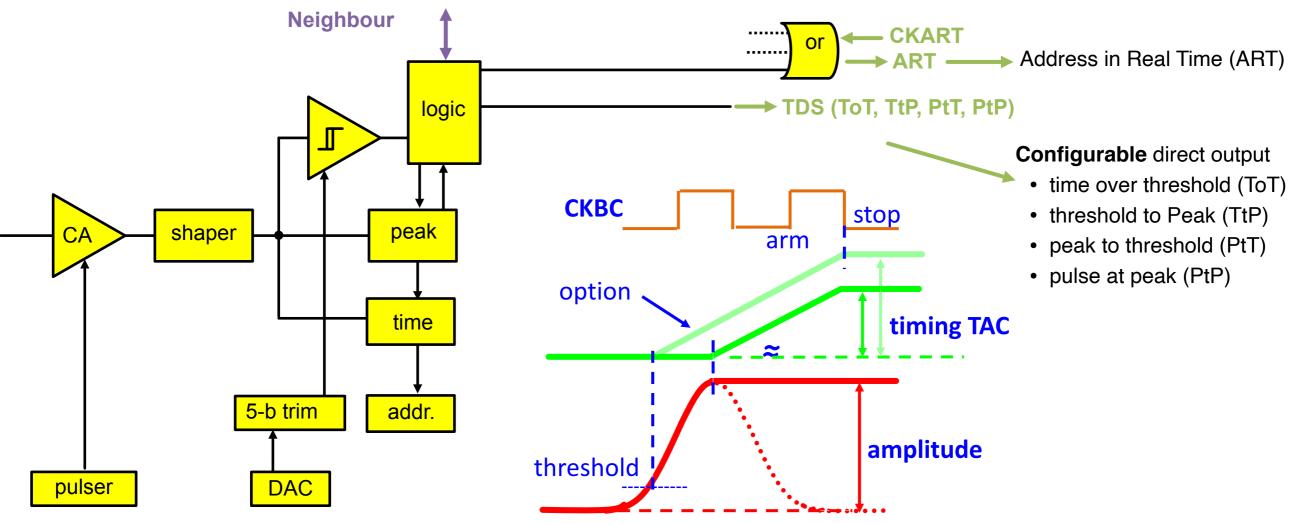
- Input transistor: PMOS, 3 stage amplifier,
 - 2 stages used for adjustable gain: 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC
 - last stage for charge inversion (positive or negative)
- Input capacitance: can operate from sub-pF to several nF
- Maximum charge: 2 pC in linear range, fast recovery from 50 pC
- Semi gaussian DDF c-shaper 3rd order
 - Configurable ion tail suppression: none, mild or strong
 - Adjustable peaking time: 25, 50, 100, 200 ns
 - Leakage-adaptive, BGR-stabilised baseline





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VMM3a Discrimination, Charge and Time

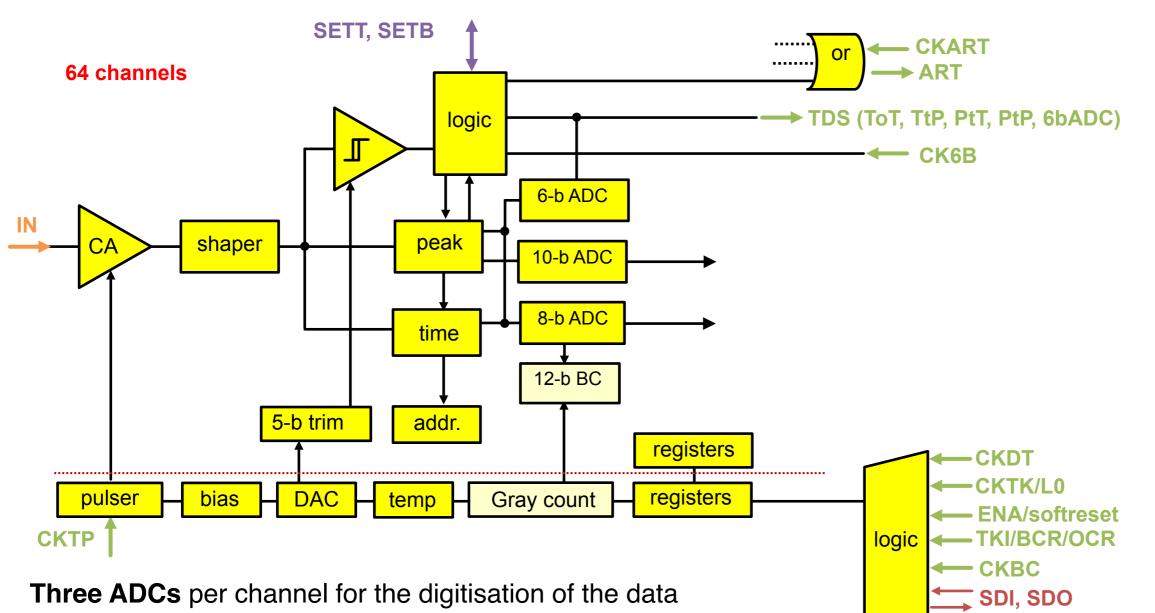


- Global 10-bit DAC for adjusting the threshold Discrimination with sub-hysterisis (effective 2mV)
- Adjustable 5-bit discrimination threshold per channel to adjust at ~mV level
- Neighbour logic to trigger sub-threshold channels with inter-chip communication
- Configurable direct output per channel and serial fast output of address as an OR of all channels
- Peak detection: measurement of peak amplitude and storage in analog memory
- **Time detection**: measurement of **peak/threshold** timing through a configurable time to amplitude converter (**TAC**: 60, 100, 350, 650 ns) and storage in analog memory
 - Clock working mode on synchronous machines but also as strobe for asynchronous operations





VMM3a ADCs



- 6-bit ADC, single stage conversion with adjustable conversion time and offset, completes within 25 ns from peak
- 10-bit ADC, 200 ns adjustable conversion time/offset, for peak amplitude conversion
- 20-bit timing information with 8-bit ADC, 100 ns conversion time + 12-bit Gray-code counter, BC clock
- 2 step mode conversion for 10-bit & 8-bit ADCs First stage the comparison identifies one of the macro-cells and at the second stage the micro-cell is identified, possibility to jump through macro-cells

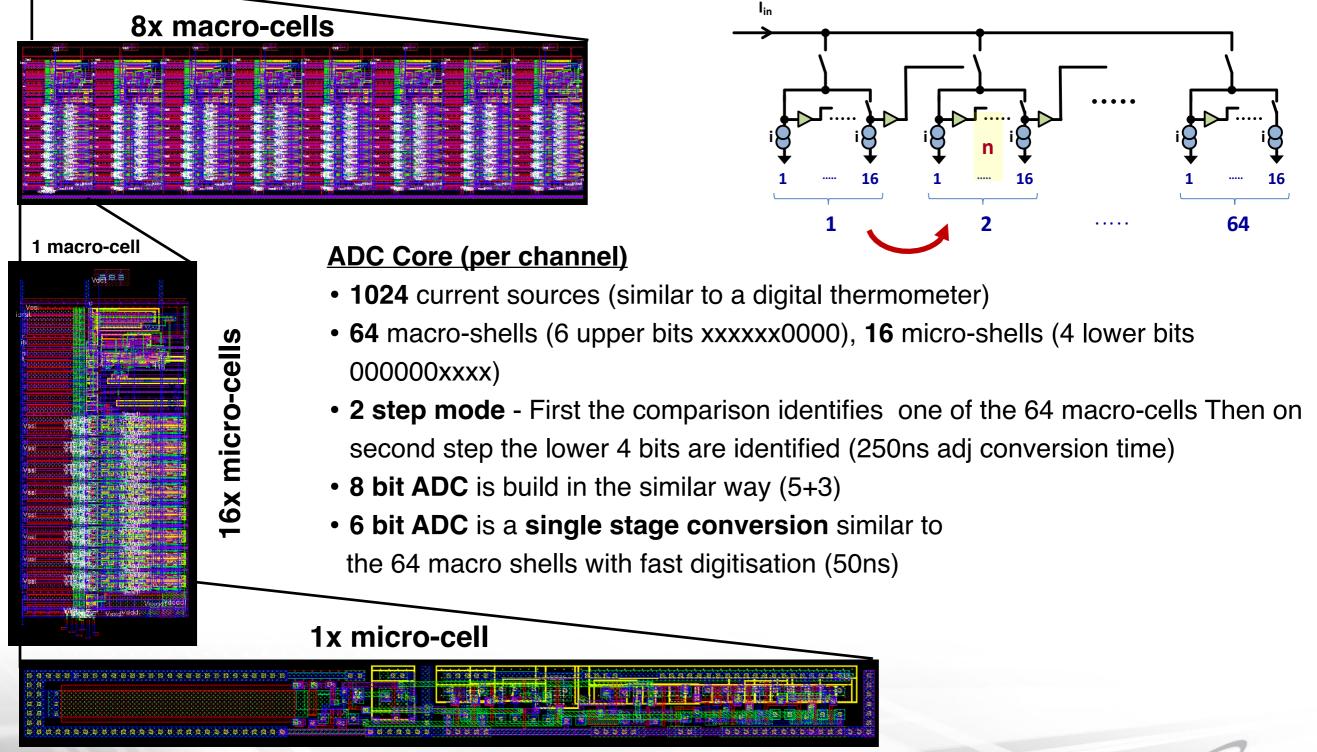




SCK, CS

10-bit Current-Mode Domino ADC - Functionality

ADC Cells

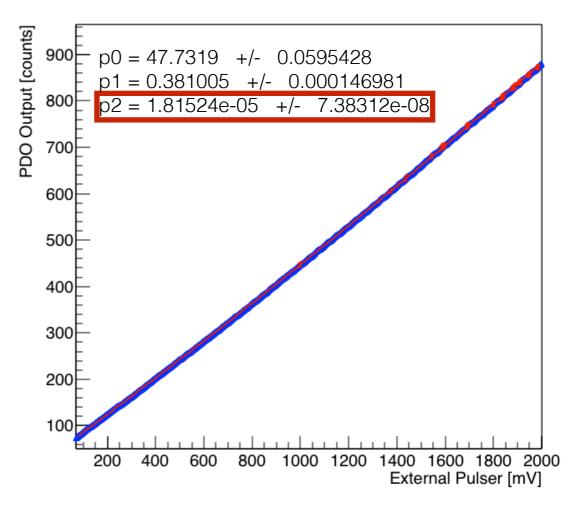


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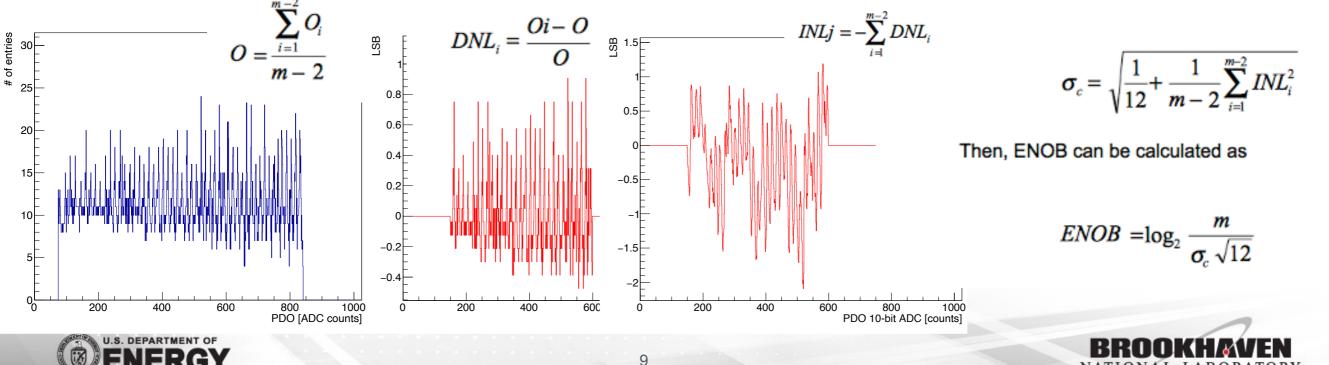


ADC Performance - 10bit example

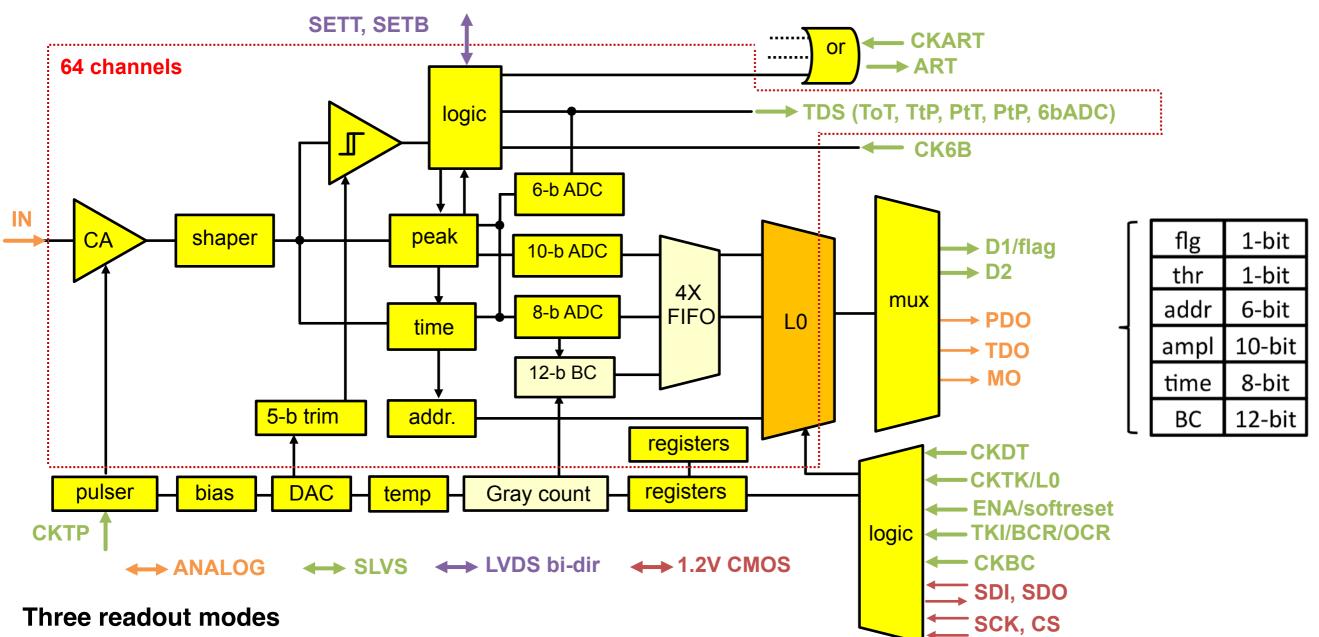
- In order to evaluate the ADC performance, a full
 scan with fine step was performed
- The ADC cannot be driven with a sinusoidal waveform for accurate estimation of its "noise" from the FFT
- In that sense the DNL and INL is calculated and used to estimate the ENOB of the 10-bit ADC
- The non-linearity introduced by the ADC is of the order of 2x10⁻⁵
- Equivalent number of bits ~8 (noise free) for the 10-bit ADC



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VMM3a Readout & Overall Architecture



- Mixed mode with peak & time analog output + address (external ADCs)
- Digital continuous with internal ADCs and 38-bit data at 2 outputs with 200MHz DDR, trigger-less or with external trigger and auto reset
- Level-0 processor external trigger mode with 64-deep latency FIFO programmable acceptance windows with 8b/10b encoding. Each channel could achieve 4MHz, total latency 16us

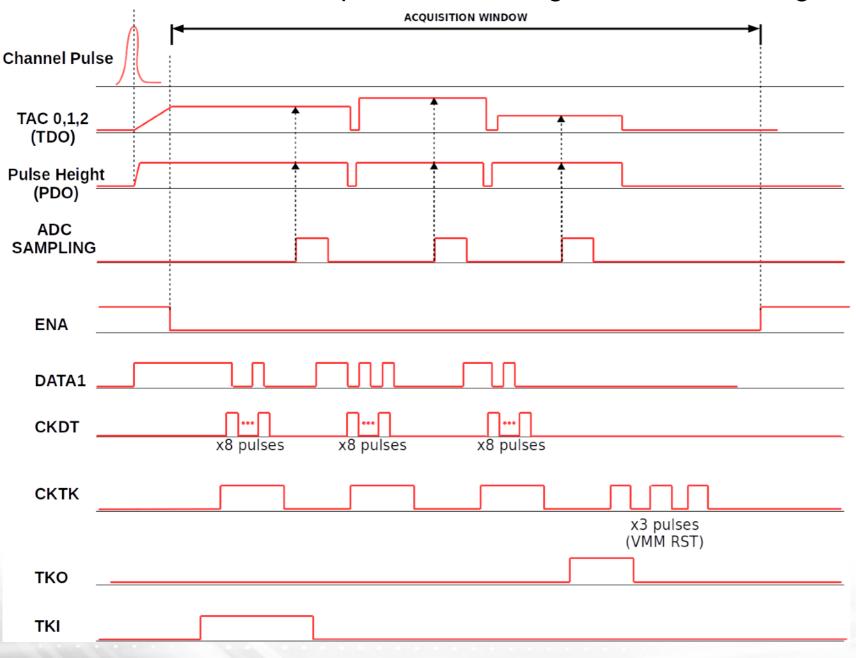




Modes of operation - Analog

In two-phase (analog) mode which is the mode originally implemented in the VMM1, the ASIC operates in two separate phases: acquisition and readout - During the acquisition phase the events are processed and stored in the analog memories of the peak and time detectors. As soon as a first event is processed, a flag is raised at the digital output.

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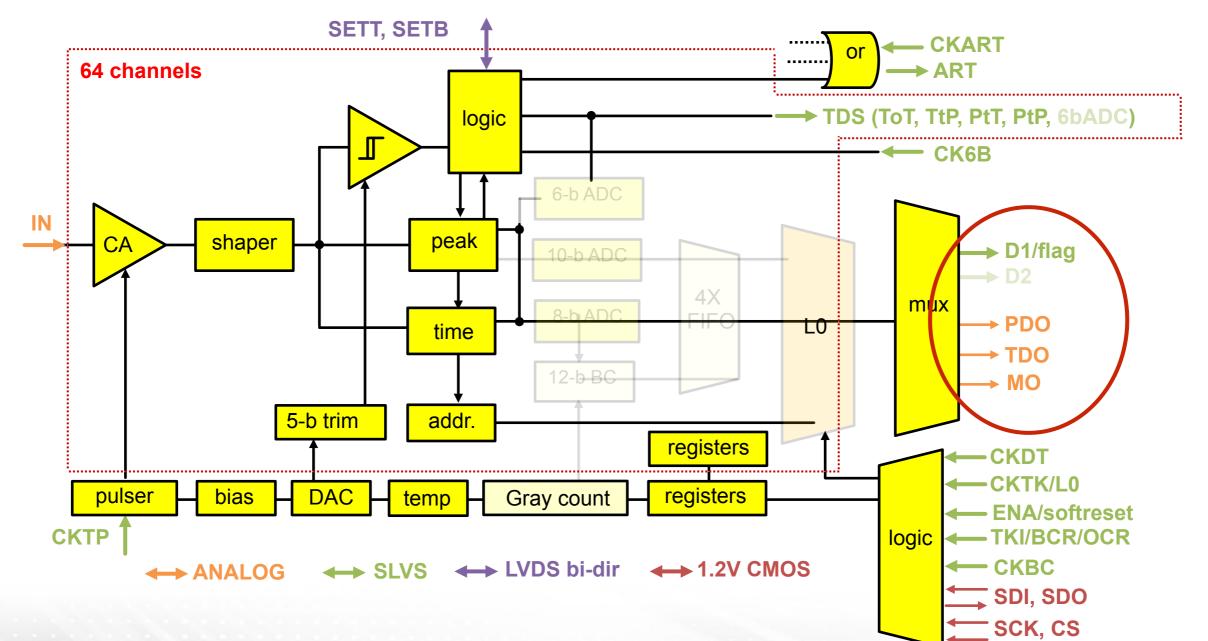


Once the process is complete the **ASIC can be switched readout phase**. The first set of amplitude and time voltages is made available at the **analog outputs**. The **address of the channel is serialised** and made available at the digital output using **six data clocks**.



Modes of operation - Analog

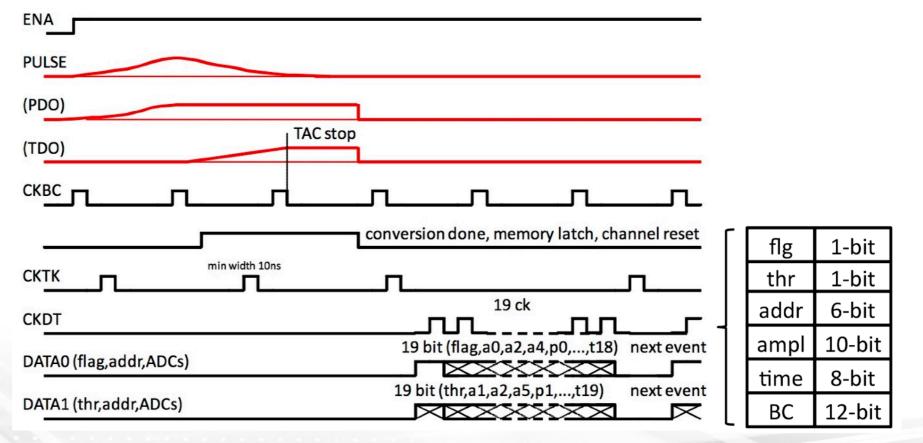
- · In this mode all analog buffers are multiplexed in the analog outputs
- Lengthy operation since each analog signal needs to be sampled while the address is read out serially





Modes of operation - Continuous

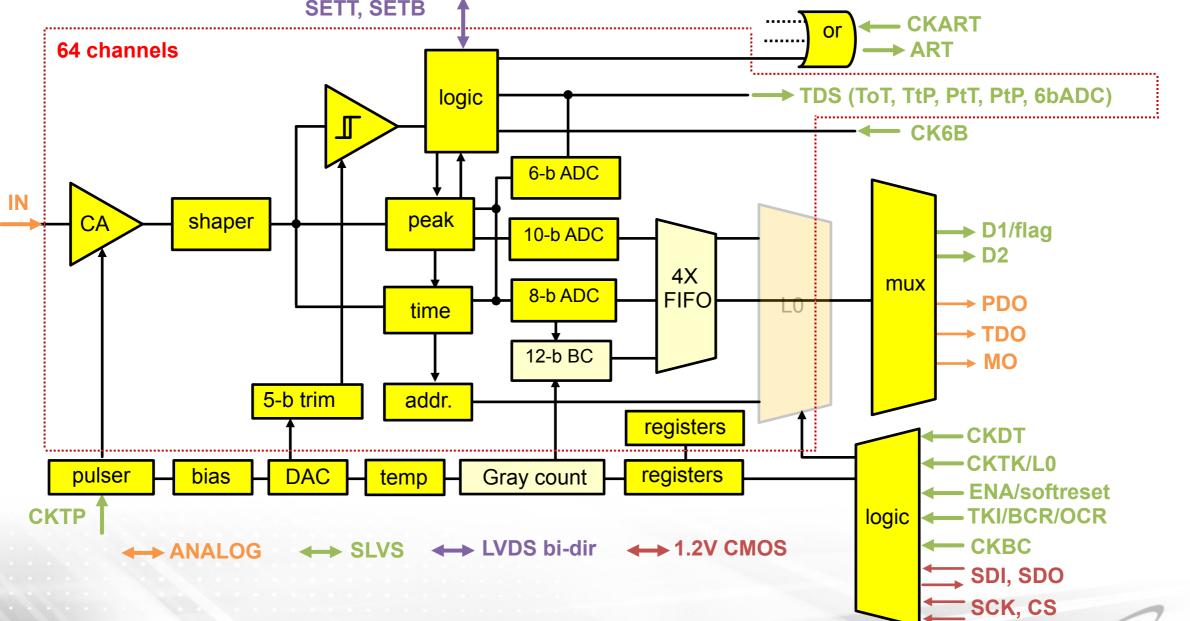
- Trigger-less mode with peak and time detectors convert the voltages into currents routed to the 6/10-bit ADC and 8-bit ADC respectively.
- The 10-bit ADC provides a high resolution A/D conversion of the peak amplitude
- The 8-bit ADC provides the A/D conversion of the timing (measured using the TAC peak or the threshold to a stop signal). Time associated with global 12-bit counter.
- In the continuous mode the 64 channel direct outputs are available as well providing time-overthreshold (ToT), threshold-to-peak (TtP), peak-to-threshold (PtT), or a 10 ns pulse occurring at peak (PtP) or the 6-bit ADC. The channel self resets at the end of the timing pulse, thus providing continuous and independent operation of all 64-channels.





Modes of operation - Continuous

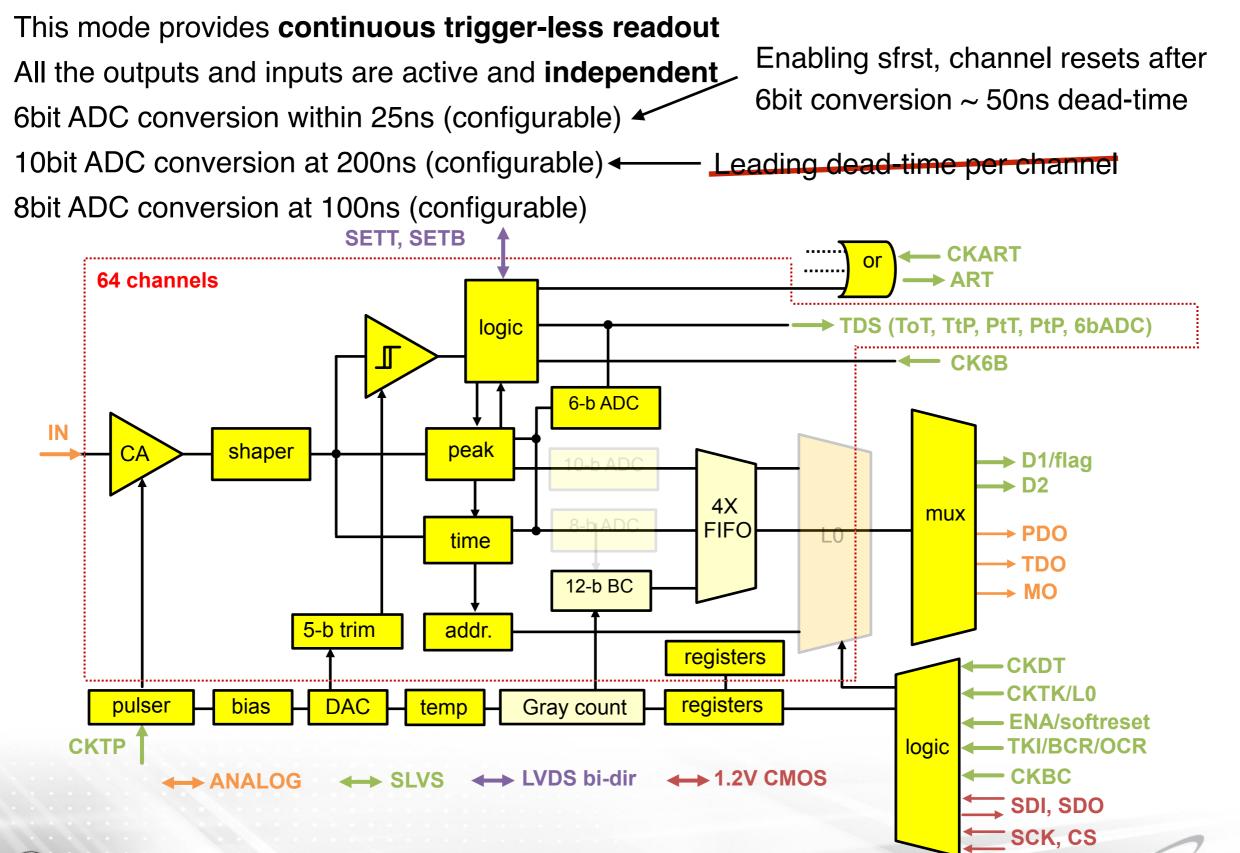
- This mode provides continuous trigger-less readout
- All the outputs and inputs are active and independent
- 6bit ADC conversion within 25ns (configurable + reset)
- 8bit ADC conversion at 100ns (configurable + reset)





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Modes of operation - Direct output

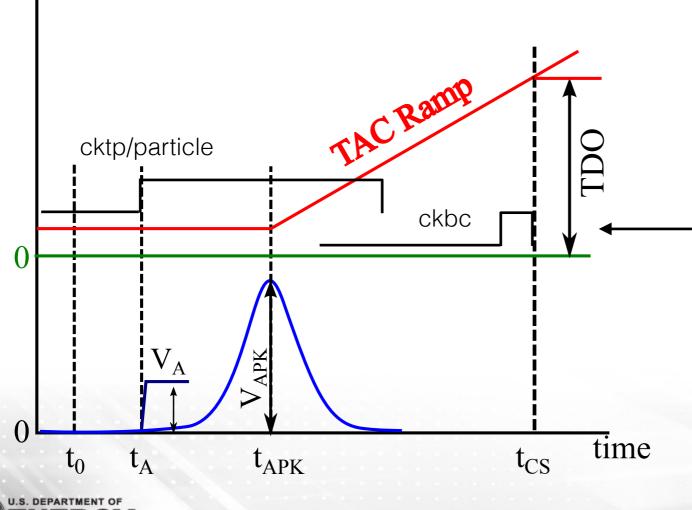




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Modes of operation - Continuous + ext trigger

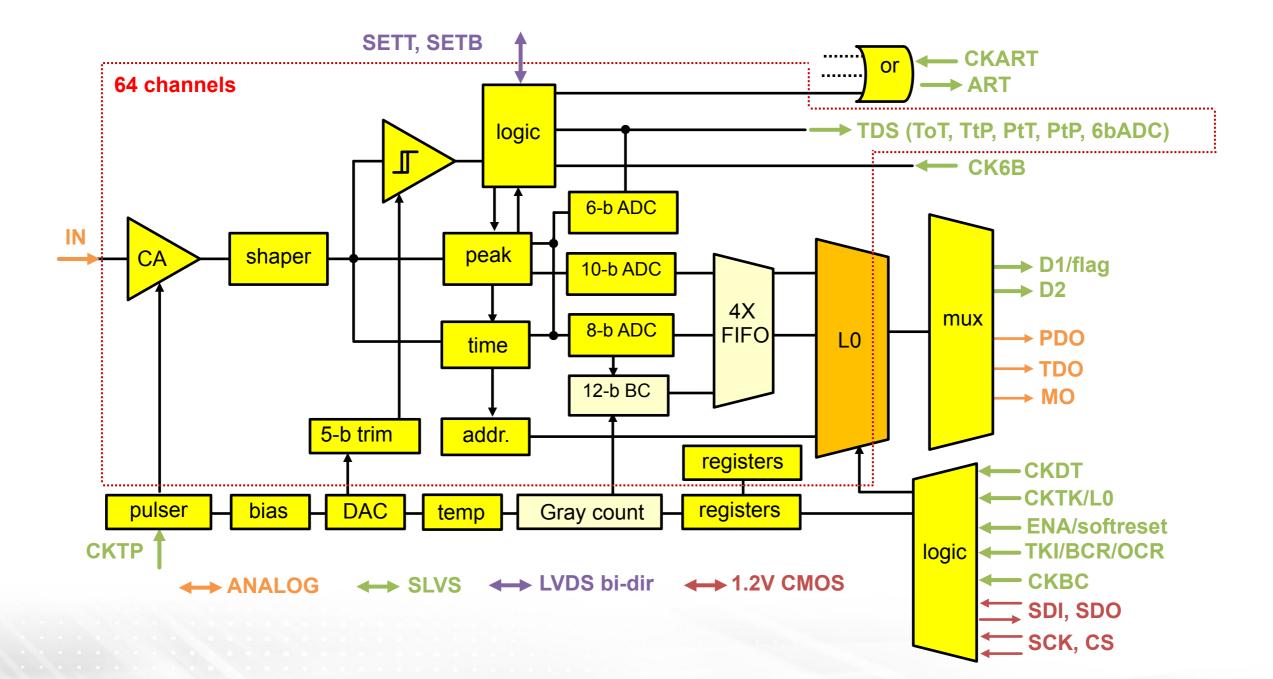
- VMM design targets synchronous machines hence can be difficult to use in an environment like a test beam where asynchronous operation is needed but precise timing is needed to be measured (drift time)
- Most chips designed for synchronous machine suffer from time jitter in such environment
- On VMM a mode was foreseen to do such measurement where the ckbc can be used as a strobe and not like a real clock
- It can be **send as a trigger signal** with a **fixed latency** achieving precise time measurements



- Trigger signal from external source
- Can be combined with register stcr where channel resets if stop signal not occurs within the TAC ramp
- Implies that trigger is propagated within the TAC ramp up time (60ns-650ns)
- The longer the TAC though the lower the resolution on 8-bit information from the ADC
- Highly correlated trigger readout and noise subtraction

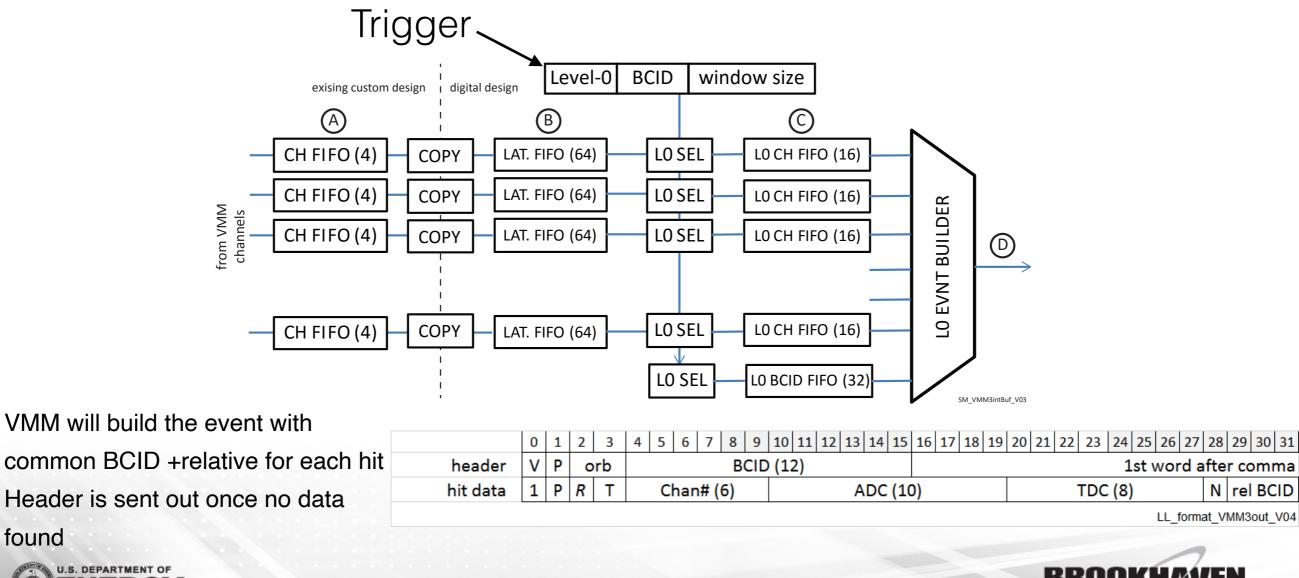


- The signal processing is done in the same way but the readout is different.
- This is an **externally triggered operation** for **synchronous** machines





- Each channel has a Level-0 Selector circuit which is connected to the output of the channel's latency FIFO.
- The selector finds events within the BCID window (maximum size of 8 BC clocks) of a Level-0 Accept and **copies them to the L0 Ch FIFO**. The data are available in the output which is running on IDLE K28.5 in two data lines and can be readout DDR at a speed of 640Mbps (160MHz clock tested, effective bandwidth 560Mbps due to 8b/10b encoding).



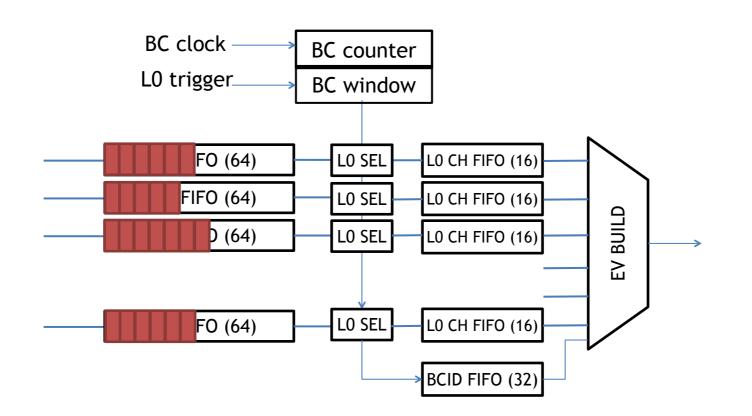
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found

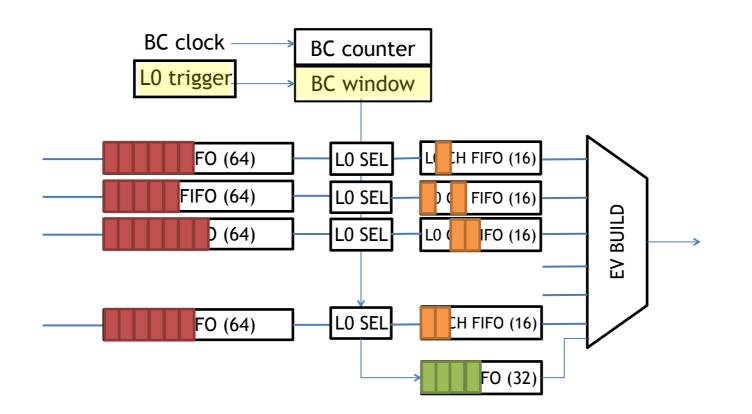


Latency FIFO takes data from the mixed-signal front-end

- FIFO designed to accommodate 4 MHz data in a 10 μs latency window
- 20-bit data: threshold, amplitude (ADC), timing (ADC)





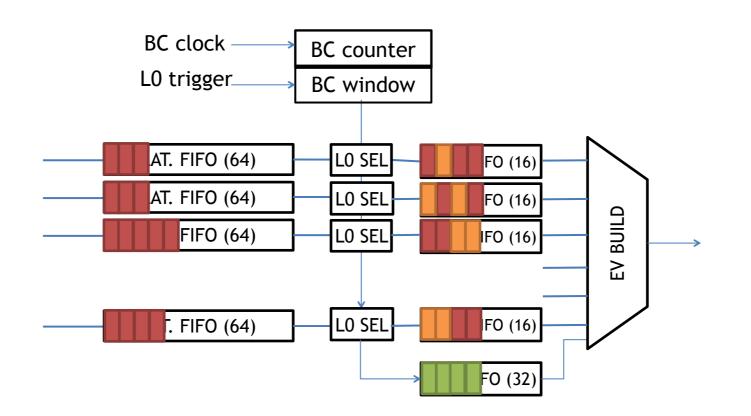


At LO trigger builds BC trigger window and selects data for the LO CH FIFO

- flushes old data
- fills non-valid data as needed (for simultaneous overflow)
- builds BCID FIFO







Builds event

- BCID followed by valid data with address
- header
- event built in < 1µs

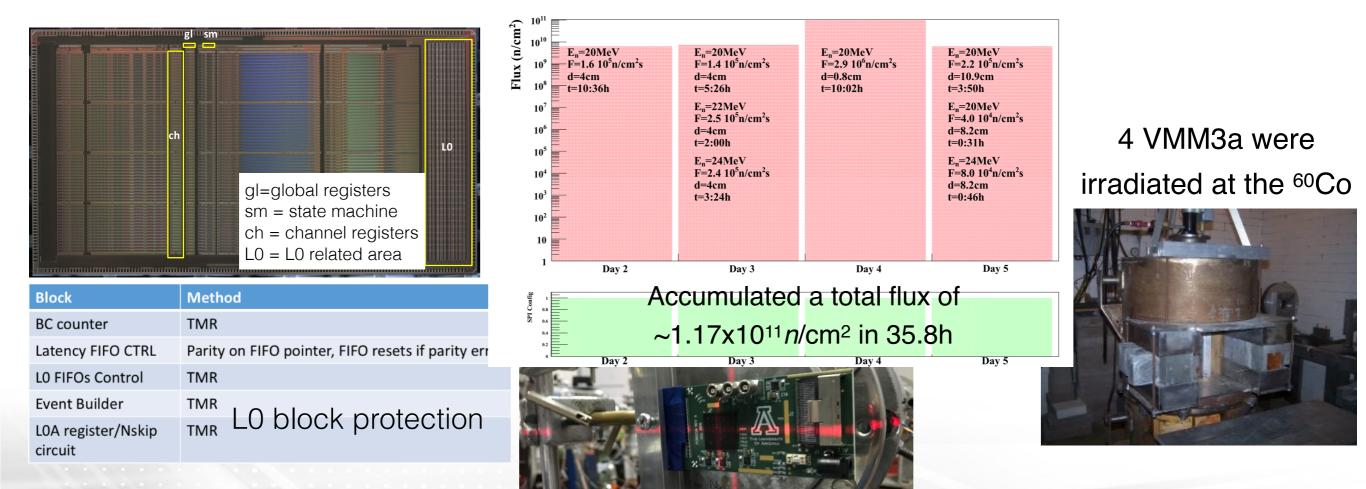
Sends data through two data links (DDR, 640MB/s)`





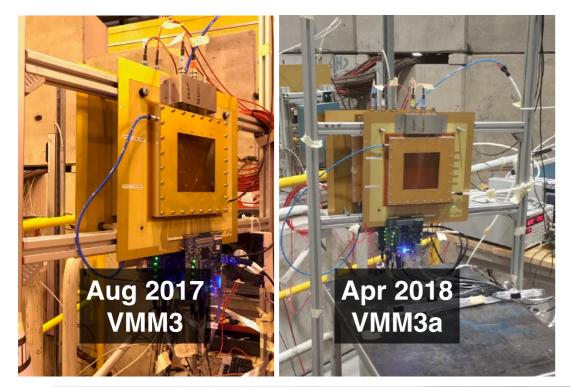
Single Event Upset & Total Ionisation Dose

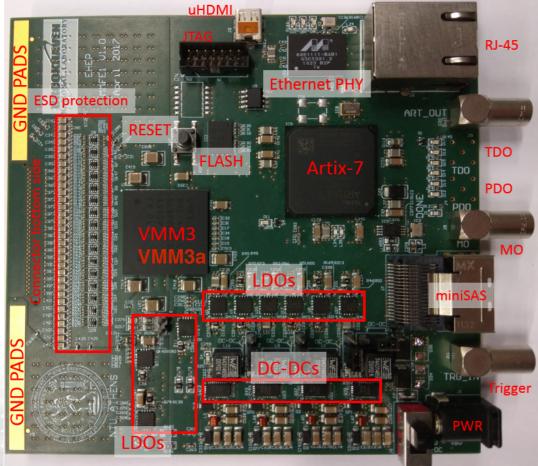
- In the VMM3a there are three types of storage elements that require SEU protection, the configuration registers, the state machine control logic and the L0 logic
- To mitigate for SEU two techniques are used:
 - Dual Interlocked Cells (DICE) for the protection of the configuration registers
 - Triple Modular Redundancy (TMR) for the state machines and the L0 Logic blocks
- L0 Data
 - Single-bit faults on data are flagged by a parity bit
 - The parity is registered in the FIFOs and transmitted outside



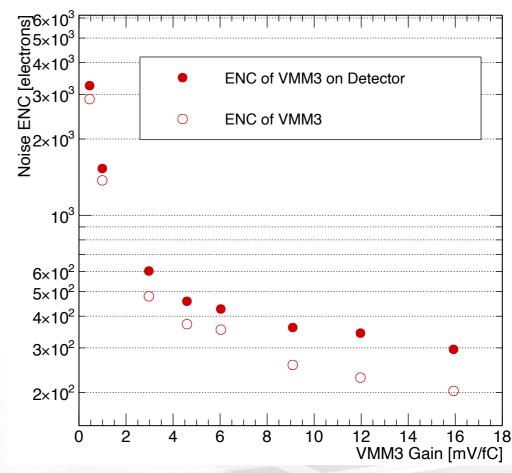


Test Beams with Resistive - Micromegas prototypes

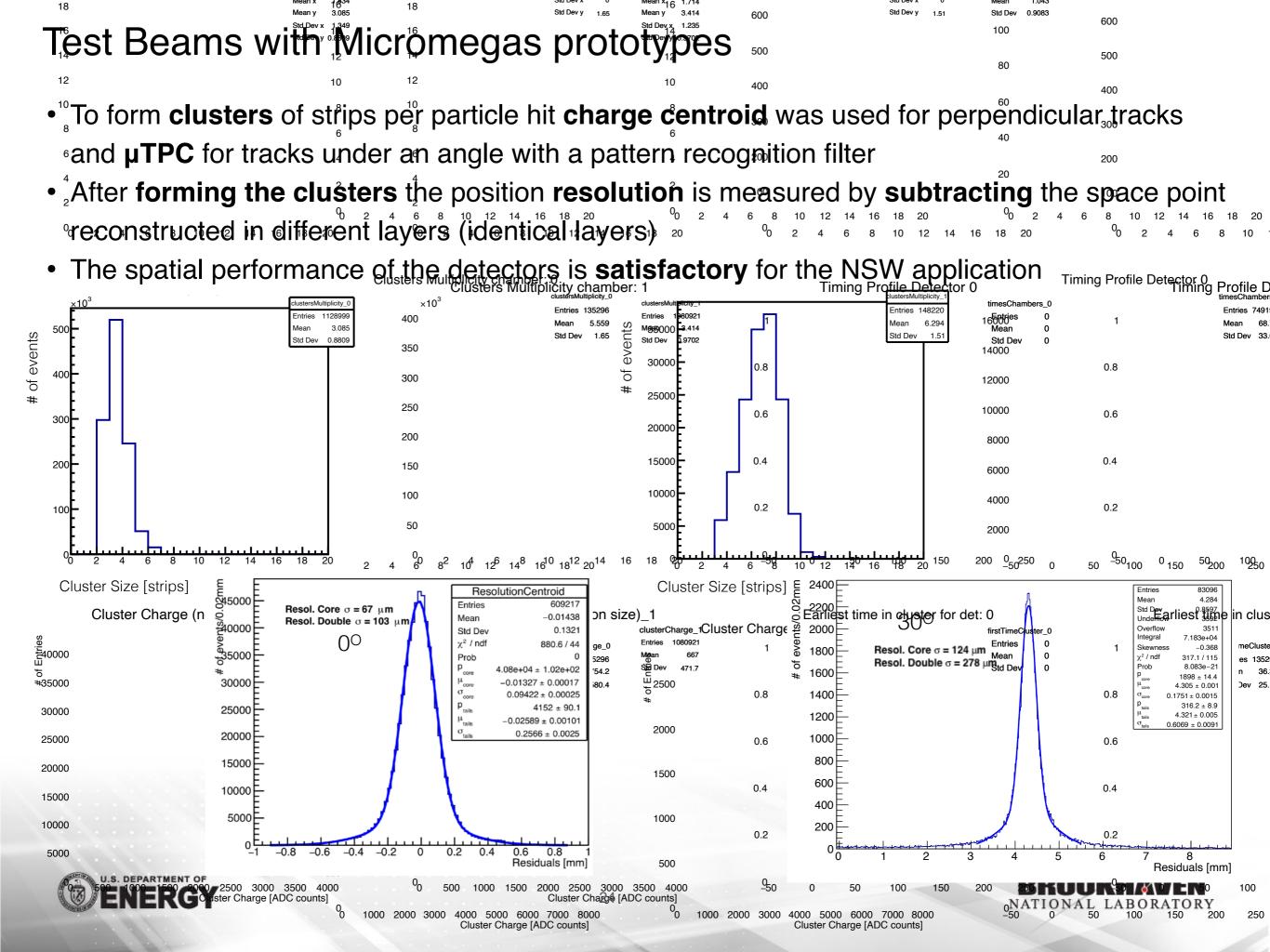




- Setup of of 2x MMFE1s on 2x Resistive Micromegas chambers (Ar+7%CO₂ 400µm pitch, 5mm drift)
- Custom made firmware and software was developed allowing to trigger with scintillator system
 - Mode to control the CKBC externally
- High data rate ~20KHz/channel (VMM can reach 4MHz), arrived at the limit of Gbps UDP connection
 Noise levels of 300 e⁻ ENC at gain 9mV/fC, 200ns







Integration with Micromegas Production modules

SCA

ATHEL

DCDC

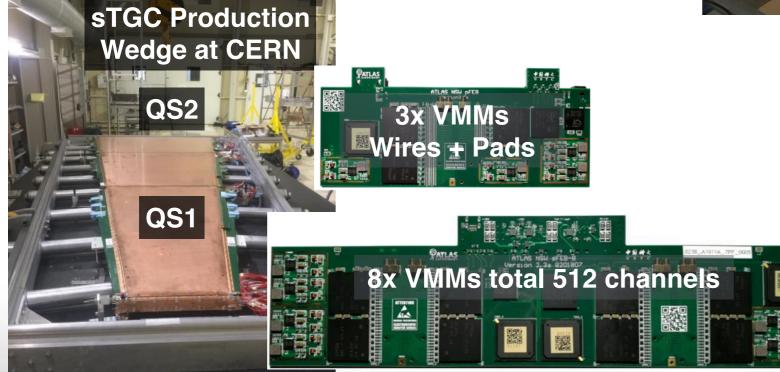
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- Micromegas & sTGC Production modules at CERN integrating the VMMs
- All the FE boards are readout through custom made 4.8Gbit serialiser boards with fibres
- Water Cooling is a must in these applications

8x VMMs total 512 channels

ROC

MMFE8





400-pin

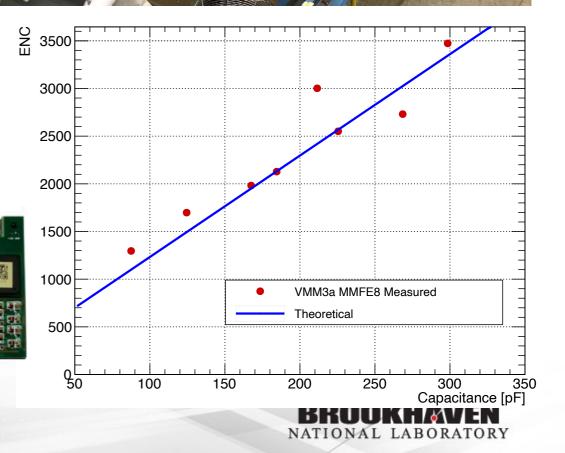
21 x 21 mm²

BGA

1mm pitch

DCDC

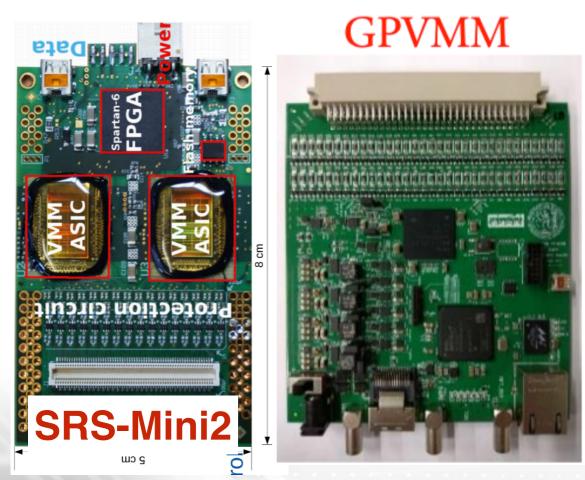




Example of applications

VMM has been as well of interest and in some cases already made it in the following other than NSW applications:

- Focal Plane Detector for NUMEN
- Interest from n_TOF at CERN
- Mu2e at Fermilab
- DUNE Near Detector at Fermilab
- CERN RD51 SRS system (replace APV hybrids) which is a hub for many other applications









Applications - Future SRS VMM users / interested

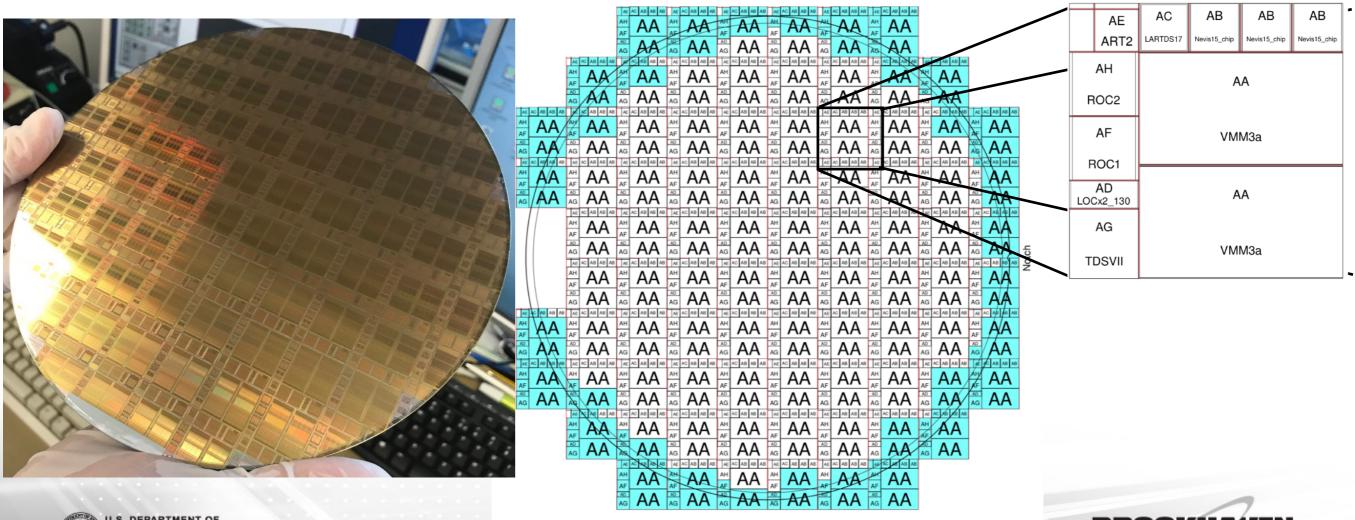
| Group | Application | VMM hybrids | Contact |
|---|--|---------------|---------------------------------|
| ESS Lund / BrightnESS | NMX instrument @ ESS | 164 | Dorothea PFEIFFER |
| University of Science and Technology of China | RICH R&D for future colliders in China (CEPC and STCF) | 156 | LUI Jianbei |
| Bonn University | BASTARD neutron detector | 71 | Jochen KAMINSKI Markus KÖHLI |
| Mainz University | MAGIX experiment @ MESA* | 211 | Stefano CAIAZZA |
| Budker Institute of Nuclear Physics, Novosibirsk | µWell MPGD R&D | 22 | Lev I. SHEKHTMAN |
| INFN Tieste | Generic R&D | 10 | Silvia DALLA TORRE |
| Tsukuba University | ALICE FoCal, Si Pads | 50 | CHUJO Tatsuya |
| GDD group CERN | Generic R&D | 16 | Eraldo OLIVERI |
| Peking University | CMS GEM upgrade | 52 | Dayong WANG |
| LMU Munich | Ion Tomography with Micromegas | 16 | Felix KLITZNER |
| LMU Munich | Medical physics with MPGDs, Si | 48 | Jona BORTFELDT |
| ETH Zurich | GBAR experiment @ CERN | ≈40 | Gianluca JANKA |
| CERN | BGV(Beam Gas Vertex) beam monitor* | 200 | Robert KIEFFER |
| University of Virginia, Charlottesville | EIC tracker @ RHIC* | Not known yet | Kondo GNANVO |





VMM Production

- The VMM is produced in a 8" wafer with 2 copies of the chip in a reticle, total 113 chips per wafer. In the same floor-plan other ATLAS ASICs are included
- ATLAS has already produced and package 70,000 Chips (RD51 another 3k chips)
- Many iterations with experts from Global Foundries to improve the yield (currently ~72% due to damage on the Baseline stabiliser circuit). Already got indications on issues in their processes
- Current experience shows yield of ~80% mainly due to BLH probably getting damaged during the process or over etching in some lines (already investigated that with GF)
- In ATLAS we had no time to further investigate the issue and moved forward to production



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VMM Future ?

- Clearly VMM is a state of the art ASIC for physics applications
- There is a big demand from several applications and experiments which clearly needs high support. I have though quite a lot of responsibilities in ATLAS as of now which limits me from providing support
- BNL has looked into how to support demands and EIC (if VMM is needed) maybe be a good opportunity to have this support (instrumentation of BNL is already quite expert in VMM)
- The main designer, G. de Geronimo resigned from BNL since VMM3 release but through these years was engaged with specific contract to advance VMM to the state that we have it today
- Clearly 130nm will be around for some years but VMM could become even more attractive
 - Move it to TSMC 65nm technology, much more reliable (many users go away from GF, CERN as well)
 - A point which has been proven difficult in VMM was the implementation of the ADCs. Clearly this is an area of improvement or maybe something from the market can be employed
 - ADC deadtime is what limits the VMM as of now to 4MHz per channel. I imagine that this can be improved if applications need it, implementing more data lines as well for more throughput
- ➡Clearly though those are my thoughts... probably I should hear yours now !





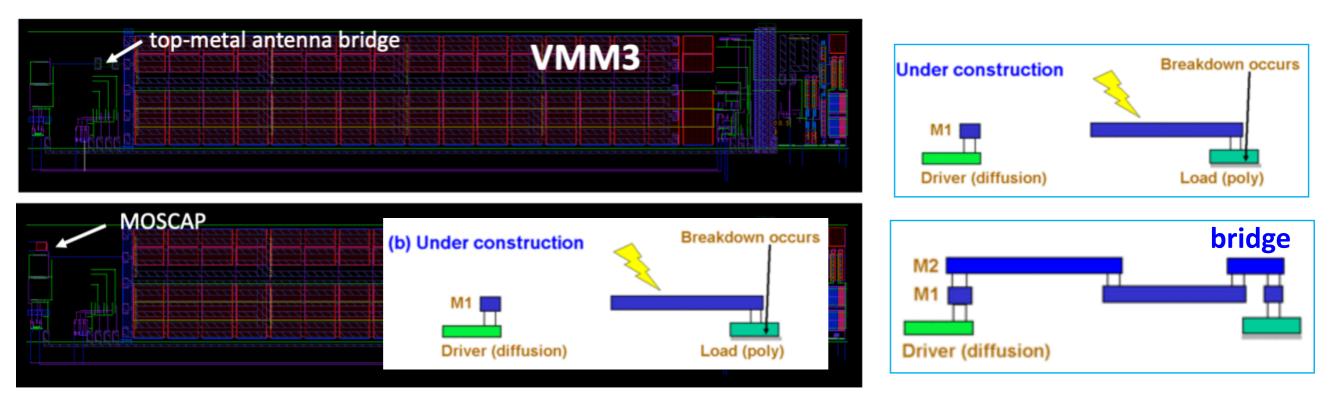
backup



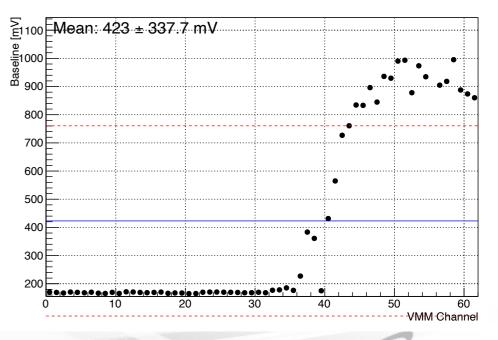


VMM BLH

- On VMM3a, under the suspicion of antenna damage, the bridge of the top layer was replaced by a MOSCAP
- · Just to note that both designs are satisfying the DRC for antenna damage



The issue cannot be explained from simulation:
 <u>Points to damage of the gate, or degradation of it</u>







The Shaper

The VMM Shaper

The VMM "semi-Gaussian" shaper responds to an event with an analog pulse, the peak amplitude of which is proportional to the event charge. The time needed to return to baseline after the peak, depends on the the time constants and the configuration of poles. The VMM facilitates a 3^{rd} order c-shaper with the combination of one real and two conjugate poles. The transfer function T(s) for such shaper is given by the following expression:

$$T(s) = \frac{1}{(s+p_1)\prod_{i=2}^{(n+1)/2} \left[(s+r_i)^2 + c_i^2 \right]} = \frac{1}{(s+p_1) \left[(s+r_2)^2 + c_2^2 \right]}, \quad n = 3$$

where n is the order of the shaper, and r_i, c_i are the real and imaging parts. The roots are:

$$(s+r_2)^2 + c_2^2 = 0 \Rightarrow s+r_2 = \pm jc_2 \Rightarrow s = -r_2 \pm jc_2$$

so the transfer function can be written with the simple fractions like :

$$T(s) = \frac{K_1}{(s+p_1)} + \frac{K_2}{(s+r_2 - jc_2)} + \frac{K_3}{(s+r_2 + jc_2)}$$
(1)

where one real pole, $\text{pole}_{\emptyset} = -p_1$ and the two complex $\text{pole}_1 = -r_2 + jc_2$ and $\text{pole}_2 = -r_2 - jc_2 = p_1^*$, $\text{Rel}_1 = -r_2$, $\text{Spole}_1 = c_2$. The coefficients K_i are :



VMM Registers

| shm routes making monitor b PDO output see enables fast recovery from high charge shf(0) [0], shf(0) [1] makeg output https: [1] enable (TDO, PDO, MO) stat stat enables bipolar hape sm5-sm0, smx monitor multiplexing. enables ([0] enabled) stat enables fast rest of the bond bipolar hape sm5-sm0, smx monitor multiplexing. enables ([0] enabled) stat enables fast rest of the bond bipolar hape stat, sm1 common monitor: smx, sm5-sm0 [0 00000 to 00100], pulser DAC (after pulser switch), threshold DAC, hand- gap reference, the emperature sensor) stat enable sw1 1002 termination on dch1 stat, sm0 [0 1] channels to to 63 monitor (AC) and high-leakage operation (enables SLH) streamle monitor: smx, sm5-sm0 [1] streamle monitor smx, sm5-sm0 [1] streamle monitor smx, sm5-sm0 [1] streamle monitor: smx, sm5-sm0 [1] streamle monitor smx, sm5-sm0 [1] streamle smipolar streamle monitor smx, sm | Global bits (defaults are 0) | Description | Global bits (defaults are 0) | Description |
|--|--|--|------------------------------|---|
| shin (b) (b) ship (b) (c) show (c) | sp | input charge polarity ([0] negative, [1] positive) | s32 | skips channels 16-47 and makes 15 and 48 neighbors |
| soft [0 1], shpn [0 1], shpn [0 1], shanp [0 1], enable (TDO, PDO, MO) skp enabage current disable [0] enable(TDO, PDO, MO) sig leakage current disable [0] enable(TDO, PDO, MO) skp skp enables bing ramp at threshold sinf-sam0, senx monitor multiplexing. Sfst enables find remainston on ckbc app reference, temperature sensor) enables diversion on ckbc skp enables diversion on ckbc sing [0 1], sfam [0 1] ART enable (sfa [1]) and mode (sfam [0] timing at thresh- old, [] timing at peakl skp enables diversion on ckbc st1,40 [00 01 10 11] peaktime [20, 00, 50, 25 ns] skp skped [000:11] skped [000:11] sg2_sel,26[000:11] gain (0, 5, 1, 3, 5, 0, 9, 12, IomV/fC) skped [000:11] | sdp | disable-at-peak | stlc | enables mild tail cancellation (when enabled, overrides sbip) |
| ist leakage current disable (0) emabled) sm5-sm0, scmx monitor milliplexing. sm5-sm0, scmx monitor milliplexing. sm5-sm0, scmx monitor milliplexing. sm5-sm0, scmx monitor milliplexing. sfm [0 1], sfam [0 1] channel to notice: scmx, sm5-sm0 [0 000001 to 000100, paker DAC (after paker switch), threshold DAC, hand-gap reference, temperature sease) stvst sfn [0 1], sfam [0 1] ART enable (sfa [1]) and mode (sfam [0] timing at threshold stvst sfn [0 1], sfam [0 1] ART enable (sfa [1]) and mode (sfam [0] timing at threshold stvst sfn [0 1] enables (sfa [1]) and mode (sfam [0] timing at threshold stp 1001 termination on ckthi stst [0 1] enables (sfa [1]) and mode (sfam [0] timing at threshold stp 1001 termination on ckthi stst [0 1] enables (sfa [1]) and mode (sfam [0] timing at threshold stp 1001 termination on ckthi stot [0 1] timing outputs control 1 (sfb must be disabled) slockitot stot [0 1] timing outputs control 1 (sfb must be disabled) slockitor stot [0 1] timing outputs control 1 (sfb must be disabled) slockitor stot [0 1] enables shc 1001 trainging BC offset rollower idual stot [0 1] enables bid (strigger sensibid) slockitest | sbmx | routes analog monitor to PDO output | srec | enables fast recovery from high charge |
| sm5-sm0, semx monitor multiplexing sfst mohe by 1000 termination on ekb of Common munitors came, sm5-sm0 [0 000001 to 000100], pulser DAC (after pulser switch), threshold DAC, band- gap reference, temperature sensor) sfst mohe by 1000 termination on ekb of chunnel monitors came, sm5-sm0 [0 000000 to 111111], channels 0 to 63 abstraction on ekb should termination on ekb sfn [0 1], sfam [0 1] ART cnable (sfn [1) and mode (sfam [0] timing at thresh- old, [1] timing at pask) should termination on ekb st1.st0 [0 01 10 11] predstime (200, 100, 50, 25 ns) should termination on ekb sg2.gs2.gs0 [000:111] enables full-mirror (AC) and high-leakage operation (emables SLH) stot [0 1] enables full-mirror (AC) and high-leakage operation (emables SLH) stot [0 1] enables direct-ourigut logic (both imag) and shole enables direct-ourigut logic (both imag) and shole enables direct-ourigut logic (both imag) and shole enables direct-ourigut logic (both imag) and shole st0t9-sc110b file stot [00 01 101] stot [0 1] enables direct-ourigut logic (both imag) and shole enables direct-ourigut logic (both imag) and shole st0t9-sc110b file stot [00 01 101] stot [0 1] enables full-mirror (AC) (10/sbit ADC conv. time (increase subtracts 60 ns) stot [0 1] enables high resolution ADC (10/sbit ADC conv. time (increase subtracts 60 ns) stot stot [0, sc20b, sc110b both ADC conversion time stotb, sc20b stot [0 1] transcates 0.5 Mirror< | sbft [0 1], sbfp [0 1], sbfm [0 1] | analog output buffers, [1] enable (TDO, PDO, MO) | sbip | enables bipolar shape |
| Common monitor: scmx, sm5-sm0 [0 00000 to 000100], puker DAC (after puker switch), threshold DAC, hand- gap reference, temperature sensor) e. channel monitor: scmx, sm5-sm0 [1 00000 to 111111], channels 0 to 63 ART enable (sfa [1]) and mode (sfam [0] timing at thresh- odd, [1] timing at peak) ART enable (sfa [1]) and mode (sfam [0] timing at thresh- odd, [1] timing at peak) stat.stf (0 0 11 0 11] peaktime (200, 100, 50, 25 ms) stat set [0 1] cmable shz, 100, 12 termination on ckta stat.stf (0 0 01 10 11] peaktime (200, 100, 50, 25 ms) stot [0 1] cmable shz, 100, 12 termination on ckta stot [0 1] cmable shz, 100, 12 termination on ckta stot [0 1] cmable shz, 100, 12 termination on ckta stot [0 1] timing outputs control [(sfb must be disable) stot [0 1] test pake (loc), 10, 11]; TP, ToT, PtP, PT tPtP: puks to-threshold (not available with s10b) PtP: puks to-threshold (not available with s10b) PtP: puks to-threshold (not available with s10b) test pake (loc) 100 11 11 test pake DAC stot [0 01 10 11] cmable shigh resolution ADCs (10/, 800, 650 ms) stot [0 01 10 11] test pake (loc), se20b Shot enables discrimination stot back ind, se20b Shot anables shigh resolution ADCs (10/, 800, 506 fos ms) stot [0 01 10 11] test pake (loc) 100 11 test pake DAC stot stot (loc) sead three servers to make shight and the conversion time stob and back edge serialized AHT enable sdcds dual clock edge seria | slg | leakage current disable ([0] enabled) | srat | enables timing ramp at threshold |
| puber DAC (after puker switch), threshold DAC, band- gap reference, temperature sensor)slvsthenable sky 1000 termination on dtpsight of ference, temperature sensor)i. channel montor: sens, sm.5-sm0 [1 000000 to 11111], channels 0 to 63slvsthenable sky 1000 termination on dtatsfn [0 1], sfam [0 1]ART enable (fal [1]) and mode (sfam [0] timing at thresh- old, [1] timing at peak)slvsthenable sky 1000 termination on detatst.at0 [0 0 10 11]peaktime (20, 100, 50, 25 ns.)slvsthenable sky 1000 termination on detatst.at0 [0 0 10 11]peaktime (20, 100, 50, 25 ns.)slvsthenable sky 1000 termination on detatst.at0 [0 0 1 0 11]peaktime (20, 100, 50, 25 ns.)slvsthenable sky 1000 termination on detatst.at0 [0 0 1 0 11]enables full-mirror (AC) and high-leakage operation (enables SLH)slvsthenable sky 1000 termination on detatst.at0 [0 0 1]iming attracts control 1 (6h must he disabled)slvsthenable sky 1000 termination on detatstot [0 1]enables full-mirror (AC) and high-leakage operation (enables SLH)sl.deanenable L0 core / reset core k gate (Lift 0stot [0 1]enables (direct-output logic (hot must he disabled))sl.deanenable L0 core / reset core k gate (Lift 0stot [0 1]enables direct-output logic (hot maing and s6h)sl.deanenable L0 core / reset core k gate (Lift 0stot [0 1]enables direct-output logic (hot maing and s6h)sl.deanenable L0 core / reset core k gate (Lift 0stot [0 1]enables direct-output logic (hot maing and s6h)sl.dekinvinvert BCCLs< | sm5-sm0, scmx | monitor multiplexing. | sfrst | enables fast reset at 6-b completion |
| publer DAC (after publer switch), threshold DAC, band- gap reference, temperature sensor)skstelenable sky 1000 (termination on cktra harmed bot to 63channel ontion: senx, sm5-sm0 [1 000000 to 11111], channels to to 63skstkenable sky 1000 (termination on cktrsfa [0 1], sfam [0 1]ART enable (sfa [1]) and mode (sfam [0] timing at thresh- old, [1] timing at peak)skstkenable sky 1000 (termination on cktrst1,st0 [0 00 10 11]peaktime [20, 010, 55, 25 ns)skstkenable sky 1000 (termination on cktrst1,st0 [0 01 10 11]peaktime [20, 010, 55, 25 ns)skstkenable sky 1000 (termination on cktrst1,st0 [0 01 01 11]peaktime [20, 010, 55, 25 ns)skstkenable sky 1000 (termination on cktrst1,st0 [0 1]enables full-mirror (AC) and high-leakage operation (enables SLH) stor [0 1]iming outputs control [66 huse the dishelor]stor [0 1]iming outputs control [66 huse the dishelor]sky 66 huse the dishelor]stor [0 1]enables diret-output logic (both timing and s6b)skip.306 humber of LD triggers to skip on overflowstor [0 1]enables diret-output logic (both timing and s6b)skip.306 humber of LD triggers to skip on overflowstor [0 1]enables high resolution ADC (107, SH ADC enable)skip.306 humber of LD triggers to skip on overflowstor [0 1]enables high resolution ADC (107, SH ADC enable)skip.316 humber of LD trigger st1 and date anablestor [0 1]termination ADC (107, SH ADC enable)skip.316 humber of LD trigger st1 and date anablestor [0 1]trigger st1 and date anablestor [0 1]tri | | • Common monitor: scmx, sm5-sm0 [0 000001 to 000100], | slvsbc | enable slvs 100Ω termination on ckbc |
| gap reference, temperature sensor) endured motior: sure, sensor) channel motior: sure, sensor) channel motior: sure, sensor)slottkenable slot 1000 termination on ckltsfa [0 1], sfam [0 1] odd, [1] timing at peak)ART enable (sfa [1]) and mode (sfam [0] timing at thresh- odd, [1] timing at peak)slottkenable slot 1000 termination on ckena slottkst1,at0 [00 01 10 1]peaktime (200, 100, 50, 25 ns.)enable slot 1000 termination on ckena slottkslottkenable slot 1000 termination on ckena slottksg2.sg1.sg0 (00:11)gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/C)slottkslottkenable slot 1000 termination on ckena slottkstot [0 1]enable slot-interve (Arrange neable timing outputs control 1 (6b) must be disabled) • stop stot [00.110, 11]: TP/ToT.PP.PP.T • TP: threshold-to-prask • Tor: time-over-threshold • PP: pisst-at-peak (100s) (not available with s10b) • PP.T; peak-to-turbeshold (not available with s10b) • PP.T; peak-to- | | | slvstp | enable slvs 100Ω termination on cktp |
| • e-damel monitors senx, sm5-sm0 [1 00000 to 111111], channels to to 63situation on claimination on claiminatin on claimination on claiminatin on claimination on | | | slvstk | enable slvs 100Ω termination on cktk |
| chamels 0 to 63slstartenable sits 100 01 comination on ckrtsfa [0 1], sfam [0 1]ART enable (sfa [1]) and mode (sfam [0] tring at thresh- odd, [1] tring at peak)sltsstälenable sits 100 01 termination on ckrdist1.at0 [00 01 10 1]peaktime (200, 100, 50, 25 ns)sltsstälenable sits 100 01 termination on ckrdisfn [0 1]enables full-mirror (AC) and high-leakage operation (enables SLH)slvsädenable sitxed sing 10 core / reset termination on ckrdisg2.sg1.sg0 [000:11]gain (0.5, 1, 3, 45, 6, 9, 12, 16 mV/fC)SL0enaVdisabled on core / reset termination on ckrdisito [0 1]iming outputs control 1 (Sb must be disabled)stopsato (0,0,1,0,11)Thy: Thy:Tor,Top:P.P.PTThy: threshold-to-peakTOT: time-over-thresholdSL0enaVConset termshold core / reset ore & gate clk if 010 offset.locl 1]enables direct-output logic (both timing and 66b)Size of trigger windowwindow - 0/2.2sttt [0 1]enables direct-output logic (both timing and 66b)sL0cktestenables clocks when L0 core disabled (test)stdt=skil [0 0 through 1:1]tat pulse PACsL0cktestenables clocks when L0 core disabled (test)stdt=skil [0 0 through 1:1]tat pulse PACsL0cktestenables clocks when D ored fissabled (test)stdt=skil 0 0 through 1:1]tat pulse PACsL0cktestenables aurmel at input node from nomina In/stdt=skil 0 0 through 1:1]tat pulse PACsL0cktestenables aurmel at input node from nomina In/skdtbs.dtdnal clock edge serialized AIRT enableskg.slb, skdnincreases bias curren | | | slvsdt | enable slvs 100Ω termination on ckdt |
| sfa [0 1], sfam [0 1]And randow (sam) [0 1 mining at makest1, st0 [0 0 11 0 11]peaktime (200, 100, 50, 25 ms)slobeenable sits 100 Ω termination on ckemst0 0 0 1 10 11]peaktime (200, 100, 50, 25 ms)slobeslobeenable sits 100 Ω termination on ckemsg2, sg1, sg0 [000:111]gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)slobeslobeslobemake sits 100 Ω termination on ckemsg2, sg1, sg0 [000:111]gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)slobeslobemember sits 100 Ωtermination on ckemsg2, sg1, sg0 [000:111]gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)slobeslobemember sits 100 Ωslobesg2, sg1, sg0 [000:111]gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)slobeslobemember sits 100 Ωsg1, sg1, sg1, sg1, sg1, sg1, sg1, sg1, | | | slvsart | enable slvs 100Ω termination on ckart |
| stl [0 1]old, [1] timing at peak)silvenastl st0 [0 01 10 11]peaktime (200, 100, 50, 25 n.s)silvenaenable ski 100 ?1 ermination on ckmastr [0 1]enables full-miror (AC) and high-leakage operation (enables SLH)silvenaenable ski 100 ?1 ermination on ckmasg2.sg1.sg0 [000.111]gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)silvenasilvenaenable ski 100 ?1 ermination on ckmasg2.sg1.sg0 [000.111]gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)silvenaenable ski 100 ?1 ermination on ckmasto [0 1]neighbor (channel and thip) triggering enablebioliset.0:11L0 BC offsetstot [0 1]timing outputs control 1 (e6b must be disabled)offset.10:11Channel tagging BC offsetrDP: tripsek-to-kki (los) (not available with s10b)PD: pube-sto-kki (los) (not available with s10b)size of trigger windowstot [0 1]enables sub-lystersis discriminationtract ai:05Max hits per L0stot [0 00 110 11]rAC stope adjustment (60, 100, 350, 650 ns)sl.0ckinwinvert DCKstdt skil (0 bo through 1:1]coarse threshold DACsl.0ckinwinvert DCKsktb skil DDreables fibr resolution DAC (10/skil ADC cnaversion timesl.0ckinwinvert DCKsktb skil ADC conversion timestil Ada anables 6-bit ADC conversion modestgcextreme charge handling compensationsklbshil Ada cok edge serialized ART enablestil and cok edge serialized ART enablestil anal cok edge serialized ART enablesklckibdual cok edge serialized ART enableslouslouslous | | | slvstki | enable slvs 100Ω termination on cktki |
| stl.std [00 01 10 11]peaktime (200, 100, 50, 25 ns)stnsfm [0 1]enables full-mirror (AC) and high-leakage operation (enables SLH)stg2ge1ge1000.111gain (0.5, 1.3, 4.5, 6, 9, 1.2, 16 mV/fC)sogneighbor (channel and chip) triggering enablestot [0 1]timing outputs control 1 (ebi must be disabled)stot [0 1]timing outputs control 1 (ebi must be disabled)stot [0 1]timing outputs control 1 (ebi must be disabled)stot [0 1]timing outputs control 1 (ebi must be disabled)stot [0 1]time-over-thresholdv TtP: threshold+to-peakwindow.i0:2ststfor 1: time-over-thresholdv TtP: puls-at-poak (10ns) (not available with s10b)sl.dekteststl.std: [0 1]enables direct-output logic (both timing and s6b)stl.std: [0 1]enables direct-output logic (both timing and s6b)stl.std: [0 0 1 10 11]TAC (slope adjustment (60, 100, 350, 650 ns)stl.std: [0 0 1 10 11]test pulse at-poak (60, 100, 350, 650 ns)stl.std: [0 0 1 both ADC conversion modestb8-bit ADC conversion modestb8-bit ADC conversion modestb8-bit ADC conversion modestbslob dial clock edge serialized Attr enabledual clock edge serialized data enablestbsdual clock edge serialized data enablestbdual cloc | sfa $[0 \ 1]$, sfam $[0 \ 1]$ | | slvsena | enable slvs 100Ω termination on ckena |
| sfm [0 1]cables full-mirror (AC) and high-leakage operation (enables SLH)sldenaVdisable mixed signal functions when L0 enabledsg2.sg1.sg0 [000:111]gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)reset Hard reset Hard reset Hard reset Hard reset when bdh highstot [0 1]timing outputs control 1 (sfb must be disabled)slDenaenable L0 core / reset core & gate clk if 0stot [0 1]timing outputs control 1 (sfb must be disabled)slDenaenable L0 core / reset core & gate clk if 0stot [0 1]timing outputs control 1 (sfb must be disabled)slDenaenable L0 core / reset core & gate clk if 0stot [0 1]timing outputs control 1 (sfb must be disabled)truncate: 0:5Max hits per L0stot [0 1]enables direct-output logic (bott timing and sfb)slDektestenable clocks when L0 core disabled (test)stot_stop [0 1]enables direct-output logic (bott timing and sfb)slDektestenable clocks when L0 core disabled (test)stot_stop [0 0:11 011]test puise DACslDektestenable clocks when L0 core disabled (test)stot_stop [0:01 trungh 1:1]test puise DACslDektestslDektestsed06b, scl10bs-bit ADC conversion imodeslbsbit ADC conversion imodesbbsbit ADC conversion imodeslpslpsdckadual clock edge serialized ABT enabledual clock edge serialized ABT enablesdckadual clock edge serialized 6-bit ADCslbsdckadual clock edge serialized 6-bit ADC conversion imodesdckadual clock edge serialized 6-bit ADCsdckadual clock | at1 at0 [00 01 10 11] | | slvs6b | enable slvs 100Ω termination on ck6b |
| sg2.sg1.sg0 [000:111]gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)sngneighbor (channel and chip) triggering enablestor [0 1]timing outputs control 1 (s6b musk be disabled)stor [0 1]exps.stor([0.01,10,11]: TPL7D,TPLP,PtTTPL: threshold-to-peakintra-exet (1.00 peak (1.0 | | | sL0enaV | disable mixed signal functions when L0 enabled |
| sngneighbor (channel and chip) triggering enableslubenaenable LD core / rest core & gate cik it 0stot [0 1]timing outputs control 1 (s6b must be disabled)slubenaenable LD core / rest core & gate cik it 0stot [0 1]timing outputs control 1 (s6b must be disabled)offset.i0:11LD core / rest core & gate cik it 0stot [0 1]timing outputs control 1 (s6b must be disabled)offset.i0:11Channel tagging BC offsetTtP: threshold-to-peakTT: time-over-threshold (not available with s10b)offset.i0:11Channel tagging BC offsetttt [0 1]enables direct-output logic (both timing and s6b)slubenawindow.i0:2Size of trigger windowsttl [0 1]enables direct-output logic (both timing and s6b)slubenaslubenawindow.i0:2Size of trigger windowsttl [0 0]enables direct-output logic (both timing and s6b)slubenaslubenawindow.i0:2Size of trigger windowstdps-dtp0 [0:0 through 1:1]coarse threshold (not available with s10b)slubenaincreases bias current at input node from nominal In/stdps-dtp0 [0:0 through 1:1]test pulse DACslub ADC conv. time (increase subtracts 60 ns)slub slub, slubsc06b, sc16b, sc26b6-bit ADC conversion imdeslabslub ADC conversion imdesdckadual clock edge serialized ALT enableddual clock edge serialized ALT enablesdckadual clock edge serialized ALT enabletristates analog outputs with token, used in analog modestlysenables lide recourtorl 2slvsenables direct output IOsstvs <td< td=""><td></td><td></td><td>reset reset</td><td>Hard reset when both high</td></td<> | | | reset reset | Hard reset when both high |
| singInegrifor (channel and Chip) Higgering enablestot [01]timing outputs control 1 (s6b musc be disabled) • stpp-stot[00,0.1,0,11]: ThP,ToT,PtP,PtT • TtP: threshold-to-peak • ToT: time-over-threshold • PtP: palse-at-peak (100s) (not available with s10b) • StdDstdui 0 101 11]Channel tagging BC offlower • Window.i0:2std10consection (60, 100, 350, 650 ns)SLOcktest • enables direct-output logic (both timing and s6b)SLOcktest • enable cocks when L0 core disabled (test) • SLOdkinv • invert DCKstd9-sdp0 [00 through 1:1]coarse threshold DACSLOdkinvinvert DCKsd09-sdp0 [00 through 1:1]test pulse DACsth, skhincreases bias current at input node from nominal 1n/ 15nA or 300nA respectivelysd06b, sc16b, sc26b6-bit ADC conversion timestgcextreme charge handling compensationsd026xdual clock edge serialized AT enableThere are two banks of 96 global registers Each channel has a configuration of 24 bitssdckbdual clock edge serialized AT enableEach channel has a configuration of 24 bitssdvsenables direct output IOsenables direct output IOssdvsenables direct output IOsenables direct output IOssdvsenables direct output IOs | | | sL0ena | enable L0 core / reset core & gate clk if 0 |
| stpp.stoi(00,01,0,11]: TtP,ToT,PtP,PtT TtP: threshold-to-peak ToT: time-over-threshold PtP: pubse-at-peak (10ns) (not available with s10b) PtT: peak-to-threshold (not available with s | _ | · · · · · · · · · · · · · · · · · · · | l0offset_i0:11 | |
| • stpp,stol(00,01,01,01,01,01,01,01,01,01,01,01,01,0 | stot $\begin{bmatrix} 0 & 1 \end{bmatrix}$ | | offset_i0:11 | Channel tagging BC offset |
| It: It::sinde-to-peak • To: time-cover-threshold • PtP: pulse-at-peak (10ns) (not available with s10b) • Stole-state-state state s | | | rollover_i0:11 | 00 0 |
| Image: 1 bit infectore-oneshindinterver-oneshind• PtF: pulse-at-peak (10ns) (not available with s10b)• sttl [0 1]enables sub-tysteresis discriminationstcl, stc0 [00 01 10 11]TAC slope adjustment (60, 100, 350, 650 ns)stcl, stc0 [00 01 10 11]TAC slope adjustment (60, 100, 350, 650 ns)stdp-sdt0 [0:0 through 1:1]coarse threshold DACsdp9-sdp0 [0:0 through 1:1]coarse threshold DACsc00b, sc10b, sc10b10-bit ADC conv. time (increase subtracts 60 ns)sc00b, sc10b, sc26b6-bit ADC conversion timesb8-bit ADC conversion timesb8-bit ADC conversion timesdbenables 6-bit ADC (requires sttt enabled)s10benables 6-bit ADC (requires sttt enabled)sdckadual clock edge serialized data enablesdckadual clock edge serialized ART enablesdckbdual clock edge serialized ART enableskvenables direct output IOsskvenables direct output IOsstrenables direct output IOsstrenables auto-reset (at the end of the ramp, if no stop occurs)occurs)enables auto-reset (at the end of the ramp, if no stop occurs) | | _ | window_i0:2 | |
| Image: PtT: pask-ar-peak (1008) (not available with s10b)nskip_i0:6Number of L0 triggers to skip on overflowSttl [0 1]enables direct-output logic (both timing and s6b)sL0cktestenable clocks when L0 core disabled (test)stb [0 1]enables sub-hysteresis discriminationinvert BCCLKstc1,stc0 [00 01 10 11]TAC slope adjustment (60, 100, 350, 650 ns)sL0ckinvinvert BCCLKsdt9-sdt0 [0:0 through 1:1]test pubs DACnskip_i0:6Number of BCID - 0xFE8sc010b,sc10b10-bit ADC conv. time (increase subtracts 60 ns)sbit ADC conv. time (increase subtracts 60 ns)stgcextreme charge handling compensationsc06b, sc16b, sc26b6-bit ADC conversion modestgcextreme charge handling compensationsc06b, sc16benables high resolution ADCs (10/8-bit ADC enable)stgcextreme charge handling compensationsc06benables high resolution ADCs (10/8-bit ADC enable)stgcextreme charge handling compensationsc06benables high resolution ADCs (10/8-bit ADC enable)stgcextreme charge handling compensationsc06benables high resolution ADCs (10/8-bit ADC enable)stgcextreme charge handling compensationsc06benables direct output lOstristates analog outputs with token, used in analog modetristates analog outputs with token, used in analog modestpp [0 1]timing outputs control 2storenables direct output lOsstcrenables direct output lOsenables direct output lOsstcrenables direct output lOsenables direct output lOsstcrenab | | | truncate_i0:5 | |
| sttt [0 1]enables direct-output logic (both timing and s6b)sl.Ocktestenable clocks when L0 core disabled (test)skl [0 1]enables sub-hysteresis discriminationsl.Ocktestenable clocks when L0 core disabled (test)stcl,stc0 [00 01 10 11]TAC slope adjustment (60, 100, 350, 650 ns)sl.Ocktestsl.Ocktestsl.Ocktestsdt9-sdt0 [0:0 through 1:1]test pulse DACnskipm.imagic number on BCID - 0xFE8sc00b,sc10b10-bit ADC conv. time (increase subtracts 60 ns)slh, slxhlincrease bias current at input node from nominal 1n/sc00b, sc16b, sc26b6-bit ADC conversion timestgcextreme charge handling compensationsb8-bit ADC conversion modestgcstgcsc0bb, sc16b, sc26b6-bit ADC (requires stt enabled)stgcstgcsdcksdual clock edge serialized data enablestdcksdual clock edge serialized ART enablesdckadual clock edge serialized ART enablestor tristates analog outputs with token, used in analog modestpp [0 1]timing outputs control 2storstcrenables direct output IOSenables direct output IOSstcrenables direct output IOSstcrenables auto-reset (at the end of the ramp, if no stop occurs) | | | nskip_i0:6 | - |
| ssh [0 1]enables sub-hysteresis discriminationsLOckinvinvert BCCLKstcl,stcl (00 01 10 11]TAC slope adjustment (60, 100, 350, 650 ns.)sLOckinvinvert DCKsdt9-sdt0 [0:0 through 1:1]coarse threshold DACinvert BCCLKsdp9-sdp0 [0:0 through 1:1]test pulse DACnaskipm.imagic number on BCID - 0xFE8sc00b,sc110b10-bit ADC conv. time (increase subtracts 60 ns)sh, slxhincreases bias current at input node from nominal 1n/sc00b, sc16b, sc26b6-bit ADC conversion timestgeextreme charge handling compensationsb8-bit ADC conversion modestgeextreme charge handling compensationsl0benables 6-bit ADC (requires sttt enabled)tristates analog outputs with token, used in analog modesdckadual clock edge serialized ART enablesdrvtristates analog outputs with token, used in analog modestpp [0 1]timing outputs control 2slvsenables direct output IOsstcrenables auto-reset (at the end of the ramp, if no stop occurs) | sttt [0,1] | | sL0cktest | enable clocks when L0 core disabled (test) |
| stc1,stc0 [00 01 10 11]TAC slope adjustment (60, 100, 350, 650 ns)invert DCKsdt9-sdt0 [0:0 through 1:1]coarse threshold DACnskipm.imagic number on BCID - 0xFE8sdp9-sdp0 [0:0 through 1:1]test pulse DACincreases bias current at input node from nominal 1n/sc010b,sc110b10-bit ADC conv. time (increase subtracts 60 ns)slh, slxhincreases bias current at input node from nominal 1n/sc08b,sc18b8-bit ADC conv. time (increase subtracts 60 ns)stgcextreme charge handling compensationsc06b, sc16b, sc26b6-bit ADC conversion timestgcextreme charge handling compensationsb8-bit ADC conversion modestgcextreme charge handling compensationsc06b, sc16b, sc26b6-bit ADC (requires stt enabled)stgcextreme charge handling compensationsc06b, sc16b, sc26bdual clock edge serialized data enablestgcEach channel has a configuration of 24 bitssdckadual clock edge serialized 6-bit enablesdck6bdual clock edge serialized 6-bit enablesdck6bdual clock edge serialized 6-bit enablesdck6bdual clock edge serialized 6-bit enablesdrvtristates analog outputs with token, used in analog modestpp [0 1]stcrenables direct output IOsstcrenables direct output IOsstcrenables auto-reset (at the end of the ramp, if no stop occurs) | | | sL0ckinv | invert BCCLK |
| sdt9-sdt0 [0:0 through 1:1] coarse threshold DAC magic number on BCID - 0sFE8 sdp9-sdp0 [0:0 through 1:1] test pulse DAC slh, slxh increases bias current at input node from nominal 1nA sc00b,sc10b 10-bit ADC conv. time (increase subtracts 60 ns) slh, slxh increases bias current at input node from nominal 1nA sc08b,sc18b 8-bit ADC conv. time (increase subtracts 60 ns) stgc extreme charge handling compensation sc08b,sc18b 8-bit ADC conversion time stgc extreme charge handling compensation s6b enables 6-bit ADC (requires sttt enabled) makic number on 96 global registers sdcks dual clock edge serialized ART enable makic number on 96 global registers sdrv tristates analog outputs with token, used in analog mode tristates analog outputs with token, used in analog mode stcr enables direct output IOs enables direct output IOs enables direct output IOs stcr enables direct output IOs enables direct output IOs enables direct output IOs stcr enables direct output IOs enables direct output IOs enables direct output IOs | | · | sL0dckinv | invert DCK |
| sdp9-sdp0 [0:0 through 1:1] test pulse DAC increases bias current at input node from nominal 1nA sc010b,sc110b 10-bit ADC conv. time (increase subtracts 60 ns) stp stp sc08b,sc18b 8-bit ADC conv. time (increase subtracts 60 ns) stg extreme charge handling compensation sc08b,sc18b 8-bit ADC conversion time stg extreme charge handling compensation sc08b,sc18b 8-bit ADC conversion mode extreme charge handling compensation sc08b enables 6-bit ADC (requires sttt enabled) extreme charge handling compensation sl0b enables high resolution ADCs (10/8-bit ADC enable) there are two banks of 96 global registers sdcks dual clock edge serialized ART enable Each channel has a configuration of 24 bits sdck6b dual clock edge serialized 6-bit enable enables direct output IOs slvs enables direct output IOs enables direct output IOs stcr enables direct output IOs enables auto-reset (at the end of the ramp, if no stop occurs) | | | nskipm_i | magic number on BCID - 0xFE8 |
| sups-supsinitial backinitial backinitial backsc010b,sc110b10-bit ADC conv. time (increase subtracts 60 ns)isin, stm15nA or 300nA respectivelysc08b,sc18b8-bit ADC conv. time (increase subtracts 60 ns)stgcextreme charge handling compensationsc06b, sc16b, sc26b6-bit ADC conversion timestgcisin, stm15nA or 300nA respectivelysc06b, sc16b, sc26b6-bit ADC conversion modestgcisin, stm15nA or 300nA respectivelysc06b, sc16b, sc26b6-bit ADC conversion modeisin, stmisin, stm15nA or 300nA respectivelysc06benables 6-bit ADC (requires sttt enabled)isin, stm15nA or 300nA respectivelysc06benables 6-bit ADC (requires sttt enabled)isin, stmisin, stm15nA or 300nA respectivelysc06benables high resolution ADCs (10/8-bit ADC enable)isin, stmisin, stmisin, stmsdckadual clock edge serialized data enableisin, stmisin, stmIsin, stmsdckadual clock edge serialized ART enableisin, stmisin, stmisin, stmsdrewtristates analog outputs with token, used in analog modeisin, stmisin, stmisin, stmstrenables direct output IOsisin, stmisin, stmisin, stmisin, stmstcrenables auto-reset (at the end of the ramp, if no stop occurs)isin, stmisin, stmisin, stm | , | | | |
| score No-bit ADC conv. time (increase subtracts 60 ns) score 8-bit ADC conv. time (increase subtracts 60 ns) score 6-bit ADC conversion time score 6-bit ADC conversion mode score enables 6-bit ADC (requires sttt enabled) score enables high resolution ADCs (10/8-bit ADC enable) sdcks dual clock edge serialized data enable sdcka dual clock edge serialized data enable sdckb dual clock edge serialized 6-bit enable sdrw tristates analog outputs with token, used in analog mode strp [0 1] timing outputs control 2 slvs enables direct output IOs stcr enables auto-reset (at the end of the ramp, if no stop occurs) | | - | sin, sixh | - |
| sc06b, sc16b, sc26b6-bit ADC conversion times8b8-bit ADC conversion modes6benables 6-bit ADC (requires sttt enabled)s10benables high resolution ADCs (10/8-bit ADC enable)sdcksdual clock edge serialized data enablesdckadual clock edge serialized ART enablesdckbdual clock edge serialized 6-bit enablesdckbdual clock edge serialized 6-bit enablesdrvtristates analog outputs with token, used in analog modestpp [0 1]timing outputs control 2slvsenables direct output IOsstcrenables auto-reset (at the end of the ramp, if no stop occurs) | , | | stgc | |
| s8b8-bit ADC conversion modes6benables 6-bit ADC (requires sttt enabled)s10benables high resolution ADCs (10/8-bit ADC enable)sdcksdual clock edge serialized data enablesdckadual clock edge serialized ART enablesdck6bdual clock edge serialized 6-bit enablesdck6bdual clock edge serialized 6-bit enablesdrvtristates analog outputs with token, used in analog modestpp [0 1]timing outputs control 2slvsenables direct output IOsstcrenables auto-reset (at the end of the ramp, if no stop occurs) | , | | | |
| s6benables 6-bit ADC (requires sttt enabled)s10benables high resolution ADCs (10/8-bit ADC enable)sdcksdual clock edge serialized data enablesdckadual clock edge serialized ART enablesdck6bdual clock edge serialized 6-bit enablesdrvtristates analog outputs with token, used in analog modestpp [0 1]timing outputs control 2slvsenables direct output IOsstcrenables auto-reset (at the end of the ramp, if no stop occurs) | , , | | | |
| s10benables high resolution ADCs (10/8-bit ADC enable)sdcksdual clock edge serialized data enablesdckadual clock edge serialized ART enablesdck6bdual clock edge serialized 6-bit enablesdrvtristates analog outputs with token, used in analog modestpp [0 1]timing outputs control 2slvsenables direct output IOsstcrenables auto-reset (at the end of the ramp, if no stop occurs) | | | | |
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| sdckadual clock edge serialized ART enablesdck6bdual clock edge serialized 6-bit enablesdrvtristates analog outputs with token, used in analog modestpp [0 1]timing outputs control 2slvsenables direct output IOsstcrenables auto-reset (at the end of the ramp, if no stop occurs) | | | | • • |
| sdckadual clock edge serialized AKT enablesdckabdual clock edge serialized 6-bit enablesdrvtristates analog outputs with token, used in analog modestpp [0 1]timing outputs control 2slvsenables direct output IOsstcrenables auto-reset (at the end of the ramp, if no stop occurs) | | <u> </u> | Each channel | has a configuration of 24 bits |
| sdrvtristates analog outputs with token, used in analog modestpp [0 1]timing outputs control 2slvsenables direct output IOsstcrenables auto-reset (at the end of the ramp, if no stop occurs) | | <u> </u> | | |
| stpp [0 1] timing outputs control 2 slvs enables direct output IOs stcr enables auto-reset (at the end of the ramp, if no stop occurs) | | 0 | | |
| slvs enables direct output IOs stcr enables auto-reset (at the end of the ramp, if no stop occurs) | | | | |
| stcr enables auto-reset (at the end of the ramp, if no stop occurs) | | | | |
| ster occurs) | slvs | enables direct output IOs | | |
| | stcr | | | |
| soar chables After hag synchronization (tran to next tran) | ssart | enables ART flag synchronization (trail to next trail) | | 1 |

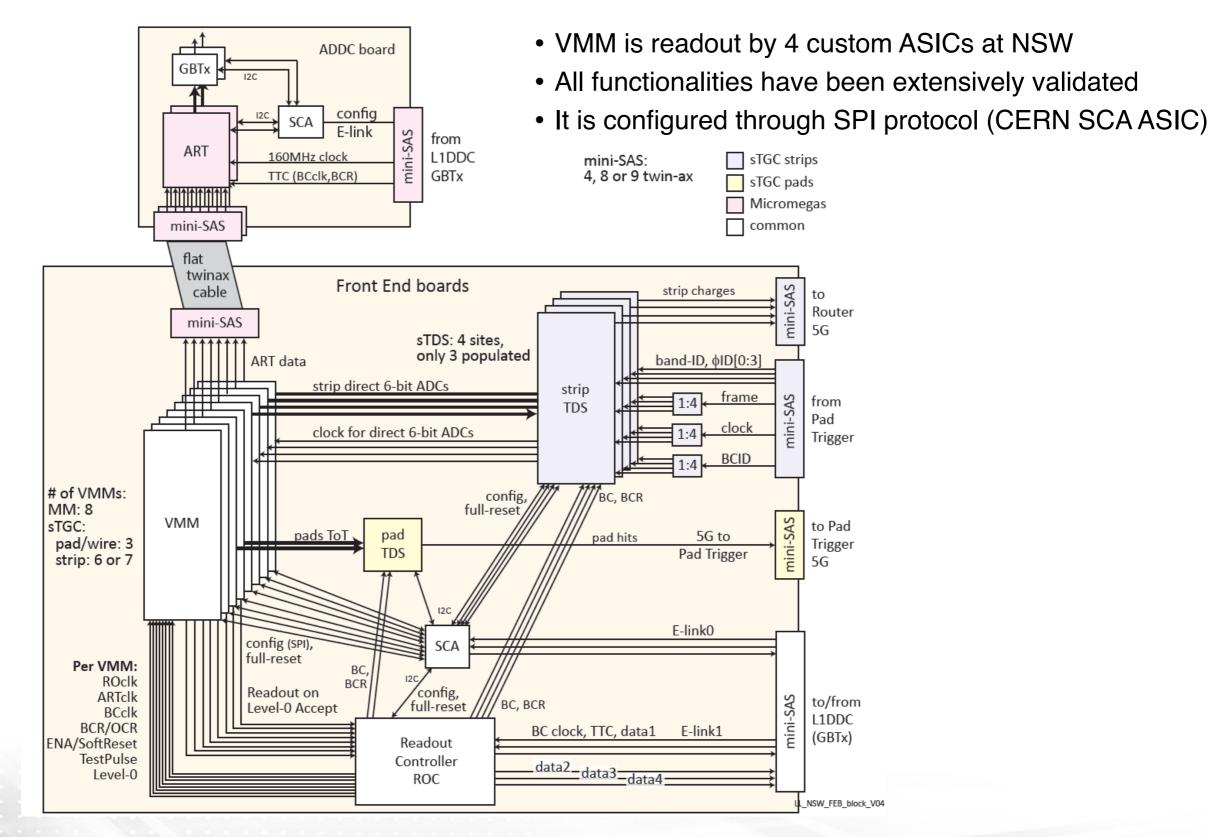


VMM Connectivity on the BGA (NSW)

| Name, Position | Con- nection | In, Out or I/O | Type of Signal or Max/Min | Description | |
|--------------------------------|-----------------|-------------------------|---------------------------------|--|--|
| sett A19-20 | VMM | I/O | Custom LVDS Bi-directional | Channel 0 force-neighbor signal | |
| setb Y19-20 | VMM | I/O | Custom LVDS Bi-directional | Channel 63 force-neighbor signal | <pre> Inter chip communication </pre> |
| ckbc (BCclk) C15-16 | ROC | In | SLVS | Bunch crossing clock of 40 MHz / External trigger signal | Can use different frequencies |
| cktp (Test Pulse) B15-16 | ROC | In | SLVS | Test pulse clock | should be longer that the peaking |
| cktk (Level-0) D13-14 | ROC | In | SLVS | Token clock / L0 (digital NSW mode) | Trigger on L0, data finder on Continuous |
| ckdt (ROclk) E15-16 | ROC | In | SLVS | Data clock | |
| ckart (ARTclk) D19-20 | ROC | In | SLVS | ART clock | |
| sdi B17 | SCA | In | CMOS | Configuration data input | |
| sdo B18 | | Out | CMOS | Configuration data output (not used, HiZ state in NSW) | |
| cs B19 | SCA | In | CMOS | Chip Select, active low | Configuration |
| sck B20 | SCA | In | CMOS | Input SPI clock | |
| t0-t63 E17-W20 | TDS | Out | SLVS | Direct digital outputs | 64 outputs - one per channel |
| mo C9 | SCA | Out | 0-1 V | Analog output for calibration | Analog output - Can see the actual waveform |
| tki (BCR/OCR) C13-14 | ROC | In | SLVS | Token input (an. mode) / (BCR- OCR) / acceptance window in non-L0 cont. mode | but also threshold DAC, pulser DAC, temperature, BGR |
| tko B13-14 | | Out | SLVS | Token output (analog mode, not used in NSW) | |
| ena (ENA/Soft Reset) C17-18 | ROC | In | SLVS | Acquisition start/stop | |
| ck6b C19-20 | TDS | In | SLVS | 6-bit ADC Clock | |
| art E13-14 | ART2GBT | Out | SLVS | Address in Real Time | |
| data0 D15-16 | ROC | Out | SLVS | data line | } ← Data |
| data1 D17-18 | ROC | Out | SLVS | data line first bit, flag in cont. | |
| U.S. DEPARTMENT | UF | | | | BROOKHAVEN |



VMM3a connectivity at NSW application





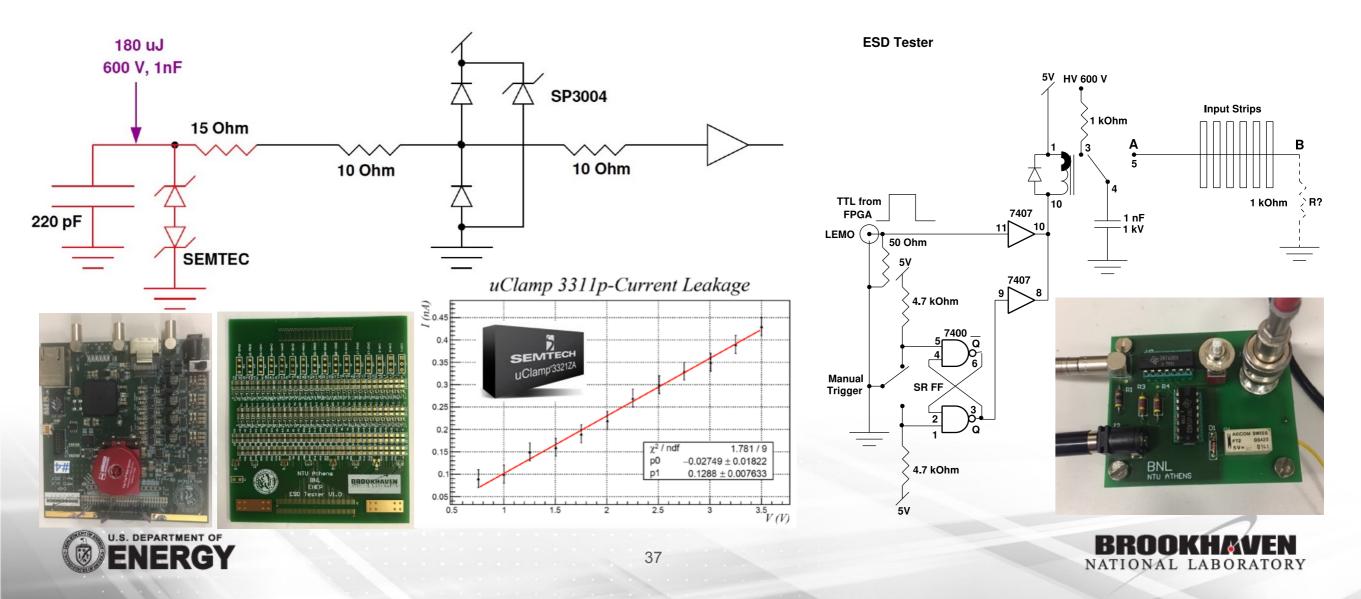
| Ê File I Vertical ↔ Timebase I Trigger 	 Display | Cursors 🗈 Measure 🖬 Math 🗠 A | nalysis 🗙 Utilities 🚯 Support | DO |
|--|------------------------------|-------------------------------|---|
| | | | |
| | | | |
| | | | DDDDDDDDDDDDDDDDDDDDDDDDDDD 55 |
| ENA OS | | Data | D6" |
| SDI | Pulse | 500ns after | |
| | | | |
| | | | |
| TKO | | | D14 |
| 6B | | | D15 |
| C1 DC1M Digital1 10 100 mV/div -407.50 mV 6.25 kS TELEDYNE LECROY | | | Timebase -1.30 µs Trigger D5 500 ns/div Auto 1.50 \vee 12.5 kS 2.5 GS/s Edge Positive 1/2/2009 7:41:59 PM 1/2/2009 7:41:59 PM 1/2/2009 7:41:59 PM |





Input protection schema

- Since the VMM2, we have experience major channel (initial NUP4114 issue). Moving to **130nm technology** made the requirements on **input protection higher**. Current protection scheme based on the SP3004 seems inadequate to protect the VMM front ends
- A dedicated ESD testing procedure was lunched allowing a systematic test of the VMM input.
- A VMM board (MMFE1) with Panasonic connector and a VMM socket was developed to perform systematic tests. On top a Panasonic based connector daughter-board was built to test different protection schemes and different footprints.
- 220 pF capacitor emulates typical MM strip capacitance, a channel like this survived repeated discharges while without protection is dead after a single discharge. Then **survived zapping overnight (>30,000 discharges)**



Temperature monitoring

The IBM CMOS8RF Design Manual specifies the operating temperature range to be from $-55 \,^{\circ}$ C to $125 \,^{\circ}$ C. However device life time degrades rapidly at high temperatures. The case temperature should be kept below $50 \,^{\circ}$ C and preferably in the range 30–40 and should be verified and compared to the junction temperature provided by the VMM ASIC. The VMM includes a temperature sensor which can be read out by appropriately programming the monitor output and digitized by the SCA setting (in configuration mode) scmx = 0, sm5–sm0 = 000100 (see Table 6). The die temperature is approximately given by:

$$^{\circ}\mathrm{C} = \frac{725 - V_{\mathrm{sensor}}}{1.85}$$

where V_{sensor} is the temperature sensor reading in mV. The case temperature of a single-chip

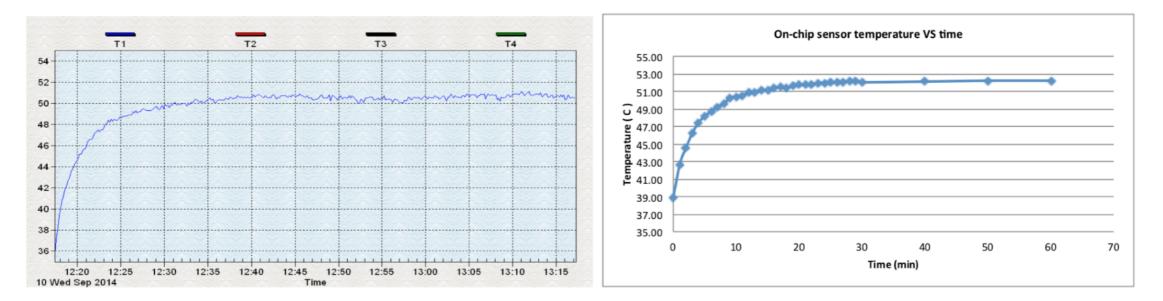


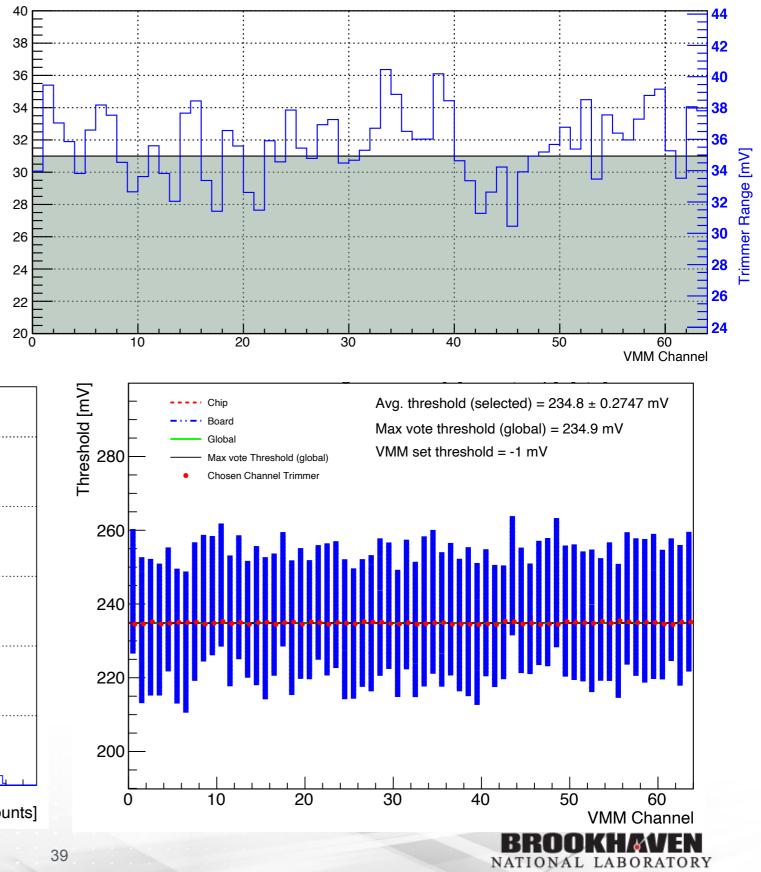
Figure 8: Left plot, the VMM case temperature. Right plot, the junction temperature as a function of time after turn-ON

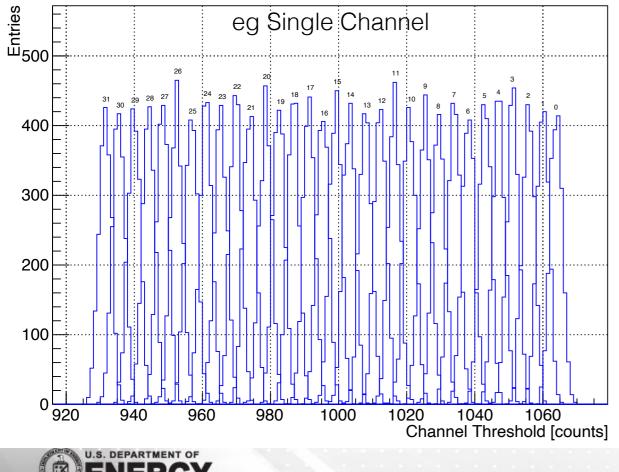


Calibration - channel trimming

Trimmer Range [steps]

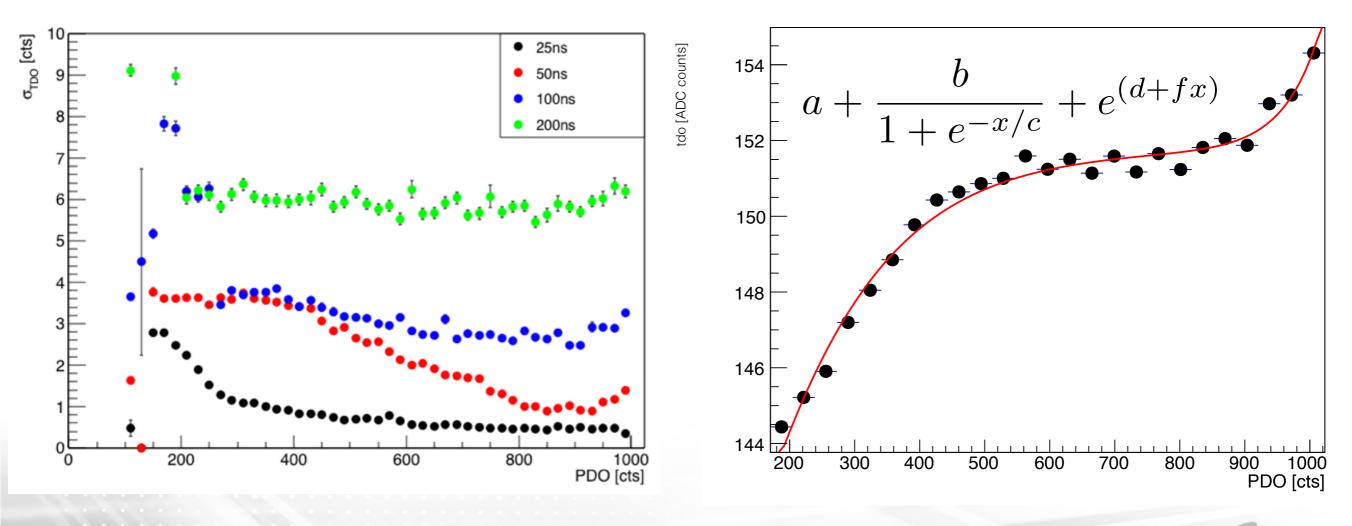
- Full scan performed on the channel
 trimmers across full threshold range
- Found that the **full range** of 31 counts shows normal behaviour
- Minimum range of 30mV across all channels, good uniformity.
- Equalisation can be performed easily





Calibration - channel time walk and resolution

- Calibration of the following:
 - **Timing resolution along amplitude**: This is taking into account on the fitting of the event as an error. Other errors like the longitudinal diffusion is negligible with respect this.
 - **Time walk**: There is a dependance of the time finding (peak or threshold) from the signal amplitude. This is a correction applied on the timing reconstruction. Fitting the full distribution will improve more the results. To be done.

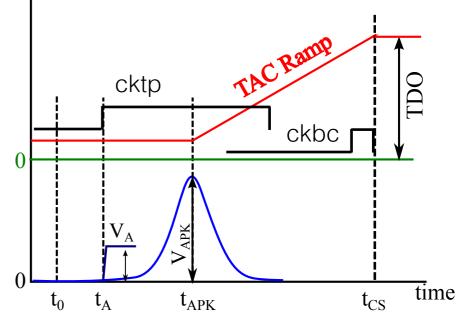






Calibration - TAC

- Calibration of the TAC for different ramps was automatically performed. Skewing clocks method (NSW mode, VMM3/3a) and latency method (Not NSW VMM3) were used to extract the ramping rate and pedestal.
- Uniformity is good, the extracted constants were used in analysis to convert from ADC counts to ns







of channel



Calibration - Charge

- VMM features as well an internal pulser which can cover the full range on all the gain settings
- Varying the input and measuring the PDO, a charge/gain calibration can be done for each channel Slope: 0.7748 ± 4.069e-06 mV/cts xADC Samples [mV] 800

700

600

500

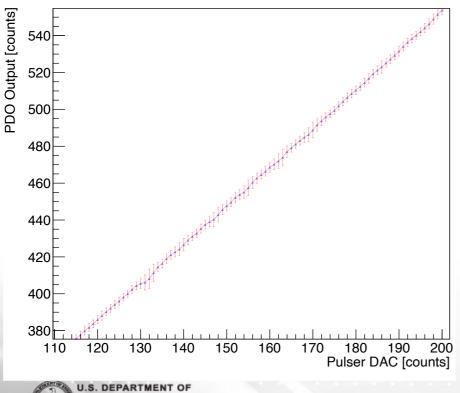
400

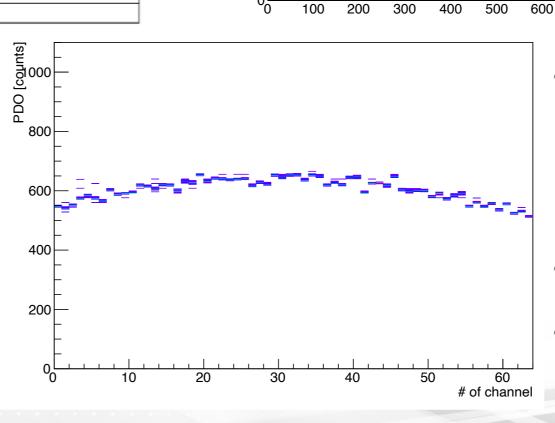
300

200

100

| | Channel bits (defaults are 0) | Description |
|--|-------------------------------|--|
| | sc [0 1] | large sensor capacitance mode ([0] $<\!\!\sim\!\!200\mathrm{pF}$, [1] $>\!\!\sim\!\!200\mathrm{pF}$) |
| | sl [0 1] | leakage current disable [0=enabled] |
| | st [0 1] | 300 fF test capacitor [1=enabled] |
| | sth [0 1] | multiplies test capacitor by 10 |
| | sm [0 1] | mask enable [1=enabled] |
| | sd0-sd4 [0:0 through 1:1] | trim threshold DAC, $1mV$ step ([0:0] trim $0V$, [1:1] trim -29 mV) |
| smx [0 1] | | channel monitor mode ([0] analog output, [1] trimmed threshold)) |
| sz010b, sz110b, sz210b, sz310b, sz410b | | 10-bit ADC zero |
| sz08b, sz18b, sz28b, sz38b | | 8-bit ADC zero |
| | sz06b, sz16b, sz26b | 6-bit ADC zero |





Constant : 32.82 ± 0.001417 mV

In the effort of • improving the ADCs a gain difference was introduced to the channels,

900

DAC [counts]

1000

700

800

Not big effect for ulletadjacent channels

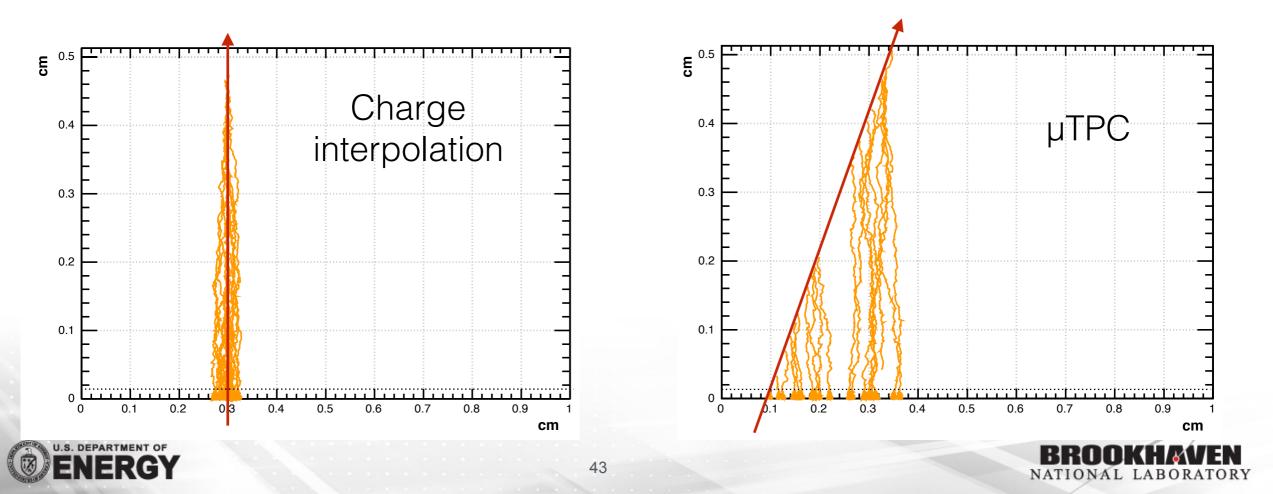
NATIONAL LABORATORY

• Small loss of dynamic range



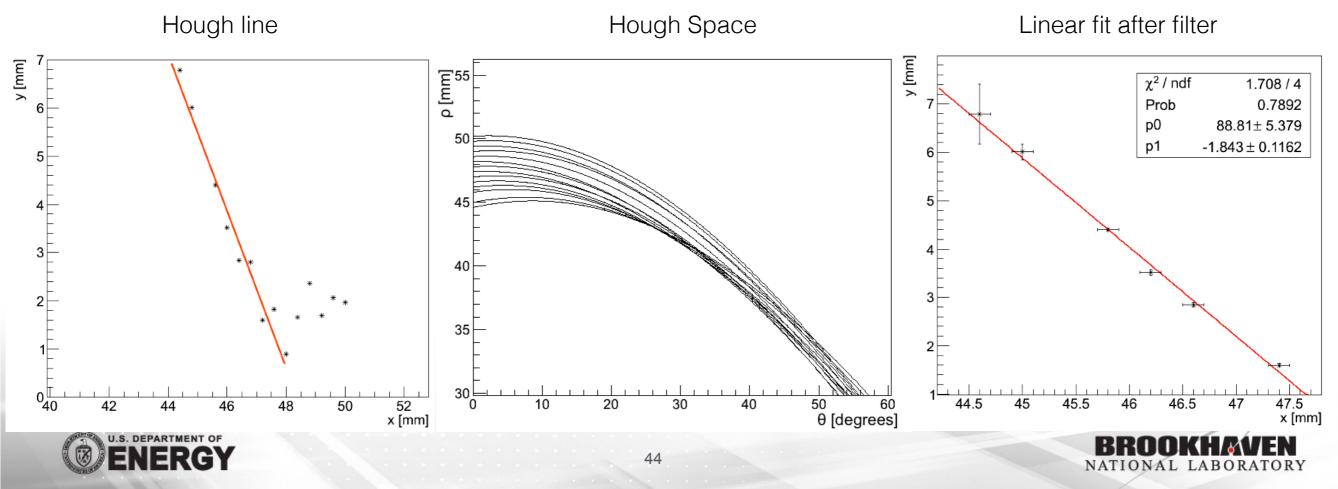
μTPC - The concept

- In the NSW the **track range** is 5°-28° for the tracks originated from the IP
- It is mandatory to be able to **reconstruct the position** of a particle that transversed the detector under an angle **with high resolution**
- The charge centroid method is proven not to be able to provide good resolution for tracks over 5°.
- Instead a **new method** was implemented in the Micromegas called the μTPC
- This method implies on measuring with high accuracy (<3ns) the arrival time of the primary ionisation above a strip.



μTPC - **Clustering** under an angle

- Clustering strips for inclined tracks is a challenging task due to:
 - Ionisation statistics, there are fluctuations on primary cluster generation that can give "holes" in between a cluster of strips depending on the incident track angle
 - Generation of delta electrons
 - Multiple track events
 - Noise in the system
- For this reason, a pattern recognition technique including the Hough Transform is used as a filter efficiently removing noise, delta electrons, separating double track events



VMM Embedded Readout Software (VERSO)

- For the test-beams, a **DAQ + control software** was **developed** allowing operations like configuration and calibration. Highly configurable, multi-threaded and reliable (VMM electronics)
- The applications is developed in Qt and C++ based on a UDP handshake protocol

| | | X VERSO - v4.2.1 |
|-----------------------------------|--|--|
| Run Control | Run Status Start Run Run # 0 ◆ ✓ Write Ntupli Write Raw VMM2 VMM3 L0 R/O DataFlow | Setup /Software/vmm_readout_software/readout_configuration/DAQ_config_2MM.xml Ø UCIrvine University of California, Irvine Ø Irvine Irvine Invine Ø Invine Invine |
| Operation parameters (FPGA) | Counters0Triggers0Hits0Event Stop-1No ConfigCommunicationpen CommunicaticAll Boards AliveIPv. 1921802# FEB SelectAll \bullet OnfigureFEB SelectVMM12345678SelectDead Time65535 ϕ CKTC ART T/OFixed WindowSetCKTK & CKBCCKTK & CKBC Freq. (M2 ϕ 0 ϕ DefaultsCKTPNumber of Pulses to S-1Skew (steps)Period00 ϕ × 1ns30000 ϕ × 200nsWidth4 ϕ > 50PefaultsSetMonitor Sampling50 ϕ FPGA ResetVMM3 Hard Reset | Messages Global Registers 1 Global Registers 2 Channel Registers Calibration Set IP Message Reportin |
| Data flow monitor | Rates Occupancy Delta 10 | VERSO DataFlow VERSO DataFlow 00.00.01 00.00.02 00.00.03 00.00.04 Record trigger rate Record trigger r |
| S. DEPARTMENT OF | | 45 XA |