

# Electronics Status at USTC

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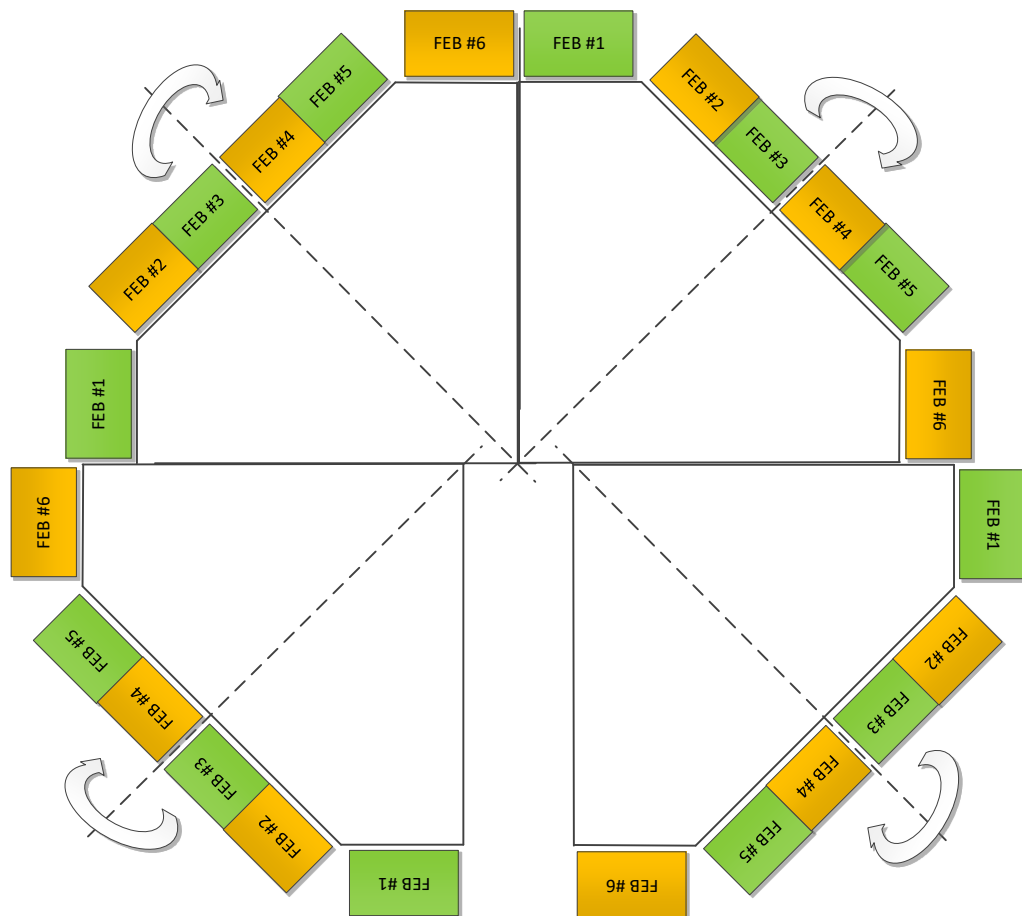
University of Science and Technology of China

# Outline

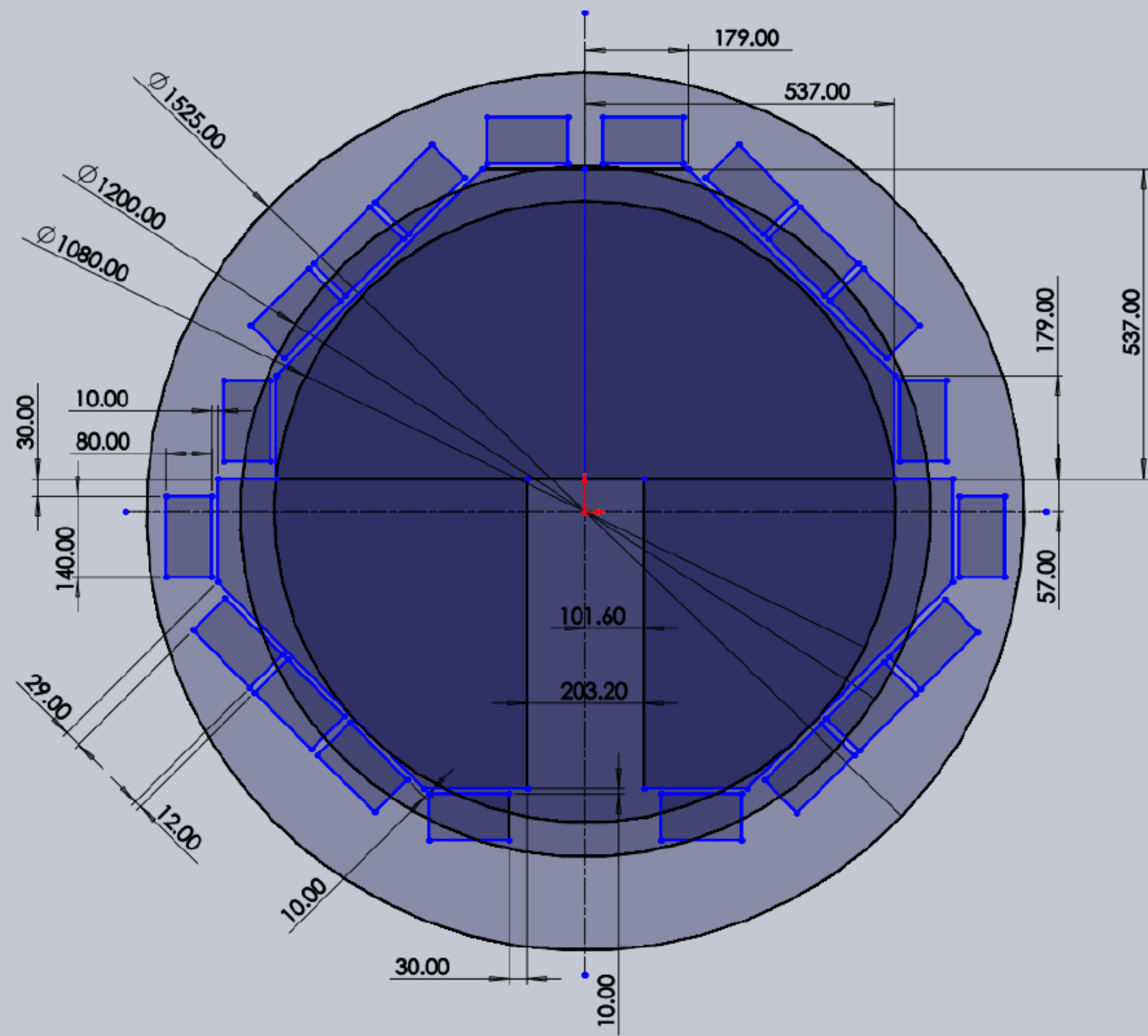
- System Architecture
- FEB Status
- VMM3 Usage on FEB
- ROD Status
- Adapter Board design

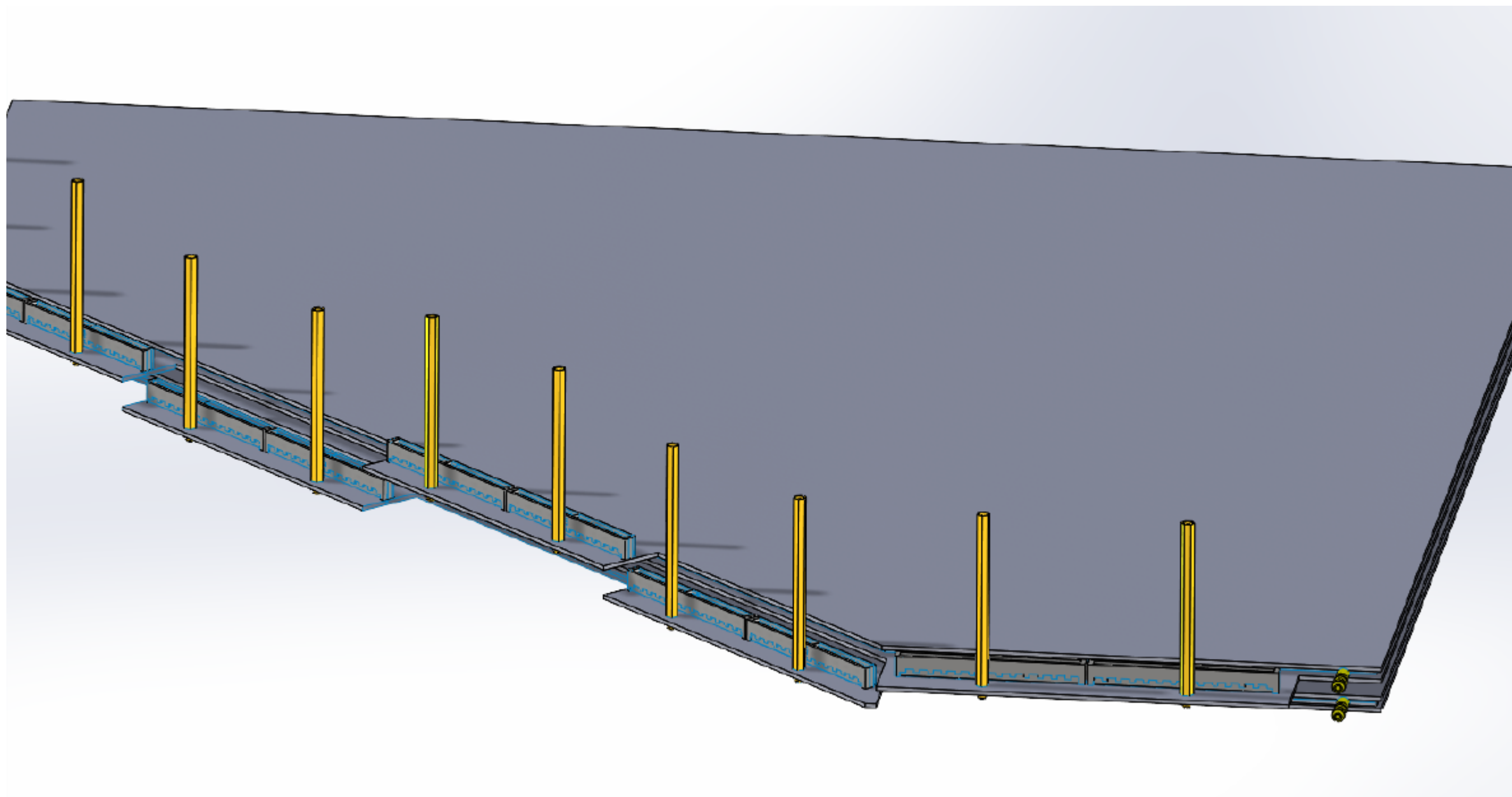
# System Architecture

# Complete sTGC layer

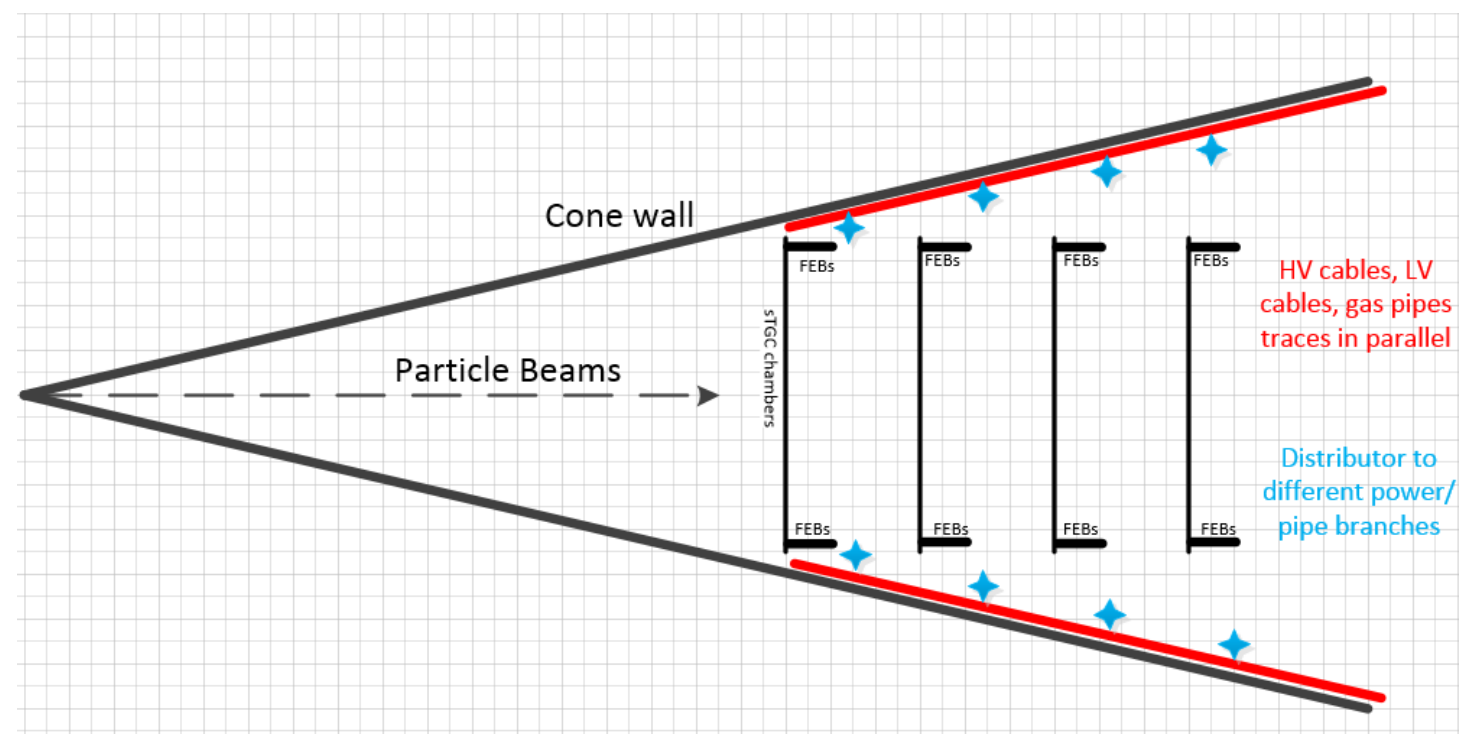


- The strips of each sTGC layer can be handled by 24 Front-End Boards.
- In total, there will need 96 FEBs for 4 sTGC layers.
- The **innermost** sTGC layer locate in the cone at the place with diameter of **152cm**
- About 10cm gap between the sTGC border and the cone
- FEB boards are vertically inserted in the sTGC chamber.





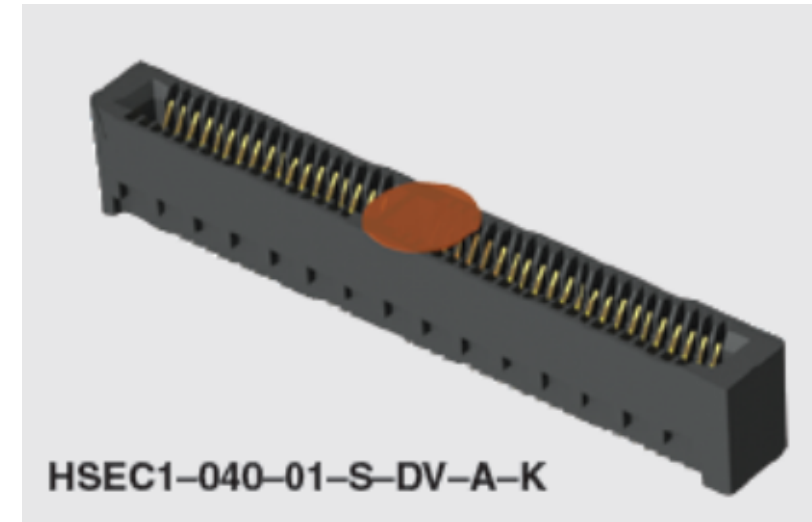
# Layout in the cone



- **7-inch** distance between adjacent sTGC chambers.
- FEBs are vertically inserted into the connector slots on chamber.
- FEBs are almost parallel to the particle beams.
- 3-6 power cables can be grouped together and then distributed to each FEB near the chamber.

# Connector between chamber and FEB

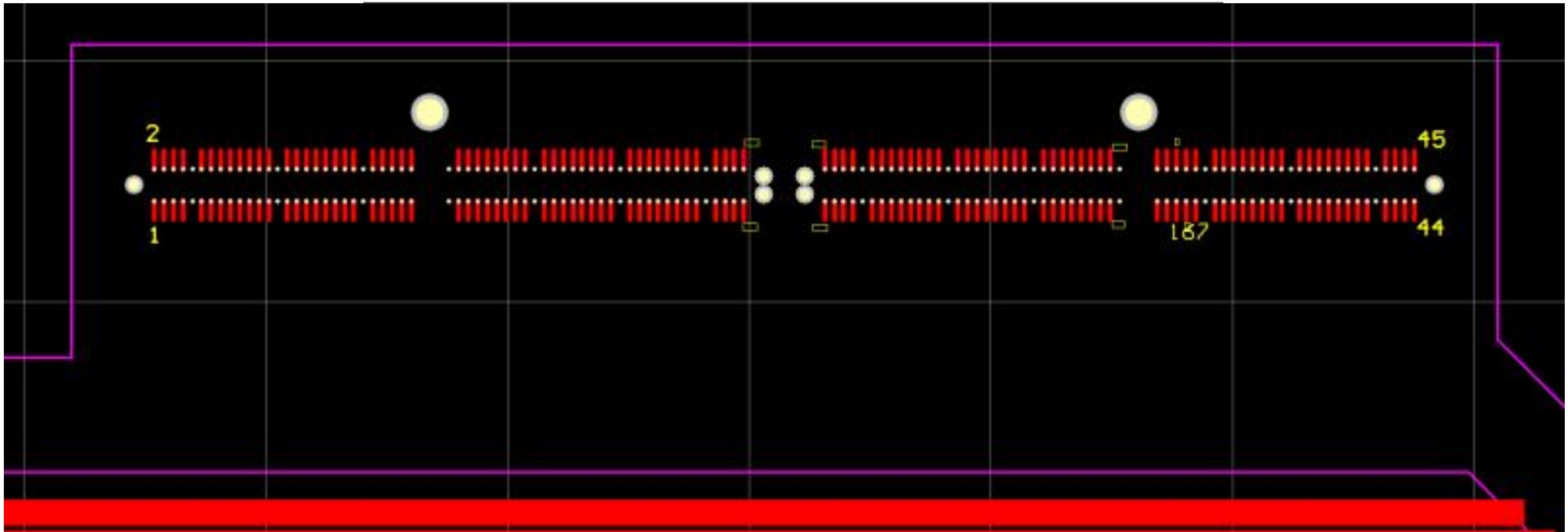
- Connector P/N on chamber: SAMTEC HSEC1-060-01-S-DV-A-K, used as board **slot connector**
- Connector size on chamber: 69.5 \* 5.6 \* 7.8mm (L\*W\*H)
- 1.0mm pitch, dual rows, 60 positions/row
- 120 strip signals can be connected to the connector
- Surface-mounted, can be soldered manually.
- No connectors needed on FEB: **Golden fingers on both layers of FEB**
- Each FEB contains two connectors, capable of up 240 strip channels (sTGC chamber can supply ~210 strips for each FEB).





# Connector Pin Map

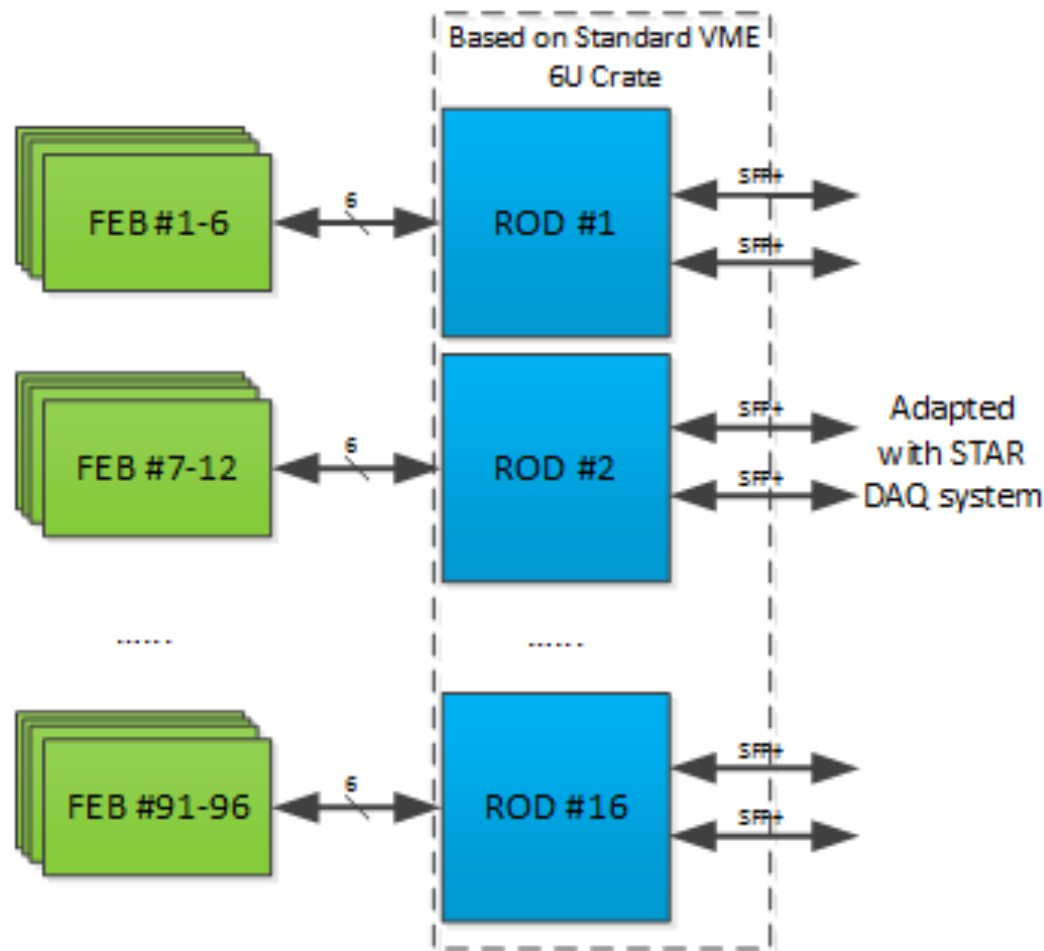
- 120 positions: 14 for signal Ground (marked with 'G'), 106 for strips.



Golden fingers on FEB

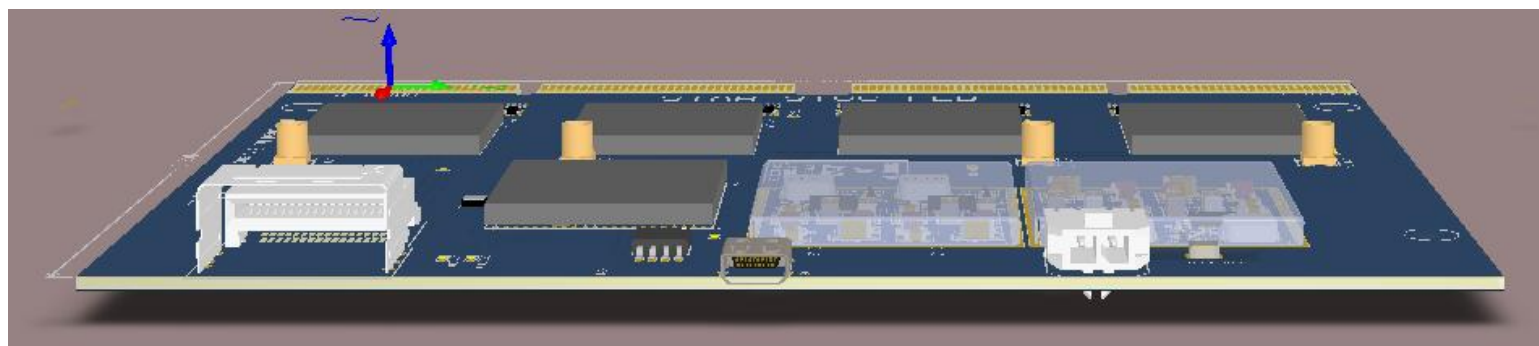
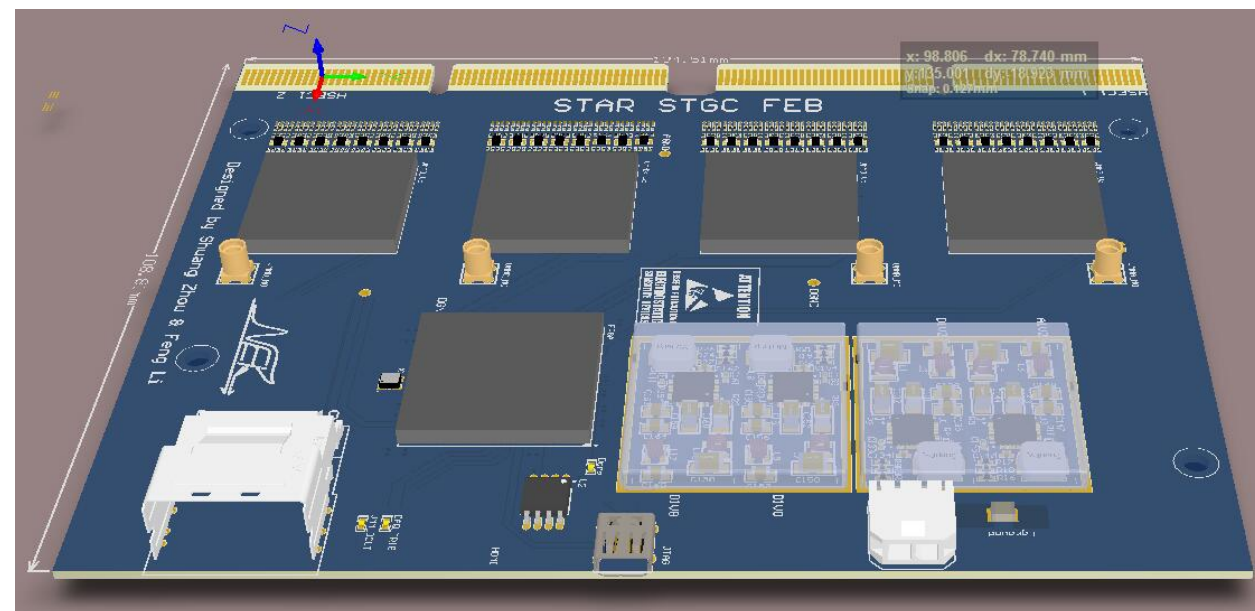
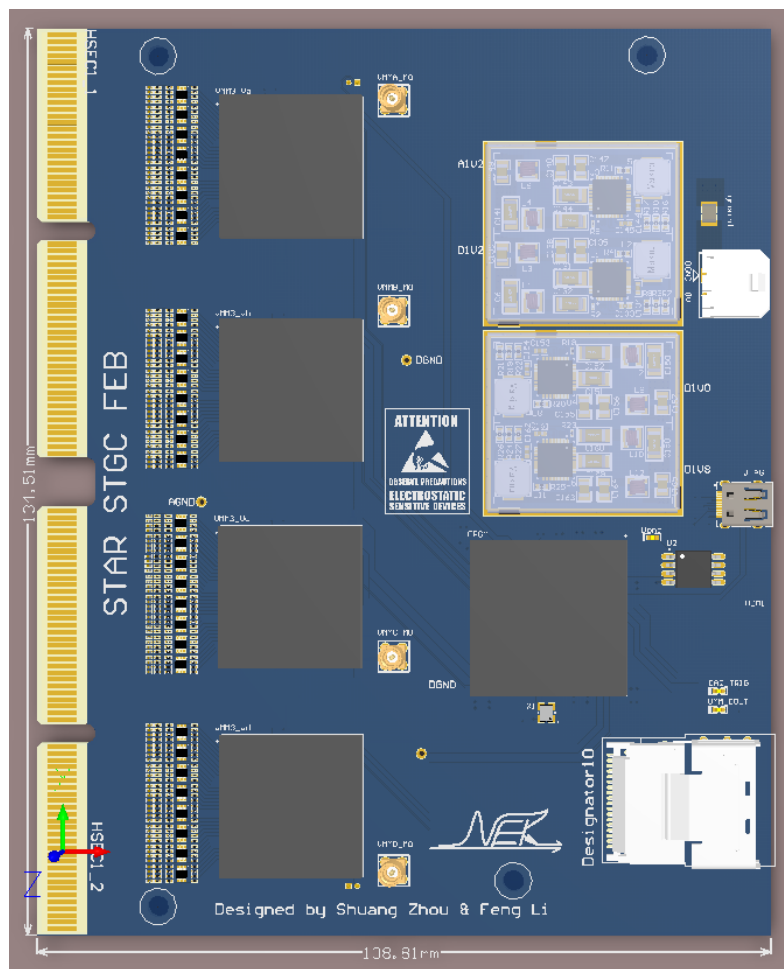
# Read-out Electronics Architecture

- 96 Front-End Boards
- 16 Read Out Driver Module
- ROD modules are designed based on Standard **VME 6U** Crate(with DC power supply)



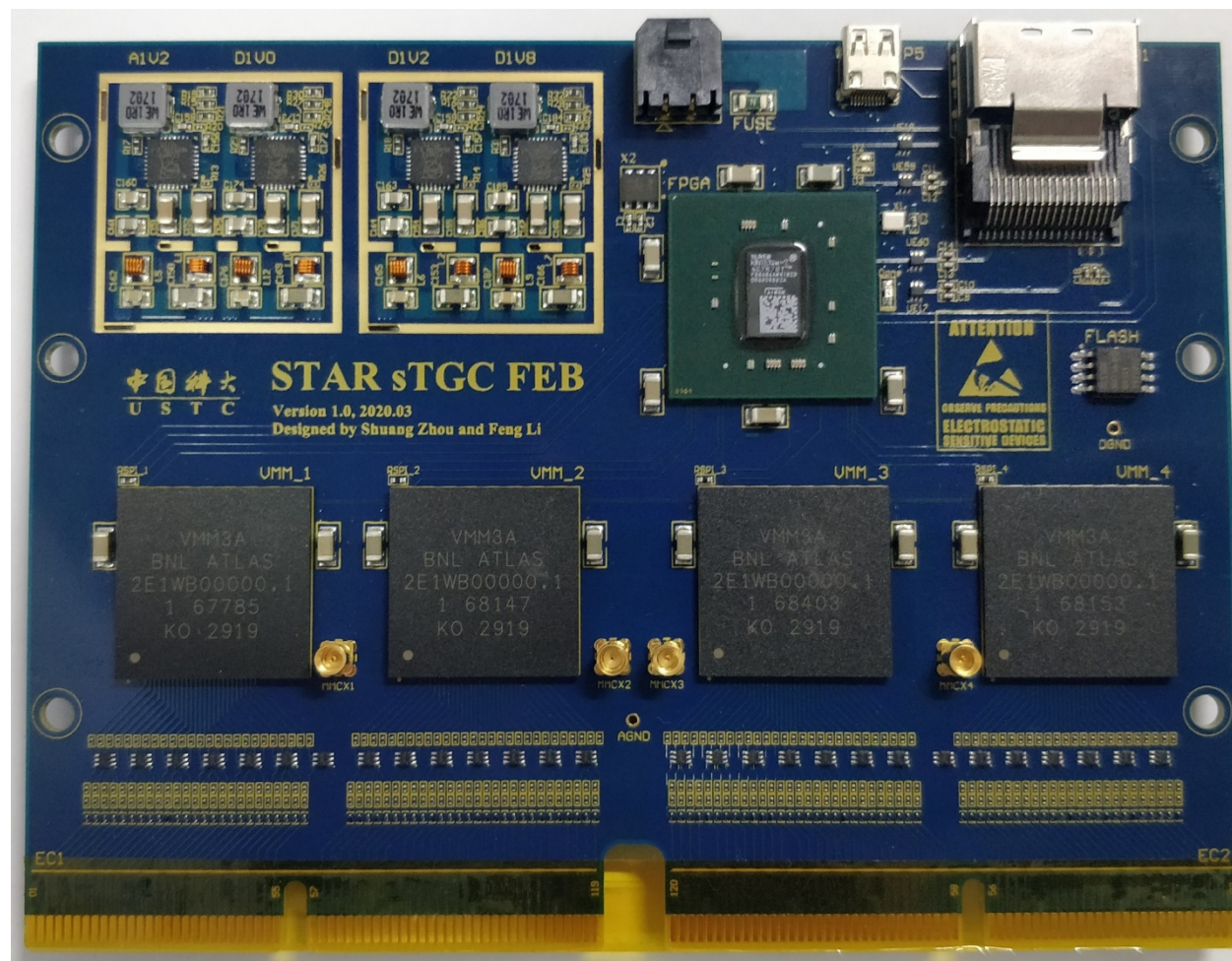
# FEB Status

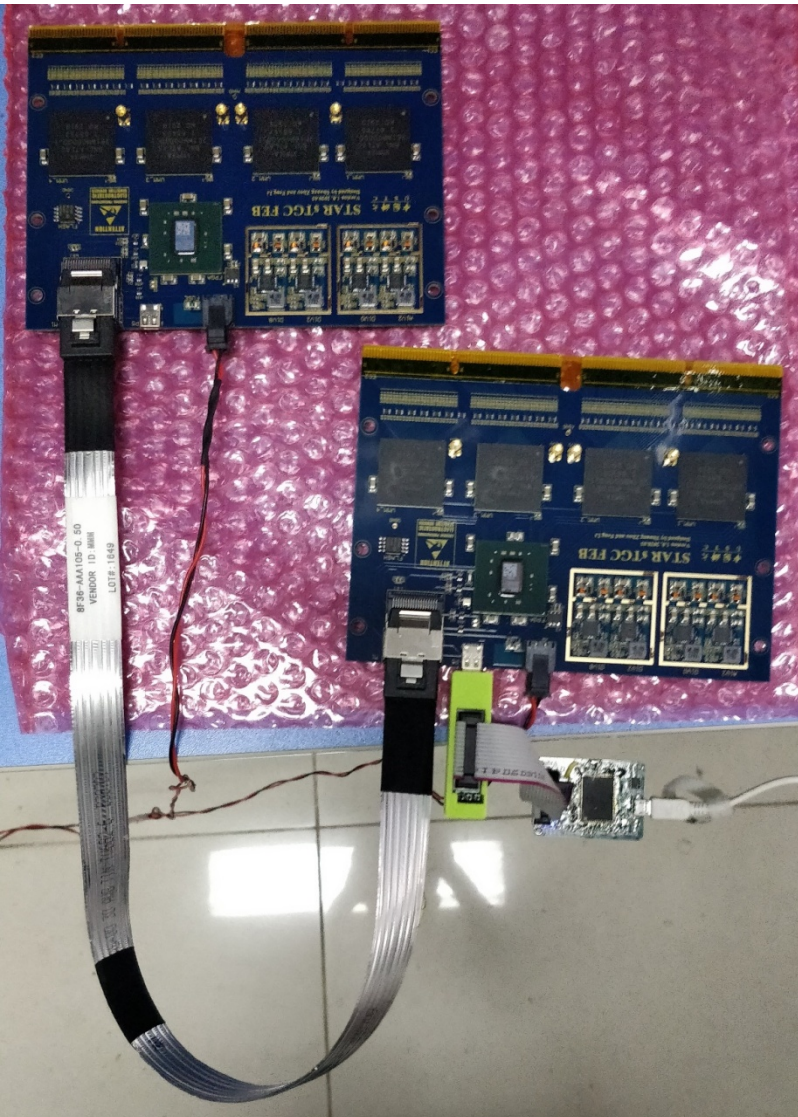
# 3D show of FEB



- FEB is shown on the right.
- Test the performance of the GTX link .
- The VMM configuration and readout.
- Check the power supply of the FEB.
- FEB weight:
  - shown < 70g
  - cooling pad and cages ( power ) < 20g
  - data cable and power cable < 15g
  - .....

**FEB weight < 110g**





- Test the performance of the GTX link at 4 Gbps by Xilinx IBERT core.
- The left picture shows the test platform, and the results are shown below.
- Test the GTX link with different length of the mini-SAS cable (0.5m, 1m, 2m, 3m), and the GTX link works steadily at all length.
- Power: 10V, 0.8A (4 VMMs configured and readout, GTX activated).

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	RX PLL Status	TX PLL Status
Ungrouped Links (0)											
Link Group 0 (1)							Reset	PRBS 7-bit	PRBS 7-bit		
Link 0	MGT_X0Y3/TX	MGT_X0Y3/RX	4.000 Gbps	4.544E12	0E0	2.2E-13	Reset	PRBS 7-bit	PRBS 7-bit	Locked	Locked

## Completed work:

1. VMM configuration and readout. We can configure VMM in right mode, and readout the events data of test pulses from VMM.
2. Reformat events data. Add Cyclic Redundancy Check in each data packet, and scramble the data stream before transmitting.
3. Transmit data packets at 4 Gbps by GTX.
4. Slow data links(40Mbps) tests. Slow data links between FEB and ROD, include the clock signal, the trigger signal, and the commands.

## Next to do:

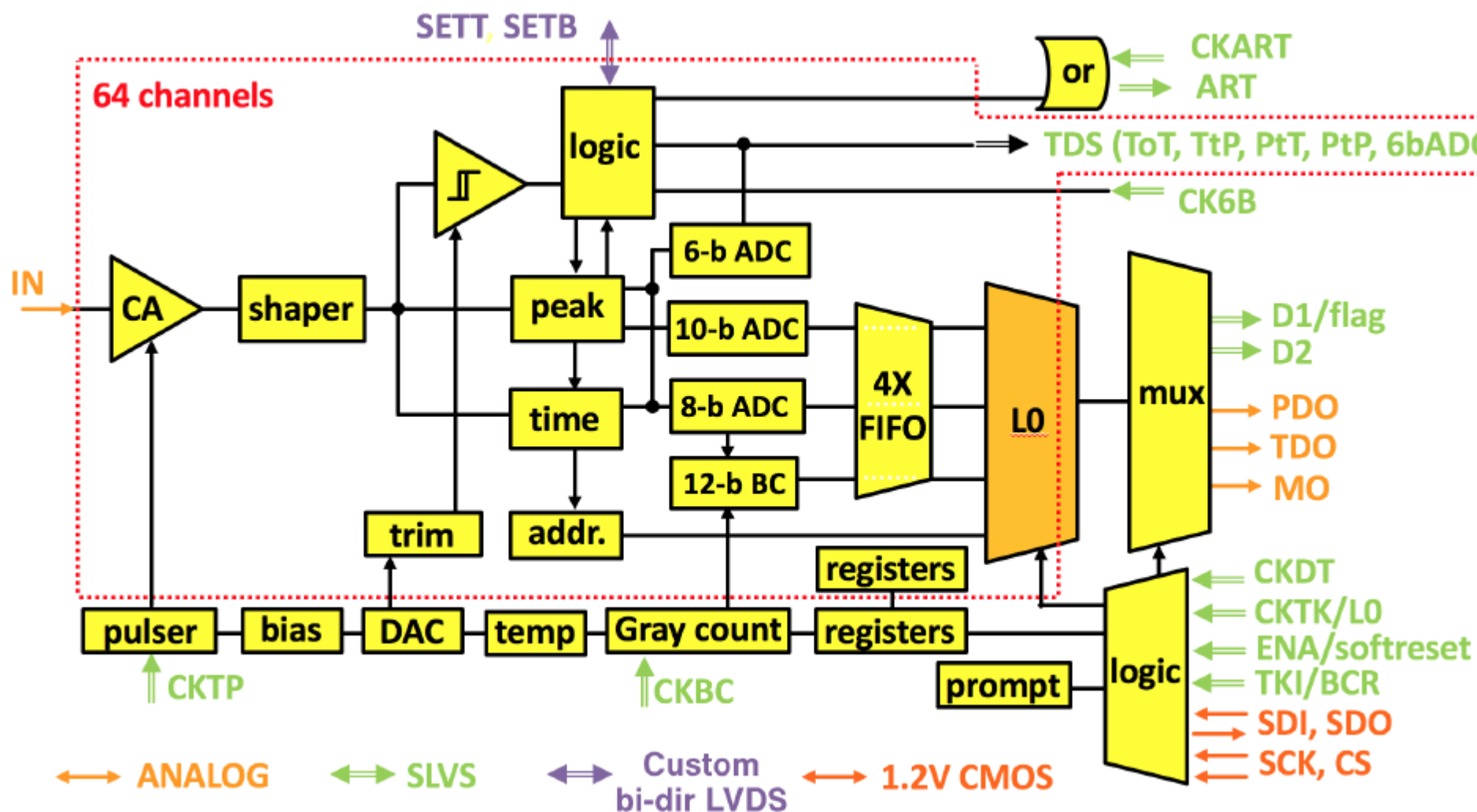
1. Test VMM readout with the external test pulse.
2. Monitor the temperature sensor of VMM.
3. Power connector and Data connector will be replaced by vertical types in the next version of FEB.



# VMM3 usage on FEB

configuration and readout

# Architecture of VMM3



# VMM3 configuration

- Global register: 192 bits
  - Charge polarity
  - Gain(0.5,1,3,4.5,6,9,12,16mV/fC)
  - Peaking Time(200,100,50,25ns)
  - Coarse threshold DAC
  - Test Pulse DAC
  - .....

**Global Configuration Reg**

<input checked="" type="checkbox"/> sp:input charge polarity	<input checked="" type="checkbox"/> slvs:enable direct output IOs
<input type="checkbox"/> sdp:disable at peak	<input type="checkbox"/> sdrv:tristates analog outputs with token
<input checked="" type="checkbox"/> sbmx:routess analog monitor to PDO output	<input type="checkbox"/> stcr:enable auto reset
<input checked="" type="checkbox"/> sbft:enable TDO buffer	<input type="checkbox"/> ssart:enable ART flag synchronization
<input checked="" type="checkbox"/> sbfp:enable PDO buffer	<input type="checkbox"/> srec:enable fast recovery from high charge
<input checked="" type="checkbox"/> sbfm:enable MO buffer	<input type="checkbox"/> s32:skip Ch16-47 and make 15 and 48 neighbors
<input type="checkbox"/> slg:leakage current disable	<input type="checkbox"/> sbip:enable bipolar shape
Channel Monitor <input type="button" value="v"/> Ch50 <input type="button" value="v"/>	<input type="checkbox"/> srat:enable timing ramp at threshold
<input type="checkbox"/> sfa:ART enable Timing at threshold <input type="button" value="v"/>	<input type="checkbox"/> sfrst:enable fast reset at 6-b completion
Peaktime 50ns <input type="button" value="v"/>	<input checked="" type="checkbox"/> stlc:enable mild tail cancellation
<input checked="" type="checkbox"/> sfm:enable dynamic discharge for AC coupling	<input checked="" type="checkbox"/> slvsbc:enable slvs 100ohm on ckbc
Gain 3.0 mV/fC <input type="button" value="v"/>	<input checked="" type="checkbox"/> slvstp:enable slvs 100ohm on cktp
<input type="checkbox"/> sng:enable neighbor triggering	<input checked="" type="checkbox"/> slvstk:enable slvs 100ohm on cktk
TtP:threshold-to-peak <input type="button" value="v"/>	<input checked="" type="checkbox"/> slvsdt:enable slvs 100ohm on ckdt
<input type="checkbox"/> sttt:enable direct-output logic	<input checked="" type="checkbox"/> slvsart:enable slvs 100ohm on ckart
<input type="checkbox"/> ssh:enable sub-hysteresis discrimination	<input checked="" type="checkbox"/> slvstki:enable slvs 100ohm on cktki
TAC slope adjustment:60ns <input type="button" value="v"/>	<input checked="" type="checkbox"/> slvsena:enable slvs 100ohm on ckena
300 <input type="button" value="v"/> sdt:Coarse threshold DAC (10bit)	<input checked="" type="checkbox"/> slvs6b:enable slvs 100ohm on ck6b
800 <input type="button" value="v"/> sdp90:Test pulse DAC (10bit)	<input type="checkbox"/> sLOenaV:disable mixed signal functions when LO enabled
10bit ADC conversion time : 00 <input type="button" value="v"/>	<input type="checkbox"/> reset[1]:Hard reset <input type="checkbox"/> reset[0]:Hard reset
8bit ADC conversion time : 00 <input type="button" value="v"/>	<input type="checkbox"/> sLOena:enable LO core and clk
6bit ADC conversion time : 000 <input type="button" value="v"/>	0 <input type="button" value="v"/> l0offset_i:LO BC offset (12bit)
<input type="checkbox"/> s8b:8bit ADC conversion mode	0 <input type="button" value="v"/> offset_i:Channel tagging BC offset (12bit)
<input checked="" type="checkbox"/> s6b:enable 6bit ADC	0 <input type="button" value="v"/> rollover_i:Channel tagging BC rollover (12bit)
<input checked="" type="checkbox"/> s10b:enable high resolution ADCs	0 <input type="button" value="v"/> window_i:Size of trigger window (3bit)
<input type="checkbox"/> sdcks:enable dual clock edge serialized data	0 <input type="button" value="v"/> truncate_i:Max hits per LO (6bit)
<input type="checkbox"/> sdoka:enable dual clock edge serialized ART	0 <input type="button" value="v"/> nskip_i:Number of LO triggers to skip on overflow
<input type="checkbox"/> sdck6b:enable dual clock edge serialized 6bit	<input type="checkbox"/> sLOcktest:enable clocks when LO core disabled(test)
	<input type="checkbox"/> sLOckinv:invert BC clk
	<input type="checkbox"/> sLOdckinv:invert DCK
	<input type="checkbox"/> nskipm_i:BCID skip

# VMM3 configuration

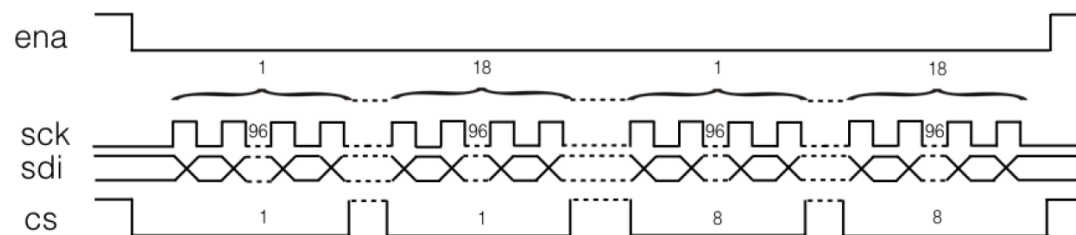
- Channel register: 24 bits/CH
  - Threshold trimming
  - Internal test pulse
  - .....

## Channel Configuration Reg

<b>sc:</b> large sensor capacitance mode([0]<200pF [1]>200pF)	<b>sm:</b> mask enable([1=enable])
<b>sl:</b> leakage current disable([0=enable])	<b>sd:</b> trim threshold DAC, 1mV step
<b>st:</b> 300pF test capacitor([1=enable])	<b>sz10b:</b> 10-bit ADC zero
<b>sh:</b> multiplies test capacitor by 10	<b>sz8b:</b> 8-bit ADC zero
<b>smx:</b> channel monitor mode([0=analog output] [trimmed threshold])	<b>sz6b:</b> 6-bit ADC zero

- VMM Configuration Process:

- $192 + 24 * 64 = 1728$  bits
- configure VMM through SPI.
- Each VMM can be configured individually.
- 18\*96-bits: 2\*96-bits for global registers, 16\*96-bits for channel registers.



# VMM3 configuration GUI

VMM3 Config

### Channel Configuration Reg

**sc:** large sensor capacitance mode([0]<200pF [1]>200pF)  
**sl:** leakage current disable([0]=enable)  
**st:** 300pF test capacitor([1]=enable)  
**sh:** multiplies test capacitor by 10  
**smx:** channel monitor mode([0]=analog output] [trimmed threshold])

Ch	sc	sl	st	sh	sm	smx	sd	sz10b	sz8b	sz6b	Ch	sc	sl	st	sh	sm	smx	sd	sz10b	sz8b	sz6b
Ch 0	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch32	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch33	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch34	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch35	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 4	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch36	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 5	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch37	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 6	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch38	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 7	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch39	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
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Ch 9	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch41	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
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Ch12	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch44	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
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Ch16	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch48	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch17	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch49	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch18	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch50	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch19	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch51	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch20	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch52	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch21	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch53	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch22	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch54	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
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Ch26	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch58	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch27	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch59	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch28	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch60	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch29	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch61	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch30	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch62	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch31	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Ch63	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
All10	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	All11	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

### Global Configuration Reg

sp:input charge polarity  
 sdp:disable at peak  
 sbmx:routes analog monitor to PDO output  
 sbft:enable TDO buffer  
 sbfp:enable PDO buffer  
 sbfm:enable MO buffer  
 slg:leakage current disable  
 slvs:enable direct output IOs  
 sdrv:tristates analog outputs with token  
 stor:enable auto reset  
 sstart:enable ART flag synchronization  
 srec:enable fast recovery from high charge  
 s32:skip Ch16-47 and make 15 and 48 neighbors  
 sbip:enable bipolar shape  
 srat:enable timing ramp at threshold  
 sfrst:enable fast reset at 6-b completion  
 stlc:enable mild tail cancellation  
 silvsbc: enable slvs 100ohm on okbe  
 silvstp: enable slvs 100ohm on oktp  
 silvstk: enable slvs 100ohm on oktk  
 silvsdt: enable slvs 100ohm on okdt  
 silvsart:enable slvs 100ohm on okart  
 silvstki:enable slvs 100ohm on oktki  
 silvsena:enable slvs 100ohm on klena  
 silvs6b: enable slvs 100ohm on ok6b  
 sLDenaV:disable mixed signal functions when LD enabled  
 reset[1]:Hard reset     reset[0]:Hard reset  
 sLDena:enable LD core and clk  
 lloffset\_i:LD BC offset (12bit)  
 offset\_i:Channel tagging BC offset (12bit)  
 rollover\_i:Channel tagging BC rollover (12bit)  
 window\_i:Size of trigger window (3bit)  
 truncate\_i:Max hits per LD (6bit)  
 nskip\_i:Number of LD triggers to skip on overflow  
 sLDoktest:enable clocks when LD core disabled(test)  
 sLDokinv:invert BC clk  
 sLDokinv:invert DCK  
 nskipm\_i:BCID skip

**Channel Monitor**    Ch21  
 Timing at threshold  
 Feaktime 50ns  
 sfm:enable dynamic discharge for AC coupling  
 Gain 3.0 mV/EC  
 sng:enable neighbor triggering  
 TFP:threshold-to-peak  
 sttt:enable direct-output logic  
 ssh:enable sub-hysteresis discrimination  
 TAC slope adjustment:60ns  
 400    sdt:Coarse threshold DAC (10bit)  
 800    sdp90:Test pulse DAC (10bit)  
 10bit ADC conversion time : 00  
 8bit ADC conversion time : 00  
 6bit ADC conversion time : 000  
 s8b:8bit ADC conversion mode  
 s6b:enable 6bit ADC  
 s10b:enable high resolution ADCs  
 sdxks: enable dual clock edge serialized data  
 sdxka: enable dual clock edge serialized ART  
 sdxk6b:enable dual clock edge serialized 6bit

### Operation

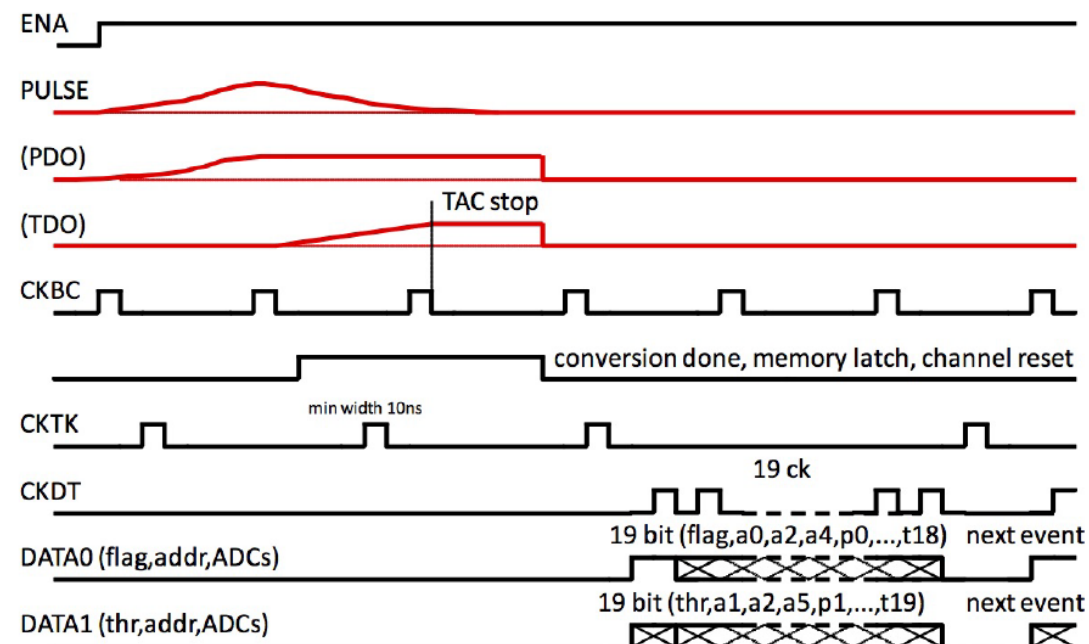
pFEB 0    sFEB 0     VMM0    VMM4    0    QuickMonitor    FEB PDO Scan     Bypass Mode  
 pFEB 1    sFEB 1     VMM1    VMM5    Buffer This VMM    reserved    STGC FEB  
 pFEB 2    sFEB 2     VMM2    VMM6    Load Config Data    Chl + 1    Export Commands  
 pFEB 3    sFEB 3     VMM3    VMM7    Save Config Data    Scan Chl    Config VMM3

- Used for ATLAS FEB mass inspection
- Can be transplanted to be used for STAR FEB test before shipment.

## VMM Mode: Non-ATLAS Continuous Mode.

### VMM Data Format:

Each event data is 38 bits, contains 1 bit flag, 1 bit threshold, 6 bits channel ID, 10 bits PDO, 8 bits TDO, and 12 bits BCID.

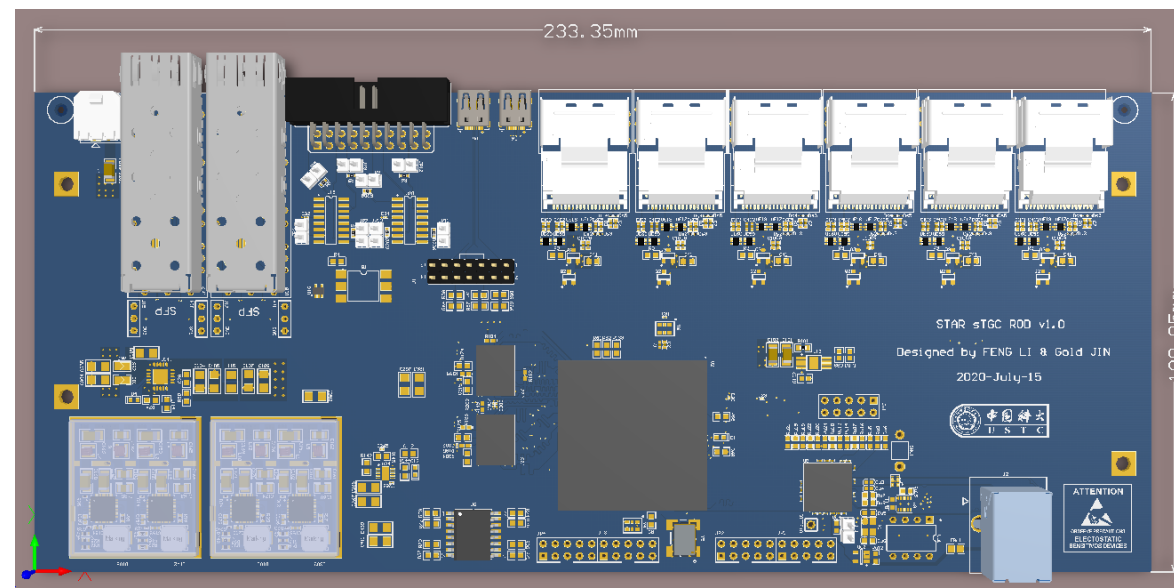
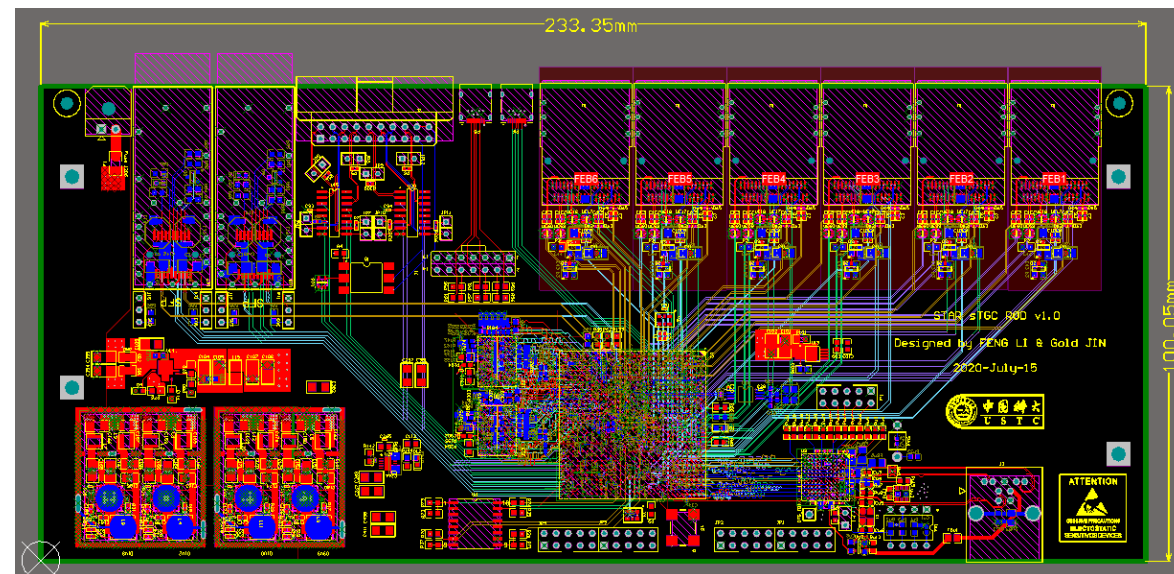


hit data	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
	F	N	Chan# (6)						ADC (10)										TDC (8)								BCID (12)											

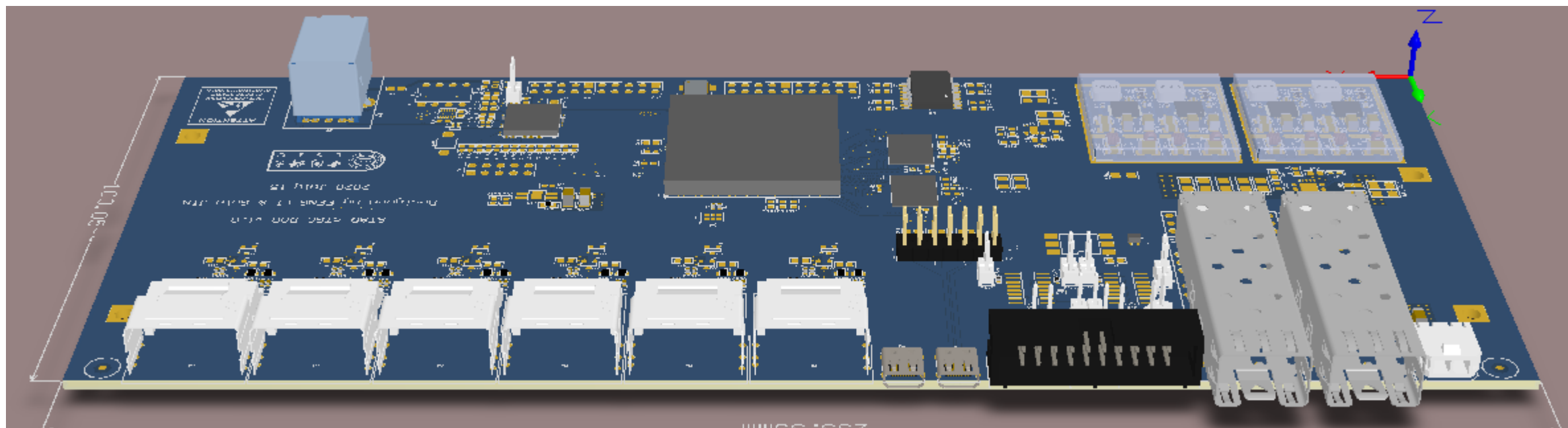
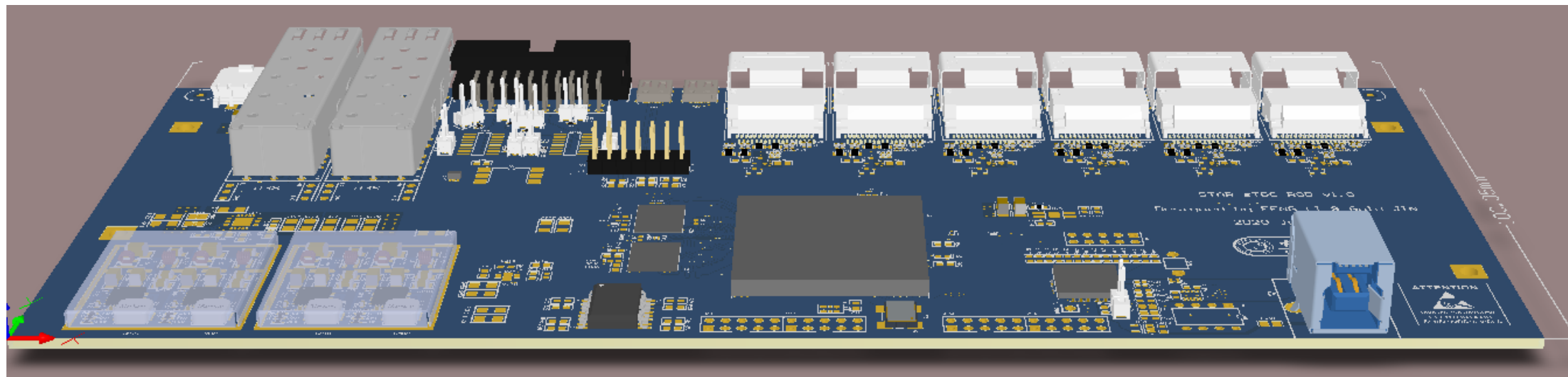
# ROD Status

# ROD Architecture

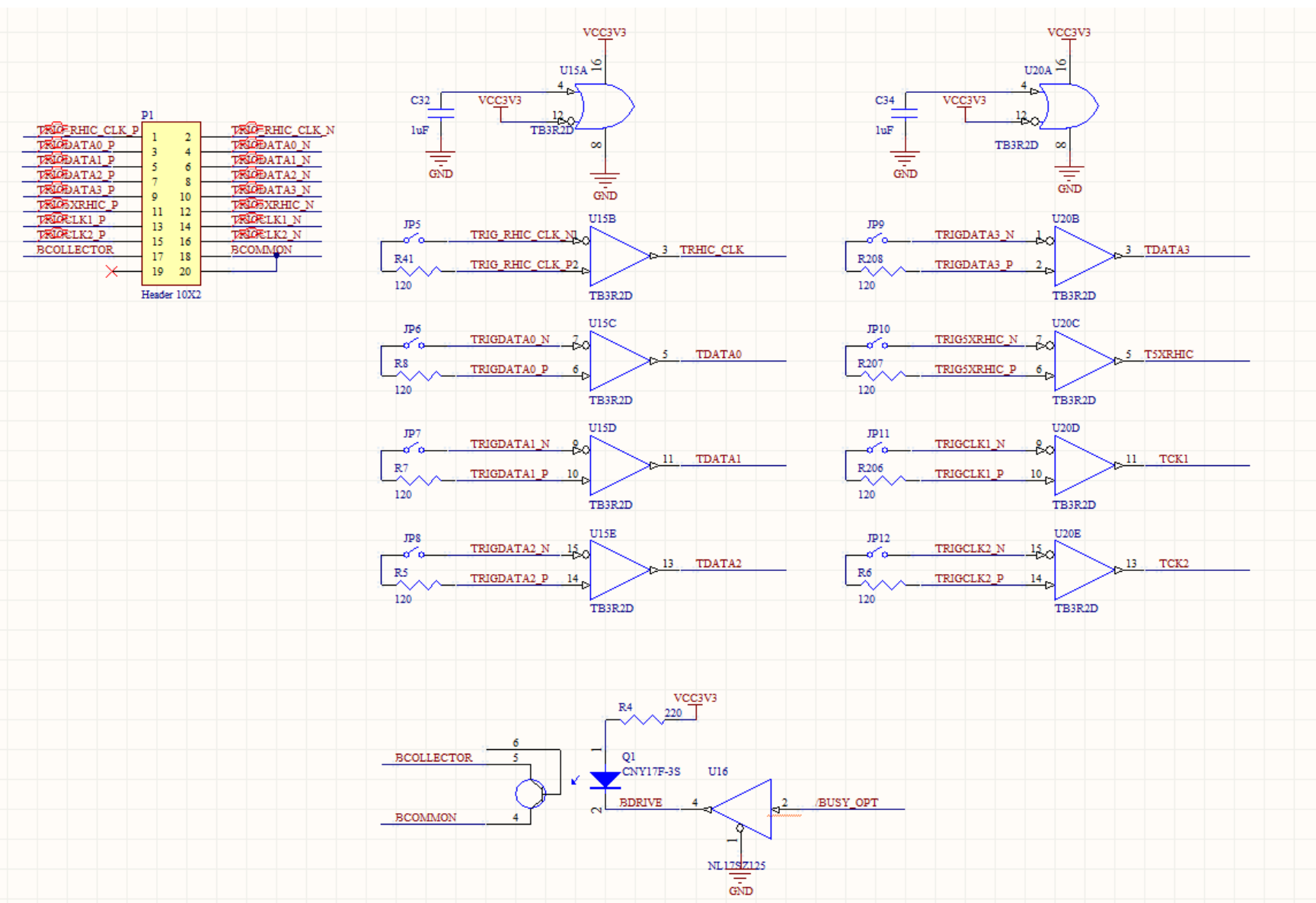
- 6 DATA connectors compatible with 6 FEBs
- Xilinx Kintex-7 FPGA: XC7K325T-2FFG900I
- FEAST power modules
- 2 optical fiber SFP+ to communicate with STAR DAQ (1 for spare)
- ROD size: 233\*100mm
- TCD circuit for STAR DAQ connection.
- USB3.0 connector added for communication with PC(not necessary for STAR).







# TCD circuit



- LVPECL(from cable)  
→ LVTTTL → FPGA
- 120-ohm resistors kept  
but only one board  
needs to solder them
- Busy signal from  
FPGA will return to  
TCD board.

# POWER

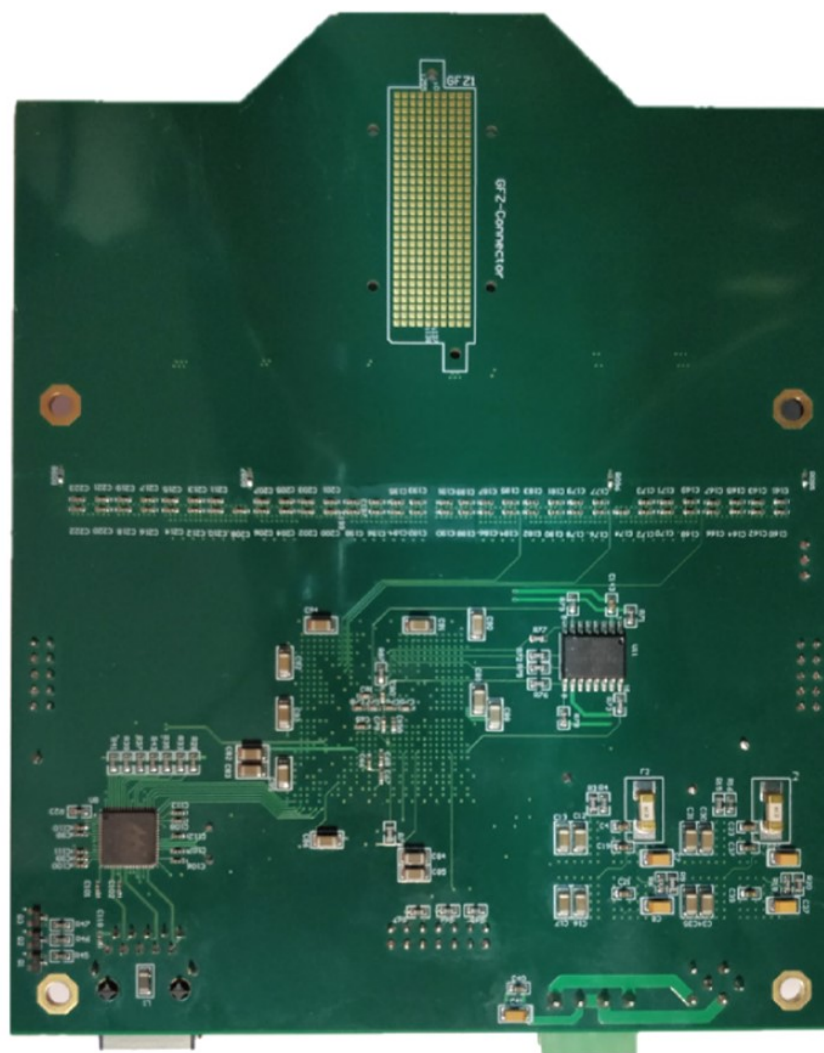
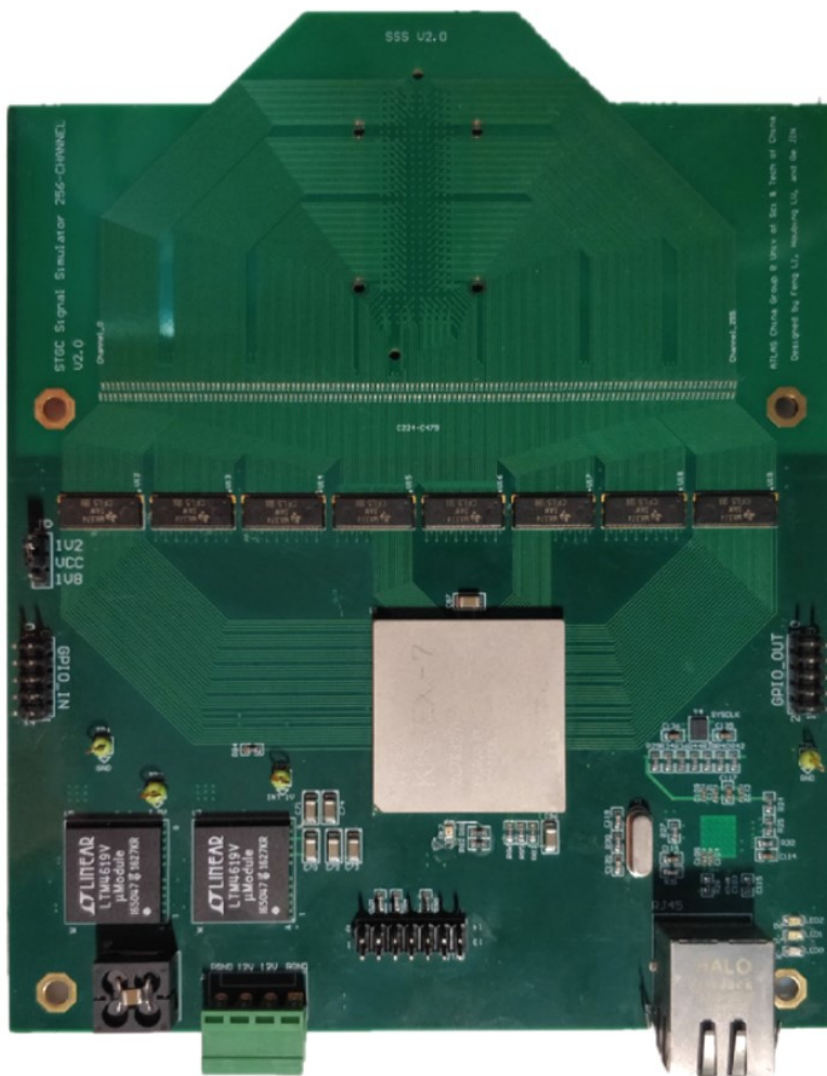
- 4 FEAST ASICs used:
  - Digital 3.3V: SFP+ Powering, SPI Flash, TCD, GPIO
    - DDR\_1.5V(LDO): DDR powering
      - 0.75V(LDO):DDR reference voltage
  - Digital 1.0V: FPGA core voltage and MGT\_AVCC
  - Digital 1.2V: MGT\_AVTT
  - Digital 1.8V: FEB links

# Board Status

- ROD boards will be back early August. Then 1-2 weeks for soldering.
- Firmware development ongoing:
  - Decode data packet; Descramble; CRC
  - 10G SFP+ code transplanting;
  - DDR3 code development

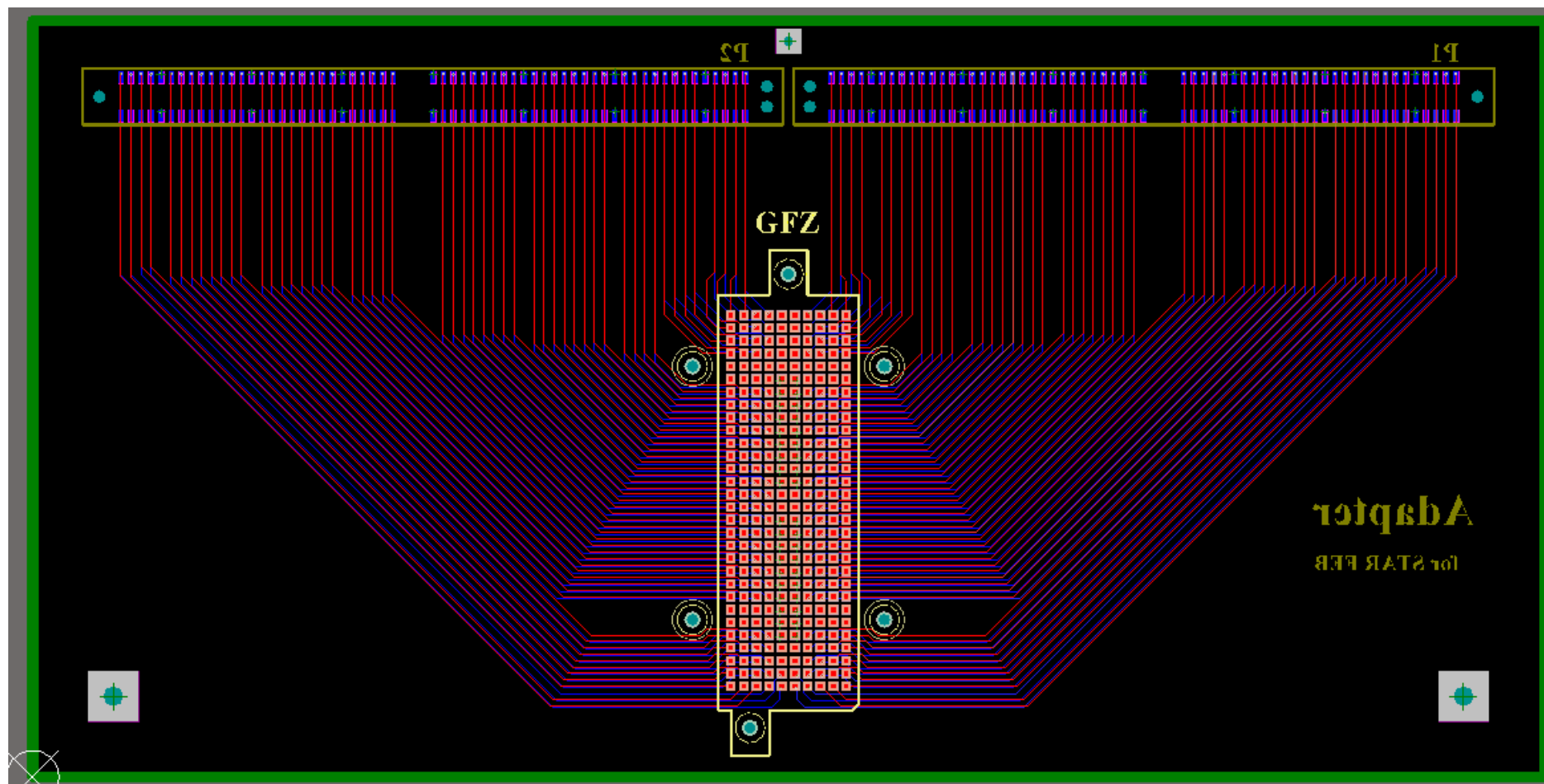
# Adapter between FEB and Simulator Board

# STGC Signal Simulator board

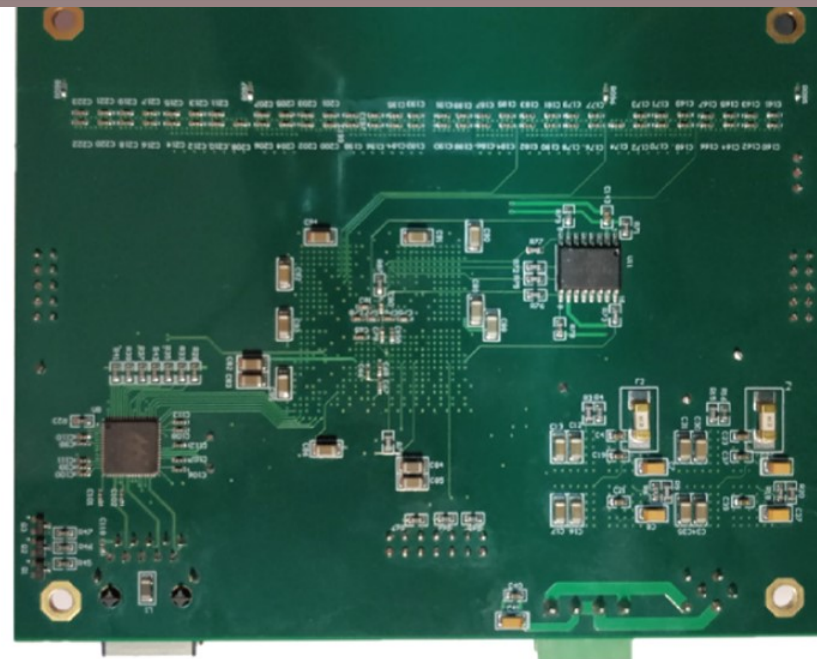
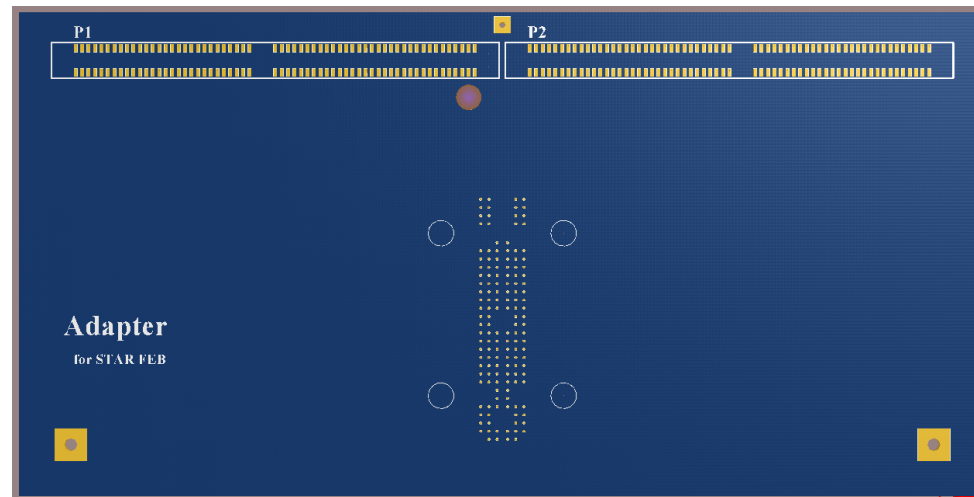


- 256 channels charge output,  $\sim 0.4\text{pC}$
- Used as external test pulse source for FEB

# Adapter board design



# Connection





Thanks!